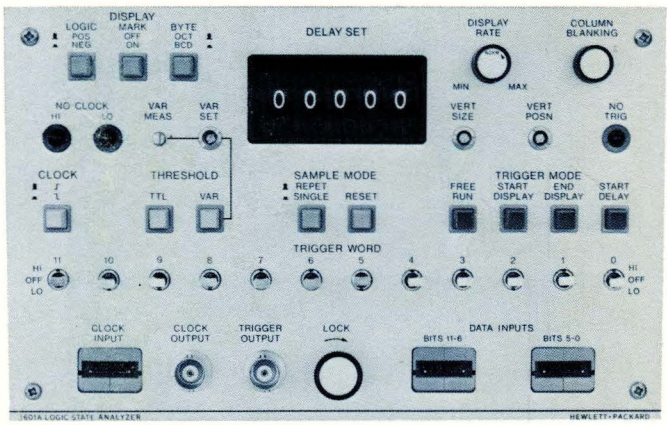
OPERATING AND SERVICE MANUAL

LOGIC STATE ANALYZER

1601A



HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

MODEL 1601A
LOGIC STATE ANALYZER

SERIALS PREFIXED: 1351A

Refer to Section VII for instruments with other Serial Prefixes.

HEWLETT-PACKARD COMPANY/COLORADO SPRINGS DIVISION
1900 GARDEN OF THE GODS ROAD, COLORADO SPRINGS, COLORADO, U.S.A.

Manual Part Number 01601-90903
Microfiche Part Number 01601-90803.

PRINTED: FEB 1974

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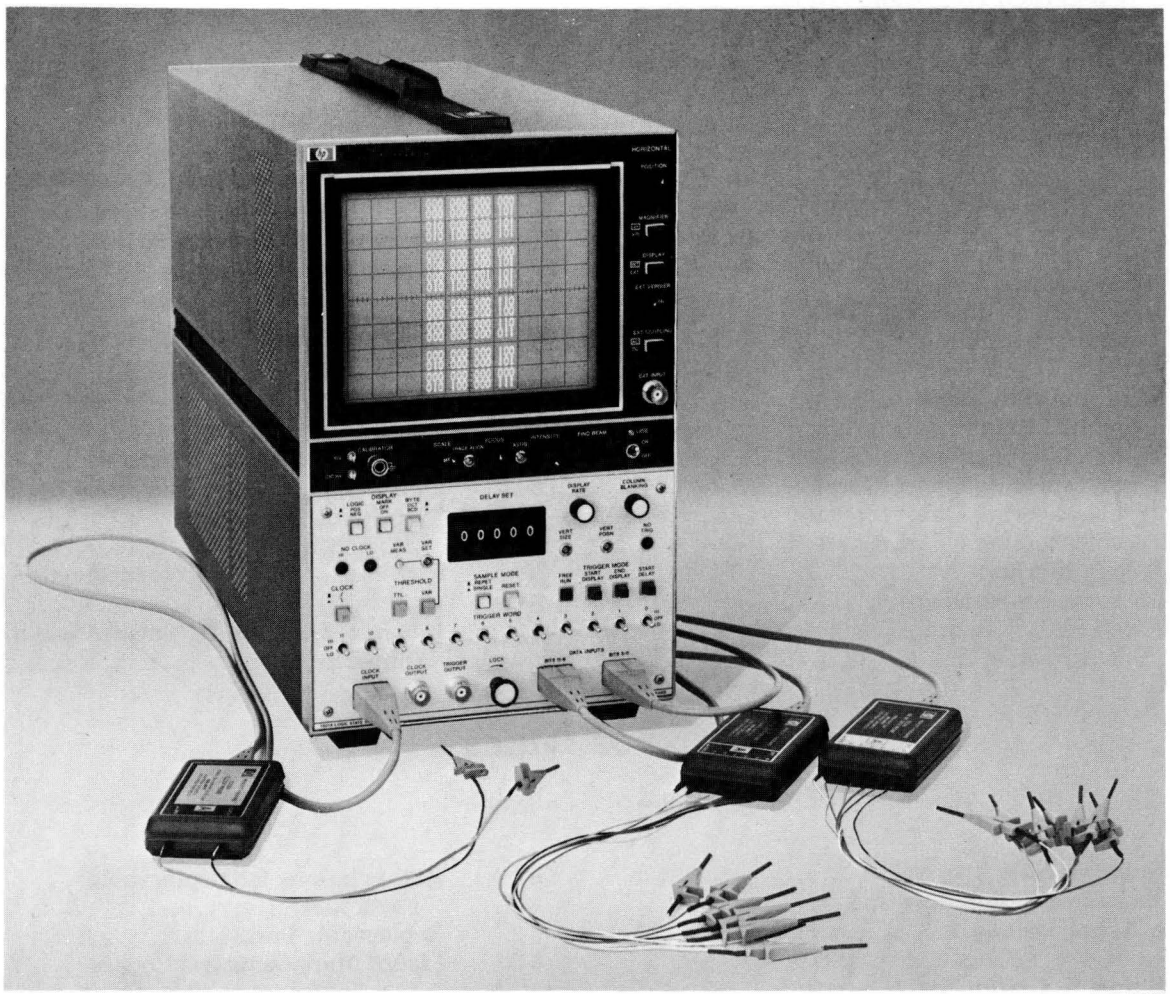


Figure 1-1. Model 1601A Logic State Analyzer

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual provides operating and servicing information for the Hewlett-Packard Model 1601A Logic State Analyzer (figure 1-1). The manual is divided into eight sections, each covering a specific topic or aspect of the instrument. All schematics are located at the rear of the manual and can be unfolded and used for reference while reading any part of the manual.

1-3. This section contains a description of the Model 1601A. The instrument specifications are listed in Table 1-1. Table 1-2 lists and describes abbreviations used in this manual except for Section VI. Special accessories available for this instrument are also described in this section. Standard options are described in Section VII.

1-4. DESCRIPTION.

1-5. The Model 1601A is a full width plug-in unit compatible with HP-180 series oscilloscope mainframes. Containing both vertical and horizontal circuitry, the instrument displays the digits "1" and "0" on the CRT. These digits provide an indication of functional states of parallel input logic streams.

1-6. When installed in an HP 180-series oscilloscope mainframe and connected to clock and data monitoring probes, the Model 1601A will display sixteen sequential twelve bit words of parallel logical data such as important register states or qualifiers. The monitored data can be any available positive or negative logic function up to twelve bits in width, with a maximum clock rate of ten megabits per second. A clock input, from the system under test, controls the flow of monitored data into the Model 1601A memory. The clock input may be a positive or negative signal, synchronous with the monitored data.

1-7. A preset trigger word, set on the front panel, controls the position of the sixteen word display in reference to the input data stream. Depending on the mode selected, the display starts at the trigger word, ends at the trigger word, or is delayed up to 99,999 clock input pulses after the trigger word.

Table 1-1. Specifications

CLOCK AND DATA INPUTS

(Using HP 10230A Clock Probe and two HP 10231A Six Bit Data Probes)

REPETITION RATE: 0 to 10 Megabits/sec.

INPUT RC: 40 ±3K ohms shunted by ≤14 pF.

INPUT BIAS CURRENT: ≤30 μA.

INPUT THRESHOLD: TTL, fixed at +1.45 ±0.05 Vdc. Variable, to ±10 Vdc.

MINIMUM INPUT SWING: [0.4 +10% of threshold voltage] V p-p.

MAXIMUM INPUT:
Level, ≤ +15 Vdc; ≥ —15 Vdc.
Swing, 15 V peak from threshold.

MINIMUM CLOCK PULSE WIDTH: 25 nsec.

MINIMUM SETUP TIME (time data must be present prior to clock transition): 35 nsec (typically 20 nsec).

MINIMUM HOLD TIME (time data must be present after clock transition): 0 (typically —5 nsec).

DISPLAY RATE

Variable from <40 msec to >5 seconds.

CLOCK AND TRIGGER OUTPUTS

HIGH: ≥2V into 50 ohms. (Line driver interface.)

LOW: ≤0.4V into 50 ohms. (Line driver interface.)

WIDTH: Approximately 40 nsec (RZ format).

GENERAL

WEIGHT: Net, 5¼ lb (2.34 kg); Shipping, 10¼ lb (4.65 kg).

POWER REQUIREMENTS: Supplied by HP 180-series oscilloscope mainframes.

PROBE POWER: Supplies power to operate one HP 10230A Clock Probe and two HP 10231A Six Bit Data Probes.

ENVIRONMENT:
Temperature: 0° to 55°C.
Humidity: to 95% relative humidity to 40°C.
Altitude: to 15,000 feet.
Vibration: vibrated in three planes for 15 min. each with 0.010 in. excursion, 10 to 55 Hz.

1-8. During repetitive operation, the display is periodically updated by incoming data. To monitor infrequent or one-time-only events, the display can be set to a single shot mode. In this mode, gathered data is retained and displayed until manually reset.

1-9. Other features include: a free run mode which allows all incoming data words to be displayed; arrangement of the display in four bytes of three bits each (octal format), or in three bytes of four bits each (binary coded decimal format); intensification of the trigger word; and the capability of blanking out columns of bits, starting with the most significant bit.

1-10. WARRANTY.

1-11. The instrument is certified and warranted as stated in the front of this manual.

CAUTION

The warranty may be void for instruments having a mutilated serial number tag.

1-12. ACCESSORIES REQUIRED.

1-13. One Clock Probe, HP Model 10230A, and two Six Bit Data Probes, HP Model 10231A, are required for use with the Model 1601A. Refer to the operating and service literature supplied with these probes for further information.

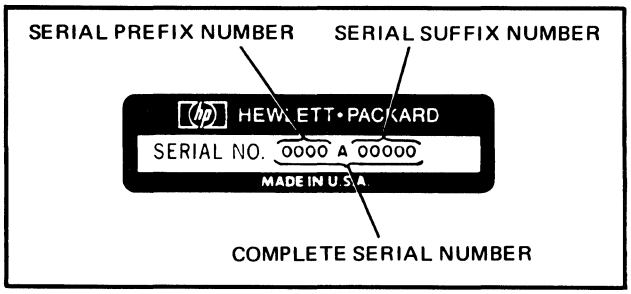


Figure 1-2. Instrument Serial Number

1-14. INSTRUMENT AND MANUAL IDENTIFICATION.

1-15. This manual applies directly to Model 1601A instruments with a serial prefix number as listed on the manual title page. The serial prefix number is the first group of digits in the instrument serial number (figure 1-2). The instrument serial number is on a tag located on the rear of the instrument.

1-16. Check the serial prefix number of the instrument. If the serial prefix number is different from that listed on the title page of this manual, refer to Section VII for instructions to adapt this manual for proper instrument coverage.

1-17. INQUIRIES.

1-18. Refer any questions regarding the manual, or the instrument to the nearest HP Sales/Service Office. Always identify the instrument by model number, complete name, and complete serial number in all correspondence. Refer to the rear of this manual for a world-wide listing of HP Sales/Service Offices.

Table 1-2. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	ASSEMBLY	E	MISC. ELECTRICAL PART	P	PLUG	U	INTEGRATED CIRCUIT (UNREPAIRABLE)
AT	ATTENUATOR RESISTIVE TERMINATION	F	FUSE	PS	POWER SUPPLY	V	VACUUM TUBE, NEON BULB, PHOTOCELL, ETC.
B	MOTOR, FAN	FL	FILTER	Q	TRANSISTOR	VR	VOLTAGE REGULATOR (DIODE)
BT	BATTERY	H	HARDWARE	R	RESISTOR	W	CABLE
C	CAPACITOR	J	JACK	RT	THERMISTOR	X	SOCKET
CP	COUPLING	K	RELAY	S	SWITCH	Y	CRYSTAL
CR	DIODE	L	INDUCTOR	T	TRANSFORMER	Z	NETWORK
DL	DELAY LINE	LS	SPEAKER	TB	TERMINAL BOARD		
DS	DEVICE SIGNALING (LAMP)	M	METER	TP	TEST POINT		
		MP	MECHANICAL PART				

ABBREVIATIONS

A	AMPERE(S)	F	FARAD(S)	n	NANO (10^{-9})	rfi	RADIO FREQUENCY INTERFERENCE
A	AMPERE TURN(S)	FET	FIELD-EFFECT TRANSISTOR(S)	nc	NORMALLY CLOSED	rms	ROOT MEAN SQUARE
ampl	AMPLIFIER(S)	G	GIGA (10^{9})	no.	NORMALLY OPEN	rwv	REVERSE WORKING VOLTAGE
assy	ASSEMBLY	gnd	GROUND(ED)	npn	NEGATIVE-POSITIVE-NEGATIVE	SCR	SILICON CONTROLLED RECTIFIER
ampltd	AMPLITUDE			ns	NANOSECOND	sec	SECOND(S)
bd	BOARD(S)	H	HENRY(IES)	p	PICO (10^{-12})	std	STANDARD
bp	BANDPASS	hr	HOUR(S)	pc	PRINTED (ETCHED) CIRCUIT(S)	trmr	TRIMMER
c	CENTI (10^{-2})	HP	HEWLETT-PACKARD	pk	PEAK	u	MICRO (10^{-6})
C	CARBON	Hz	HERTZ	pnp	POSITIVE-NEGATIVE-POSITIVE	usec	MICROSECOND
ccw	COUNTERCLOCKWISE	if.	INTERMEDIATE FREQ.	p/o	PART OF	V	VOLTS
coax.	COAXIAL	intl	INTERNAL	p-p	PEAK-TO-PEAK	var	VARIABLE
coef	COEFFICIENT	k	KILO (10^{3})	prgm	PROGRAM	w/	WITH
com	COMMON	lb	POUND(S)	prv	PEAK INVERSE VOLTAGE(S)	w/o	WITHOUT
CRT	CATHODE-RAY TUBE	lpf	LOW-PASS FILTER(S)	ps	PICOSECOND	wiv	WORKING INVERSE VOLTAGE
cw	CLOCKWISE	m	MILLI (10^{-3})	pwv	PEAK WORKING VOLTAGE		
d	DECI (10^{-1})	M	MEGA (10^{6})	rf	RADIO FREQUENCY		
dB	DECIBEL	ms	MILLISECOND				
ext	EXTERNAL						

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains instructions for performing an initial inspection of the Model 1601A. Installation procedures and precautions are presented in step-by-step order. The procedures for making a claim for warranty repairs and for repacking the instrument for shipment are also described in this section.

2-3. INITIAL INSPECTION.

2-4. The instrument was inspected mechanically and electrically before shipment. Upon receipt, inspect it for damage that may have occurred in transit. Check for broken knobs, bent or broken connectors, and dents or scratches. If damage is found, refer to the claims paragraph in this section. Retain the packing material for possible future use.

2-5. Check the electrical performance of the instrument immediately after receipt. Refer to Section V for the performance check procedure. The performance check will determine whether or not the instrument is operating within the specifications listed in table 1-1. Initial performance and accuracy of the instrument are certified as stated in the front of this manual. If the instrument does not operate as specified, refer to the claims paragraph in this section.

2-6. PREPARATION FOR USE.

2-7. Operating power for the Model 1601A is supplied by the oscilloscope mainframe. To install the Model 1601A, proceed as follows:

a. Rotate front panel LOCK knob fully ccw.

b. Slide instrument into plug-in compartment of oscilloscope mainframe.

c. Rotate LOCK knob cw until Model 1601A is seated snugly in oscilloscope mainframe. Do not overtighten.

2-8. Connect one Clock Probe, HP Model 10230A, to front panel CLOCK INPUT connector, and two Six Bit Data Probes, HP Model 10231A, to front panel DATA INPUT connectors. Exercise care when connecting probes to prevent damage to connectors.

2-9. INSTRUMENT COMPATIBILITY.

2-10. Model 1601A will operate in any mainframe in the HP 180-series.

2-11. CLAIMS.

2-12. The warranty statement applicable to this instrument is printed in the front of this manual. If physical damage is found or if operation is not as specified when the instrument is received, notify the carrier and nearest HP Service Office immediately (refer to the list in back of this manual for addresses). The HP Sales/Service Office will arrange for repair or replacement without waiting for settlement of the claim with the carrier.

2-13. REPACKING FOR SHIPMENT.

2-14. If Model 1601A is to be shipped to an HP Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-15. Use the original shipping carton and packing material. If the original packing material is not available, the HP Sales/Service Office will provide information and recommendations on materials to be used. Materials used for shipping an instrument normally include the following:

a. A double-walled carton; refer to table 2-1 for test strength required.

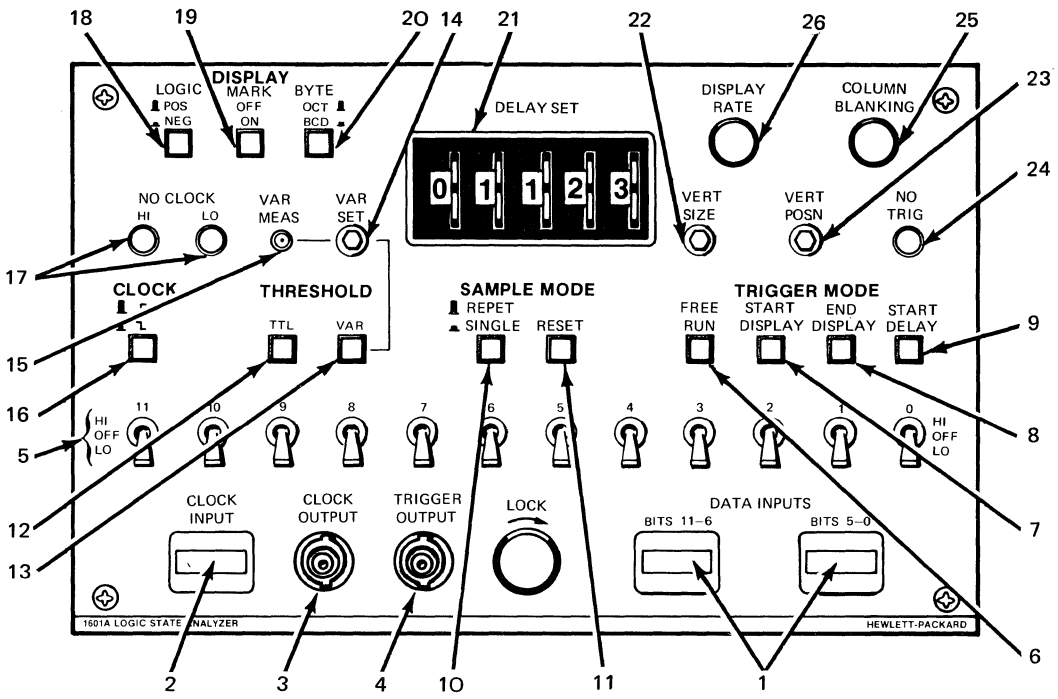
b. Heavy paper or sheets or cardboard to protect all instrument surfaces; use a nonabrasive material such as polyurethane or cushioned paper such as Kimpak around all projecting parts.

c. At least 4 inches of tightly-packed, industry approved, shock-absorbing material such as extra-firm polyurethane foam.

d. Heavy-duty shipping tape for securing outside of carton.

Table 2-1. Shipping Carton Test Strength

Gross Weight (lb)	Carton Test Strength (lb)
up to 10	200
10 to 30	275
30 to 120	350
120 to 140	500
140 to 160	600



1. DATA INPUTS. Monitored data input connectors. Each connector supplies six channels.

2. CLOCK INPUT. Clocking signal input connector.

3. CLOCK OUTPUT. Output connector for buffered CLOCK INPUT signal, converted to TTL level.

4. TRIGGER OUTPUT. Output connector for TTL level pulse generated when the input data meets triggering requirements.

5. TRIGGER WORD. Control switches for selecting triggering word.

6. FREE RUN. The equivalent of setting all TRIGGER WORD switches to OFF.

7. START DISPLAY. The word set by the TRIGGER WORD switches becomes the first displayed word. The next 15 CLOCK INPUT pulses trigger the remaining 15 displayed words.

8. END DISPLAY. The word set by the TRIGGER WORD switches becomes the last displayed word. The display is started 15 CLOCK INPUT pulses before the TRIGGER WORD.

9. START DELAY. The display start is delayed from the TRIGGER WORDby the number of CLOCK INPUT pulses preset on the DELAY SET thumbwheels.

10. SINGLE/REPET. When in REPET (Repetitive), the input data repetitively updates the Model 1601A input memory. When trigger requirements are met, data is displayed for a time determined by DISPLAY RATE. When in SINGLE, input data is inhibited from loading the memory after trigger requirements are met. Memory contents are continuously displayed until RESET is pushed.

11. RESET. In SINGLE mode, allows the memory to regather input data and update the display.

12. TTL. Set input threshold of the clock and data monitor probes to +1.5V.

13. VAR. Allows input threshold of the clock and monitor probes to be adjusted by VAR SET.

14. VAR SET. Screwdriver adjustment for varying clock and monitor probes input threshold level over a range of ±10V.

Figure 3-1. Front Panel Controls, Connectors, and Indicators

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section contains an explanation of the Model 1601A operating controls and connectors, display modes, display formats, operating considerations, operators checks and adjustments, and step-by-step operating instructions.

3-3. CONTROLS AND CONNECTORS.

3-4. Figure 3-1 shows the Model 1601A front panel and provides functional descriptions of operating controls, indicators, and connectors.

3-5. CLOCK AND DATA INPUTS.

3-6. Clock and data inputs to the Model 1601A are supplied by monitor probes which connect to the front panel CLOCK INPUT and DATA INPUTS connectors. Each monitor probe comprises connecting devices and buffer amplifier - comparators. Input threshold levels for the monitor probe buffer amplifier - comparators are supplied by the Model 1601A. One clock probe and two six channel data probes are required for use with the Model 1601A. Refer to the operating and service literature supplied with the probes for further information.

3-7. DISPLAY MODES.

3-8. Triggering requirements for the Model 1601A are satisfied when a 1 to 12 bit input data word in sync with a CLOCK INPUT pulse matches the TRIGGER WORD switch settings. Starting with the least significant bit (LSB) the switches are set to HI to recognize a positive logic state, LO to recognize a negative logic state, or to OFF for non-required or don't-care input channels. Once triggering requirements are met, the Model 1601A will display 16 sequential words of input data in one of several modes.

3-9. SAMPLE MODE.

3-10. In the repetitive (REPET) sampling mode displayed data is periodically updated every 10 msec to 10 sec (approximately) depending on the setting

15. VAR MEAS. Test point for monitoring VAR SET threshold voltage level.

16. CLOCK slope. Determines whether incoming data is strobed into the instrument on the positive-going edge (out position) or negative-going edge (in position), of the CLOCK INPUT.

17. NO CLOCK HI/LO. Warning light to indicate state of CLOCK INPUT if no display is present.

18. LOGIC NEG/POS. Matches displayed characters to desired logic polarity. POS for positive logic (the most positive level is a 1), or NEG for negative logic (the most negative level is a 1.)

19. MARK ON/OFF. Intensifies the TRIGGER WORD.

20. BYTE BCD/OCT. BCD arranges the displayed 12 bit word format into three bytes of four bits each. OCT arranges the displayed 12 bit word format into four bytes of three bits each.

21. DELAY SET. Thumbwheels used in the START DELAY Trigger Mode to set the number of CLOCK INPUT pulses the display start is delayed from the selected TRIGGER WORD.

22. VERT SIZE. Screwdriver adjustment for setting the vertical size of the 16 word display on the CRT.

23. VERT POSN. Screwdriver adjustment for setting the vertical position of the 16 word display on the CRT.

24. NO TRIG. Warning light to indicate absence of internally generated display trigger. (The display trigger occurs when the input data meets the triggering requirements.)

25. COLUMN BLANKING. Knob adjustment to blank out unused columns. Blanking begins with the most significant bit. The least significant bit cannot be blanked.

26. DISPLAY RATE. Knob adjustment to determine the length of time a 16 word display is retained on the CRT before being updated by the input data.

Figure 3-1. Front Panel Controls, Connectors, and Indicators (Cont'd)

of the DISPLAY RATE control. In the single shot (SINGLE) sampling mode new data is not displayed until the RESET button is pushed. Then one 16 word data block is displayed until RESET is again pushed.

3-11. TRIGGER MODE.

3-12. Free Run. The FREE RUN triggering mode overrides the TRIGGER WORD switch settings. This triggering mode is the equivalent of setting all TRIGGER WORD switches to OFF. Triggering requirements are satisfied by each CLOCK INPUT pulse and all input data words are displayed.

3-13. Start Display. In START DISPLAY, the triggering word (the input data word matching the TRIGGER WORD settings) is positioned at the top of the display with the next 15 input data words positioned in order below the triggering word.

3-14. End Display. In END DISPLAY, the 15 input data words preceding the triggering word are displayed in order from the top of the display with the triggering word positioned at the bottom.

3-15. Start Delay. In START DELAY, any 16 word data block from 0 to 99,999 CLOCK INPUT pluses following the triggering word can be selected for display. The number of CLOCK INPUT pulses that display start is delayed from the triggering word is set on the DELAY SET thumbwheels.

3-16. DISPLAY FORMATS.

3-17. The following controls enable the Model 1601A operator to select the most usable display format for his application.

3-18. Display Rate. The DISPLAY RATE control determines the length of time a given 16 word data block is displayed on the CRT before being updated by new input data. The time between data block updates can be set from approximately 10 msec (fully ccw) to approximately ten seconds (fully cw). Normal setting of the DISPLAY RATE control is from the fully ccw position to the maximum usable update rate.

3-19. Column Blanking. The COLUMN BLANKING adjustment is used to eliminate unused vertical columns on the display. EXAMPLE: When monitoring a series of eight-bit data words, the four unused vertical columns can be removed from the CRT display by adjustment of COLUMN BLANKING. Blanking begins with the most significant bit column. The least significant bit cannot be blanked.

3-20. Logic Neg/Pos. The POS position (out) causes the most positive input voltage level to be displayed as a one, and the most negative level to be displayed as a zero. In NEG (in position), the most negative input level is displayed as a one, and the most positive level is displayed as a zero.

3-21. Mark On/Off. When ON, the triggering word is intensified slightly more than the other displayed data words. In the START DELAY triggering mode, with a DELAY SET of 1 or more, the triggering word is not displayed on the CRT.

3-22. Byte BCD/Octal. In the BCD (binary coded decimal) position (in) displayed data is arranged into four-bit bytes. In OCT (octal) position (out) displayed data is arranged into three-bit bytes.

3-23. OPERATING CONSIDERATIONS.

3-24. The Model 1601A will operate in HP-180 series oscilloscope mainframes. Refer to the mainframe operating and service manual for additional information concerning installation, initial turn-on procedures, adjustments, and operational checks.

3-25. OPERATOR'S CHECKS AND ADJUSTMENTS.

3-26. The following procedure delineates operators preoperational checks and adjustments. Refer to Section V for additional information concerning performance testing and internal adjustments. Refer to Section VIII for troubleshooting information.

Note

Clock and data monitor probes need not be connected for this procedure.

a. Remove power from oscilloscope mainframe.

b. Set Model 1601A controls as follows:

SAMPLE MODE	SINGLE
TRIGGER MODE	FREE RUN
LOGIC	POS
MARK	OFF
BYTE	OCT
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw

c. Apply power and adjust oscilloscope controls to view display.

d. Observe a 12 bit wide, 16 word display on the CRT.

e. Adjust VERT POSN to center 16 word display on the CRT.

f. Adjust VERT SIZE so that first and last words are just inside the upper and lower CRT graticule lines.

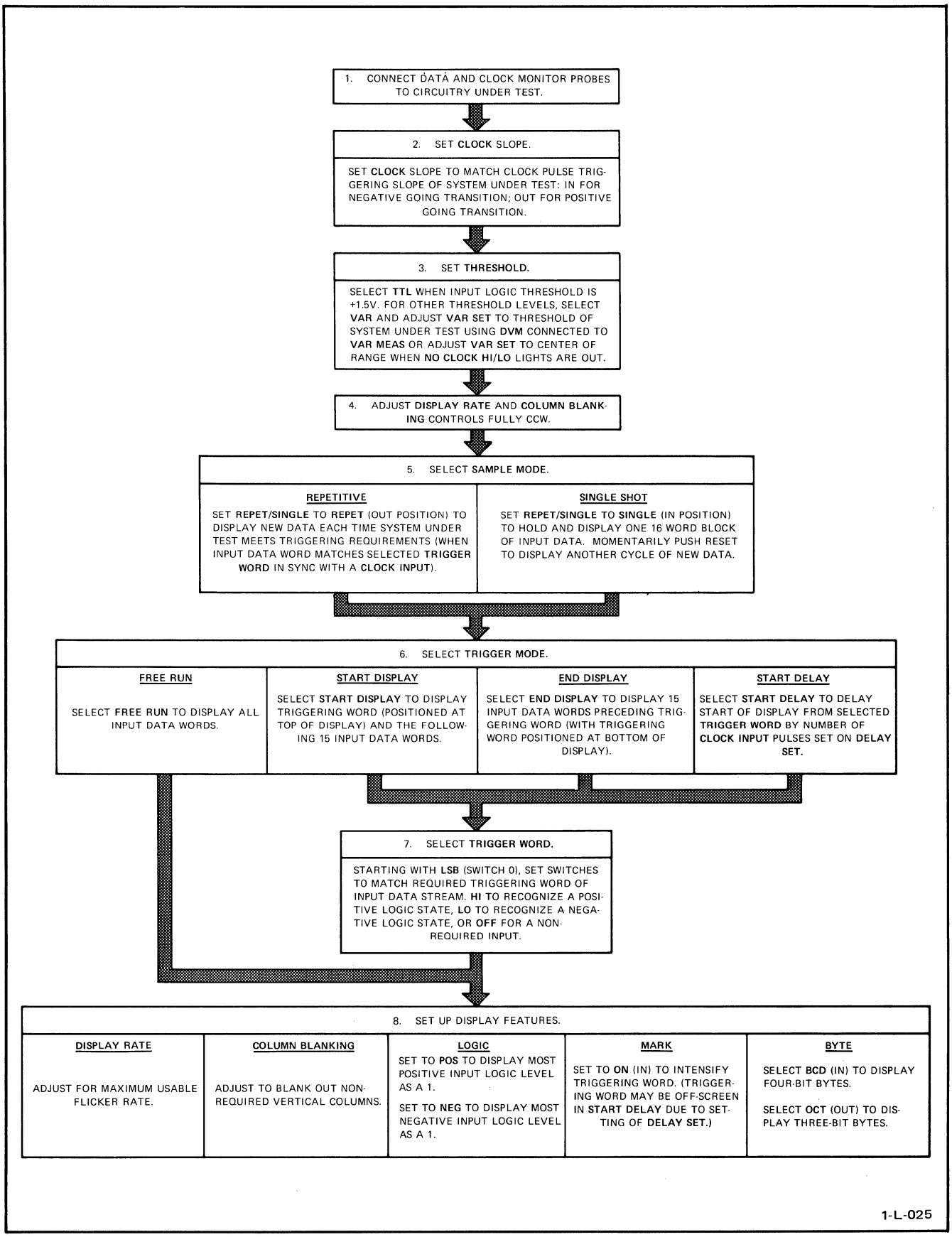


Figure 3-2. Operating Procedure

g. Set BYTE to BCD and observe that display format changes from four three-bit bytes to three four-bit bytes.

h. Set LOGIC to NEG and observe that all zeros change to ones, and that all ones change to zeros.

i. Set DISPLAY MARK to ON, set TRIGGER MODE to START DISPLAY and observe that first word is intensified.

j. Set TRIGGER MODE to END DISPLAY and observe that last word is intensified.

k. Rotate COLUMN BLANKING cw and observe that vertical columns are blanked out starting with the most significant bit (MSB).

l. Rotate COLUMN BLANKING fully cw and observe that the least significant bit (LSB) column remains on the CRT.

m. Rotate COLUMN BLANKING fully ccw.

n. Set TRIGGER MODE to FREE RUN, momentarily push RESET, and observe that entire display is blanked. (If clock and data monitor probes are connected to active circuitry, a new block of data will be displayed when RESET is pushed.)

o. Remove, then reapply power, and observe a 12 bit wide, 16 word display on the CRT.

3-27. OPERATING PROCEDURE.

3-28. The Model 1601A operating procedure is shown in figure 3-2. Refer to the oscilloscope operating and service manual for related operating information.

3-29. SINGLE SAMPLE MODE

3-30. The Model 1601A requires a minimum of sixteen CLOCK INPUT pulses to generate a display. Thus, a display may not appear when observing single shot phenomena of less than sixteen discrete states. Pushing the CLOCK slope control will generate artificial clock pulses and allow the stored data to be displayed.

SECTION IV

PRINCIPLES OF OPERATION

4-1. INTRODUCTION.

4-2. This section describes the Model 1601A block diagram principles of operation. The instrument block diagram and schematics are located in section VIII.

4-3. When installed in an HP 180-series oscilloscope mainframe, the Model 1601A displays sixteen sequential 12-bit words of parallel input data on the CRT from top to bottom. Input data is supplied by clock and data probes consisting of circuit connecting devices and buffer-comparators. Operating and service information for the clock and data probe is contained in documentation supplied with each probe.

4-4. The CRT display consists of the binary digits "1" and "0". These digits provide a functional indication of input data states. A clock input, from the system under test, strobes input data into the Model 1601A memory. In the REPET (repetitive) SAMPLE MODE, incoming data automatically updates the memory each sampling cycle. In the SINGLE (single shot) SAMPLE MODE, gathered data is retained and displayed until manually reset. A preset TRIGGER WORD, set on the front panel, controls the position of the sixteen word display in reference to the input data stream. Depending on the TRIGGER MODE selected, the display starts at the triggering word, ends at the triggering word, or is delayed up to 99,999 clock input pulses after the triggering word.

4-5. BASIC INFORMATION.

4-6. The following paragraphs describe logic conventions used to describe the Model 1601A principles of operation.

4-7. LOGIC STATES.

4-8. The terms HI and LO describe the output states of logical circuit elements. HI indicates the most positive dc level, and LO indicates the most negative dc level produced by a given circuit element.

4-9. LOGIC TERMS.

4-10. Interconnecting signals (logic terms) in the Model 1601A are assigned names which indicate the respective active state and function of a signal.

4-11. A prefix letter (H, L, P, or N) indicates the active state of the term and the remaining letters indicate its function. An H prefix indicates the term function is active in the HI state, and an L prefix indicates the term is active in the LO state. For edge controlled devices, the prefix P indicates the term function is active on the positive-going transition, and the prefix N indicates the term function is active on the negative-going transition.

4-12. Logic term functional definitions and points of origin are listed alphabetically in table 4-1.

4-13. LOGIC CIRCUITRY.

4-14. Most of the integrated circuits in the Model 1601A are in the TTL (Transistor-Transistor Logic) family of digital devices. A LO output from a TTL device is $\leq$0.4V and a HI output is $\geq$2.5V.

4-15. FUNCTIONAL OPERATION.

4-16. Figure 4-1 presents the functional operation of the Model 1601A in reference to the input data stream. The instrument alternates between a data sampling cycle and a display cycle. Progression from a sample/display set can be repetitive (REPET) or manual (SINGLE). During a data sampling cycle, input data is gathered and loaded into the memory according to the requirements of the selected TRIGGER MODE. When the data of interest has been gathered and stored in the memory, a display cycle is initiated. Stored data is read out of the memory and applied to the CRT as update information. When all stored data has been read and displayed, the instrument is ready for another data sampling cycle.

4-17. Figure 4-2 presents the functional sequence of events within the Model 1601A for the data sampling and display cycles.

4-18. DATA SAMPLING CYCLE.

4-19. Each word of input data is temporarily stored before being loaded into the memory. The input data is also compared (after temporary storage) with the front panel TRIGGER WORD switch positions. When an input data word matches the preset TRIGGER WORD, the Model 1601A performs a data acquisition algorithm. The operation of the data acquisition algorithm is controlled by the TRIGGER MODE selected. The algorithm controls memory loading and determines when gathered data is ready for display. When all algorithmic requirements have been satisfied, HDR occurs. The occurrence of HDR transfers the Model 1601A into a display cycle.

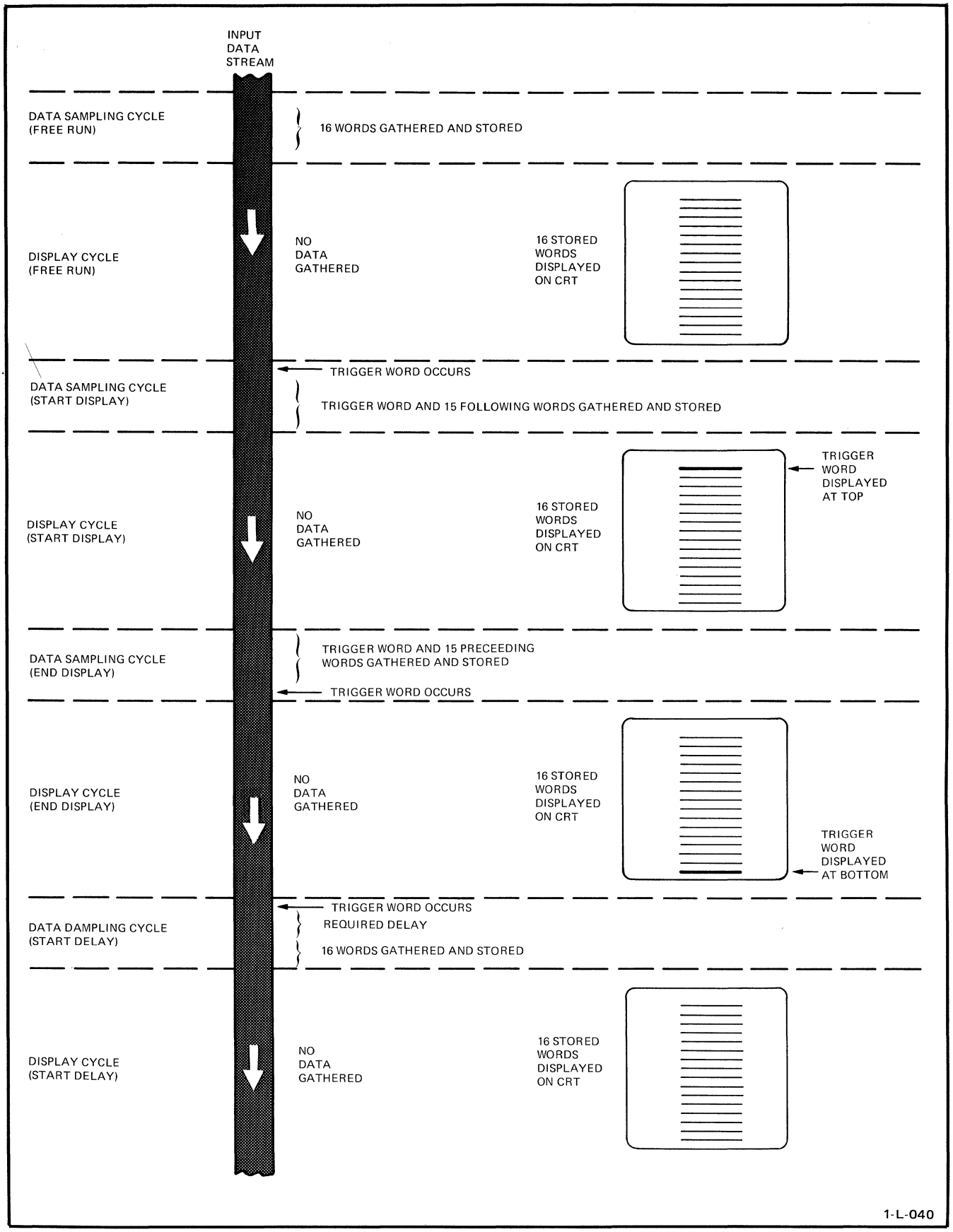


Figure 4-1. Functional Operation

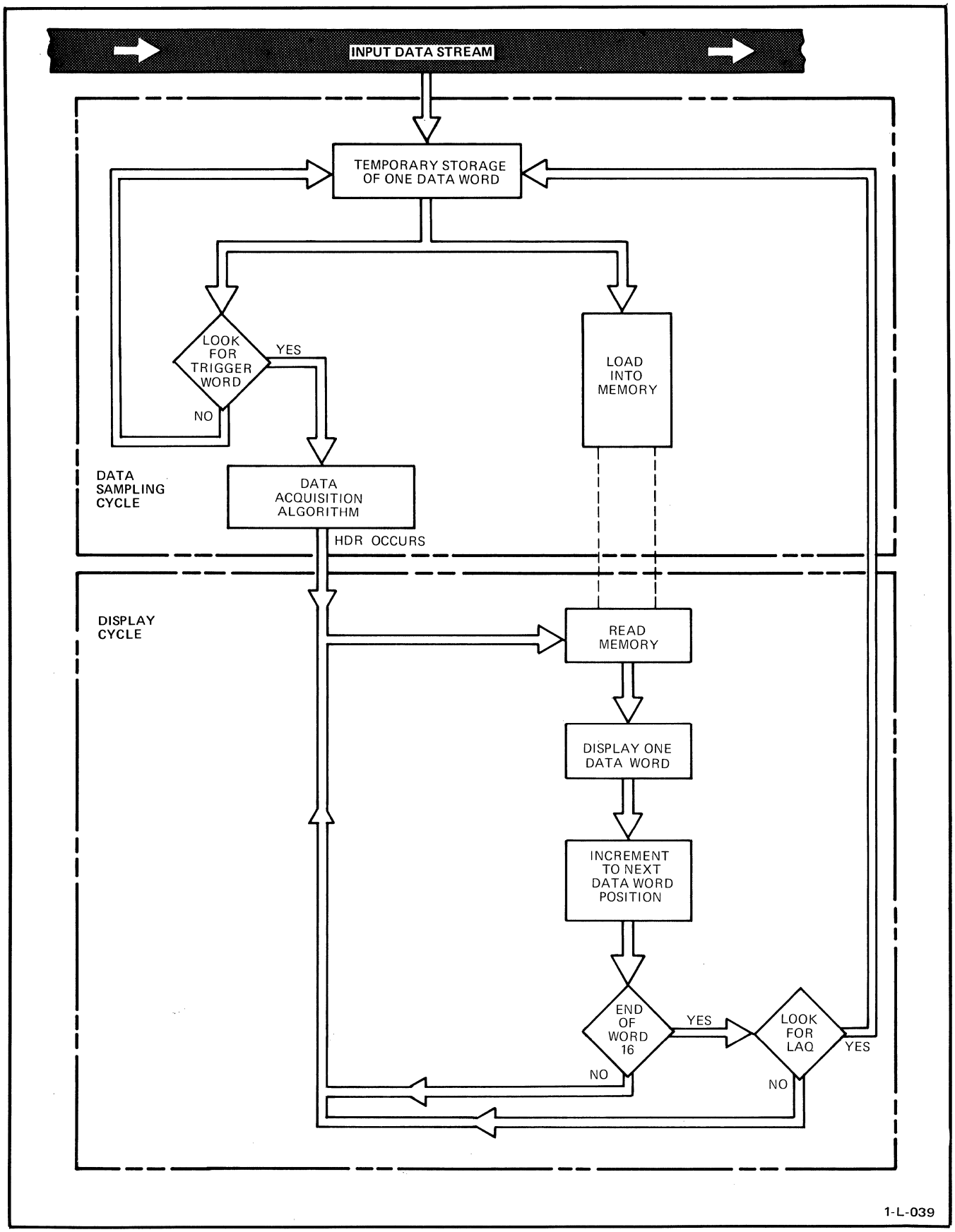


Figure 4-2. Functional Sequence of Events

4-20. DISPLAY CYCLE.

4-21. The display cycle begins with the occurrence of HDR. Information stored in the memory during the previous data sampling cycle is read out and displayed one word at a time. At the end of each displayed word, the Model 1601A increments to the next data word position on the CRT. This process continues until the end of the sixteenth displayed word. At the end of the sixteenth word, the instrument checks the SAMPLE MODE selected and the DISPLAY RATE control setting to determine if new data is required. When new data is not required, the display cycle repeats. When new data is required, the term LAQ (Low Acquire) occurs. The occurrence of LAQ transfers the Model 1601A into a data sampling cycle.

4-22. BLOCK DIAGRAM.

4-23. Figure 8-3 is the Model 1601A block diagram. Heavy lines enclose circuitry contained on a specific schematic. The instrument contains two major sections, a data sampling section and a display section. The data sampling section consists of the circuitry shown on schematics 4, 5, 6, and 7. The display section consists of the circuitry shown on schematics 8, 9, and 10.

4-24. DATA SAMPLING SECTION.

4-25. Input Control. Inputs to the Model 1601A are supplied by a clock probe and two data probes. The input threshold level for the clock and data probes is originated by the Model 1601A threshold supply. With the TTL (Transistor-Transistor Logic) pushbutton in, the threshold level is fixed at +1.5V. With VAR selected, the threshold level is variable from +10V to —10V by VAR SET. The threshold supply also supplies two clock slope commands (SS and SI) to the clock probe. These commands, controlled by the CLOCK pushbutton, determine which transition of the input clock signal transfers input data into the Model 1601A.

4-26. The clock probe supplies three buffered inputs, PCLK, NCLK, and CLK AVG. The leading edge transitions of PCLK and NCLK are syncronous with data inputs from the data probes. When CLOCK is out (⌐), the leading edge transition of PCLK goes from negative to positive, and the leading edge transition of NCLK goes from positive to negative. With these conditions, data is clocked into the Model 1601A on the positive going transition of the input clock signal. When CLOCK is in, (¬), the leading edge transitions of PCLK and NCLK reverse direction and data is clocked on the negative going transition of the input clock signal.

4-27. PCLK transfers input data into temporary storage, and enables the data acquisition control circuitry to begin a data acquisition algorithm after the occurrence of LAQ. The clock shaping circuitry isolates and amplifies NCLK for production of HACL (a 40 ns wide internal clocking signal), and the front panel CLOCK OUTPUT signal. CLK AVG is a dc average of the input clock signal from the system under test. CLK AVG is compared with the threshold voltage for control of the NO CLOCK HI/LO indicators.

4-28. Temporary Storage. Buffered input data from the data probes is applied to a series of D flip-flops for temporary storage. The temporary storage flip-flops produce two complimented 12-bit output words, T0 through T11 and $\overline{T0}$ through $\overline{T11}$. When clocked by PCLK both output words are applied to the pattern recognition gates and the $\overline{T}$ word is applied to the memory. The pattern recognition gates compare the TRIGGER WORD switch settings with each input data word. When a match occurs, LTRIG, a 40 ns pulse enabled by HACL, is produced. LTRIG is applied to the data acquisition control circuitry for control in the data acquisition algorithm and inverted to produce the front panel TRIGGER OUTPUT signal.

4-29. Memory/Multiplexer. The memory/multiplexer and associated circuit (including the front panel LOGIC NEG/POS switch) converts the T temporary storage word into a control signal (LZER) which determines whether a one or a zero is displayed on the CRT for a given bit of input data.

4-30. During a data sampling cycle, the states of LWE and LDR enable the $\overline{T}$ outputs from temporary storage to be loaded into the memory. When data acquisition is completed, and a display cycle begins, memory loading is inhibited and memory read-out and multiplexing begin. The states of LDR, PMAC and SCH3 (most significant output bit of horizontal state counter) control memory readout. The horizontal state counter outputs SCH0, SCH1, and SCH2 address the multiplexer.

4-31. The complimentary outputs of the multiplexer are applied to polarity control gates and compared with the position of the LOGIC NEG/POS pushbutton. When in POS (out) the states of LZER causes the most positive input logic level to be displayed as a one on the CRT. When in NEG (in), the states of LZER causes the most negative input logic level to be displayed as a one.

4-32. Data Acquisition Control. The data acquisition circuitry controls the memory loading, delay generator action, and the transfer from a data sampling cycle to a display cycle. The action of the data acquisition circuitry is controlled by the TRIGGER MODE selected, the occurrence of LAQ (a transfer from a display to a data sampling cycle), and the occurrence of LTRIG (a match of an input data word to the TRIGGER WORD switch settings).

4-33. The TRIGGER MODE switches control the status of three commands, LFR, LSRT, and LNDLY. These commands set up data acquisition requirements for a specific TRIGGER MODE. The occurrence of LAQ ends a display cycle and begins data acquisition. The occurrence of LTRIG synchronizes data acquisition with the input data stream and the occurrence of HDR ends data acquisition and begins a new display cycle.

4-34. Figure 4-3 illustrates the data acquisition requirements for each TRIGGER MODE. In FREE RUN, memory loading begins at the occurrence of LAQ without regard to a preset TRIGGER WORD. When sixteen data words have been stored, HDR occurs and a display cycle begins. In START DISPLAY, the occurrence of LTRIG enables memory loading. After the triggering word and the following fifteen data words have been loaded, HDR occurs. In END DISPLAY, input data words are continuously loaded in the memory until LTRIG. The occurrence of LTRIG stops memory loading with the triggering word, and enables HDR. In START DELAY, the occurrence of LTRIG enables the Delay Generator to count the number of CLOCK INPUT pulses preset on the DELAY SET thumbwheels. At Delay Generator terminal count, the memory is loaded with sixteen words and HDR occurs.

4-35. During data acquisition several control signals occur. LWE, enabled during a sampling cycle, is a clocking signal which controls memory loading. PMAC is the Delay Generator clock signal during a sampling cycle, and the memory increment command during a display cycle. Both LWE and PMAC are functions of HACL during a sampling cycle. When a display cycle starts, LWE is disabled and PMAC becomes a function of PMAI from the display section. HDEN and LNDLY activate the delay generator in the START DELAY TRIGGER MODE. HEN1, HEN2, and HNDLY indicate that the delay generator has counted the required number of input clock pulses and that data acquisition may begin. HBR1 controls first line intensification in the display section. LDR and HDR indicate to other circuit blocks the transfer between data sampling and display cycles.

4-36. DISPLAY SECTION.

4-37. The display section of the Model 1601A contains the necessary circuitry to generate horizontal, vertical, and unblanking drive to an oscilloscope CRT. Contained on these output signals is information which both positions the CRT electron beam, and determines whether a one or a zero is displayed. Data words are displayed from top to bottom, with specific bits displayed from right to left (Least Significant Bit to Most Significant Bit).

4-38. The horizontal and vertical drive circuits are synchronized together during a display cycle. When a display cycle begins, both the horizontal and vertical circuits are enabled and data is applied to the CRT. When the first data word has been displayed, the vertical circuitry moves the CRT electron beam to the second word position and the next data word is displayed. This process continues until the end of the sixteenth data word. If new data is required, LAQ occurs and a new data sampling cycle is initiated. If new data is not required, the memory contents are re-read and displayed as required.

4-39. When LAQ occurs, the display section is reset and the horizontal and vertical drive circuitry is reset and held in their beginning states until the next display cycle starts.

4-40. In the SINGLE SAMPLE MODE, a display cycle continues until LAQ is manually generated when RESET is pushed. In addition, when SINGLE is selected before power turn-on, display control logic determines that the Model 1601A will start-up in a display cycle at initial power application. This allows an initial CRT display whether or not probes are connected.

4-41. Character Generation. To display a zero on the CRT, the Model 1601A superimposes sine wave signals on the horizontal and vertical drive outputs. The horizontal sine wave signal is shifted 90 degrees in phase from the vertical signal causing the CRT electron beam to display a small lissajou pattern on the CRT face. By inhibiting the sine wave signal to the horizontal drive circuitry, leaving vertical deflection with no corresponding horizontal deflection, the CRT electron beam displays a one.

4-42. One/Zero Switch. The control signal LZER from the memory/multiplexer circuitry controls the one/zero switch. When an input data bit is to be displayed as a zero, the state of LZER enables 100 kHz to be applied to the horizontal drive circuitry. When an input data bit is to be displayed as a one, the state of LZER inhibits the application of 100 kHz to the horizontal drive circuitry.

4-43. Oscillator Circuitry. A 100 kHz free running oscillator generates the sine wave signal used for character generation and for display timing. Character size is adjusted by A2R50 which controls the oscillator output amplitude. The 100 kHz sine wave is applied to a Schmitt Trigger and a divide by two flip-flop to produce 50 kHz complimentary display timing signal PDCL and NDCL.

4-44. Display Control. Display control determines the length of a display cycle by controlling the time between HDR and LAQ.

4-45. In the REPET SAMPLE MODE, the occurrence of HDR starts a display cycle. During a display cycle, LHR enables the horizontal state counter, and HDE enables the vertical state counter. With the

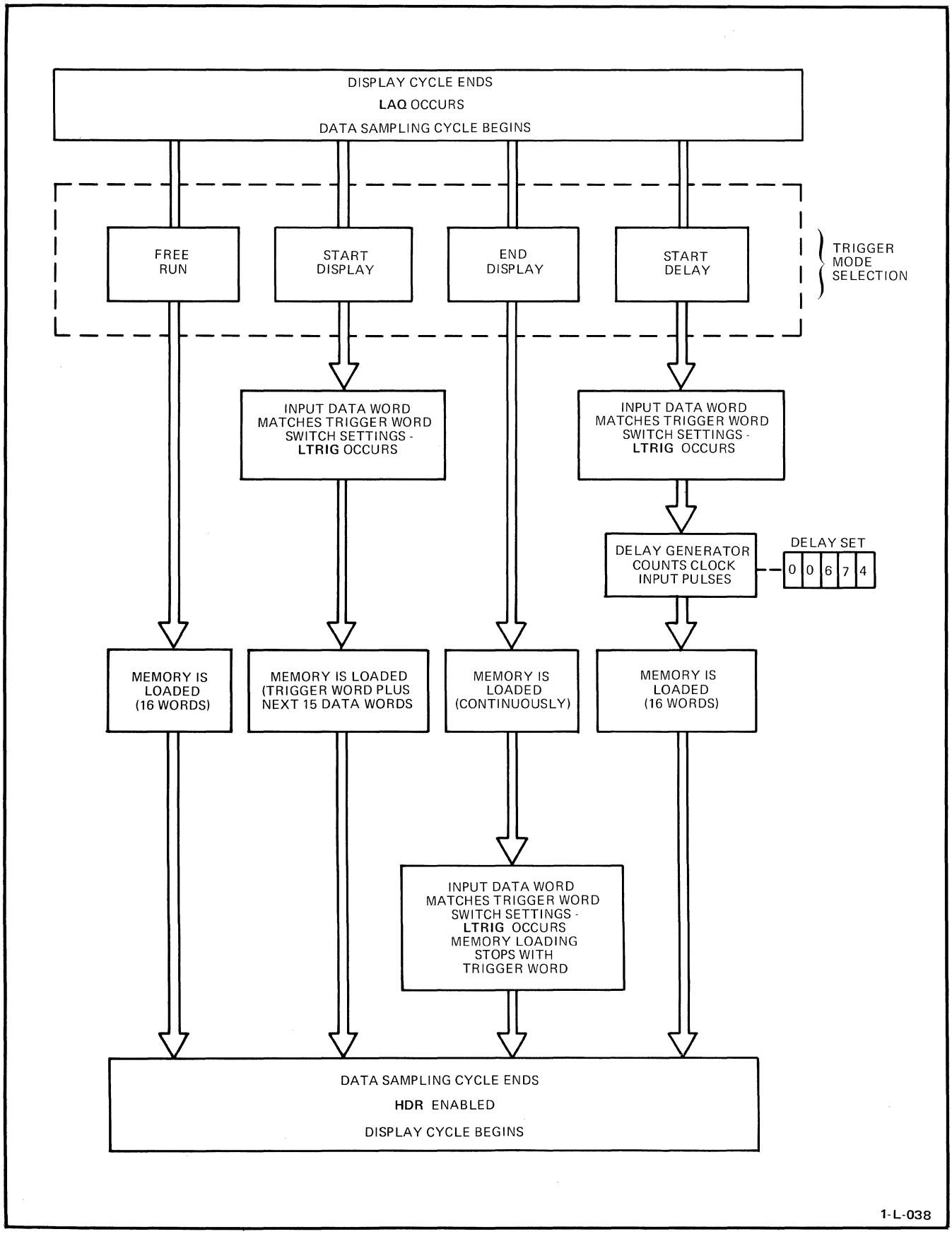


Figure 4-3. Data Acquisition Requirements

state counters operating, the contents of the memory are read and data is displayed on the CRT. At the end of the sixteenth displayed word, SCV3 attempts to initiate LAQ and transfer the Model 1601A into a new data sampling cycle.

4-46. If a high data update rate is required, (caused by a ccw setting of DISPLAY RATE), VS3 is allowed to initiate LAQ at the end of the sixteenth displayed word of alternate 16 word data blocks. If a low data update rate is required (caused by a cw setting of DISPLAY RATE), existing data in the memory is re-read and displayed until the display time required by the setting of DISPLAY RATE is satisfied. When the DISPLAY RATE requirement is satisfied, LAQ is allowed to occur, resetting the horizontal and vertical state counters to their beginning states, terminating the display cycle, and transferring the Model 1601A to a data sampling cycle.

4-47. During a display cycle, PMAI is supplied to data acquisition control for memory read-out timing. PMAI is a function of HVLI which is the horizontal state counter terminal count and occurs at the end of each displayed horizontal word.

4-48. Horizontal Drive Circuitry. The horizontal state counter has a capacity of twelve states, one for each bit position of a displayed horizontal word. When enabled by LHR, the horizontal state counter counts PDCL pulses to a full count (12 states). When twelve states have been produced, HVLI occurs. HVLI resets the horizontal state counter to its beginning state and enables the vertical state counter to advance one state which positions the beam for the next displayed word.

4-49. The horizontal state counter outputs (SCH0 through SCH3) are applied to a ROM (Read Only Memory) which converts them to a series of twelve 4-bit coded words. SCH0 through SCH3 are also applied to the data sampling section to address the multiplexer. The ROM output words are converted by a D/A (digital to analog) converter to produce a twelve position staircased horizontal drive current ramp. 100 kHz is superimposed on the appropriate step of the horizontal ramp when a zero is to be displayed on the CRT.

4-50. Vertical Drive Circuitry. The vertical state counter has a capacity for sixteen states, one for each word position of a sixteen word CRT display. HDE enables the vertical state counter during a display cycle. At the end of each displayed horizontal word, HVLI enables the vertical state counter to be incremented to the next state by PDCL. The vertical state counter outputs (SCV0 through SCV3) are converted by a D/A converter to produce a sixteen position staircased vertical current ramp. For each step of the vertical ramp, one twelve step horizontal ramp is produced. SCV3 is also applied to display control for generation of LAQ. 100 kHz is superimposed on the vertical ramp for character generation.

4-51. The vertical current ramp is applied to a differential amplifier to produce vertical deflection voltage to the CRT plates. VERT SIZE and VERT POSN adjust the vertical drive output to compensate for differences in CRT characteristics.

4-52. CRT Unblanking. The Model 1601A operates in HP 180-series mainframes which require approximately 2 mA of current to unblank the CRT at a normal intensity level. An increase in the current supplied to the mainframe will cause a corresponding increase of displayed intensity.

4-53. During a display cycle, HDE and NDCL enable the unblanking gate current source to supply approximately 2 mA to the mainframe gate amplifier for each displayed bit. A cw adjustment of the COLUMN BLANKING control generates an inhibit function which blanks out unused columns. The inhibit function is controlled by LHR and PDCL.

4-54. Triggering word intensification is actuated by the MARK pushbutton except during the FREE RUN TRIGGER MODE. As there is no specific triggering word in FREE RUN, LFR inhibits intensification. In the START DISPLAY TRIGGER MODE, first word intensification is enabled by HBR1, SCV0 through SCV3 identify the occurrence the first word. In the END DISPLAY TRIGGER MODE, last word intensification is enabled by LSRT while HVTC identifies the occurrence of the last word. In the START DELAY TRIGGER MODE, with a DELAY SET of one or more, intensification is inhibited by the state of HBR1.

Table 4-1. 1601A LOGIC TABLE

TERM	FUNCTION	ORIGIN
CLK AVG	Clock Average. A dc average of the clocking signal from the system under test. Compared with THRESHOLD for operation of NO CLOCK HI/LO indicators.	Clock probe input applied to CLOCK INPUT connector. Schematic 4, J3, PIN 16
DEH0-DEH3	Decoded Horizontal Bits 0 through 3. ROM output bits. Each 4-bit word indicates a specific horizontal bit position in a displayed word. The output words change with the state of LOCT, the output of the BYTE switch.	Schematic 7, A2U37
HACL	HI, Acquisition Clock. A reshaped, amplified NCLK. Used for data acquisition timing. Applied to front panel CLOCK OUTPUT connector.	Schematic 7, A2U22A, PIN 3
HBR1	HI, Brighten Word 1. When HI, enables intensification of triggering word in START DISPLAY trigger Mode. HBR1 = HI, in START DISPLAY and START DELAY when DELAY SET = 00000. HBR1 = LO in FREE RUN and END DISPLAY.	Schematic 7, A1U31B, PIN 4
HDE	HI, Display Enable. HI state occurs during display cycle. Applies parallel enable to Vertical State Counter, and enables unblanking.	Schematic 9, U2U35B, PIN 9
HDLE	HI, Delay Enable. When HI (during sampling cycle), allows Delay Generator (A1A2) to start if in START DELAY.	Schematic 7, A2U28B, PIN 9
HDR	HI, Data Ready. HI state occurs at end of data acquisition algorithm. Indicates end of sampling cycle and beginning of display cycle.	Schematic 7, A2U30D, PIN 8
HEN1, HEN2	HI, Enable 1 and 2. Delay Generator outputs. HEN1-HI indicates terminal count of 10^{0} decade. HEN2-HI indicates terminal count of 10^{1} thru 10^{4} decades. Both outputs remain LO in START DISPLAY and END DISPLAY.	Schematic 8, EN1, A2A1U1, PIN 15 EN2, A2A1U5, PIN 15
HINT	HI, Intensify. When HI, allows intensification of triggering word.	Schematic 10, A4S1B
HNDLY	HI, No Delay. A control signal to the State Counter. When HI (in START DISPLAY and in START DELAY with no DELAY SET), it enables LTRIG to start the State Counter. When LO (in START DELAY with DELAY SET of one or more), it enables HEN1 and HEN2 to start the State Counter.	Schematic 8, A2A1U7B, PIN 6
HNT	HI, No Trigger. Compliment of HDLE. A NO TRIG indicator control signal. Remains HI if LTRIG does not occur during a sampling cycle.	Schematic 7, A2U28B, PIN 8
HSS	HI, Single Sample. Control signal to Display Control Circuiting which holds instrument in the SINGLE Sample Mode.	Schematic 9, SINGLE/REPET switch, A3S1E.
HVLI	HI, Vertical Line Increment. Terminal Count of the Horizontal State Counter. When HI (at horizontal bit position 12), allows the Vertical State Counter to increment one count to the next displayed word position, and enables PMAI.	Schematic 9, A2U36, PIN 15
HVTC	HI, Vertical Terminal Count. Terminal Count of the Vertical State Counter. When HI (at the 16th displayed word), identifies the occurrence of the last displayed word to the last line intensifier.	Schematic 9, A2U38, PIN 15

Table 4-1. 1601A LOGIC TABLE (Cont'd)

TERM	FUNCTION	ORIGIN
LAQ	LO, Acquire. LO state occurs at end of display cycle. Transfers instrument into sampling cycle.	Schematic 9, A2U34B, PIN 1
LCLR	LO, Clear. LO state occurs during time of LAQ. Resets data acquisition circuitry for the beginning of a data acquisition algorithm.	Schematic 7, A2U28A, PIN 6
LDE	LO, Display Enable. LO state occurs during display cycle. Applies parallel enable to the Horizontal State Counter (through U40A), and enables operation of DISPLAY RATE control.	Schematic 9, A2U35B, PIN 8
LDR	LO, Data Ready. When LO (during a display cycle), inhibits memory loading and operation of Delay Generator. LO to HI transition controls HNDLY generation in START DELAY.	Schematic 7, A2U30C, PIN 3
LFR	LO, Free Run. Data acquisition algorithm control signal. When LO (FREE RUN in), places instrument in FREE RUN Trigger Mode. LFR = LO in FREE RUN. LFR = HI in START DISPLAY, END DISPLAY, and START DELAY.	Schematic 7, FREE RUN switch, A3S1F
LHR	LO, Horizontal Reset. Horizontal State Counter parallel enable signal. At Horizontal State Counter terminal count (12th bit position on CRT) LHR goes LO, resetting Horizontal State Counter and COLUMN BLANKING circuitry.	Schematic 9, A2U40A, PIN 8
LNDLY	LO, No Delay. Delay Generator control signal. When HI, arms Delay Generator. When LO, disables Delay Generator. LNDLY = HI in FREE RUN and START DELAY. LNDLY = LO in START DISPLAY and END DISPLAY.	Schematic 7, START DISPLAY Switch, A3S1G
LOCT	LO, Octal. Address control signal for ROM (A2U37). When LO, displayed bit format is four 3-bit bytes (OCT). When HI, displayed bit format is there 4-bits (BCD).	Schematic 9, A4S1C
LPOS	LO, Positive. When LO (POS position), the most positive level of the input data is displayed as a one on the CRT.	Schematic 6, LOGIC NEG/POS Switch, A4S1A
LSRT	LO, START. Data acquisition algorithm control signal. LSRT = LO in START DISPLAY and START DELAY. LSRT = HI in FREE RUN and END DISPLAY.	Schematic 7, START DISPLAY Switch, A3S1G
LTRIG	LO, Trigger. Triggering signal (LO state) indicating input data matches settings of TRIGGER WORD switches.	Schematic 5, A2U13, PIN 8
LWE	LO, Write Enable. Clocking signal to allow memory loading. Occurs during data sampling cycle (when LDR is HI).	Schematic 7, A2U22B, PIN 6
LZER	LO, Zero. Determines whether a one or a zero is displayed on the CRT. When LO, 100 kHz is applied to the Horizontal D/A converter causing a zero to be displayed.	Schematic 6, A2U19 A and B, PINS 3 and 11
NCLK	Negative (Transition) Clock. A buffered TTL reproduction of the clocking signal from the system under test. The compliment of PCLK.	Clock Probe input applied to CLOCK INPUT connector. Schematic 4, J4, PIN 11
NDCL	Negative Display Clock. The compliment of PDCL. A 50 kHz clocking signal used in unblanking control.	Schematic 9, A2U46A, PIN 6

Table 4-1. 1601A LOGIC TABLE (Cont'd)

TERM	FUNCTION	ORIGIN
PCLK	Positive (Transition) Clock. A buffered TTL reproduction of the clocking signal from the system under test.	Clock Probe input applied to CLOCK INPUT connector. Schematic 4, J3, PINS 12, 13
PDCL	Positive Display Clock. A 50 kHz clocking signal used for timing and syncronization in the display section circuiting.	Schematic 9, A2U46A, PIN 5
PMAC	Positive (Transition), Memory Address Clock. Addresses memory for readout during display cycle (a function of PMAI) and advances delay generator during sampling cycle (a function of LWE).	Schematic 7, A2U22D, PIN 11
PMAI	Positive Memory Address Increment. A 50 kHz clocking signal which increments memory readout during a display cycle. Inhibited at Horizontal State Counter Terminal count by HVLI.	Schematic 9, A2U34C, PIN 8
S0H-S11H	Trigger Word switch outputs for the HI position. TERM = +5V when applicable switch placed in HI and ≈ —.6V when OFF or LO.	Schematic 5, A6S0 thru S11
S0L-S11L	Trigger Word switch outputs for the LO position. TERM = +5V when applicable switch is placed in LO and ≈ —.6V when OFF or HI.	Schematic 5, A6S0 thru S11
SI	Slope Invert. Clock slope command signal to the Clock Probe. The compliment of SS. SI = HI when CLOCK is ⎍ (out), and LO when CLOCK is ⎏ (in).	Schematic 7, A2U21A, PIN 6
SS	Slope Switch. Clock slope command signal to the Clock Probe. SS and SI control the PCLK and NCLK leading edge transitions in reference to the clocking signal from the system under test. SS = LO when CLOCK is ⎍ (out) and HI when CLOCK is ⎏(in).	Schematic 7, CLOCK switch, A3S1A
T0-T11	Temporary Storage register output bits 0 thru 11.	Schematic 5, U1 thru U6.
$\overline{\text{T0-T11}}$	Complimented Temporary Storage register output bits 0 thru 11.	Schematic 5, U1 thru U6
THRESHOLD	A dc level applied to the Clock and Date Probes which matches the probe comparator switching threshold to the system under test.	Schematic 7, A2U20, PIN 6
SCH0-SCH3	Horizontal State Counter output bits 0 through 3. The 12 output states (representing specific horizontal bit positions in a displayed word) address the ROM and the multiplexer.	Schematic 9, A2U36
SCV0-SCV3	Vertical State Counter output bits 0 thru 3. The 16 output states (representing specific word positions on the CRT) are converted by the Vertical D/A Converter to 16 position staircased vertical deflection ramps.	Schematic 9, A2U38

SECTION V

PERFORMANCE CHECK AND ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section contains step-by-step procedures for checking instrument specifications (table 1-1), functional capabilities, and for making internal adjustments.

5-3. TEST EQUIPMENT.

5-4. Test equipment required for procedures in this section is listed in Table 5-1. Test equipment equivalent to that recommended may be substituted, provided it meets the required characteristics listed in the table. For best results, use recently calibrated test equipment.

5-5. PERFORMANCE CHECK.

5-6. The performance check describes procedures for an initial operational check, for checking specifications listed in table 1-1, and for a functional check of all other instrument capabilities. The performance check can be used as part of an incoming inspection, as a periodic operational test, or to check calibration after repair or adjustments have been made. Specific checks can be made separately if desired. If instrument does not perform as specified, refer to the fault isolation procedure in Section VIII.

5-7. A table (performance check record) is provided at the end of the performance check for recording the measurements obtained in the first running of the procedure. This record may be used to compare measurements taken at later dates with the original. The first time the performance check is made, enter the results on the performance check record. Remove the record from the manual and file it for future reference. Be sure to include the instrument serial number on the record for identification.

5-8. INITIAL OPERATIONAL CHECK.

5-9. The following procedure is an initial operational check. The test equipment setup described herein is used as a basis for several of the specification and functional checks, and for waveforms and dc levels shown on the schematics in Section VIII.

a. Refer to figure 5-1 for recommended test equipment setup.

b. Apply waveforms shown in figure 5-2 to the clock and data probe (bits 0 through 11) inputs of the Model 1601A.

c. Set Model 1601A controls as follows:

CLOCK	⌐ (out)
THRESHOLD	TTL
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw
SAMPLE MODE	REPET
TRIGGER MODE	START DISPLAY
TRIGGER WORD	bits 0 through 11 to HI
LOGIC	POS

d. Adjust Model 1601A mainframe controls to observe a 12 bit wide, 16 word display of all ones.

e. Set TRIGGER WORD switch 3 to OFF.

f. Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded. This check indicates that the Model 1601A is properly accepting and displaying data supplied to the probe inputs.

5-10. SPECIFICATION CHECK.

5-11. Paragraphs 5-12 through 5-20 contain performance checks of specifications listed in table 1-1.

5-12. Input RC. Specification: 40 ±3K ohms shunted by ≤14 pF.

a. Apply power to Model 1601A and set THRESHOLD to VAR.

b. Connect a clock probe and 2 data probes to the Model 1601A input connectors.

c. Connect all color-coded connecting leads and circuit probe tips to the clock and data probes.

d. Using multimeter, monitor VAR MEAS and adjust VAR SET to +10 Vdc.

Note

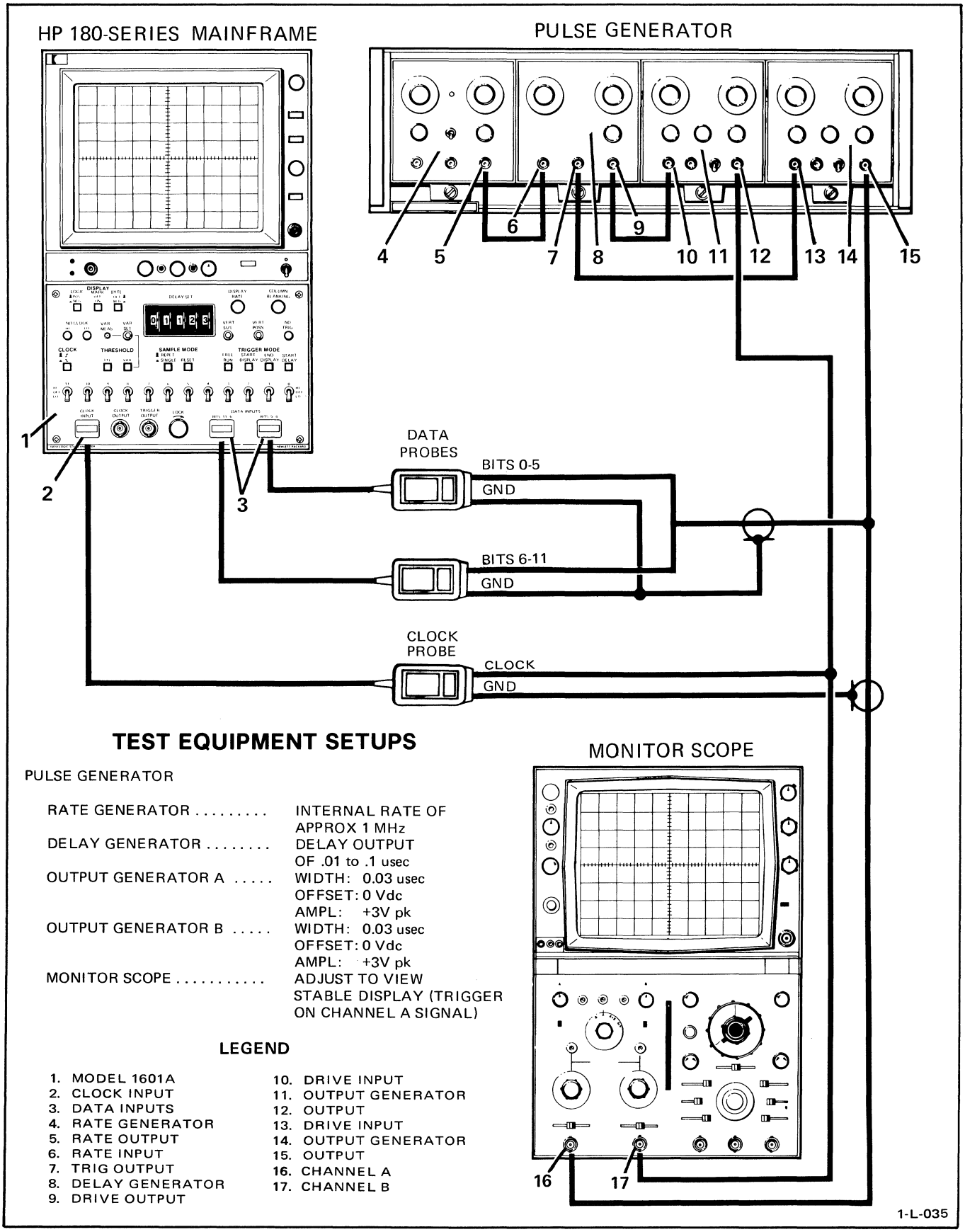
When making input RC measurements, keep leads straight and untangled. For accurate measurements, connect probe ground lead to meter ground terminal.

e. Using multimeter, sequentially measure resistance between each data probe bit input and ground, and between the clock probe clock input and ground. Observe that each measurement is 40 ±3K ohms.

Table 5-1. Recommended Test Equipment

Instrument Type	Recommended Model	Required Characteristics	Required For
Oscilloscope Mainframe	HP 180-series	No substitute	Performance Check, Adjustments, and Troubleshooting
Clock Probe	HP 10230A	No substitute	Performance Check and Troubleshooting
Six-Bit Data Probe	HP 10231A	No substitute	Performance Check and Troubleshooting
Monitor Oscilloscope	HP 180-series with plug-ins	General purpose, 50 MHz	Performance Check and Troubleshooting
Vertical Plug-in	HP 1808A	50 ohm input, 50 MHz bandwidth	Performance Check and Troubleshooting
Time Base Plug-in	HP 1824A	50 nsec/div, 50 MHz bandwidth	Performance Check and Troubleshooting
Pulse Generator	HP 1900-series with plug-ins	Adjustable 0 to 10 MHz	Performance Check and Troubleshooting
Rate Generator	HP 1906A	Adjustable 0 to 10 MHz Rate Output	Performance Check and Troubleshooting
Delay Generator	HP 1909A	Adjustable 0 to 1 usec delay	Performance Check and Troubleshooting
Output Plug-in (Two)	HP 1921A	Adjustable 0 to 5 Vpk amplitude; Positive and Negative polarity; Adjustable 0 to .5 usec width; Adjustable 0 to 5V offset	Performance Check and Troubleshooting
Multimeter	HP 3340A with HP 3444A plug-in	dc current 0 to 30 uA; dc voltage, 0 to 10V; Resistance, 0 to 43K ohms	Performance Check, Adjustments, and Troubleshooting
LCR Meter	HP 4332A	Capacitance, 0 to 14 pF	Performance Check and Troubleshooting
Timer-Counter	HP 5327A	External rate input; Time interval A to B measurement with 0.1 usec	Performance Check and Troubleshooting
dc Power Supply	HP 6299A	±5 Vdc output	Performance Check and Troubleshooting
50 ohm bnc feedthru	HP 11048B	50 ohm feedthru termination	Performance Check
4-Bit Binary Counter	9316 Integrated Circuit	4-bit parallel binary output	Performance Check and Troubleshooting
Function Generator	HP 3310A	±10V offset	Performance Check

7000-A-19A



TEST EQUIPMENT SETUPS

PULSE GENERATOR

RATE GENERATOR	INTERNAL RATE OF APPROX 1 MHz
DELAY GENERATOR	DELAY OUTPUT OF .01 to .1 usec
OUTPUT GENERATOR A	WIDTH: 0.03 usec OFFSET: 0 Vdc AMPL: +3V pk
OUTPUT GENERATOR B	WIDTH: 0.03 usec OFFSET: 0 Vdc AMPL: +3V pk
MONITOR SCOPE	ADJUST TO VIEW STABLE DISPLAY (TRIGGER ON CHANNEL A SIGNAL)

LEGEND

1. MODEL 1601A
2. CLOCK INPUT
3. DATA INPUTS
4. RATE GENERATOR
5. RATE OUTPUT
6. RATE INPUT
7. TRIG OUTPUT
8. DELAY GENERATOR
9. DRIVE OUTPUT
10. DRIVE INPUT
11. OUTPUT GENERATOR
12. OUTPUT
13. DRIVE INPUT
14. OUTPUT GENERATOR
15. OUTPUT
16. CHANNEL A
17. CHANNEL B

Figure 5-1. Operational Check Test Setup

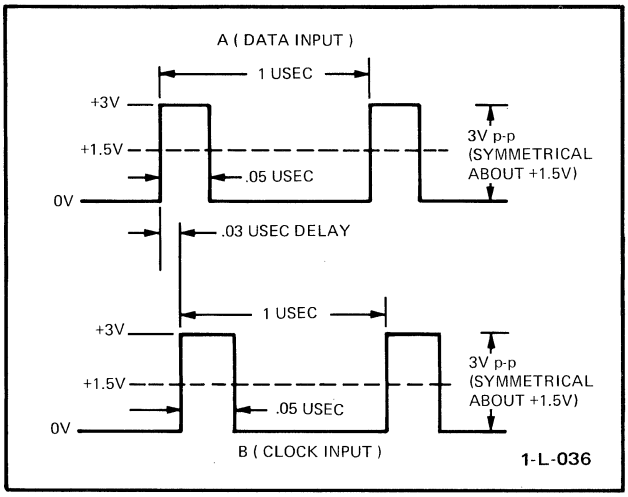


Figure 5-2. Operational Check Input Waveforms

f. Using LRC meter, sequentially measure shunt capacitance between each data probe bit input and ground, and between the clock probe clock input and ground. Observe that each measurement is ≤14 pF.

5-13. Input Bias Current. Specification:≤30 uA.

a. Remove power from Model 1601A and connect clock and data input probes.

b. Apply power to Model 1601A and set THRESHOLD to VAR.

c. Using multimeter, monitor VAR MEAS and adjust VAR SET to —10Vdc.

d. Using multimeter, measure current between each of the 12 data probe inputs and probe GND. Observe that multimeter indication is ≤30 uA for each measurement.

e. Using multimeter, measure current between the clock probe input and probe GND. Observe that multimeter indication is ≤30 uA.

5-14. Input Threshold/Logic Swing. Threshold specification: TTL, fixed at +1.5 VDC; Variable, to ±10 Vdc.
Minimum input swing: [0.4 +10% of threshold voltage] V p-p.
Maximum inputs: Level, ≤+15 Vdc, ≥—15 Vdc; Swing, 15V peak from threshold.

a. Remove power from Model 1601A and disconnect clock and data input probes.

b. Apply power to Model 1601A and press VAR pushbutton.

c. Using multimeter, monitor VAR MEAS test point while varying VAR SET from limit to limit. Observe that voltage changes smoothly and that limits are ≥+10 Vdc and ≤—10 Vdc.

Note

Refer to figure 8-8 for CLOCK INPUT and DATA INPUTS connector pin locations.

d. Using multimeter, sequentially monitor pin 9 of CLOCK INPUT and DATA INPUTS connectors while varying VAR SET from limit to limit. Observe that voltage changes smoothly and that limits are ≥+3.3 Vdc and ≤—3.3 Vdc.

e. Using multimeter, monitor VAR MEAS (TP1) and adjust VAR SET to 0.00 Vdc.

f. Using multimeter, monitor pin 9 of CLOCK INPUT and DATA INPUTS connectors and observe that multimeter indicates 0.00 ±0.05 Vdc.

g. Press TTL pushbutton.

h. Using multimeter, sequentially monitor pin 9 of CLOCK INPUT and DATA INPUTS connectors and observe that voltage is 0.5 ±0.03 Vdc.

i. Refer to figure 5-3 for suggested test equipment setup.

j. Apply test waveform shown in figure 5-4A to the clock and data probe inputs of the Model 1601A.

k. Set Model 1601A controls as follows:

CLOCK	⌊ (in)
THRESHOLD	TTL
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw
SAMPLE MODE	REPET
TRIGGER MODE	START DISPLAY
TRIGGER WORD	bits 0 through 11 to HI
LOGIC	POS

l. Adjust Model 1601A mainframe controls to view display and observe that all bits are displayed as ones.

m. Set TRIGGER WORD switch for bit 3 to OFF and alternately connect the circuit probe for bit 3 to ground and back to the signal conductor. Observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded.

n. Apply test waveform shown in figure 5-4B to the clock and data probe inputs of the Model 1601A.

o. Set THRESHOLD to VAR and adjust VAR SET for a stable display on the Model 1601A mainframe.

p. Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and

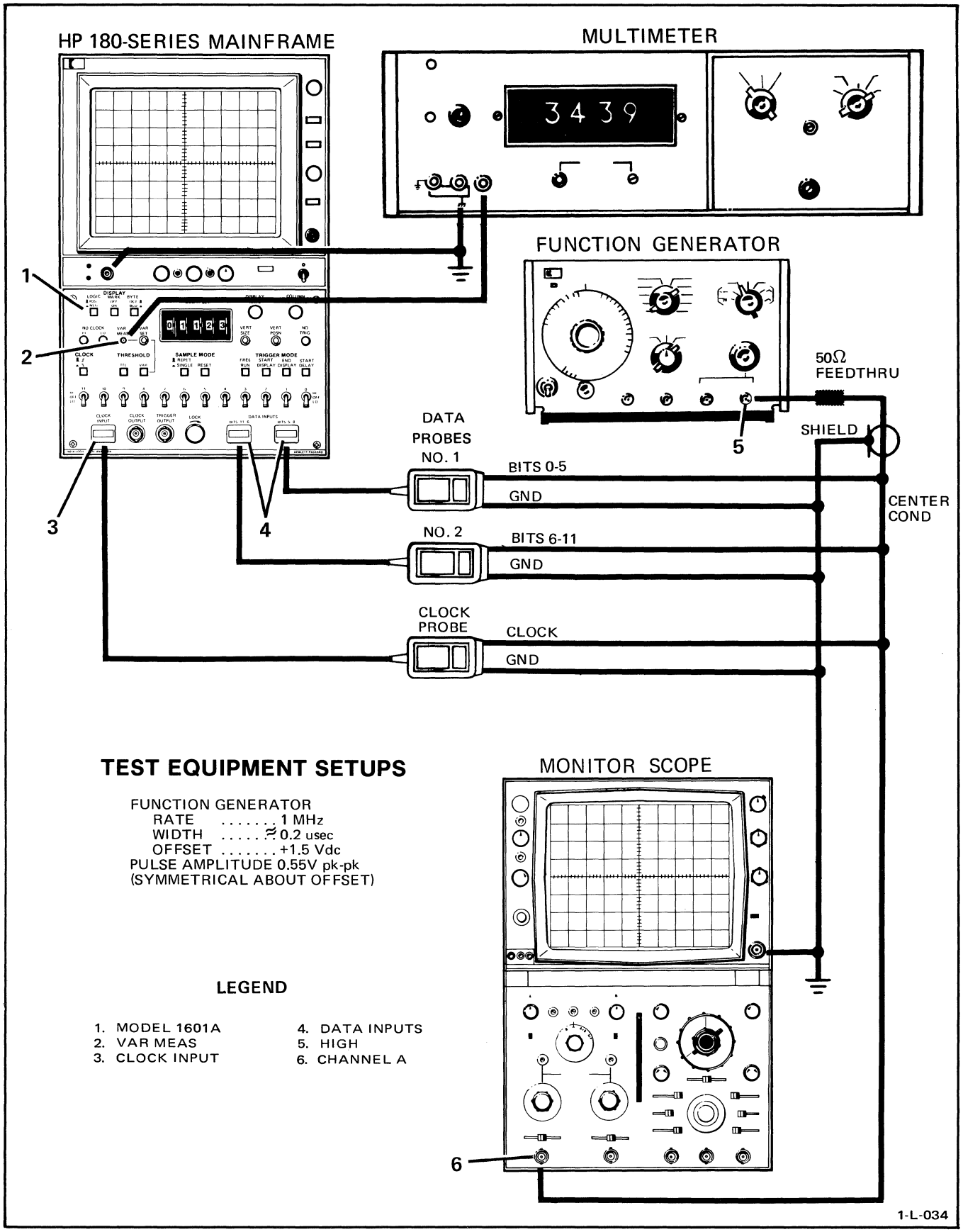


Figure 5-3. Threshold/Logic Swing Test Setup

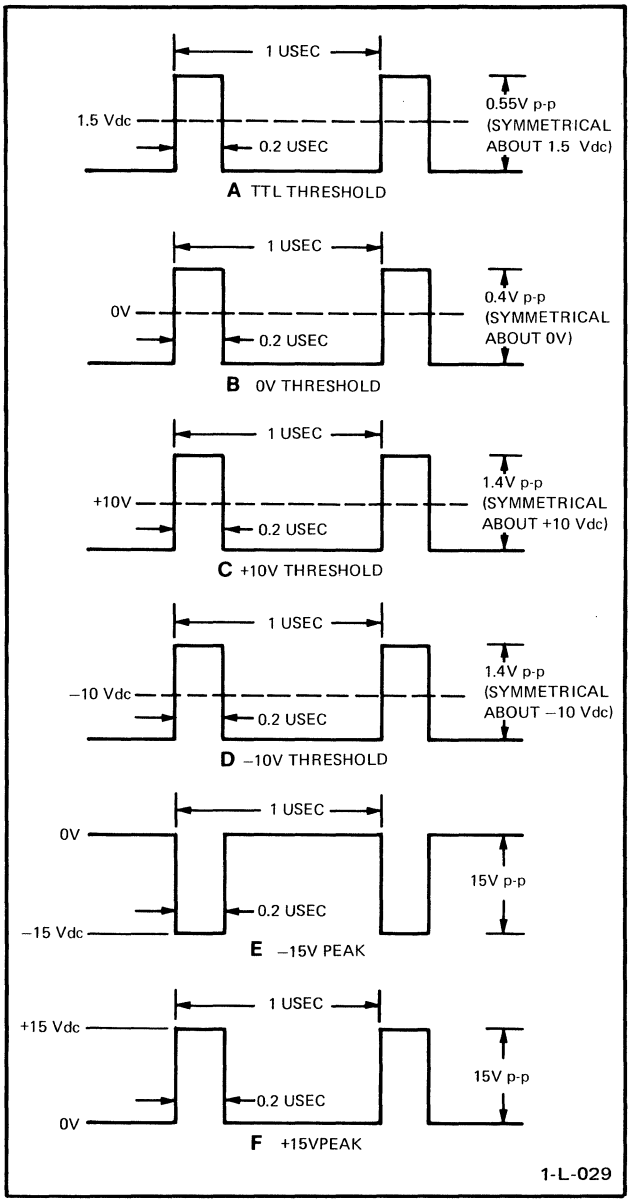


Figure 5-4. Threshold/Logic Swing Test Waveforms

observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded. (Slight readjustment of VAR SET may be necessary to obtain proper indication.)

q. Remove 50 ohm feedthrough and connect function generator output directly to clock and data probes.

r. Apply test waveform shown in figure 5-4C to the clock and data probe inputs of the Model 1601A.

s. Adjust VAR SET for a stable display of all ones on the Model 1601A mainframe.

t. Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded. (Slight readjustment of VAR SET may be necessary to obtain proper indication.)

u. Set all TRIGGER WORD switches (except switch 3) to LO. Switch 3 remains OFF.

v. Apply test waveform shown in figure 5-4D to the clock and data probe inputs of the Model 1601A.

w. Adjust VAR SET for a stable display of all zeros on the Model 1601A mainframe.

x. Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and observe that displayed column for bit 3 changes from a 0 to a 1 when probe is grounded. (Slight readjustment of VAR SET may be necessary to obtain proper indication.)

y. Apply waveform shown in figure 5-4E to the clock and data probe of the Model 1601A.

z. Set CLOCK to ⌐ (out).

aa. Adjust VAR SET for a stable display of all zeros on the Model 1601A mainframe.

ab. With multimeter connected to VAR MEAS, adjust VAR SET from —1 Vdc to —10 Vdc and observe that display remains stable.

ac. Set all TRIGGER WORD switches (except switch 3) to HI. Switch 3 remains OFF.

ad. Apply test waveform shown in figure 5-4F to the clock and data probe inputs of the Model 1601A.

ae. Adjust VAR SET for a stable display of all ones on the Model 1601A mainframe.

af. With multimeter connected to VAR MEAS, adjust VAR SET from +1 Vdc to +10 Vdc and observe that display remains stable.

5-15. Repetition Rate. Specification: 0 to 10 megabits/second.

a. Set up equipment per instructions in paragraph 5-8.

b. Apply test waveforms shown in figure 5-5 to the clock and data probe inputs of the Model 1601A.

c. Set THRESHOLD to VAR and adjust VAR SET for a stable display (displayed bits do not change state).

Note

When increasing pulse generator frequency, verify that leading edge of trigger input pulse remains delayed from the leading edge of the data input pulse at least 35 ns (see figure 5-5).

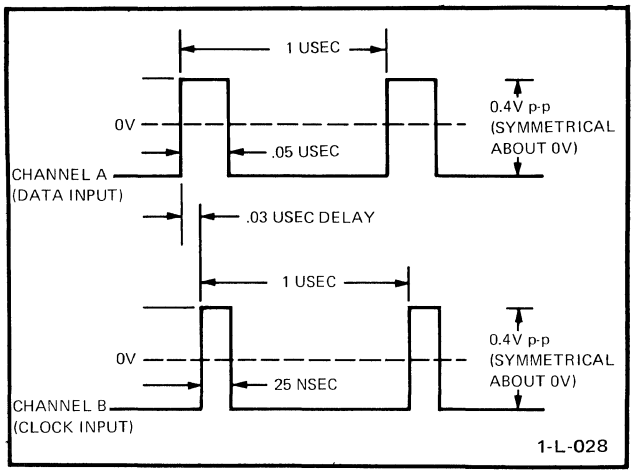


Figure 5-5. Repetition Rate Test Waveforms

d. Slowly increase pulse generator frequency control to >10 MHz. Observe that displayed bits remain stable at applied frequencies up to 10 MHz. (Small adjustments of VAR SET may be necessary to maintain stable display.)

e. Set pulse generator frequency control to 10 MHz. Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded.

5-16. Minimum Clock Pulse Width. Specification: 25 nsec.

a. Set up equipment per instructions in paragraph 5-8.

b. Slowly decrease width of pulse applied to clock input of Model 1601A. Observe that display remains visible and stable (displayed bits do not change states) for clock pulse width ≥25 ns.

c. Set CLOCK INPUT pulse width to 25 nsec. Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded.

5-17. Minimum Setup Time. (Time data must be present prior to clock transition.) Specification: 35 ns (typically 20 ns).

a. Set up equipment per instruction in paragraph 5-8. (Note any time differences between channels on monitor oscilloscope before proceeding.)

b. Slowly decrease delay time between leading edges of pulses applied to CLOCK and DATA INPUTS of Model 1601A. Observe that display remains visible and stable (displayed bits do not change states) for delay times ≤35 ns.

c. Set delay time between leading edges pulses to 35 nsec.Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded.

5-18. Minimum Hold Time. (Time data must be present after clock transition.) Specifications: 0 (typically —5 nsec).

a. Set up equipment per instructions in paragraph 5-8. (Note any time differences between channels before proceeding.)

b. Slowly increase delay time between leading edges of pulses applied to CLOCK and DATA INPUTS of Model 1601A. Observe that display remains visible and stable (displayed bits do not changes states) when the leading edge of the CLOCK INPUT pulse is coincident with the trailing edge of the DATA INPUTS pulse.

c. Set delay for coincidence between the leading edge of the CLOCK input pulse and the trailing edge of the DATA INPUTS pulse. Alternately connect the circuit probe for bit 3 to ground and back to the signal conductor and observe that displayed column for bit 3 changes from a 1 to a 0 when probe is grounded.

5-19. Display Rate. Specification: <40 msec to >5 sec.

a. Set up equipment per instructions in paragraph 5-8.

b. Remove power from Model 1601A oscilloscope mainframe and remove bottom covers. Set up timer-counter to measure period, and connect input to A2U34, pin 3 (A2TP2). Exercise care to prevent shorting to adjacent circuitry.

c. Apply power and adjust oscilloscope controls to view Model 1601A display.

d. Set DISPLAY RATE control fully ccw and observe that timer-counter indication is <40 msec.

e. Adjust DISPLAY RATE control fully cw and observe timer-counter indication is >5 seconds. Allow sufficient time for timer-counter to make several measurements.

5-20. Clock and Trigger Outputs. Specifications: High, ≥2V into 50 ohms;
LOW, ≤0.4V into 50 ohms;
WIDTH, Approximately 40 nsec.

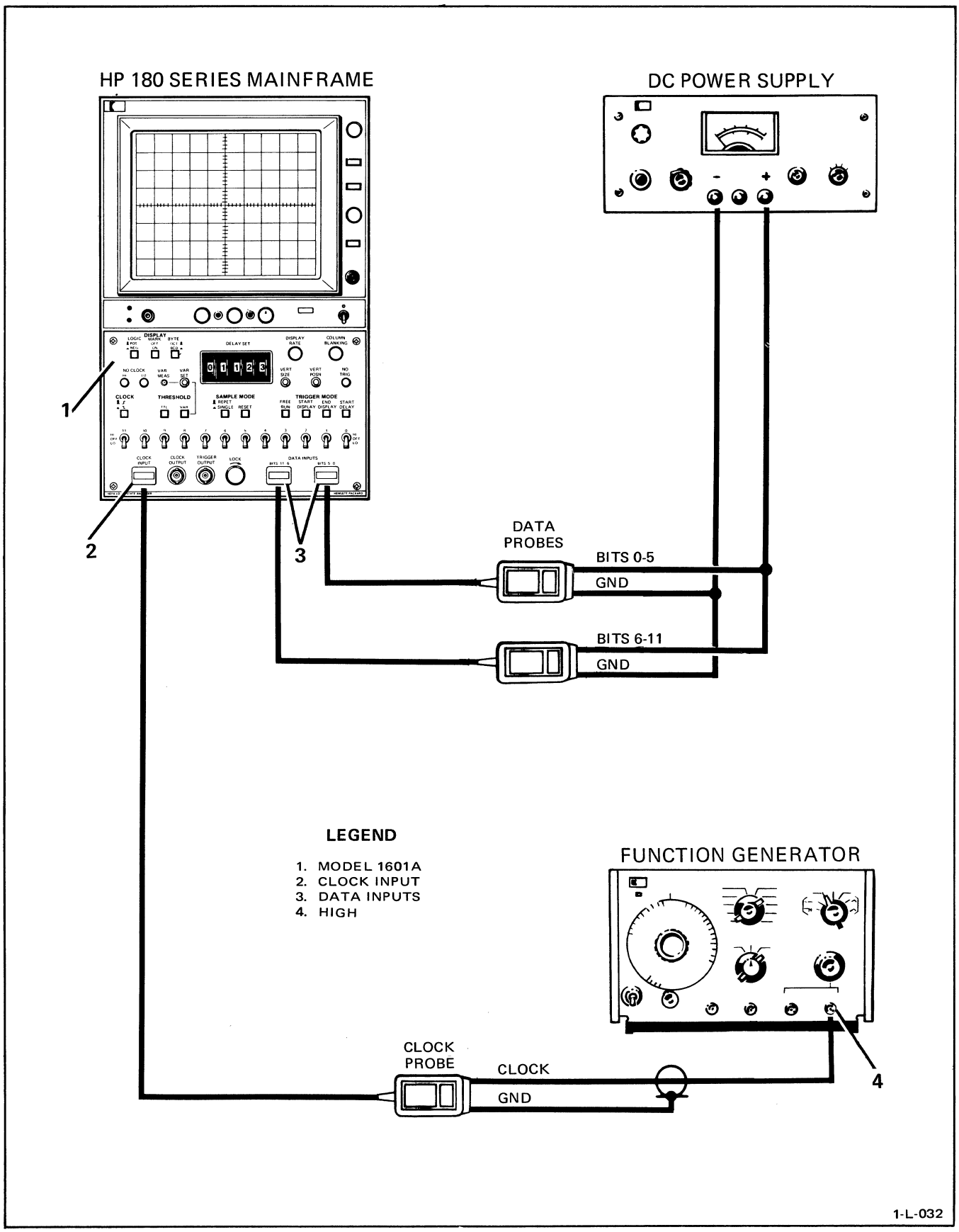


Figure 5-6. Bit Recognition/No Clock and No Trig Indicator Test Setup

a. Set up equipment per instructions in paragraph 5-8.

b. Using a 50 ohm termination, connect monitor oscilloscope to the Model 1601A CLOCK OUTPUT and TRIGGER OUTPUT connector. Observe that output pulses meet the following requirements:

High amplitude	≥+2V pk
Low amplitude	≤0.4V dc
Width	approximately 40 nsec

5-21. FUNCTIONAL CHECKS.

5-22. Paragraphs 5-23 through 5-26 contain functional checks of instrument capabilities not specified in table 1-1. Stated results of functional checks are approximate.

5-23. Operators Checks and Adjustments.
Perform the procedure delineated in paragraph 3-25 (Operators Checks and Adjustments) to check the following functional capabilities:

VERT POSN	DISPLAY
VERT SIZE	LOGIC POS/NEG
COLUMN BLANKING	MARK OFF/ON
	BYTE OCT/BCD

5-24. Bit Recognition/NO CLOCK and NO TRIG INDICATORS.

a. Refer to figure 5-6 for recommended test equipment setup.

b. Apply waveform shown in figure 5-7A to the clock probe input.

CAUTION

Do not apply more than ±15V peak to the clock or data probe inputs as damage to circuitry may result.

c. Apply +5Vdc to all data probe inputs.

d. Set Model 1601A controls as follows:

CLOCK	⌐ (out)
THRESHOLD	TTL
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw
SAMPLE MODE	REPET
TRIGGER MODE	START DISPLAY
LOGIC	POS
TRIGGER WORD	bits 0 through 11 to H1

e. Adjust Model 1601A mainframe controls to observe a 12 bit wide, 16 word stable display of all ones.

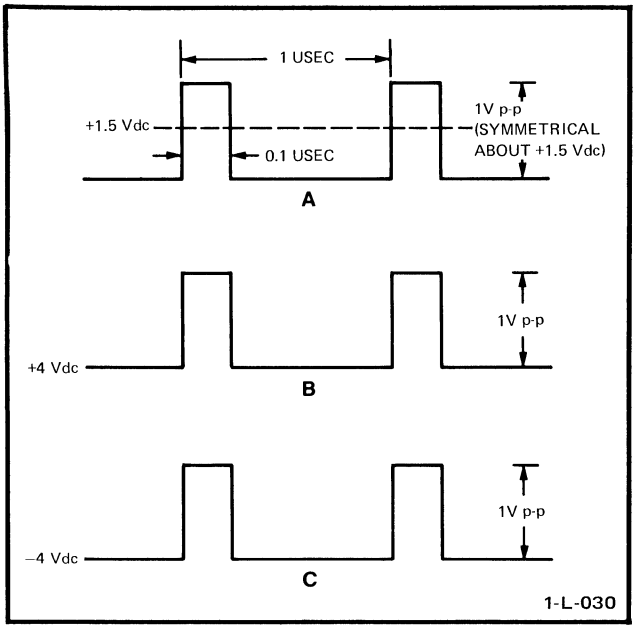


Figure 5-7. No Clock Indicator Test Waveforms

f. Adjust function generator so that baseline offset of applied waveform is +4 Vdc (ref figure 5-7B) and observe that display is blanked and that the NO CLOCK HI indicator is on.

g. Adjust function generator so that baseline offset of applied waveform is —4Vdc (ref figure 5-7C) and observe that display is blanked and that NO CLOCK LO indicator is on.

h. Adjust function generator so that waveform shown in figure 5-7A is applied to the clock probe input and observe a stable display of all ones.

i. Sequentially set each TRIGGER WORD SWITCH TO LO and then to OFF. Observe that display blanks and NO TRIG indicator lights when each switch is placed to LO and that display returns when switch is placed in OFF.

CAUTION

Do not apply more than ±15V peak to clock or data probe inputs as damage to circuitry may result.

j. Apply —5Vdc to all data probe inputs.

k. Set TRIGGER WORD switches 0 through 11 to LO and observe a display of all zeros.

l. Sequentially set each TRIGGER WORD switch to HI and back to OFF. Observe that display blanks and NO TRIG indicator lights when each switch is placed in HI and that display returns when each switch is placed in OFF.

5-25. SAMPLE MODE, TRIGGER MODE, and Pattern Recognition. To check SAMPLE MODE, TRIGGER MODE, and pattern recognition, non-repetitive, parallel input data is required. A single 4-bit binary counter integrated circuit, such as a 9316, will furnish the required signals. When connected as shown in figure 5-8, a 9316 will provide four parallel binary signals which count sequentially from 0 through 15. The test setup shown in figure 5-8 allows each of the twelve Model 1601A input channels to be exercised. Each output of the 4-bit binary counter is connected to three data input probes. These connections will provide a display of three identical BCD bytes. Table 5-2 lists the equivalent BCD, (Binary Coded Decimal) numbers for counter states 0 through 15.

a. Connect equipment as shown in figure 5-8.

b. Set Model 1601A controls as follows:

CLOCK	⌐ (out)
THRESHOLD	TTL
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw
SAMPLE MODE	REPET
TRIGGER MODE	START DISPLAY
LOGIC	POS
MARK	ON
BYTE	BCD
DELAY SET	00000

c. Apply power to test setup and adjust mainframe controls to view display.

d. Observe that display is three, identical 4-bit bytes of BCD numbers, each byte counting sequentially from 0 through 15 (see table 5-2), and that the first word (0000 0000 0000) is intensified.

e. Set TRIGGER MODE to END DISPLAY and observe that displayed BCD bytes count sequentially from 1 to 15 and end with 0 (see table 5-2). Observe that last word (0000 0000 0000) is intensified.

f. Set TRIGGER MODE to START DISPLAY.

g. Set TRIGGER WORD switches to the positions indicated for each BCD trigger word listed in table 5-2. Observe that each displayed BCD byte starts with the BCD trigger word selected by the TRIGGER WORD switches, counts through 15 (1111), then resets to 0 (0000), and continues a sequential count. If the TRIGGER WORD switches are set to HI or LO patterns other than those listed in Table 5-2 the display will blank and the NO TRIGGER indicator will light. This condition indicates that the selected trigger word is not being supplied to the data inputs.

h. Set TRIGGER MODE to FREE RUN and observe that each displayed bit is a 1 superimposed on a 0.

i. Refer to table 5-2 and set TRIGGER WORD switches for the BCD trigger word 0011 (counter state 3).

j. Set TRIGGER MODE to START DISPLAY and observe that displayed BCD bytes start with counter state 3 (0011) and continue a sequential count.

k. Set SAMPLE MODE to SINGLE and observe that display does not change.

Table 5-2. BCD Trigger Words

Counter State	BCD Trigger Word	TRIGGER WORD Switch Settings											
		11	10	9	8	7	6	5	4	3	2	1	0
0	0000	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO	LO
1	0001	LO	LO	LO	HI	LO	LO	LO	HI	LO	LO	LO	HI
2	0010	LO	LO	HI	LO	LO	LO	HI	LO	LO	LO	HI	LO
3	0011	LO	LO	HI	HI	LO	LO	HI	HI	LO	LO	HI	HI
4	0100	LO	HI	LO	LO	LO	HI	LO	LO	LO	HI	LO	LO
5	0101	LO	HI	LO	HI	LO	HI	LO	HI	LO	HI	LO	HI
6	0110	LO	HI	HI	LO	LO	HI	HI	LO	LO	HI	HI	LO
7	0111	LO	HI	HI	HI	LO	HI	HI	HI	LO	HI	HI	HI
8	1000	HI	LO	LO	LO	HI	LO	LO	LO	HI	LO	LO	LO
9	1001	HI	LO	LO	HI	HI	LO	LO	HI	HI	LO	LO	HI
10	1010	HI	LO	HI	LO	HI	LO	HI	LO	HI	LO	HI	LO
11	1011	HI	LO	HI	HI	HI	LO	HI	HI	HI	LO	HI	HI
12	1100	HI	HI	LO	LO	HI	HI	LO	LO	HI	HI	LO	LO
13	1101	HI	HI	LO	HI	HI	HI	LO	HI	HI	HI	LO	HI
14	1110	HI	HI	HI	LO	HI	HI	HI	LO	HI	HI	HI	LO
15	1111	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI	HI

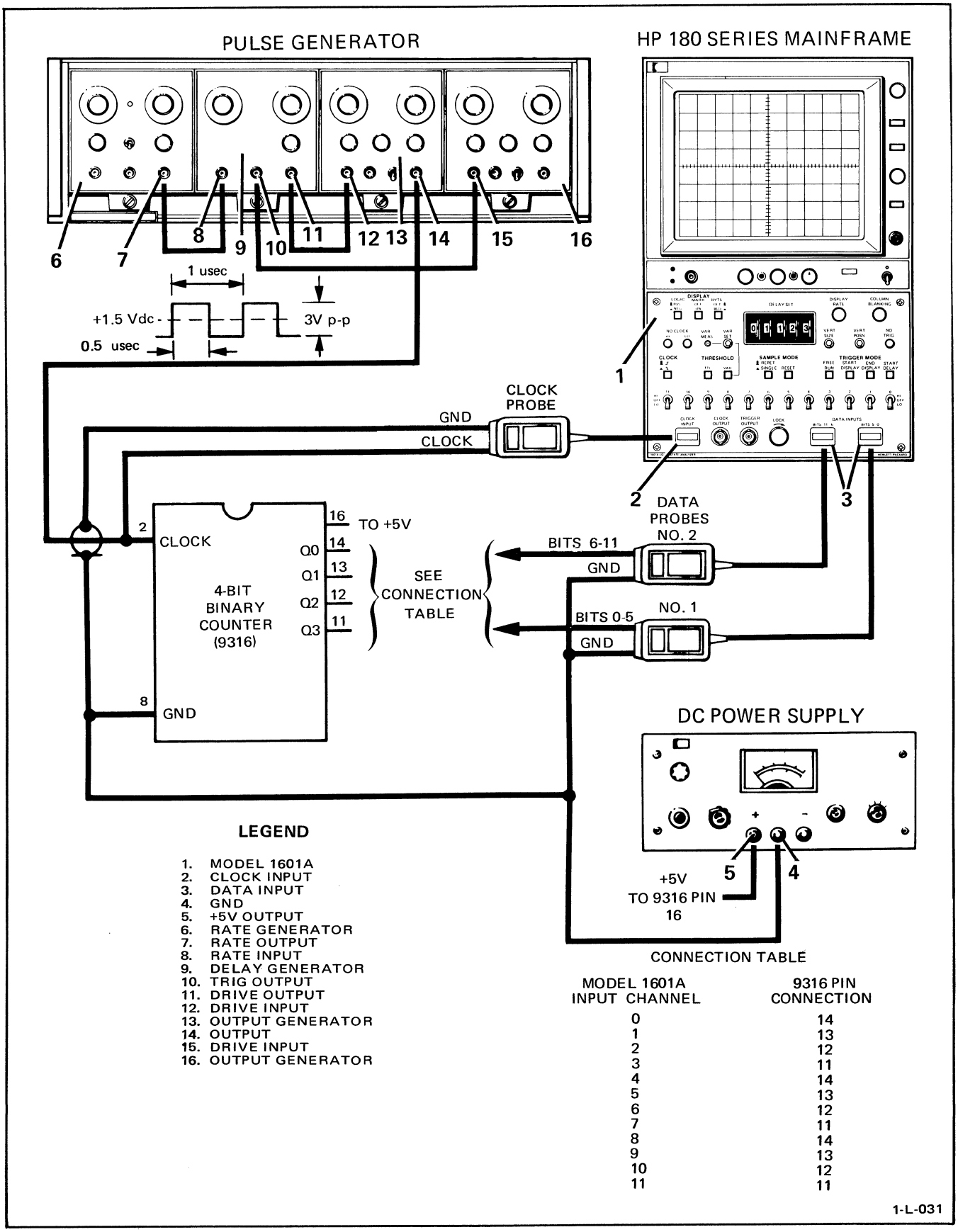


Figure 5-8. Sample Mode, Trigger Mode, and Pattern Recognition Test Setup

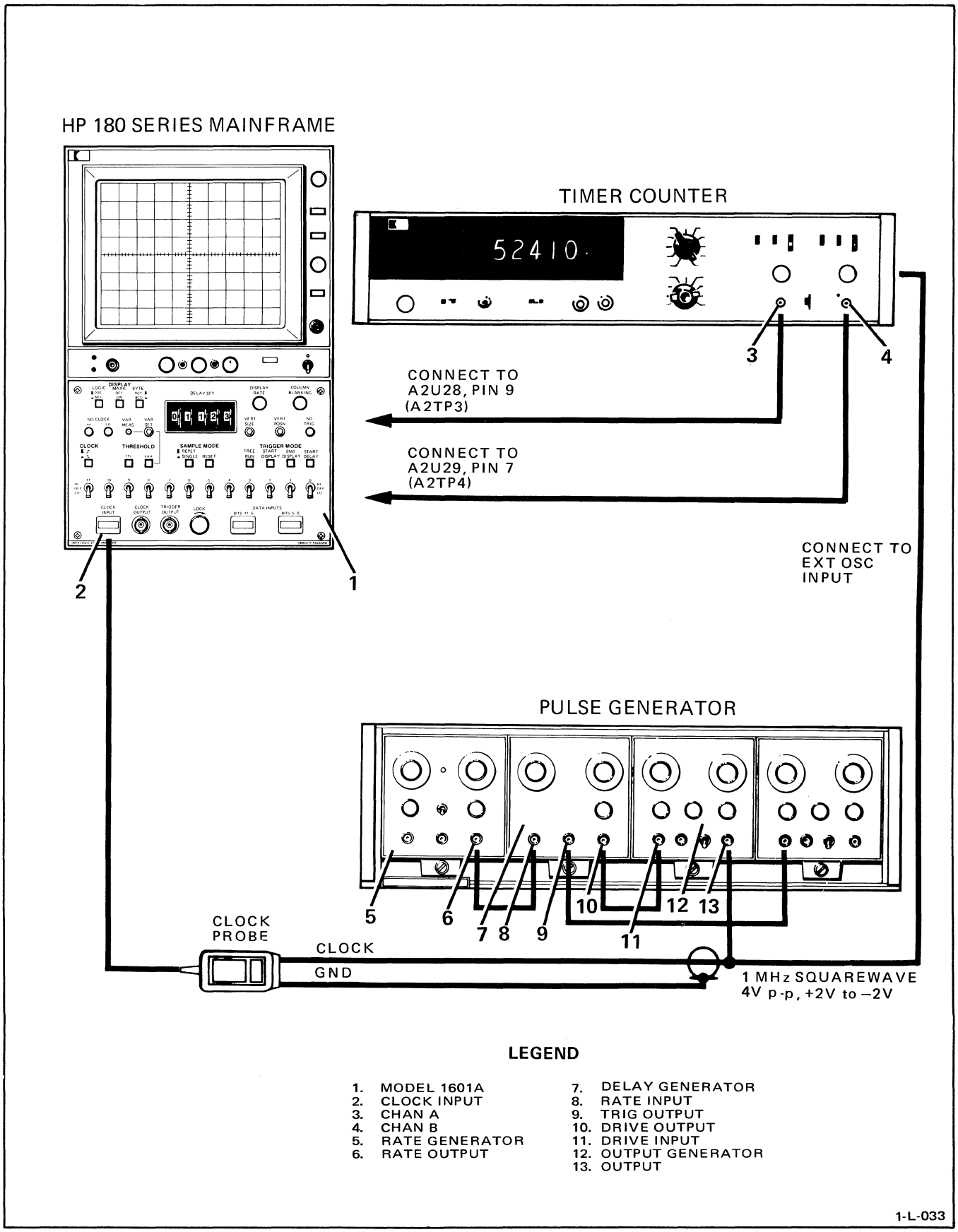


Figure 5-9. Delay Set Test Setup

l. Refer to table 5-2 and set TRIGGER WORD switches for the BCD trigger word 0101 (counter state 5) and observe that display does not change.

m. Momentarily press RESET and observe that displayed BCD bytes start with counter state 5 (0101) and continue a sequential count.

n. Set TRIGGER WORD switch 0 to LO, momentarily press RESET and observe that display blanks and NO TRIG indicator lights.

o. Set TRIGGER WORD switch 0 to HI and observe that displayed BCD bytes start with counter state 5 (0101) and continue a sequential count.

p. Set SAMPLE MODE to REPET and, set all TRIGGER WORD switches to LO.

q. Set TRIGGER MODE to START DELAY and observe that each displayed BCD byte starts with counter state 0 (0000) and continues a sequential count to state 15 (1111).

r. Set DELAY SET to 00001 and observe that each displayed BCD byte starts with counter state 1 (0001) and continues a sequential count to state 5 (1111), then resets to 0 (0000).

s. Sequentially set DELAY SET to 00002 through 00015 and observe that each displayed BCD byte starts with the BCD number equivalent to the state number appearing in DELAY SET (see table 5-2).

t. Set DELAY SET to 00016 and observe that each displayed BCD byte starts with 0 (0000) and continues a sequential count to 15 (1111).

5-26. Delay Set.

a. Refer to figure 5-9 for recommended test equipment setup.

b. Remove power from Model 1601A mainframe and remove bottom covers.

c. Connect timer-counter channel A input to A2U28, pin 9 (A2TP4) and channel B input to A2U29, pin 7 (A2TP3). Exercise care to prevent shorting to adjacent circuitry.

d. Apply waveform shown in figure 5-10 to clock probe input and to timer-counter EXT OSC input.

e. Set Model 1601A controls as follows:

CLOCK	⌐ (out)
THRESHOLD	TTL
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw
SAMPLE MODE	REPET
TRIGGER MODE	START DELAY
DELAY SET	00000
TRIGGER WORD	bits 0 through 11 to OFF
LOGIC	POS
MARK	OFF
BYTE	BCD

f. Adjust mainframe controls to view display.

g. Set timer-counter controls to observe a time interval function (A to B) with a time base of 0.1 usec (Use timer-counter external oscillator as shown in figure 5-9).

h. Set units thumbwheel of DELAY SET to 1 and observe that time-counter indicates 0.1 usec.

i. Continue rotating DELAY SET units thumbwheel from 1 through 9 and observe that timer counter numerical indication is identical to the number selected on DELAY SET.

j. Repeat steps h and i for each DELAY SET thumbwheel. Observe that timer-counter indication is identical to any number selected on DELAY SET.

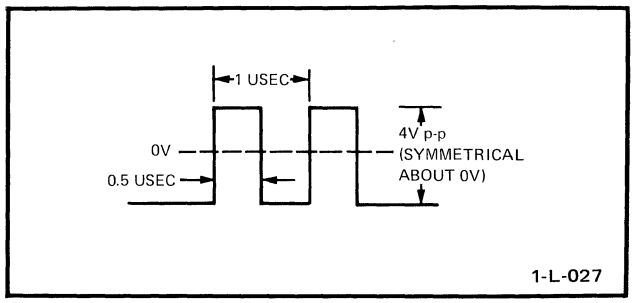


Figure 5-10. Delay Set Test Waveform

PERFORMANCE CHECK RECORD
MODEL 1601A

Instrument Serial Number _____ **Date** _____

Check	Specification	Measured
INITIAL OPERATIONAL CHECK		
Display	12 bits wide 16 words all ones	_____ _____ _____
INPUT RC		
Input Resistance	40 ±3K ohms	_____
Shunt Capacitance	⩽14 pF	_____
INPUT BIAS CURRENT		
Data Probe Inputs	⩽30 uA	_____
Clock Probe Inputs	⩽30 uA	_____
INPUT THRESHOLD/LOGIC SWING		
VAR MEAS Swing	⩾+10 Vdc to ⩽−10 Vdc	_____ _____
Threshold Swing at CLOCK/DATA INPUT Connectors	⩾+3.3 Vdc to ⩽−3.3 Vdc	_____ _____
Threshold zero output	0.00 ±0.05 Vdc	_____
TTL threshold output	0.5 ±0.03 Vdc	_____
TTL threshold waveform input	Bit 3 changes from 1 to 0	_____
0V threshold waveform input	Bit 3 changes from 1 to 0	_____
+10V threshold waveform input	Bit 3 changes from 1 to 0	_____
−10V threshold waveform input	Bit 3 changes from 0 to 1	_____
−15V pk waveform input	stable display	_____
+15V pk waveform input	stable display	_____

PERFORMANCE CHECK RECORD (Cont'd)
MODEL 1601A

Instrument Serial Number _____ **Date** _____

Check	Specification	Measured
REPETITION RATE		
Applied frequencies ≤10 MHz	Stable display at ≤10 MHz	_____
Applied frequency of 10 MHz	Bit 3 changes from 1 to 0	_____
MINIMUM CLOCK PULSE WIDTH		
Applied clock pulse widths ≥25 ns	stable display at ≥25 ns	_____
Applied clock pulse width of 25 ns	Bit 3 changes from 1 to 0	_____
MINIMUM SETUP TIME		
Delay times ≥35 ns	stable display at ≥35 ns	_____
Delay time of 35 ns	Bit 3 changes from 1 to 0	_____
MINIMUM HOLD TIME		
Data input trailing edge transition coincident with clock input leading edge transition (0 Hold time).	stable display at at 0 Hold	_____
	Bit 3 changes from 1 to 0	_____
DISPLAY RATE		
DISPLAY RATE fully ccw	<40 msec	_____
DISPLAY RATE fully cw	>5 sec	_____
CLOCK AND TRIGGER OUTPUTS		
CLOCK OUTPUT	HI, ≥+2V pk LO, ≤+0.4V Width, ≈ 40 ns	_____ _____ _____

PERFORMANCE CHECK RECORD (Cont'd)
MODEL 1601A

Instrument Serial Number _____ **Date** _____

Check	Specification	Measured
TRIGGER OUTPUT	HI, ≥+2V pk LO, ≤+0.4V Width, ≈ 40 ns	_____ _____ _____
OPERATORS CHECKS AND ADJUSTMENTS		
VERT POSN	Centers display	_____
VERT SIZE	display size	_____
BYTE OCT BCD	 four 3-bit bytes three 4-bit bytes	 _____ _____
LOGIC POS/NEG	Changes ones to zeros and zeros to ones	_____ _____
MARK START DISPLAY END DISPLAY	 first word intensified last word intensified	 _____ _____
COLUMN BLANKING	Vertical columns are blanked	_____ _____
fully cw	LSB remains	_____
BIT RECOGNITION/NO CLOCK and NO TRIG INDICATORS		
+5 Vdc input, all TRIGGER WORD switches HI	12 bits wide 16 words all ones	_____ _____ _____
+4 Vdc baseline clock waveform	display blanks NO CLOCK HI lights	_____ _____ _____
–4 Vdc baseline clock waveform	display blanks NO CLOCK LO lights	_____ _____
Each TRIGGER WORD switch to LO, then OFF	display blanks and NO TRIG lights for each LO	_____ _____

PERFORMANCE CHECK RECORD (Cont'd)
MODEL 1601A

Instrument Serial Number _____ **Date** _____

Check	Specification	Measured
–5 Vdc input, all TRIGGER WORD switches LO	12 bits wide 16 words all zeros	_____ _____ _____
Each TRIGGER WORD switch to HI, then OFF	display blanks and NO TRIG lights for each HI	_____ _____ _____
SAMPLE MODE, TRIGGER MODE and PATTERN RECOGNITION		
REPET, START DISPLAY	three 4-bit bytes sequential count first word intensified	_____ _____ _____ _____
END DISPLAY	sequential count last word intensified	_____ _____ _____
TRIGGER WORD switch settings vs BCD trigger word	display starts with each selected BCD trigger word	_____ _____ _____
FREE RUN	superimposed ones and zeros	_____ _____
SINGLE, START DISPLAY		
TRIGGER WORD = 0011	display starts with 0011	_____ _____
TRIGGER WORD = 0101	display starts with 0101 when RESET is pushed	_____ _____ _____
TRIGGER WORD switch 0 to LO	display blanks and NO TRIG lights when RESET is pushed	_____ _____ _____ _____
TRIGGER WORD switch 0 to HI	display returns	_____
REPET, START DELAY		
DELAY SET from 0 to 15	display starts with each DELAY SET selection	_____ _____ _____

PERFORMANCE CHECK RECORD (Cont'd)
MODEL 1601A

Instrument Serial Number _____ **Date** _____

Check	Specification	Measured
DELAY SET to 16	display starts with 0000	_____
DELAY SET	timer counter readout matches each DELAY SET selection	_____

5-27. ADJUSTMENTS.

5-28. The following paragraphs describe procedures to calibrate the instrument so that it will perform as specified in table 1-1. The adjustment procedure can be done in sequence, or separate adjustments can be performed by following the steps outlined in the appropriate paragraph. The locations of adjustment controls are shown in illustrations adjacent to the text describing a specific adjustment. Use a nonmetallic screwdriver and recently calibrated test equipment with characteristics specified in Table 5-1. After adjustments are complete, check instrument performance with the performance check procedure at the beginning of this section.

Note

Adjustments are performed with oscilloscope mainframe bottom covers removed, or with Model 1601A installed on Model 10407B 180 system plug-in extender.

5-29. +5V POWER SUPPLY.

5-30. Adjust the +5V power supply as follows:

a. Remove power and connect a clock and two data probes.

b. Connect multimeter between A2TP1 and chassis ground.

c. Apply instrument power and allow 15 minutes for warm-up.

d. Adjust A1R6 (see figure 5-11) for +5 ±0.01 Vdc.

e. Remove instrument power and disconnect multimeter.

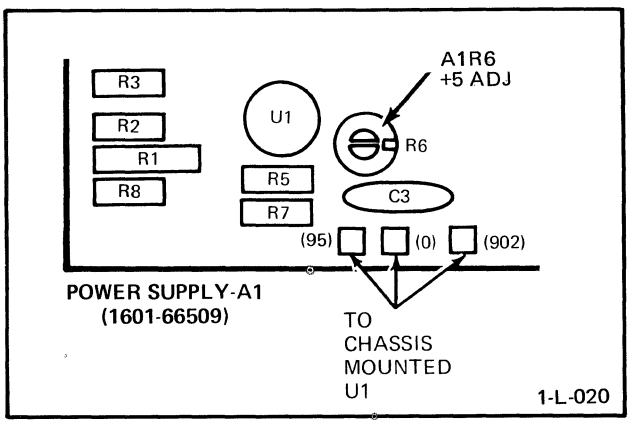


Figure 5-11. +5V Adjustment Location

5-31. CHARACTER SIZE.

5-32. Adjust displayed character size as follows:

Note

Clock and data monitor probes need not be connected for this procedure.

a. Remove power from oscilloscope mainframe.

b. Set Model 1601A controls as follows:

SAMPLE MODE	SINGLE
TRIGGER MODE	FREE RUN
LOGIC	POS
MARK	OFF
BYTE	OCT
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw

c. Apply power and adjust oscilloscope controls to view display.

d. Observe a 12 bit wide, 16 word display on the CRT. (If display is all ones, set LOGIC to NEG.)

e. Adjust VERT POSN (A5R4) to center 16 word display on the CRT.

f. Adjust VERT SIZE (A5R3) so that first and last words are just inside the upper and lower CRT graticule lines.

g. Adjust A2R54 (see figure 5-12) so that displayed characters are as large as possible without overlapping. Allow sufficient space between characters for convenient viewing.

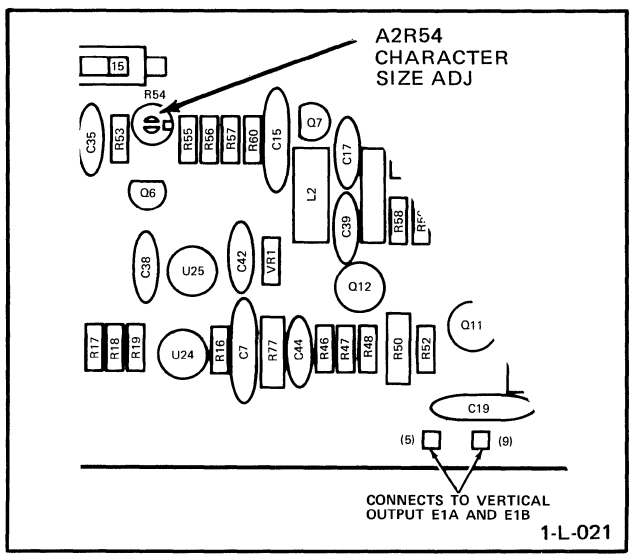


Figure 5-12. Character Size Adjustment Location

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering replacement parts. The abbreviations used in the parts list are described in table 6-1. Table 6-2 lists the parts in alphanumeric order by reference designator and includes the manufacturer and manufacturer's part number. Table 6-3 contains the list of manufacturers' codes.

6-3. ORDERING INFORMATION.

6-4. To obtain replacement parts from Hewlett-Packard, address order or inquiry to the nearest Hewlett-Packard Sales/Service Office and supply the following information:

a. Instrument model and serial number.

b. HP part number of item(s).

c. Quantity of part(s) desired.

d. Reference designator of part(s).

6-5. To order a part not listed in the table, provide the following information:

a. Instrument model and serial number.

b. Description of the part, including function and location in the instrument.

c. Quantity desired.

Table 6-1. Abbreviations for Replaceable Parts List

A	AMPERE(S)	H	HENRY(IES)	NPN	NEGATIVE-POSITIVE-NEGATIVE	RWV	REVERSE WORKING VOLTAGE
ASSY	ASSEMBLY	HG	MERCURY				
		HP	HEWLETT-PACKARD	NSR	NOT SEPARATELY REPLACEABLE	S-B	SLOW-BLOW
BD	BOARD(S)	HZ	HERTZ			SCR	SILICON CONTROLLED RECTIFIER
BH	BINDER HEAD						
BP	BANDPASS	IF	INTERMEDIATE FREQ.				
		IMPG	IMPREGNATED	OBD	ORDER BY DESCRIPTION	SE	SELENIUM
C	CENTI (10^{-2})	INCD	INCANDESCENT			SEC	SECOND(S)
CAR	CARBON	INCL	INCLUDE(S)	OH	OVAL HEAD	SECT	SECTION(S)
CCW	COUNTERCLOCKWISE	INS	INSULATION(ED)	OX	OXIDE	SI	SILICON
CER	CERAMIC	INT	INTERNAL			SIL	SILVER
CMO	CABINET MOUNT ONLY			P	PEAK	SL	SLIDE
COAX	COAXIAL	K	KILO (10^{3})	PC	PRINTED (ETCHED) CIRCUIT(S)	SP	SINGLE POLE
COEF	COEFFICIENT	KG	KILOGRAM			SPL	SPECIAL
COMP	COMPOSITION			PF	PICOFARADS	ST	SINGLE THROW
CONN	CONNECTOR(S)	LB	POUND(S)	PHL	PHILLIPS	STD	STANDARD
CRT	CATHODE-RAY TUBE	LH	LEFT HAND	PIV	PEAK INVERSE VOLTAGE(S)	TA	TANTALUM
CW	CLOCKWISE	LIN	LINEAR TAPER			TD	TIME DELAY
		LOG	LOGARITHMIC TAPER	PNP	POSITIVE-NEGATIVE-POSITIVE	TFL	TEFLON
D	DECI (10^{-1})	LPF	LOW-PASS FILTER(S)			TGL	TOGGLE
DEPC	DEPOSITED CARBON	LVR	LEVER	P/O	PART OF	THYR	THYRISTOR
DP	DOUBLE POLE			PORC	PORCELAIN	TI	TITANIUM
DT	DOUBLE THROW	M	MILLI (10^{-3})	POS	POSITION(S)	TNLDIO	TUNNEL DIODE(S)
		MEG	MEGA (10^{6})	POT	POTENTIOMETER(S)	TOL	TOLERANCE
ELECT	ELECTROLYTIC	MET FILM	METAL FILM	P-P	PEAK-TO-PEAK	TRIM	TRIMMER
ENCAP	ENCAPSULATED	MET OX	METAL OXIDE	PRGM	PROGRAM		
EXT	EXTERNAL	MFR	MANUFACTURER	PS	POLYSTYRENE		
		MINAT	MINIATURE	PWV	PEAK WORKING VOLTAGE	U	MICRO (10^{-6})
F	FARAD(S)	MOM	MOMENTARY				
FET	FIELD-EFFECT TRANSISTOR(S)	MTG	MOUNTING			V	VOLTS
		MY	MYLAR	RECT	RECTIFIER(S)	VAR	VARIABLE
FH	FLAT HEAD			RF	RADIO FREQUENCY	VDCW	DC WORKING VOLT(S)
FIL H	FILLISTER HEAD	N	NANO (10^{-9})	RFI	RADIO FREQUENCY INTERFERENCE		
FXD	FIXED	N/C	NORMALLY CLOSED			W	WATT(S)
		NE	NEON	RH	ROUND HEAD OR RIGHT HAND	W/	WITH
G	GIGA (10^{9})	N/O	NORMALLY OPEN			WIV	WORKING INVERSE VOLTAGE
GE	GERMANIUM	NOP	NEGATIVE POSITIVE ZERO (ZERO TEMPERATURE COEFFICIENT)				
GL	GLASS			RMO	RACK MOUNT ONLY	W/O	WITHOUT
GRD	GROUNDED			RMS	ROOT MEAN SQUARE	WW	WIREWOUND

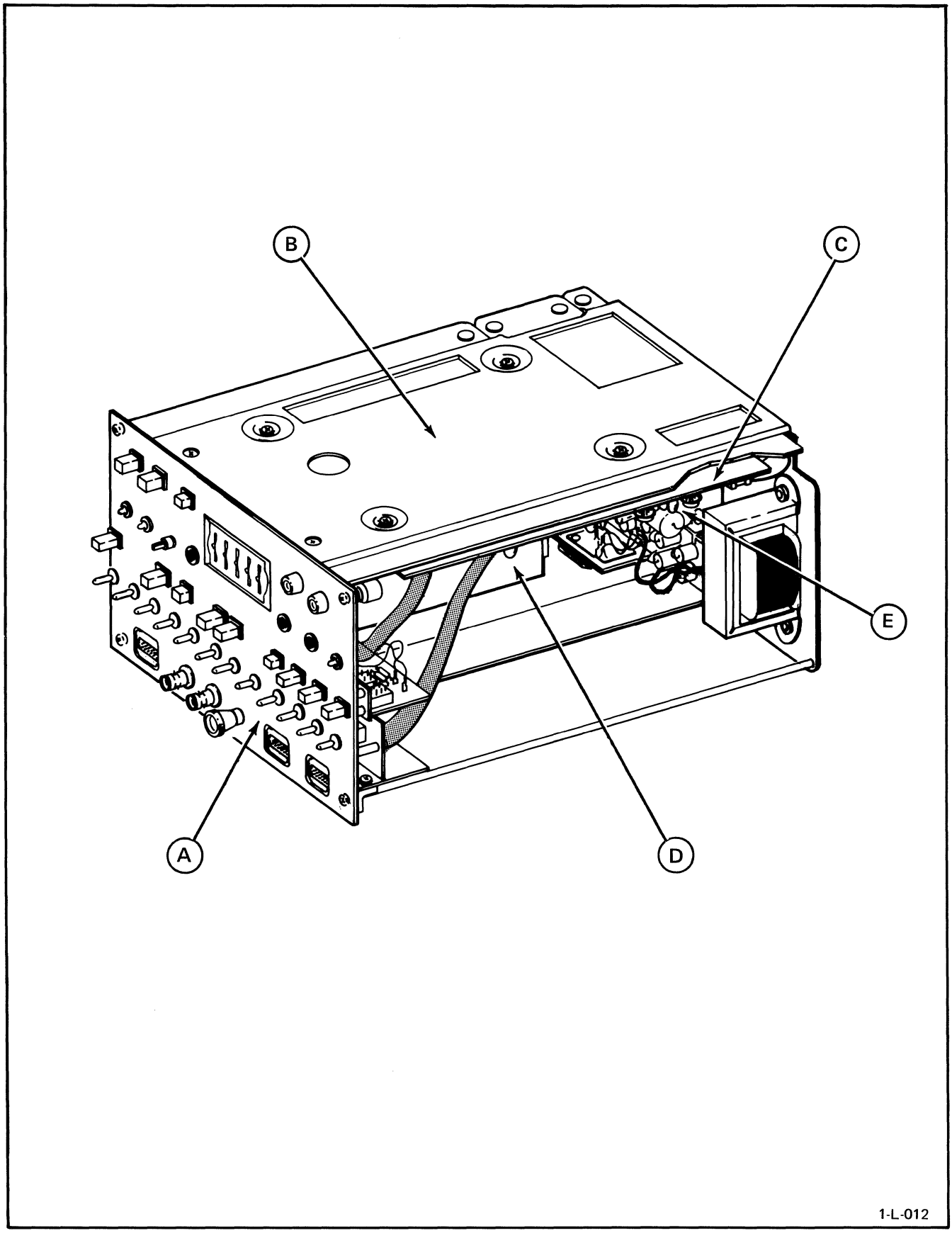
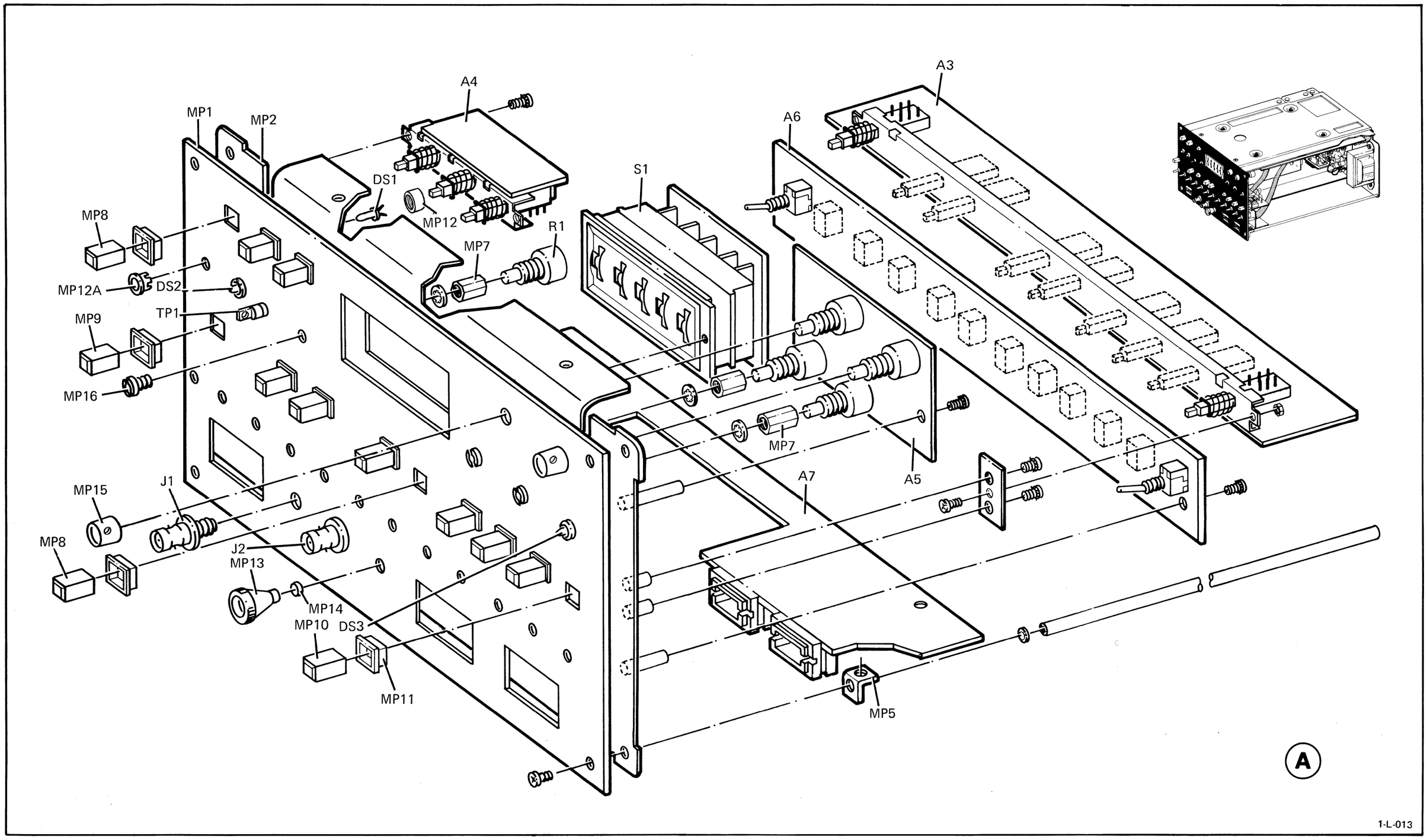
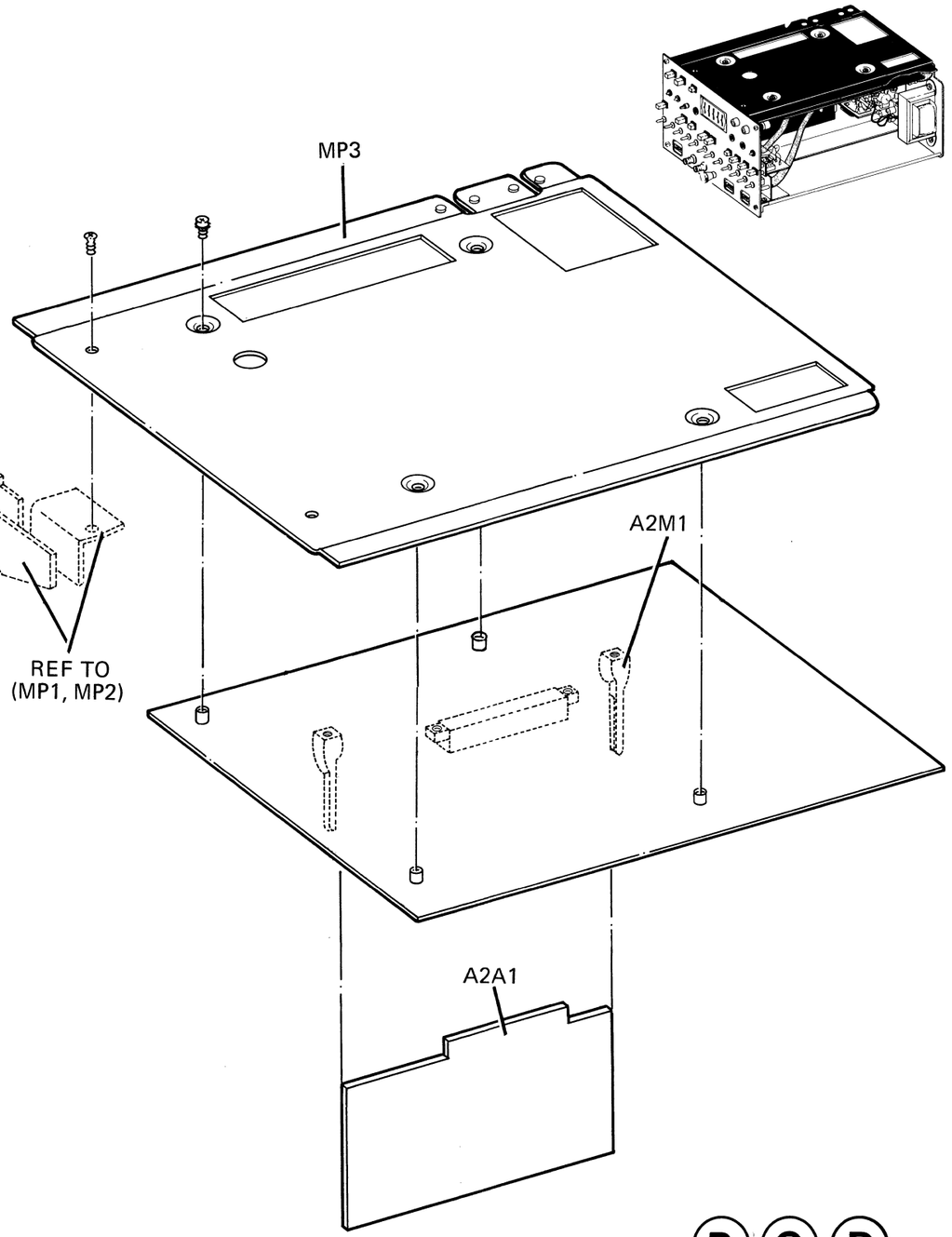


Figure 6-1. Model 1601A Illustrated Parts Breakdown (Sheet 1)



1-L-013

Figure 6-1.
Model 1601A Illustrated Parts Breakdown (Sheet 2)



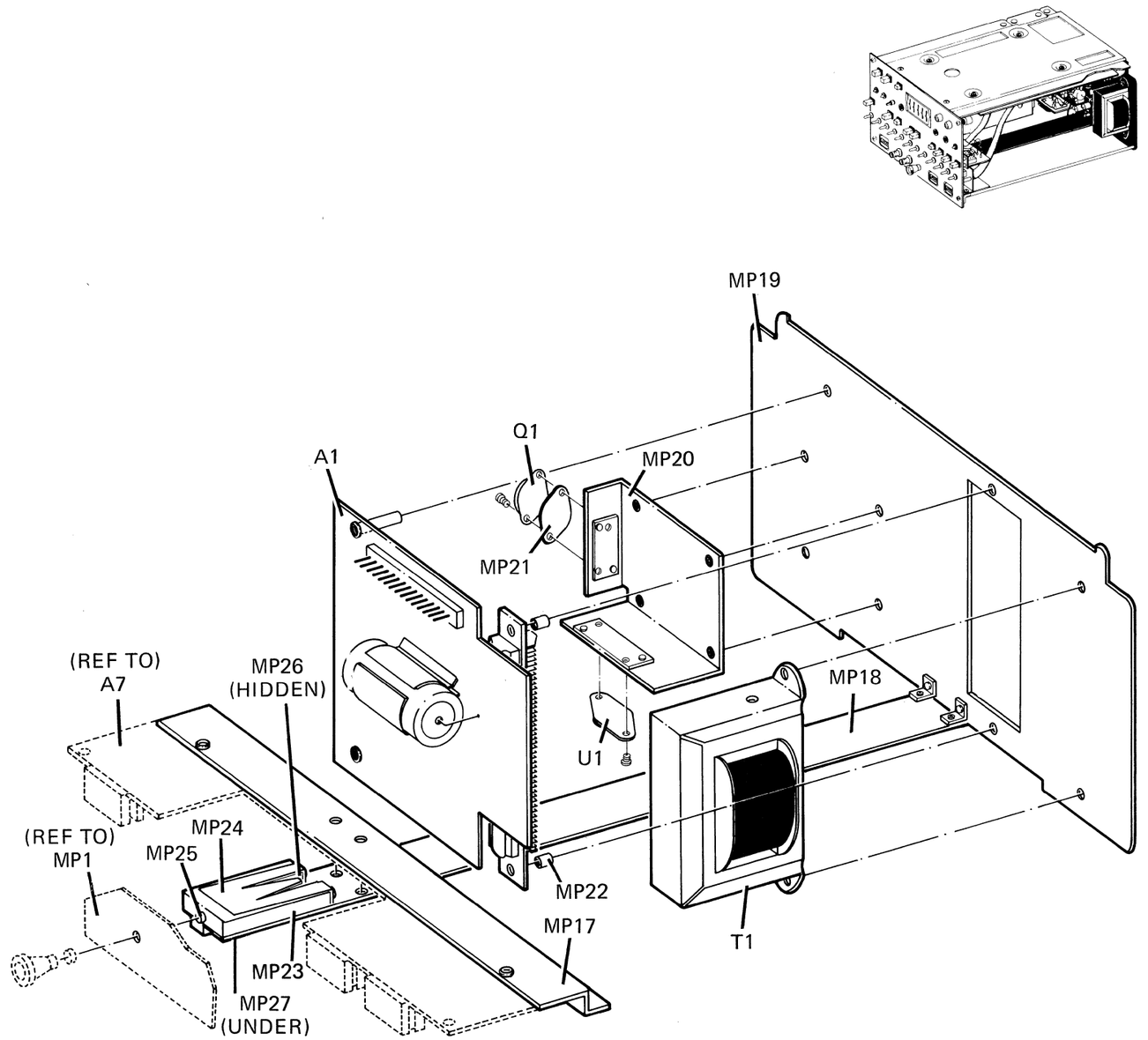


Figure 6-1. Model 1601A Illustrated Parts Breakdown (Sheet 3)

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			CHASSIS PARTS		
A1	01601-66509	1	BOARD ASSY: POWER	28480	01601-66509
A2	01601-66510	1	BOARD ASSY: PROCESSOR (MAIN)	28480	01601-66510
A2A1	01601-66502	1	BOARD ASSY: DELAY	28480	01601-66502
A3	01601-66511	1	BOARD ASSY: MODE CONTROL (PUSHBUTTON)	28480	01601-66511
A4	01601-66507	1	BOARD ASSY: DISPLAY CONTROL (PUSHBUTTON)	28480	01601-66507
A5	01601-66508	1	BOARD ASSY: DISPLAY ADJUST	28480	01601-66508
A6	01601-66504	1	BOARD ASSY: TRIGGER WORD SELECT	28480	01601-66504
A7	01601-66503	1	BOARD ASSY: DATA INPUT	28480	01601-66503
DS1	1990-0324	3	DIODE: LIGHT EMITTER, VISIBLE (SEE NOTE)	28480	1990-0324
DS2	1990-0324		DIODE: LIGHT EMITTER, VISIBLE (SEE NOTE)	28480	1990-0324
DS3	1990-0324		DIODE: LIGHT EMITTER, VISIBLE (SEE NOTE)	28480	1990-0324
J1	1250-0083	2	CONNECTOR: BNC	02660	31-221-1020
J2	1250-0083		CONNECTOR: BNC	02660	31-221-1020
MP1	01601-00201	1	PANEL: FRONT	28480	01601-00201
MP2	01601-60202	1	PANEL: FRONT-SUB	28480	01601-60202
MP3	01601-04101	1	COVER: TOP	28480	01601-04101
MP4	01601-24702	2	SUPPORT: CORNER	28480	01601-24702
MP5	01601-01201	1	BRACKET: RIGHT	28480	01601-01201
MP6	01601-01202	1	BRACKET: LEFT	28480	01601-01202
MP7	0590-0043		NUT: HEX 1/4 x 32 INTERNAL THREAD	00866	OBD
MP8	0370-0603	1	PUSHBUTTON: SQUARE, MINT GRAY	28480	0370-0603
MP9	0370-0604	1	PUSHBUTTON: SQUARE, JADE GRAY	28480	0370-0604
MP10	0370-0610	1	PUSHBUTTON: SQUARE, DARK OLIVE GREEN	28480	0370-0610
MP11	0370-0606	1	BEZEL: SQUARE, PUSHBUTTON, JADE GRAY	28480	0370-0606
MP12	1400-0540	3	CLIP: BEZEL	28480	1400-0540
MP12A	1400-0547	3	BEZEL: LED	28480	1400-0547
MP13	01815-67410	1	KNOB: LATCH	28480	01815-67410
MP14	2190-0199	1	WASHER: FLAT 0.125" ID. 0.312" OD.	86928	5610-10-31
MP15	01803-67401	2	KNOB ASSY (BAL)	28480	01803-67401
MP16	1490-0968	3	BUSHING: POTENTIOMETER 1/4-32 EXT THRD	00000	OBD
MP17	01601-01203	1	BRACKET: SUPPORT	28480	01601-01203
MP18	01601-24701	1	SUPPORT: BOTTOM	28480	01601-24701
MP19	01601-00203	1	PANEL: REAR	28480	01601-00203
MP20	01601-01101	1	HEAT SINK	28480	01601-01101
MP21	1200-0043	1	INSULATOR: TSTR MOUNTING (TO-3)	71785	293011
MP22	0380-0022	2	SPACER: POST TYPE FOR #5 HDW	76854	3457-424
MP23	01815-23101	1	RETAINER: YOKE	28480	01815-23101
MP24	01815-09101	1	SPRING: LATCH	28480	01815-09101
MP25	01815-23701	1	SHAFT: LATCH	28480	01815-23701
MP26	01815-22301	1	YOKE	28480	01815-22301
MP27	01815-05001	1	PAWL: LATCH	28480	01815-05001
MP28	01601-67401	1	KNOB ASSY	28480	01601-67401
MP29	01601-02701	1	CONTRAST FILTER: FOR MODEL 182 MAINFRAMES	28480	01601-02701
MP30	01601-02702	1	CONTRAST FILTER: FOR 180-SERIES MAINFRAMES OTHER THAN MODEL 182.	28480	01601-02702
Q1	1854-0063	1	TSTR: SI NPN	80131	2N3055
R1	2100-2635	1	R: VAR COMP 50K OHM 20% LIN 1/2W	28480	2100-2635
S1	01601-66506	1	BOARD ASSY: DELAY SET MODULE	28480	01601-66506
T1	9100-3426	1	TRANSFORMER: POWER	28480	9100-3426
TP1	0360-1646	1	TERMINAL: SOLDER STUD	17117	4338-67-0
U1	1826-0117	1	IC: REGULATOR 12 VOLT	28480	1826-0117
W1	01601-61601	3	CABLE ASSY: LED	28480	01601-61601
W2	01601-61601		CABLE ASSY: LED	28480	01601-61601
W3	01601-61601		CABLE ASSY: LED	28480	01601-61601
W4	01601-61602	1	CABLE ASSY: VAR SET	28480	01601-61602
W5	01601-61603	1	CABLE ASSY: COAX	28480	01601-61603
W6	01601-61604	1	CABLE ASSY: COAX	28480	01601-61604

NOTE

WHEN REPLACING INDICATOR, ORDER REPLACEMENT PARTS FOR MP12 AND MP12A. THE INDICATORS AND ATTACHING PARTS ARE HEAT MOLDED TOGETHER DURING ASSEMBLY AND MUST BE BROKEN APART TO SEPARATE THEM.

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A1	01601-66509		BOARD ASSY: POWER	28480	01601-66509
A1C1	0180-0420	1	C: FXD AL ELECT 8200 UF +75–10% 15 VDCW	00853	066JP822UD158
A1C2	0160-3448	2	C: FXD CER 1000 PF 10% 1000 VDCW	56289	C067B251F102KS25-CDH
A1C3	0160-0174	6	C: FXD CER 0.47 UF +80–20% 25 VDCW	56289	5C11B7S-CML
A1C4	0160-3451	21	C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A1C5	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A1C6	0160-3665	2	C: FXD CER 0.01 UF +80–20% 500 VDCW	56289	C071A501K103ZS25-CDH
A1C7	0140-0205	1	C: FXD MICA 62 PF 5% 300 VDCW	00853	RDM15E620J3C
A1C8	0160-0154	1	C: FXD MICA MY 0.0022 UF 10% 200 VDCW	56289	192P22292-PTS
A1CR1	1901-0662	4	DIODE: SI, POWER RECTIFIER	04713	MR 751
A1CR2	1901-0662		DIODE: SI, POWER RECTIFIER	04713	MR 751
A1CR3	1901-0662		DIODE: SI, POWER RECTIFIER	04713	MR 751
A1CR4	1901-0662		DIODE: SI, POWER RECTIFIER	04713	MR 751
A1CR5 THRU A1CR18	1901-0040	16	DIODE: SILICON 50 MA 30 WV	07263	FDG 1088
A1E1 THRU A1E8	0360-1653	26	TERMINAL: PIN (CDA 260)	00000	OBD
A1P1	1251-0136	1	CONNECTOR: 32 PIN MALE	02660	26-4100-32P
A1P2	1251-3243	1	CONNECTOR: PC 15 MALE CONTACT	27264	09-64-1151 (A2402-15A)
A1Q1	1854-0053	1	TSTR: SI NPN	80131	2N2218
A1R1	0812-0022	1	R: FXD WW 0.56 OHM 5% 3W	28480	0812-0022
A1R2	0698-4460	1	R: FXD FLM 649 OHM 1% 1/8W	28480	0698-4460
A1R3	0757-0438	2	R: FXD MET FLM 5.11K OHM 1% 1/8W	28480	0757-0438
A1R4	0757-0917	1	R: FXD FLM 510 OHM 2% 1/8W	28480	0757-0917
A1R5	0757-0921	1	R: FXD MET FLM 750 OHM 2% 1/8W	28480	0757-0921
A1R6	2100-1788	1	R: VAR FLM 500 OHM 10% LIN 1/2W	28480	2100-1788
A1R7	0757-0932	1	R: FXD MET FLM 2.2K OHM 2% 1/8W	28480	0757-0932
A1R8	0757-0928	1	R: FXD FLM 1.5K OHM 2% 1/8W	28480	0757-0928
A1R9 THRU A1R13	0684-1031	13	R: FXD COMP 10K OHM 10% 1/4W	01121	CB1031
A1R14	0698-8198	1	R: FXD FLM 1.58 MEGOHM 1.0% 1/8W	28480	0698-8198
A1R15	0757-0487	1	R: FXD MET FLM 825K OHM 1% 1/8W	28480	0757-0487
A1R16	0698-6248	1	R: FXD FLM 3K OHM 0.1% 1/8W	28480	0698-6248
A1R17	0698-6217	2	R: FXD 200K 5% 1/8W F TUBULAR	28480	0698-6217
A1R18	0757-0975	1	R: FXD FLM 130K OHM 2% 1/8W	28480	0757-0975
A1R19	0757-0916	1	R: FXD MET FLM 470 OHM 2% 1/8W	28480	0757-0916
A1R20	0684-5611	2	R: FXD COMP 560 OHM 10% 1/4W	01121	CB 5611
A1R21	0698-3149	1	R: FXD MET FLM 255K OHM 1% 1/8W	28480	0698-3149
A1R22	0757-0970		R: FXD FLM 82K OHM 2% 1/8W	28480	0757-0970
A1R23	0684-5611	1	R: FXD COMP 560 OHM 10% 1/4W	01121	CB 5611
A1R24	0757-0459	1	R: FXD MET FLM 56.2K OHM 1% 1/8W	28480	0757-0459
A1R25	0757-0834	1	R: FXD MET FLM 5.62K OHM 2% 1/2W	28480	0757-0834
A1R26	0684-1031	1	R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A1TP1	0360-1653		TERMINAL: PIN (CDA 260)	00000	OBD
A1TP2	0360-1653		TERMINAL: PIN (CDA 260)	00000	OBD
A1U1	1820-0196	1	IC: LINEAR VOLTAGE REGULATOR (INPUT)	28480	1820-0196
A1VR1	1902-3059	1	DIODE BREAKDOWN: SILICON 3.83V 5%	28480	1902-3059
A1VR2	1902-3048	1	DIODE BREAKDOWN: SILICON 3.48V 5%	28480	1902-3048
A2	01601-66510		BOARD ASSY: PROCESSOR	28480	01601-66510
A2C1	0160-0174		C: FXD CER 0.47 UF +80–20% 25 VDCW	56289	5C11B7S-CML
A2C2	0160-3448		C: FXD CER 1000 PF 10% 1000 VDCW	56289	C067B251F102KS25-CDH
A2C3	0140-0175	4	C: FXD MICA 39 PF 2% 300 VDCW	28480	0140-0175
A2C4	0160-2101	1	C: FXD MICA 27 PF 2% 300 VDCW	72136	RDM15E270G3C
A2C5	0140-0175		C: FXD MICA 39 PF 2% 300 VDCW	28480	0140-0175
A2C6	0140-0175		C: FXD MICA 39 PF 2% 300 VDCW	28480	0140-0175
A2C7	0160-0174		C: FXD CER 0.47 UF +80–20% 25 VDCW	56289	5C11B7S-CML
A2C8	0180-0116	2	C: FXD ELECT 6.8 UF 10% 35 VDCW	56289	150D685X9035B2-DYS
A2C9	0180-0116		C: FXD ELECT 6.8 UF 10% 35 VDCW	56289	150D685X9035B2-DYS
A2C10	0160-0174		C: FXD CER 0.47 UF +80–20% 25 VDCW	56289	5C11B7S-CML
A2C11	0180-0161	1	C: FXD ELECT 3.3 UF 20% 35 VDCW	56289	150D335X0035B2-DYS
A2C12	0160-2207	1	C: FXD MICA 300 PF 5%	28480	0160-2207
A2C13	0180-0197	7	C: FXD ELECT 2.2 UF 10% 20 VDCW	56289	150D225X9020A2-DYS
A2C14	0160-4059	1	C: FXD POLY 1.0 UF 10% 250 VDCW	80031	C280AE/AIM
A2C15	0160-2218	1	C: FXD MICA 1000 PF 5%	28480	0160-2218
A2C16	0160-0161	1	C: FXD MY 0.01 UF 10% 200 VDCW	56289	192P10392-PTS
A2C17	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A2C18	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A2C19	0160-2202	1	C: FXD MICA 75 PF 5%	28480	0160-2202
A2C20	0160-0302	1	C: FXD MY 0.018 UF 10% 200 VDCW	56289	192P18392-PTS

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2C21	0180-0229		C: FXD ELECT 33 UF 10% 10 VDCW	28480	0180-0229
A2C22	0180-0229		C: FXD ELECT 33 UF 10% 10 VDCW	28480	0180-0229
A2C23	0180-0229		C: FXD ELECT 33 UF 10% 10 VDCW	28480	0180-0229
A2C24	0180-0197		C: FXD ELECT 2.2 UF 10% 20 VDCW	56289	150D225X9020A2-DYS
A2C25 THRU A2C35	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A2C36	0180-0197		C: FXD ELECT 2.2 UF 10% 20 VDCW	56289	150D225X9020A2-DYS
A2C37 THRU A2C40	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A2C41	0180-0197		C: FXD ELECT 2.2 UF 10% 20 VDCW	56289	150D225X9020A2-DYS
A2C42	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A2C43	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A2C44	0160-3451		C: FXD CER 0.01 UF +80–20% 100 VDCW	56289	C023B101F103ZS25-CDH
A2C45	0180-0197		C: FXD ELECT 2.2 UF 10% 20 VDCW	56289	150D225X9020A2-DYS
A2C46	0180-0197		C: FXD ELECT 2.2 UF 10% 20 VDCW	56289	150D225X9020A2-DYS
A2C47	0180-0197		C: FXD ELECT 2.2 UF 10% 20 VDCW	56289	150D225X9020A2-DYS
A2CR1	1901-0535	2	DIODE: HYBRID HOT CARRIER	28480	1901-0535
A2CR2	1901-0535		DIODE: HYBRID HOT CARRIER	28480	1901-0535
A2CR3	1901-0040		DIODE: SILICON 50 MA 30 WV	07263	FDG 1088
A2CR4	1901-0579	2	DIODE: SI (SPECIAL)	03508	SE 445
A2CR5	1901-0579		DIODE: SI (SPECIAL)	03508	SE 445
A2CR6	1901-0040		DIODE: SILICON 50 MA 30 WV	07263	FDG 1088
A2E1 THRU A2E6	0360-1653		TERMINAL: PIN (CDA 260)	00000	OBD
A2E7	0340-0060	2	FEEDTHRU: INSULATED MOUNTING	28480	0340-0060
A2E8	0340-0060		FEEDTHRU: INSULATED MOUNTING	28480	0340-0060
A2J1	1251-0213	1	CONNECTOR: PC EDGE 15 CONTACT	95354	91-6915-1700-00
A2J2	1251-0649	1	CONNECTOR: POST TYPE 15 FEMALE CONTACT	27264	09-52-3151
A2J3 THRU A2J8	1200-0441	8	SOCKET: IC 14 PIN MINIATURE	28480	1200-0441
A2J9	1200-0438	2	SOCKET: IC 16 CONTACT DUAL TYPE, BROWN	00779	583529-1
A2J10	1200-0438		SOCKET: IC 16 CONTACT DUAL TYPE, BROWN	00779	583529-1
A2L1	9140-0158	1	COIL: FXD RF 1 UH 10%	99800	1025-20
A2L2	9100-1663	1	COIL: CHOKE 2700 UH 5%	99800	2500-48
A2MP1	5040-0170	2	GUIDE: PLUG-IN PC BOARD	28480	5040-0170
A2MP2	5040-0170		GUIDE: PLUG-IN PC BOARD	28480	5040-0170
A2Q1	1853-0015	2	TSTR: SI PNP	80131	2N3640
A2Q2	1853-0015		TSTR: SI PNP	80131	2N3640
A2Q3	1854-0246	1	TSTR: SI NPN	80131	2N3643
A2Q4	1853-0050	1	TSTR: SI PNP	28480	1853-0050
A2Q5	1855-0036	1	TSTR: SI FET	28480	1855-0036
A2Q6	1853-0036	2	TSTR: SI PNP	80131	2N3906
A2Q7	1853-0036		TSTR: SI PNP	80131	2N3906
A2Q8 THRU A2Q10	1854-0071	4	TSTR: SI NPN (SELECTED FROM 2N3704)	28480	1854-0071
A2Q11	1853-0022	2	TSTR: SI PNP	80131	2N941
A2Q12	1853-0022		TSTR: SI PNP	80131	2N941
A2Q13	1854-0071		TSTR: SI NPN (SELECTED FROM 2N3704)	28480	1854-0071
A2R1	0757-0472		R: FXD MET FLM 200K OHM 1% 1/8W	28480	0757-0472
A2R2	0757-0465	1	R: FXD MET FLM 100K OHM 1% 1/8W	28480	0757-0465
A2R3	0757-0463	1	R: FXD MET FLM 82.5K OHM 1% 1/8W	28480	0757-0463
A2R4	0757-0418	2	R: FXD MET FLM 619 OHM 1% 1/8W	28480	0757-0418
A2R5	0698-3447	2	R: FXD MET FLM 422 OHM 1% 1/8W	28480	0698-3447
A2R6	0684-6801	2	R: FXD COMP 68 OHM 10% 1/4W	01121	CB 6801
A2R7	0757-0433	1	R: FXD MET FLM 3.32K OHM 1% 1/8W	28480	0757-0433
A2R8	0757-0280	7	R: FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A2R9	0757-0903	2	R: FXD MET FLM 130 OHM 2% 1/4W	28480	0757-0903
A2R10	0757-0418		R: FXD MET FLM 619 OHM 1% 1/8W	28480	0757-0418
A2R11	0698-3447		R: FXD MET FLM 422 OHM 1% 1/8W	28480	0698-3447
A2R12	0684-6801		R: FXD COMP 68 OHM 10% 1/4W	01121	CB 6801
A2R13	0757-0290	1	R: FXD MET FLM 6.19K OHM 1% 1/8W	28480	0757-0290
A2R14	0757-0280		R: FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A2R15	0757-0903		R: FXD MET FLM 130 OHM 2% 1/4W	28480	0757-0903
A2R16	0684-3911	1	R: FXD COMP 390 OHM 10% 1/4W	01121	CB 3911
A2R17	0757-0280		R: FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A2R18	0757-0471	2	R: FXD MET FLM 182K OHM 1% 1/8W	28480	0757-0471
A2R19	0757-0273	2	R: FXD MET FLM 3.01K OHM 1% 1/8W	28480	0757-0273
A2R20	0757-0280		R: FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A2R21	0757-0471		R: FXD MET FLM 182K OHM 1% 1/8W	28480	0757-0471
A2R22	0757-0273		R: FXD MET FLM 3.01K OHM 1% 1/8W	28480	0757-0273
A2R23	0684-4731	4	R: FXD COMP 47K OHM 10% 1/4W	01121	CB 4731

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2R24	0684-4731		R: FXD COMP 47K OHM 10% 1/4W	01121	CB 4731
A2R25	0757-0401	1	R: FXD MET FLM 100 OHM 1% 1/8W	28480	0757-0401
A2R26	0757-0394	1	R: FXD MET FLM 51.1 OHM 1% 1/8W	28480	0757-0394
A2R27 THRU A2R29	0684-1031		R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A2R30	0684-4731		R: FXD COMP 47K OHM 10% 1/4W	01121	CB 4731
A2R31	0684-4731		R: FXD COMP 47K OHM 10% 1/4W	01121	CB 4731
A2R32	0684-1031		R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A2R33	0757-0946	3	R: FXD FLM 8.2K OHM 2% 1/8W	28480	0757-0946
A2R34	0683-2265	1	R: FXD COMP 22 MEGOHM 5% 1/4W	01121	CB 2265
A2R35	0757-0462	3	R: FXD MET FLM 75.0K OHM 1% 1/8W	28480	0757-0462
A2R36	0757-0199	1	R: FXD MET FLM 21.5K OHM 1% 1/8W	28480	0757-0199
A2R37	0757-0462		R: FXD MET FLM 75.0K OHM 1% 1/8W	28480	0757-0462
A2R38	0698-3158	1	R: FXD MET FLM 23.7K OHM 1% 1/8W	28480	0698-3158
A2R39	0684-1031		R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A2R40	0684-2221	10	R: FXD COMP 2200 OHM 10% 1/4W	01121	CB 2221
A2R41	0757-0462		R: FXD MET FLM 75.0K OHM 1% 1/8W	28480	0757-0462
A2R42	0757-0123	1	R: FXD MET FLM 34.8K OHM 1% 1/8W	28480	0757-0123
A2R43	0757-0446	1	R: FXD MET FLM 15.0K OHM 1% 1/8W	28480	0757-0446
A2R44	0757-0440	1	R: FXD MET FLM 7.50K OHM 1% 1/8W	28480	0757-0440
A2R45	0757-0946		R: FXD FLM 8.2K OHM 2% 1/8W	28480	0757-0946
A2R46	0757-0444	1	R: FXD MET FLM 12.1K OHM 1% 1/8W	28480	0757-0444
A2R47	0757-0454	2	R: FXD MET FLM 33.2K OHM 1% 1/8W	28480	0757-0454
A2R48	0757-0454		R: FXD MET FLM 33.2K OHM 1% 1/8W	28480	0757-0454
A2R49	0757-0836	2	R: FXD MET FLM 7.50K OHM 1% 1/2W	28480	0757-0836
A2R50	0757-0836		R: FXD MET FLM 7.50K OHM 1% 1/2W	28480	0757-0836
A2R51	0698-0084	1	R: FXD MET FLM 2.15K OHM 1% 1/8W	28480	0698-0084
A2R52	0757-0441	1	R: FXD MET FLM 8.25K OHM 1% 1/8W	28480	0757-0441
A2R53	0684-1031		R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A2R54	2100-2216	1	R: VAR FLM 5K OHM 10% LIN 1/2W	28480	2100-2216
A2R55	0757-0943	1	R: FXD FLM 6.2K OHM 2% 1/8W	28480	0757-0943
A2R56	0757-0907	2	R: FXD FLM 200 OHM 2% 1/8W	28480	0757-0907
A2R57	0757-0907		R: FXD FLM 200 OHM 2% 1/8W	28480	0757-0907
A2R58	0757-0946		R: FXD FLM 8.2K OHM 2% 1/8W	28480	0757-0946
A2R59	0757-0929	1	R: FXD FLM 1.6K OHM 2% 1/8W	28480	0757-0929
A2R60	0684-1031		R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A2R61	0757-0918	1	R: FXD FLM 560 OHM 2% 1/8W	28480	0757-0918
A2R62	0757-0898	1	R: FXD FLM 82 OHM 2% 1/8W	28480	0757-0898
A2R63	0757-0927	1	R: FXD FLM 1.3K OHM 2% 1/8W	28480	0757-0927
A2R64	0757-0933	1	R: FXD FLM 2.4K OHM 2% 1/8W	28480	0757-0933
A2R65	0684-1831	2	R: FXD COMP 18K OHM 10% 1/4W	01121	CB 1831
A2R66	0757-0280		R: FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A2R67	0757-0280		R: FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A2R68	0757-0280		R: FXD MET FLM 1K OHM 1% 1/8W	28480	0757-0280
A2R69 THRU A2R76	0684-2221		R: FXD COMP 2200 OHM 10% 1/4W	01121	CB 2221
A2R77	0687-1211	1	R: FXD COMP 120 OHM 10% 1/2W	01121	EB 1211
A2R78	0684-2221		R: FXD COMP 2200 OHM 10% 1/4W	01121	CB 2221
A2R79	0684-1031		R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A2R80	0684-1031		R: FXD COMP 10K OHM 10% 1/4W	01121	CB 1031
A2U1 THRU A2U6	1820-0693	6	IC: TTL SCHOTTKY DUAL D F/F W/PRESET	01295	SN74S74N
A2U7 THRU A2U12	1820-0074	6	INTEGRATED CIRCUIT: 4 WIDE, 2 INPUT INVERT	01295	SN7454N
A2U13	1820-0375	1	IC: TTL HS 8-INPT NAND GATE	01295	SN74H30N
A2U14	1820-0231	4	IC: TTL 4-BIT SYNC BINARY COUNTER	07263	U6B931659X
A2U15	1820-1106	3	IC: DIGITAL MEMORY	34649	P3101A
A2U16	1820-1106		IC: DIGITAL MEMORY	34649	P3101A
A2U17	1820-1106		IC: DIGITAL MEMORY	34649	P3101A
A2U18	1820-0615	1	IC: TTL 8-INPT MULTIPLEXER W/COM. ENABLE	04713	FAIR 9312
A2U19	1820-0094	1	IC: DTL QUAD 2-INPUT GATE	04713	SC6903PK
A2U20	1820-0203	1	IC: OPERATIONAL AMPLIFIER	07263	SL8940
A2U21	1820-0681	2	IC: TTL QUAD 2-INPT NAND GATE	01295	SN74S00N
A2U22	1820-0681		IC: TTL QUAD 2-INPT NAND GATE	01295	SN74S00N
A2U23	1820-0697	1	IC: TTL DUAL 4-INPT LINE DRIVER	01295	SN74S140N
A2U24	1820-0321	5	INTEGRATED CIRCUIT: HI-SPEED COMPARATOR	01295	SN72 710L
A2U25	1820-0321		INTEGRATED CIRCUIT: HI-SPEED COMPARATOR	01295	SN72 710L
A2U26	1820-0515	2	IC: TTL DUAL RE-TRIG/RE-SET MONO-MULTI	07263	U7B960259X
A2U27	1820-0907	2	IC: TTL TRIPLE 3-INPT NAND GATE	01295	SN7412N
A2U28	1820-0512	1	IC: TTL HS DUAL D F/F (35 MHZ MIN.)	01295	SN74H74N
A2U29	1820-0231		IC: TTL 4-BIT SYNC BINARY COUNTER	07263	U6B931659X
A2U30	1820-0370	1	IC: TTL HS QUAD 2-INPT NAND GATE	01295	SN74H00N
A2U31	1820-0328	1	IC: TTL QUAD 2-INPT NOR GATE	04713	SN7402N
A2U32	1820-0379	1	IC: TTL HS 4W 2-2-2-3 INPT AND/OR GATE	01295	SN74H52N
A2U33	1820-0515		IC: TTL DUAL RE-TRIG/RE-SET MONO-MULTI	07263	U7B960259X
A2U34	1820-0054	1	IC: TTL QUAD 2-INPT NAND GATE	01295	SN7400N
A2U35	1820-0077	3	IC: TTL DUAL D F/F	01295	SN7474N
A2U36	1820-0231		IC: TTL 4-BIT SYNC BINARY COUNTER	07263	U6B931659X
A2U37	1816-0343	1	IC: ROM BIPOLAR 256 x 4	28480	1816-0343

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
A2U38	1820-0231		IC: TTL 4-BIT SYNC BINARY COUNTER	07263	U6B931659X
A2U39	1820-1172	1	IC: TTL HEX INVERTER/DRIVER	07263	SL55494
A2U40	1820-0655	1	IC: TTL DUAL INPUT NOR GATE WITH STROBE	01295	SN23684
A2U41	1820-0907		IC: TTL TRIPLE 3-INPT NAND GATE	01295	SN7412N
A2U42	1820-0618	1	IC: TTL HEX BUFFER/DRIVER W/OPEN COLL.	01295	SN7417N
A2U43 THRU A2U45	1820-0321		INTEGRATED CIRCUIT: HI-SPEED COMPARATOR	01295	SN72 710L
A2U46	1820-0077		IC: TTL DUAL D F/F	01295	SN7474N
A2VR1	1902-0049	1	DIODE: BREAKDOWN 6.19V 5%	04713	SZ10939-122
A2A1	01601-66502		BOARD ASSY: DELAY	28480	01601-66502
A2A1C1	0180-0229		C: FXD ELECT 33 UF 10% 10 VDCW	28480	0180-0229
A2A1J1	1200-0441		SOCKET: IC 14 PIN MINIATURE	28480	1200-0441
A2A1J2	1200-0441		SOCKET: IC 14 PIN MINIATURE	28480	1200-0441
A2A1R1 THRU A2A1R20	0684-6821	41	R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A2A1U1 THRU A2A1U5	1820-0705	5	IC: TTL SYNC PRESET DECADE COUNTER	07263	U7B931059X
A2A1U6	1820-0372	1	IC: TTL TRIPLE 3-INPT AND GATE	28480	1820-0372
A2A1U7	1820-0371	1	IC: TTL HS TRIPLE 3-INPUT NAND GATE	01295	SN74H10N
A2A1U8	1820-0077		IC: TTL DUAL D F/F	01295	SN7474N
A3	01601-66511		BOARD ASSY: MODE CONTROL (PUSHBUTTON)	28480	01601-66511
A3E1 THRU A3E10	0360-1653		TERMINAL: PIN (CDA 260)	00000	OBD
A3R1	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A3R2	0757-0438		R: FXD MET FLM 5.11K OHM 1% 1/8W	28480	0757-0438
A3R3	0698-0084		R: FXD MET FLM 2.15K OHM 1% 1/8W	28480	0698-0084
A3R4	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A3R5	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A3R6	0757-0415	1	R: FXD MET FLM 475 OHM 1% 1/8W	28480	0757-0415
A3R7	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A3R8	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A3R9	0684-1211	3	R: FXD COMP 120 OHM 10% 1/4W	01121	CB 1211
A3R10	0684-1211		R: FXD COMP 120 OHM 10% 1/4W	01121	CB 1211
A3R11	0684-1211		R: FXD COMP 120 OHM 10% 1/4W	01121	CB 1211
A3R12	0684-4701	1	R: FXD COMP 47 OHM 10% 1/4W	01121	CB 4701
A3R13	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A3R14	0757-0429	1	R: FXD MET FLM 1820 OHM 1% 1/8W	28480	0757-0429
A3S1	3101-0577	1	SWITCH: PUSHBUTTON 2 PDT 12 STATION	28480	3101-0577
A3W1	8120-0618	1	CABLE ASSY: 14-PIN	28480	8120-0618
A4	01601-66507		BOARD ASSY: DISPLAY CONTROL (PUSHBUTTON)	28480	01601-66507
A4R1	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A4R2	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A4R3	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A4S1	3101-0578	1	SWITCH: PUSHBUTTON 2 PDT, 3 STATION	71590	PB-15
A4W1	8120-0621	1	CABLE ASSY	28480	8120-0621
A5	01601-66508		BOARD ASSY: DISPLAY ADJUST	28480	01601-66508
A5MP1	0590-0043	3	NUT: HEX 1/4 x 32 INTERNAL THREAD	00866	OBD
A5R1	2100-0584	1	R: VAR COMP 250K OHM 20% LIN 1/2W	28480	2100-0584
A5R2	2100-3064	1	R: VAR COMP 25K OHM 20% LIN 1/2W	28480	2100-3064
A5R3	2100-2361	1	R: VAR COMP 100K OHM 10% LIN 1/2W	28480	2100-2361
A5R4	2100-2492	1	R: VAR COMP 5K OHM 20% LIN 1/2W	28480	2100-2492
A5W1	8120-0622	1	CABLE ASSY	28480	8120-0622
A6	01601-66504		BOARD ASSY: TRIGGER WORD SELECT	28480	01601-66504
A6R1 THRU A6R12	0684-6821		R: FXD COMP 6.8K OHM 10% 1/4W	01121	CB 6821
A6S0 THRU A6S11	3101-0576	12	SWITCH: TOGGLE SPDT, SUB-MINIATURE	09353	7103-PX
A6W1	8120-0623	2	CABLE ASSY	28480	8120-0623
A6W2	8120-0623		CABLE ASSY	28480	8120-0623
A7	01601-66503		BOARD ASSY: DATA INPUT	28480	01601-66503
A7C1	0160-0174		C: FXD CER 0.47 UF +80–20% 25 VDCW	56289	5C11B75-CML
A7C2	0160-0174		C: FXD CER 0.47 UF +80–20% 25 VDCW	56289	5C11B75-CML
A7J1	01601-67601	3	CONNECTOR: 17-PIN	28480	01601-67601
A7J2	01601-67601		CONNECTOR: 17-PIN	28480	01601-67601
A7J3	01601-67601		CONNECTOR: 17-PIN	28480	01601-67601
A7U1	1820-1139	2	IC: TTL, HEX INVERTER	28480	1820-1139
A7W1	8120-0617	2	CABLE ASSY: RIBBON 16-PIN	28480	8120-0617
A7W2	8120-0617		CABLE ASSY: RIBBON 16-PIN	28480	8120-0617
A7W3	8120-0619	1	CABLE ASSY: RIBBON 14-PIN	28480	8120-0619
S1	01601-66506		BOARD ASSY: DELAY SET MODULE	28480	01601-66506
S1W1	8120-0620	2	CABLE ASSY: 14-PIN	28480	8120-0620
S1W2	8120-0620		CABLE ASSY: 14-PIN	28480	8120-0620

See introduction to this section for ordering information

Table 6-3. List of Manufacturers' Codes

MFR. NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	U.S.A. COMMON	ANY SUPPLIER OF U.S.A.	
00779	AMP INC. (AIR CRAFT MARINE PROD.)	HARRISBURG, PENNSYLVANIA	17101
00853	SANGAMO ELECTRIC CO. PICKENS DIV.	PICKENS, S. CAROLINA	29671
00866	GOE ENGINEERING CO., INC.	CITY OF INDUSTRY, CALIFORNIA	91746
01121	ALLEN BRADLEY CO.	MILWAUKEE, WISCONSIN	53204
01295	TEXAS INSTRUMENT INC. SEMICONDUCTOR COMPONENTS DIV.	DALLAS, TEXAS	75231
02660	AMPHENOL CORP.	BROADVIEW, ILLINOIS	60153
03508	G.E. CO. SEMICONDUCTOR PROD. DEPT.	SYRACUSE, NEW YORK	13201
04713	MOTOROLA SEMICONDUCTOR PROD. INC.	PHOENIX, ARIZONA	85008
07263	FAIRCHILD CAMERA & INST. CORP. SEMICONDUCTOR DIV.	MOUNTAIN VIEW, CALIFORNIA	94040
09353	C & K COMPONENTS INC.	NEWTON, MASSACHUSETTS	02158
17117	ELECTRONIC MOLDING CORP.	PAWTUCKET, RHODE ISLAND	02860
27264	MOLEX PROD. CO.	DOWNERS GROVE, ILLINOIS	60515
28480	HEWLETT-PACKARD CO. CORPORATE HQ	YOUR NEAREST HP OFFICE	
56289	SPRAGUE ELECTRIC CO.	N. ADAMS, MASSACHUSETTS	01247
71590	GLOBE UNION INC. CENTRALAB DIV.	MILWAUKEE, WISCONSIN	53201
71785	CINCH MFG. CO. DIV TRW INC.	ELK GROVE VILLAGE, ILLINOIS	60007
72136	ELECTRO MOTIVE MFG. CO., INC.	WILLIMANTIC, CONNECTICUT	06226
76854	OAK MFG. CO. DIV OAK ELECTRO/NETICS CORP.	CRYSTAL LAKE, ILLINOIS	60014
80031	MEPCO DIV. SESSIONS CLOCK CO.	MORRISTOWN, NEW JERSEY	07960
80131	ELECTRONIC INDUSTRIES ASSOCIATION	WASHINGTON D.C.	20006
86928	SEASTROM MFG. CO., INC.	GLENDALE, CALIFORNIA	91201
95354	METHODE MFG. CO.	ROLLING MEADOWS, ILLINOIS	60008
99800	DELEVAN ELECTRONICS CORP.	E. AURORA, NEW YORK	14052

SECTION VII

MANUAL CHANGES AND OPTIONS

7-1. INTRODUCTION.

7-2. This section contains information required to backdate or update this manual for a specific instrument. Description of special options and standard options are also in this section.

7-3. MANUAL CHANGES.

7-4. This manual applies directly to the instrument having the same serial prefix shown on the manual title page. If the serial prefix of the instrument is not the same as the one on the title page, find your serial prefix in table 7-1 and make the changes to the manual that are listed for that serial prefix. When making changes listed in table 7-1, make the change with the highest number first. Example: if backdating changes 1, 2, and 3 are required for your serial prefix, do change 3 first, then change 2, and finally change 1. If the serial prefix of the instrument is not listed on the title page or in table 7-1, refer to an enclosed MANUAL CHANGES sheet. If a MANUAL CHANGES sheet is supplied, make the applicable changes and all ERRATA corrections.

Table 7-1. Manual Changes

Serial Prefix	Make Changes
1338A	3
1312A	3 and 2
1311A	3 thru 1

CHANGE 1

Schematic 9,
Delete: LDE connection from pin 8 of A2U35B to pin 4 of A2U33A.
Add: Connection from pin 6 to pin 4 on A2U33A.

CHANGE 2

Table 6-2,
A2: Change HP Part No. and Mfr. Part No. to 01601-66501 (affects pages 6-5 and 6-6).
A3: Change HP Part No. and Mfr. Part No. to 01601-66511 (affects pages 6-5 and 6-9).
Delete: A2Q13, A2R79, and A2R80.
A3R6: Change to HP Part No. 0684-6821, R:FXD COMP 6800 OHM 10% 1/4W, Mfr. Code 01121, Mfr. Part No. CB 6821.
Delete: A3R14.

Page 8-23/8-24, schematic 5,
A6/A2, pin 11: Change LFR 7, 10 to read +5V.
Page 8-27, schematic 7,
A3R6: Change value to 6800.
Delete: A3R14, A2R80, A2Q13, and A2R79.
A3/A2 pin 1: Label +5V to schematics 5 and 10 in place of A2Q13.
Page 8-33, schematic 10,
A4/A2 pin 4: Relabel to read LFR, 7.

CHANGE 3

Table 6-2,

T1: Change HP Part No. and Mfr. Part No. to 9100-3404.

7-5. SPECIAL OPTIONS.

7-6. Most customer special application requirements and/or specifications can be met by factory modification of a standard instrument. A standard instrument modified in this way will carry a special option number, such as Model 0000A/Option C01.

7-7. An operating and service manual and a manual insert are provided with each special option instrument. The operating and service manual contains information about the standard instrument. The manual insert for the special option describes the factory modifications required to produce the special option instrument. Amend the operating and service manual by changing it to include all manual insert information (and CHANGED PAGES or MANUAL CHANGES sheet information, if applicable). When these changes are made, the operating and service manual will apply to the special option instrument.

7-8. If you have ordered a special option instrument and the manual insert is missing, notify the nearest Hewlett-Packard Sales/Service Office. Be sure to give a full description of the instrument, including the complete serial number and special option number.

7-9. STANDARD OPTIONS.

7-10. Standard options are modifications installed on HP instruments at the factory and are available on request. Contact the nearest Hewlett-Packard Sales/Service Office for information concerning standard options.

SECTION VIII

SCHEMATICS AND TROUBLESHOOTING

8-1. INTRODUCTION.

8-2. This section contains schematics, repair and replacement information, component-identification illustrations, waveforms, test conditions, and a troubleshooting chart.

8-3. SCHEMATICS.

8-4. The schematics indicate electronic functions of the Model 1601A circuitry. Any one schematic may include all or part of several different physical assemblies. Table 8-1 defines symbols and conventions used in the schematics. Figure 8-1 provides terminal identification drawings for semiconductors used in the Model 1601A. Figure 8-22 provides power, ground, and logic connections for integrated circuit (IC's) used in the Model 1601A.

8-5. The schematics are numbered in sequence with a bold number at the lower right-hand corner of each page. These numbers are used to cross reference signal connections between schematics. At each circuit breaking point, a notation is made of the signal name and a number (in bold type). This number indicates the associated schematic which shows the source or destination of the signal. To find the source or destination of any point on a given schematic, turn to the schematic referred to by number and find the name of the signal in question. Refer to table 4-1 for a list of logic term definitions and origins.

8-6. Square-pin connections are identified by the color code of the connecting wire. Connector pins on plugs and jacks are identified by a letter. The letters G, I, O, and Q have been omitted.

8-7. A table on each schematic lists all components shown on the schematic by reference designation. Component reference designators which have been deleted from the schematic are listed below the table.

8-8. REFERENCE DESIGNATIONS.

8-9. The unit system of reference designations used in this manual is in accordance with the provisions of USA Standard Y32.16-1968, Reference Designations for Electrical and Electronics Parts and Equipments, dated March 1, 1968. Minor variations from the standard, due to design and manufacturing practices, may be noted.

8-10. Each electrical component is assigned a class letter and number. This letter-number combination is the basic reference designation. Components which are not part of an assembly have only the basic reference designation. Components which are part of an assembly have, in addition to the basic designation, a prefix designation indicating the assembly of which the component is a part (resistor R23 on assembly A1 is called A1R23).

8-11. Assemblies are numbered consecutively. If an assembly reference designation is assigned and later deleted, that number is not reused.

8-12 COMPONENT LOCATIONS.

8-13. Locations of components on assemblies and subassemblies are shown in illustrations adjacent to the schematics. Since the schematics indicate electronic function, portions of a particular assembly may appear on several different schematics. The component-location illustration is printed next to the schematic that shows most of the circuitry on the assembly. The locations of all adjustments are shown in Section V. Exploded-view drawings showing mechanical (and some electrical) parts are located in Section VI.

8-14. REPAIR AND REPLACEMENT.

8-15. The following paragraphs provide procedures for removal and replacement of assemblies, subassemblies, and components in the Model 1601A. Special servicing instructions for the circuit boards are covered under paragraphs 8-21 through 8-28. Section VI provides a detailed parts list for use in ordering replacement parts.

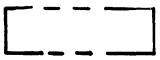
8-16. DISASSEMBLY PROCEDURES.

Note

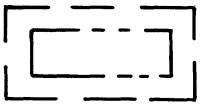
Refer to illustrations in Section VI for locations of mechanical parts (MP reference designators).

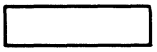
Table 8-1. Schematic Notes

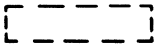
Refer to MIL-STD-15-1A for schematic symbols not listed in this table.

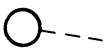
1.  Etched circuit board

2.  Assembly

3.  Etched circuit board on assembly

4.  Front-panel marking

5.  Rear-panel Marking

6.  Front-panel control

7.  Screwdriver adjustment

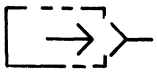
8. P/O Part of

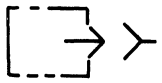
9. CW Clockwise end of variable resistor

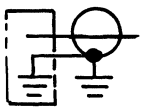
10. NC No connection

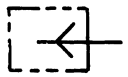
11.  Waveform test point (with number)

12.  Clamp type connector

13.  Single-pin connector on board

14.  Pin of a plug-in board (with letter or number)

15.  Coaxial cable connected directly to board

16.  Wire connected to pressure-fit socket on board

17. Main signal path

18. Primary feedback path

19. Secondary feedback path

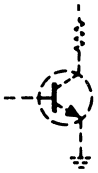
20.  Test point

21.  Field-effect transistor (N-type base)

22.  Breakdown diode (voltage regulator)

23.  Light emitting diode (LED)

24.  Step-recovery diode

25.  Circuits or components drawn with dashed lines (phantom) show function only and are not intended to be complete. The circuit or component is shown in detail on another schematic.

26. (925) Wire colors are given by numbers in parentheses using the resistor color code
[(925) is wht-red-grn]

0 - black	5 - Green
1 - Brown	6 - Blue
2 - Red	7 - Violet
3 - Orange	8 - Gray
4 - Yellow	9 - White

27. * Optimum value selected at factory, typical value shown; part may have been omitted.

28. Unless otherwise indicated:
resistance in ohms
capacitance in picofarads
inductance in microhenries

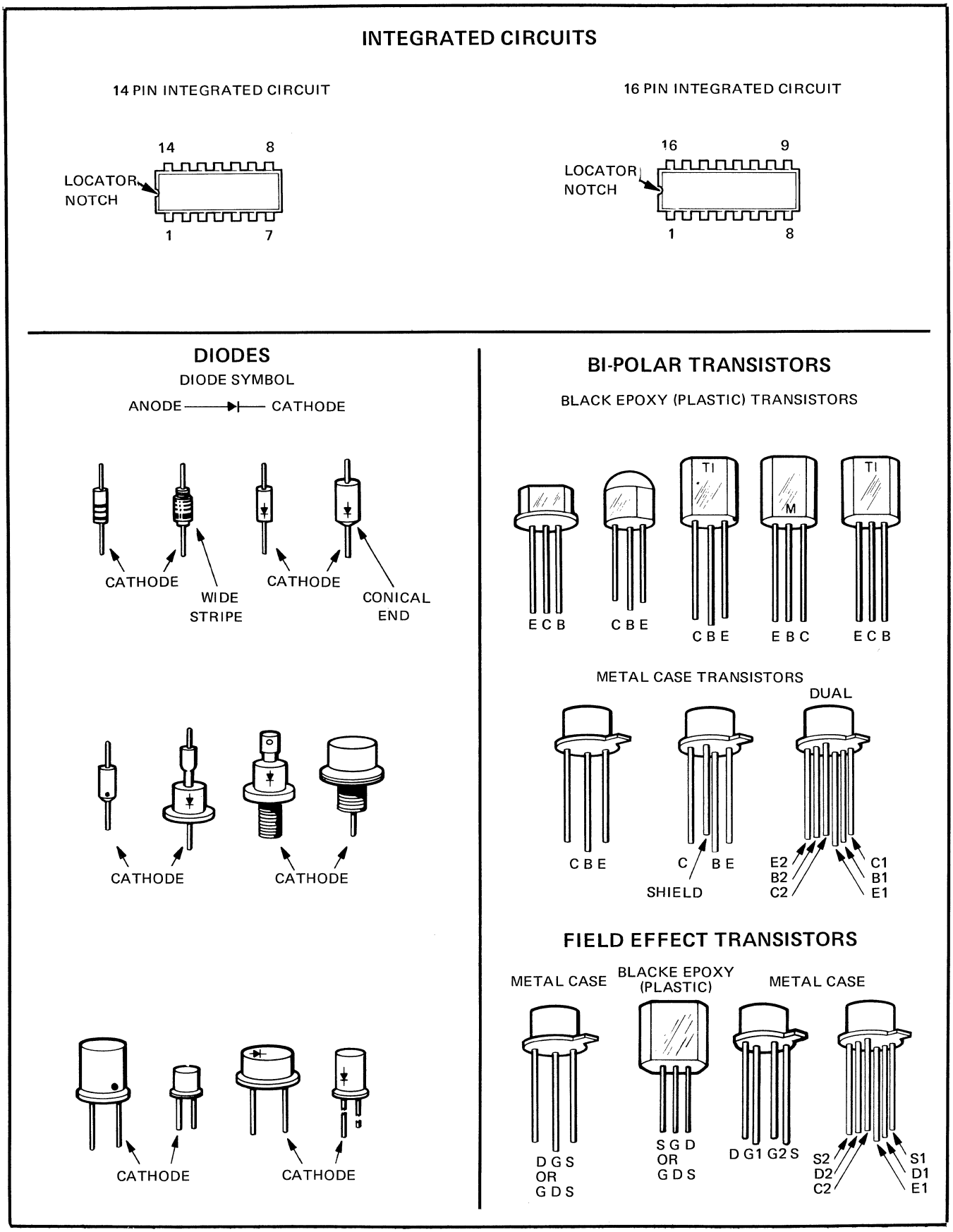


Figure 8-1. Semiconductor Terminal Identification

8-17. Front Panel Assembly Removal. Remove front panel assembly as follows:

Note

Exercise care to prevent damage to ribbon connectors. Use small screwdriver for removal.

a. Disconnect all ribbon connectors and square pin connections between front panel assembly and processor board (A2) and delay generator (A2A2). Make note of connection locations for later reassembly.

b. Remove two square pin connections between processor board and vertical output tabs E1A and B on top cover.

c. Remove top cover by removing three screws along top of rear panel, four screws holding top cover to processor board, and two screws at front of top cover.

d. Remove two screws holding bottom corners of front panel assembly to corner supports (MP-4).

e. Remove two screws holding Data Input board support bracket (MP-17) to bottom support (MP-18).

f. Remove four screws holding bottom support (MP-18) to locking yoke retainer (MP-23) and carefully remove front panel assembly from unit.

8-18. Delay Set Switch Assembly (S1) Removal. Remove DELAY SET switch assembly as follows:

a. Remove front panel assembly per paragraph 8-17.

b. Remove nuts and washers holding switch assembly to rear of front panel assembly and remove switch assembly. (Delay Set switch retaining screws are permanently mounted.)

8-19. Rear Panel/Power Supply Assembly Removal. Remove rear panel/power supply assembly as follows:

a. Remove two screws holding bottom support (MP 18) to center of rear panel.

b. Remove two screws holding corner supports (MP 4) to rear panel.

c. Remove three screws holding top cover (MP 3) to top of rear panel.

d. Carefully pull rear panel/power supply assembly to the rear. Exercise care to prevent damage to 15 pin connector (A1P2/A2J2) between power supply board (A1) and processor board (A2).

8-20. Processor Board (A2) Removal. Remove processor board as follows:

a. Disconnect two ribbon connectors from delay generator (A2A1) and remove delay generator from processor board.

b. Disconnect all ribbon connectors and square pin connections from processor board. Make note of connection locations for later reassembly.

c. Remove rear panel/power supply assembly per paragraph 8-19.

d. Remove four screws holding processor board to top cover and carefully remove processor board from unit.

8-21. SERVICING CIRCUIT BOARDS.

8-22. This instrument uses circuit boards with plated-through component holes. This allows components to be removed or replaced by unsoldering or soldering from either side of the board. When removing large components, such as potentiometers, rotate the soldering iron tip from lead to lead while applying pressure to the part to lift it from the board. HP Service Note M-20E contains additional information on the repair of circuit boards.

8-23. SEMICONDUCTOR REPLACEMENT.

8-24. Figure 8-1 is included to help identify the leads in the common shapes and sizes of semiconductor devices. When removing a semiconductor, use long-nosed pliers as a heat sink between the device and the soldering iron. When replacing a semiconductor, ensure sufficient lead length to dissipate the soldering heat by using the same length of exposed lead as was used for the original part.

8-25. INTEGRATED CIRCUIT REPLACEMENT.

8-26. Soldered IC units may be removed with soldering irons which simultaneously heat all connections (available from various manufacturers). Soldering irons with built-in desoldering tools facilitate quick removal.

CAUTION

Unless an IC has definitely failed, exercise care to prevent damage when removing or replacing it.

8-27. Use the following procedure for removing an IC with a standard soldering iron.

a. Heat IC lead solder joint. Use soldering iron with small pencil tip (e.g. Weller No. PT-H7).

b. When solder is fluid, remove it with desoldering tool (such as deluxe Model Soldapullt manufactured by Edsyn Company of California).

c. Repeat steps a and b for each IC lead until all leads are free.

d. Grasp each lead with long-nosed pliers and check that it is mechanically free from circuit board.

e. When all leads are free, carefully remove IC. Dual in-line type may be removed by gently gripping top and bottom with long-nosed pliers and rolling IC out.

f. Use desoldering tool or toothpick to remove all remaining solder from circuit board holes.

CAUTION

Exercise care to prevent IC damage with heat from the soldering iron. Work quickly.

g. Insert replacement IC into circuit board and solder it in place.

8-28. When replacing an IC, note the mark or notch used for orientation. The component identification illustrations and the IC pin-location diagrams in figure 8-1 show IC orientation.

8-29. TROUBLESHOOTING.

8-30. The most important prerequisites for successful troubleshooting are an understanding of the instrument functional operation and the correct use of front panel controls. Suspected malfunctions may be caused by improper control settings. Before performing the test and/or troubleshooting procedures, refer to Section III (Operation) for an explanation of controls, connectors, and general operating considerations, and to Section IV (Principles of Operation) for an explanation of circuit functional operation.

8-31. If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble. Check to see that all circuit board connections are making good contact and are not shorting to an adjacent circuit. If no obvious trouble is found, check the instrument supply voltages, and the external power sources.

8-32. DC VOLTAGES.

8-33. On some schematics, dc voltages are indicated at certain points in the circuit. Test equipment and control setups for making the voltage measurements are listed in paragraph 5-9. Check these setup conditions before making any measurements.

8-34. WAVEFORMS.

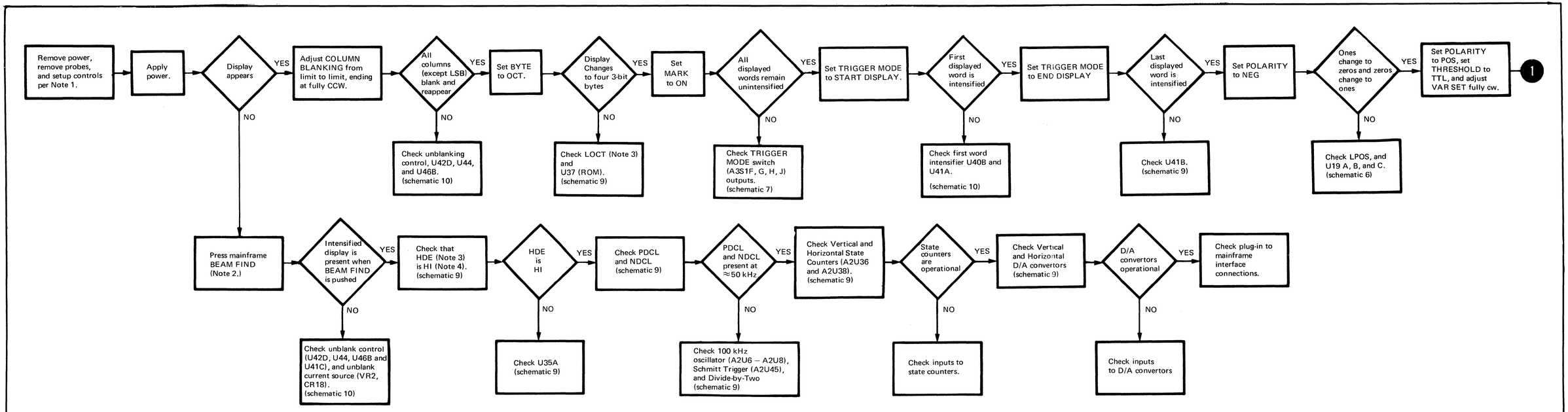
8-35. Waveforms are placed on the schematics along main signal paths. Test equipment and control setups for making these measurements are listed in paragraph 5-9. Check these setup conditions before making any measurements.

8-36. TEST POINTS.

8-37. Test points are shown on the schematics with this symbol (◉). Test points correspond to pins protruding from circuit boards and do not necessarily correspond to waveform measurement points.

8-38. FAULT ISOLATION.

8-39. Figure 8-2 provides a fault isolation procedure in flow chart form. Malfunctions can be isolated to a specific circuit or component by following the indicated step-by-step instructions. Refer to table 4-1 for a list of logic term definitions and origins.



NOTES:

1. Troubleshooting front panel setup:

CLOCK	(out)
THRESHOLD	TTL
DISPLAY RATE	fully ccw
COLUMN BLANKING	fully ccw
SAMPLE MODE	SINGLE
TRIGGER MODE	FREE RUN
TRIGGER WORD	bits 0 through 11 to OFF
LOGIC	POS
MARK	OFF
BYTE	BCD

2. Model 1601A is installed in non-storage mainframe for troubleshooting.

3. Refer to Table 4-1 for logic term definitions and origins.

4. Logic levels
   IC Logic
   HI = ⩾+2.5V
   LO = ⩽+0.4V

   Switch Logic
   HI = ≈+5V
   LO = ⩽0.4V

1-L-041

Figure 8-2.
Troubleshooting Chart (Sheet 1)

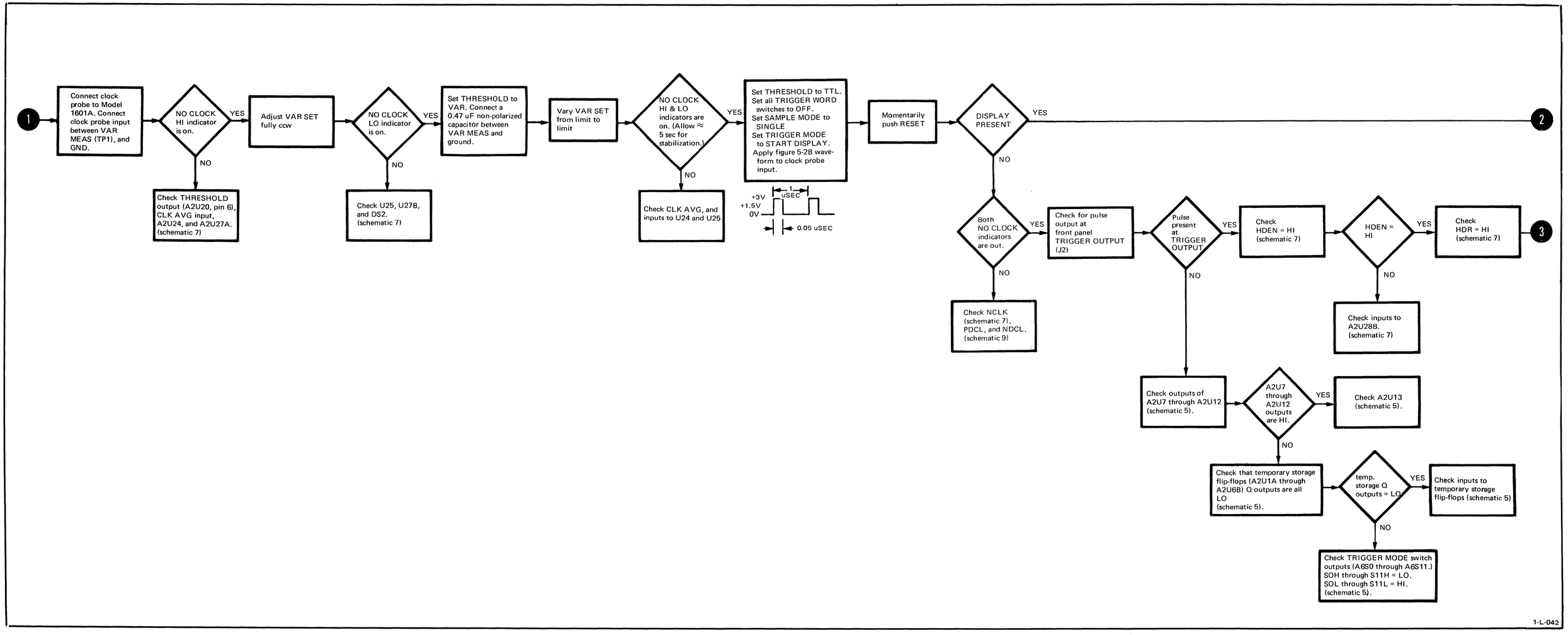


Figure 8-2. Troubleshooting Chart (Sheet 2)

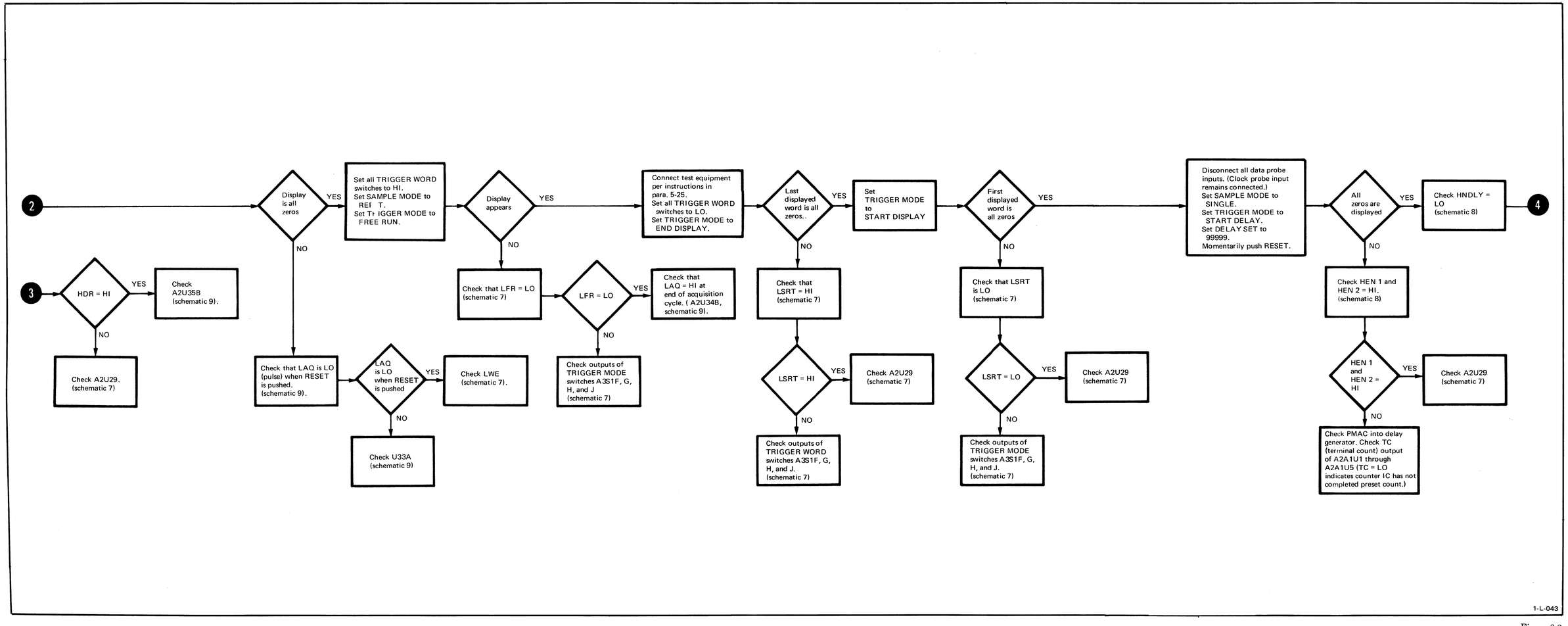


Figure 8-2.
Troubleshooting Chart (Sheet 3)

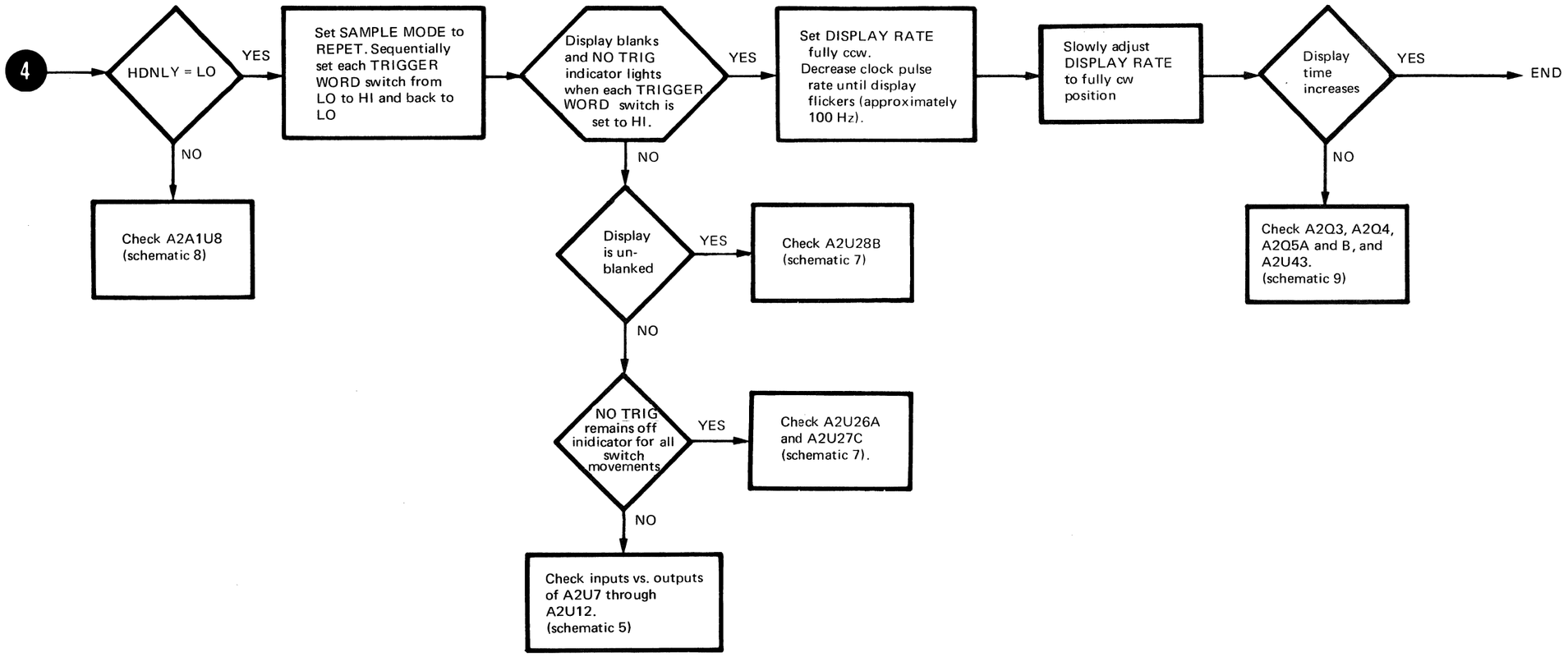


Figure 8-2. Troubleshooting Chart (Sheet 4)

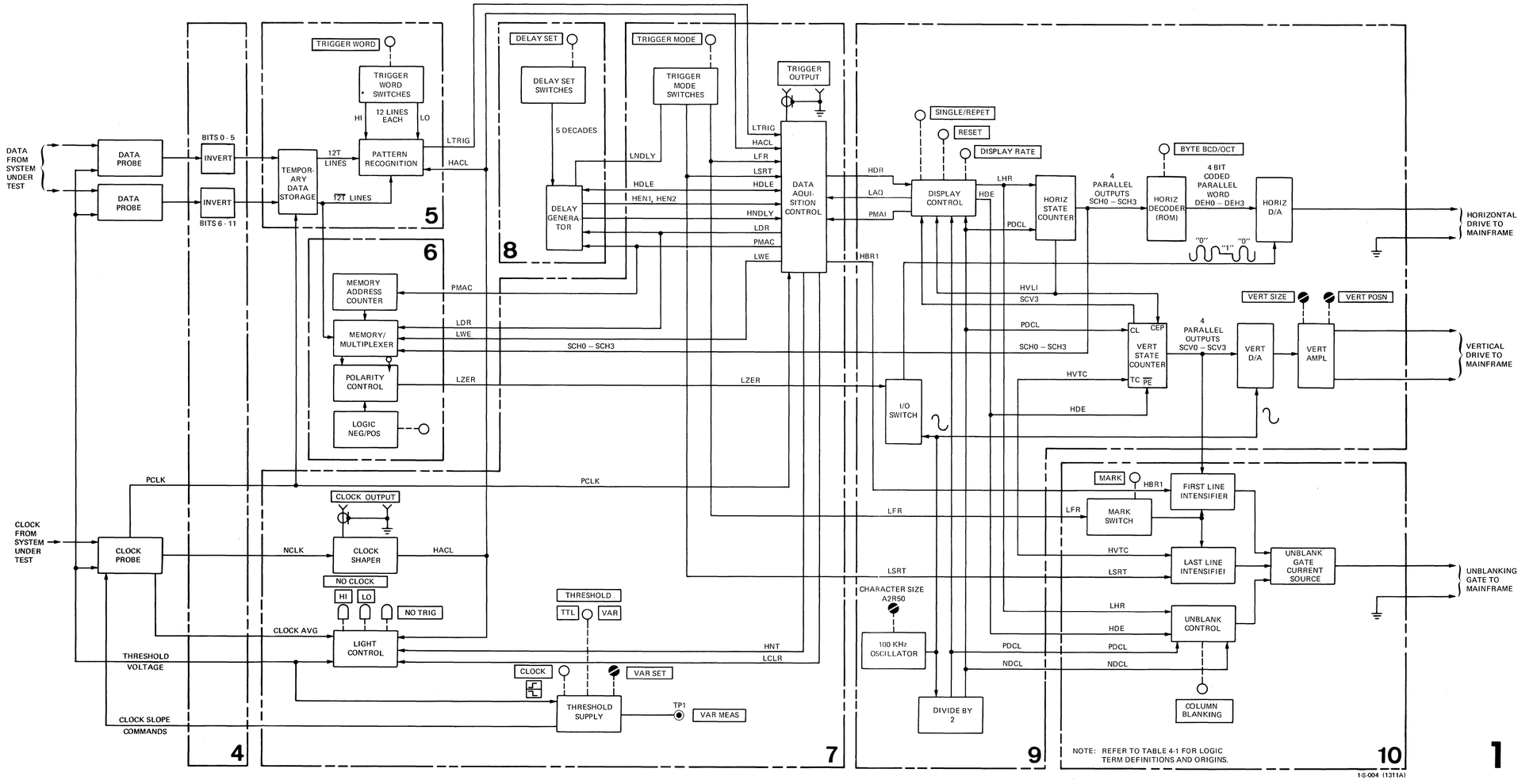
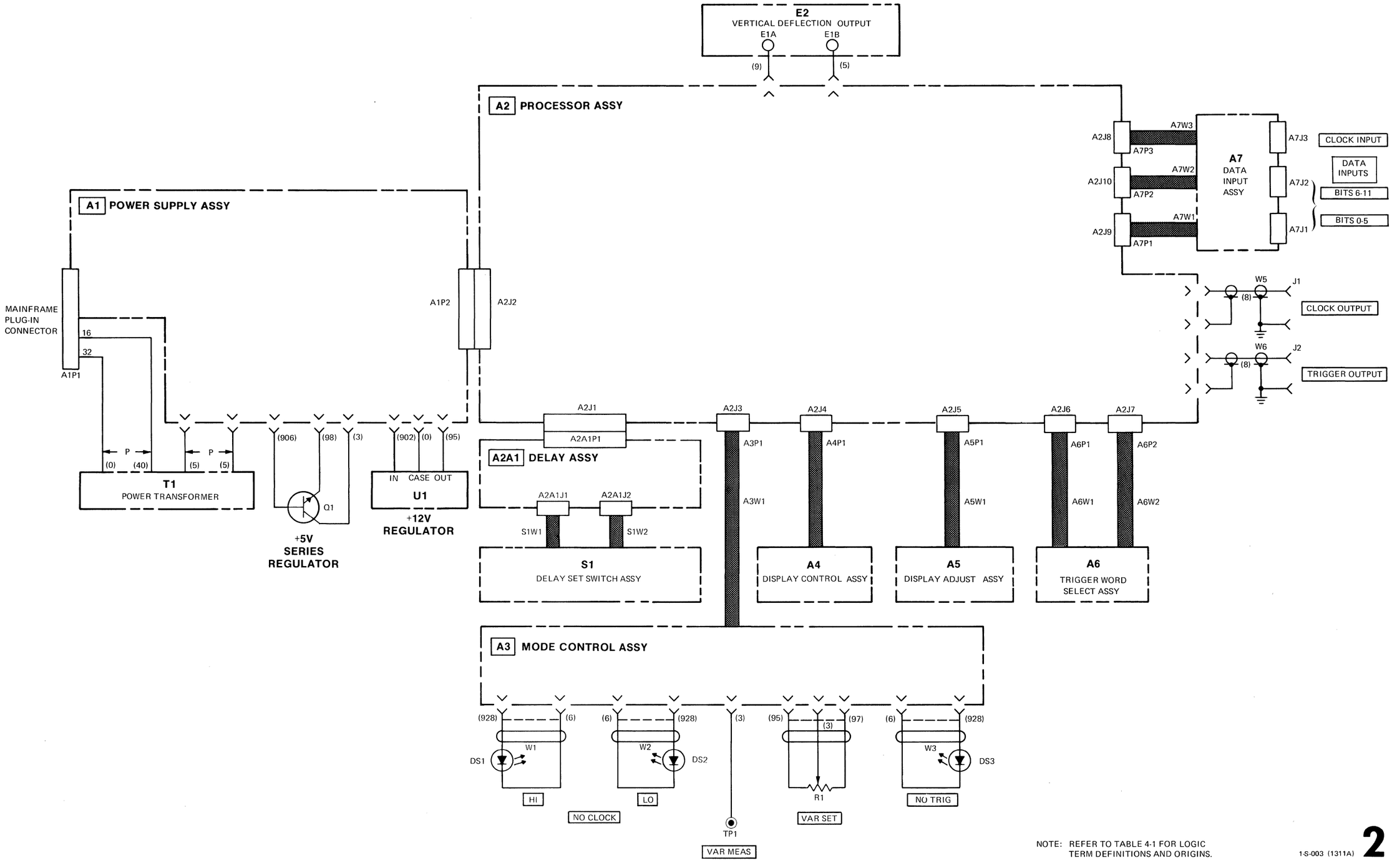


Figure 8-3.
Block Diagram
8-11/8-12

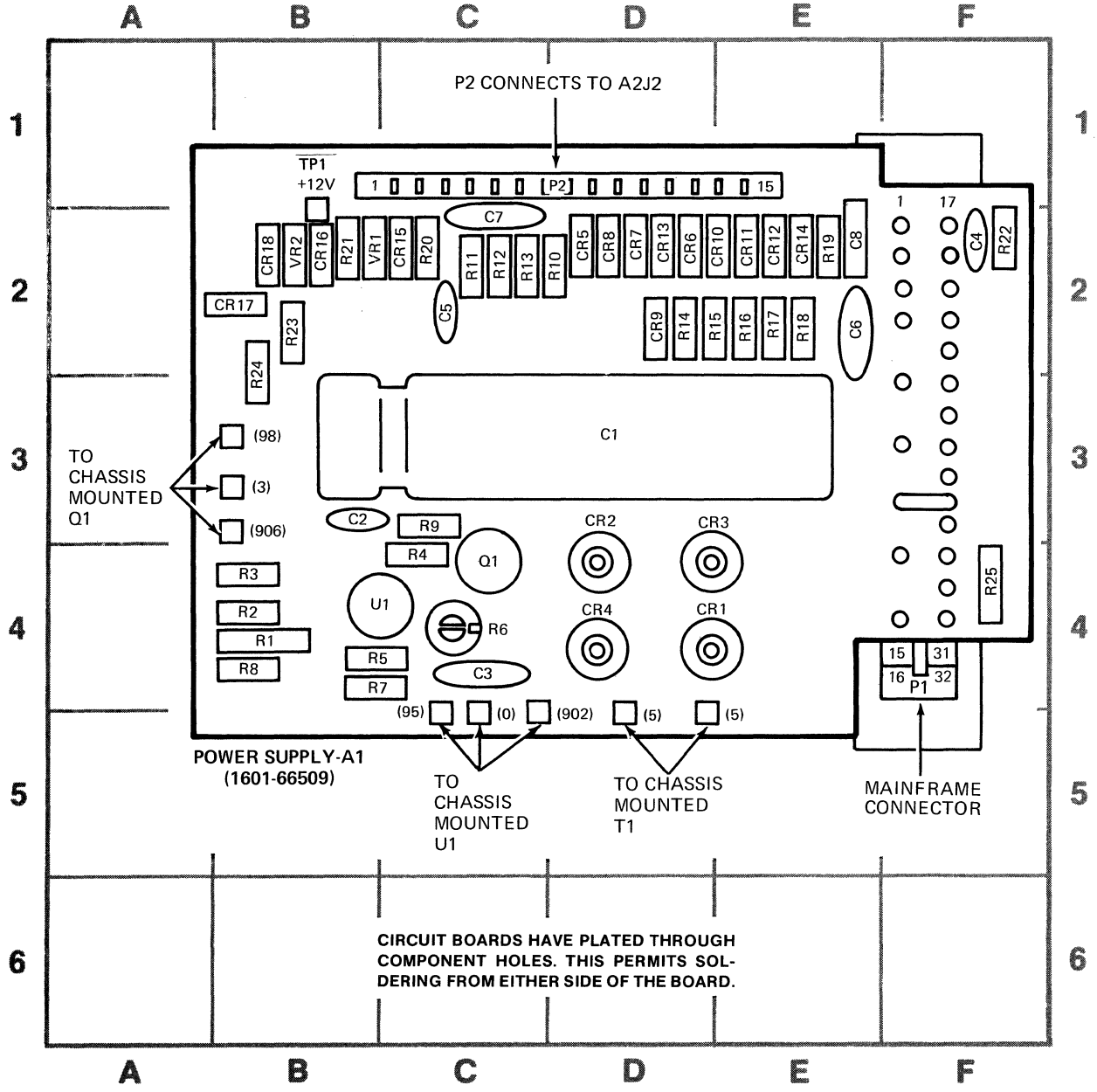


NOTE: REFER TO TABLE 4-1 FOR LOGIC TERM DEFINITIONS AND ORIGINS.

1-S-003 (1311A)

2

Figure 8-4.
Interconnection Diagram



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-3	CR2	D-3	CR11	E-2	P1	F-4	R6	C-4	R14	D-2	R22	F-2
C2	B-3	CR3	E-3	CR12	E-2	P2	D-1	R7	B-4	R15	D-2	R23	B-2
C3	C-4	CR4	D-4	CR13	D-2	Q1	C-4	R8	B-4	R16	E-2	R24	B-3
C4	F-2	CR5	D-2	CR14	E-2	R1	B-4	R9	C-3	R17	E-2	R25	F-4
C5	C-2	CR6	D-2	CR15	C-2	R2	B-4	R10	C-2	R18	E-2	T1	B-1
C6	E-2	CR7	D-2	CR16	B-2	R3	B-4	R11	C-2	R19	E-2	U1	B-4
C7	C-2	CR8	D-2	CR17	B-2	R4	C-4	R12	C-2	R20	C-2	VR1	B-2
C8	E-2	CR9	D-2	CR18	B-2	R5	B-4	R13	C-2	R21	B-2	VR2	B-2
CR1	E-4	CR10	D-2										

1601A-L-015A

Figure 8-5. Power Supply Board A1 Component Identification

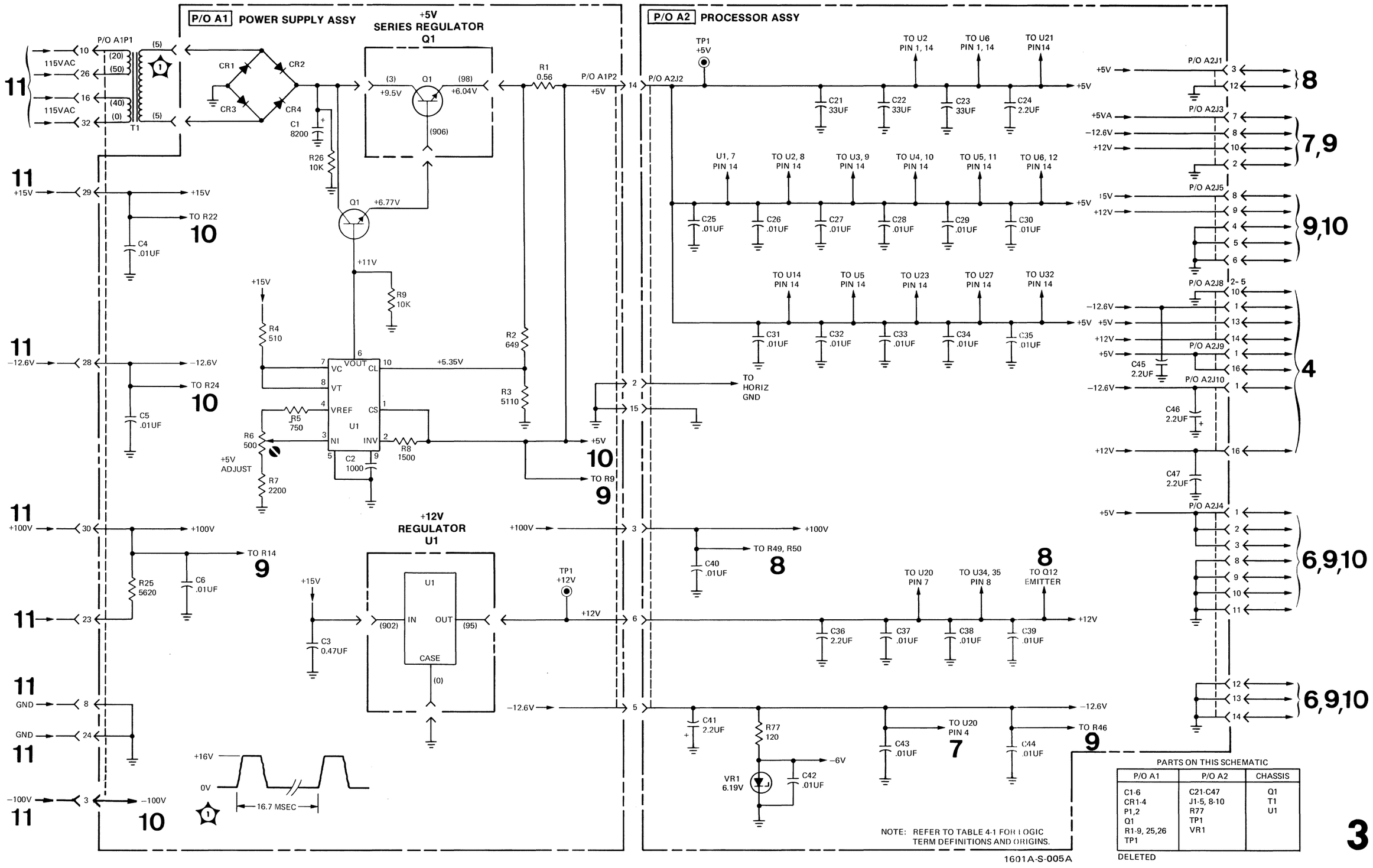
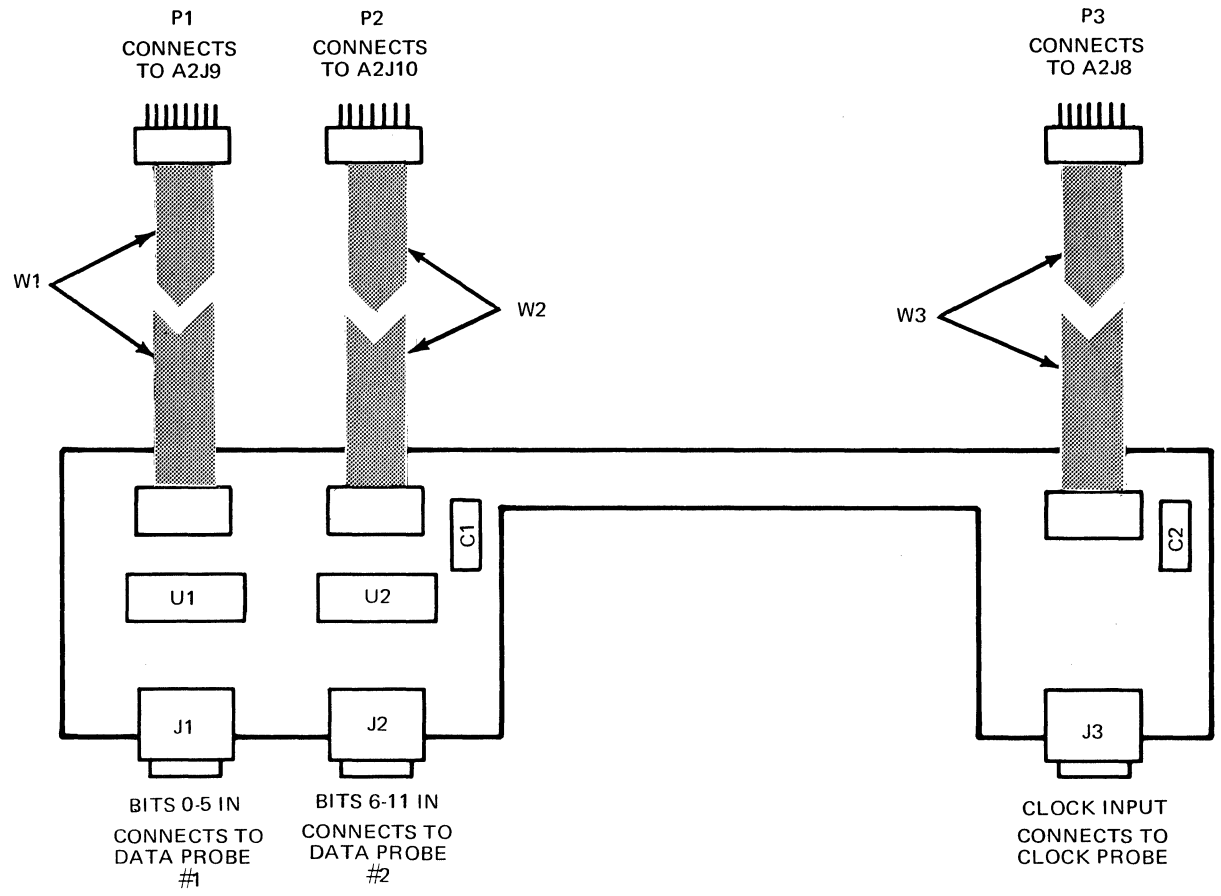


Figure 8-6.
Power Distribution Schematic 3



DATA INPUT ASSEMBLY - A7
(01601-66503)

CIRCUIT BOARDS HAVE PLATED THROUGH COMPONENT HOLES. THIS PERMITS SOLDERING FROM EITHER SIDE OF THE BOARD.

1-L-024

Figure 8-7. Data Input Assembly A7 Component Identification

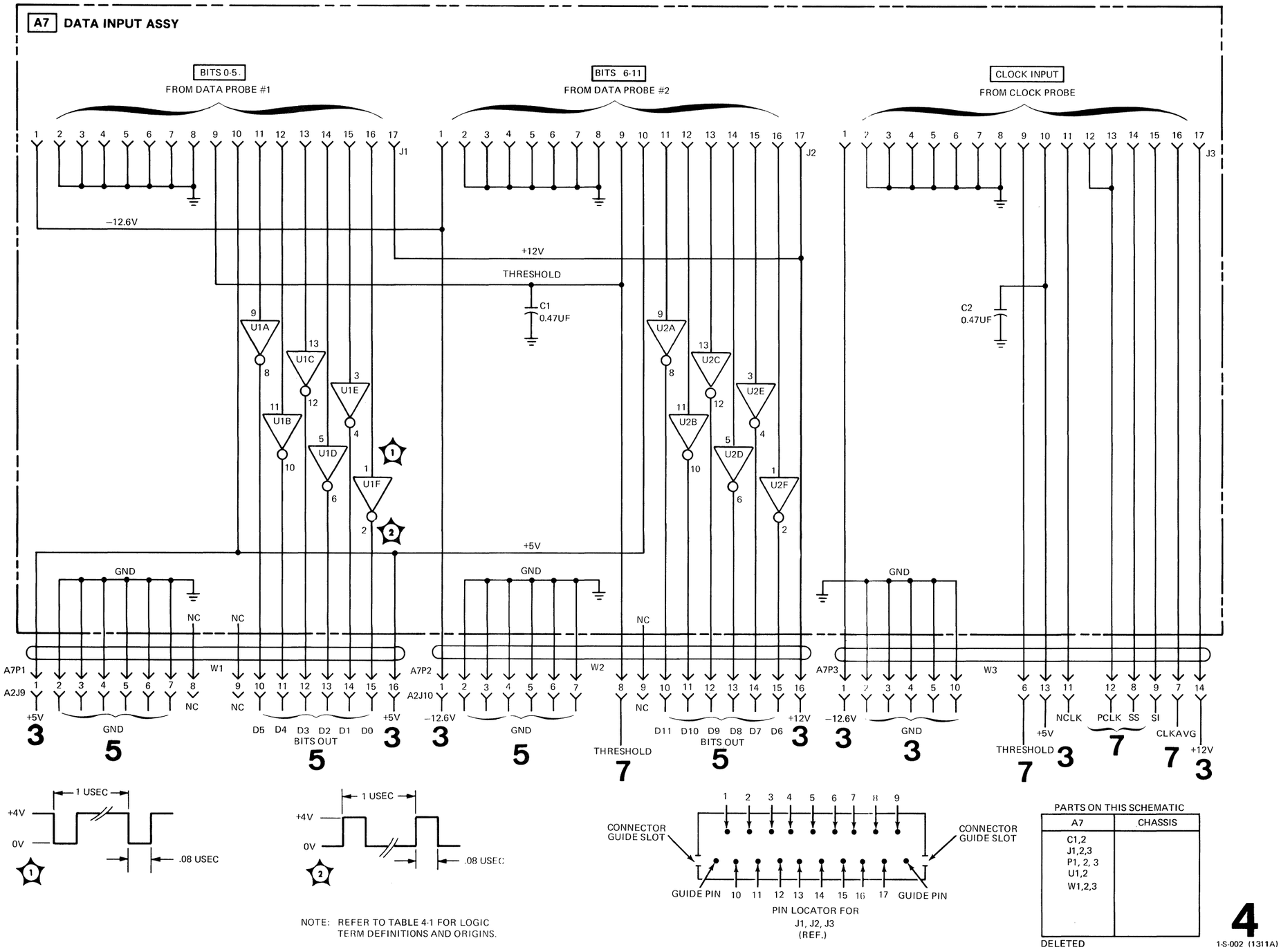
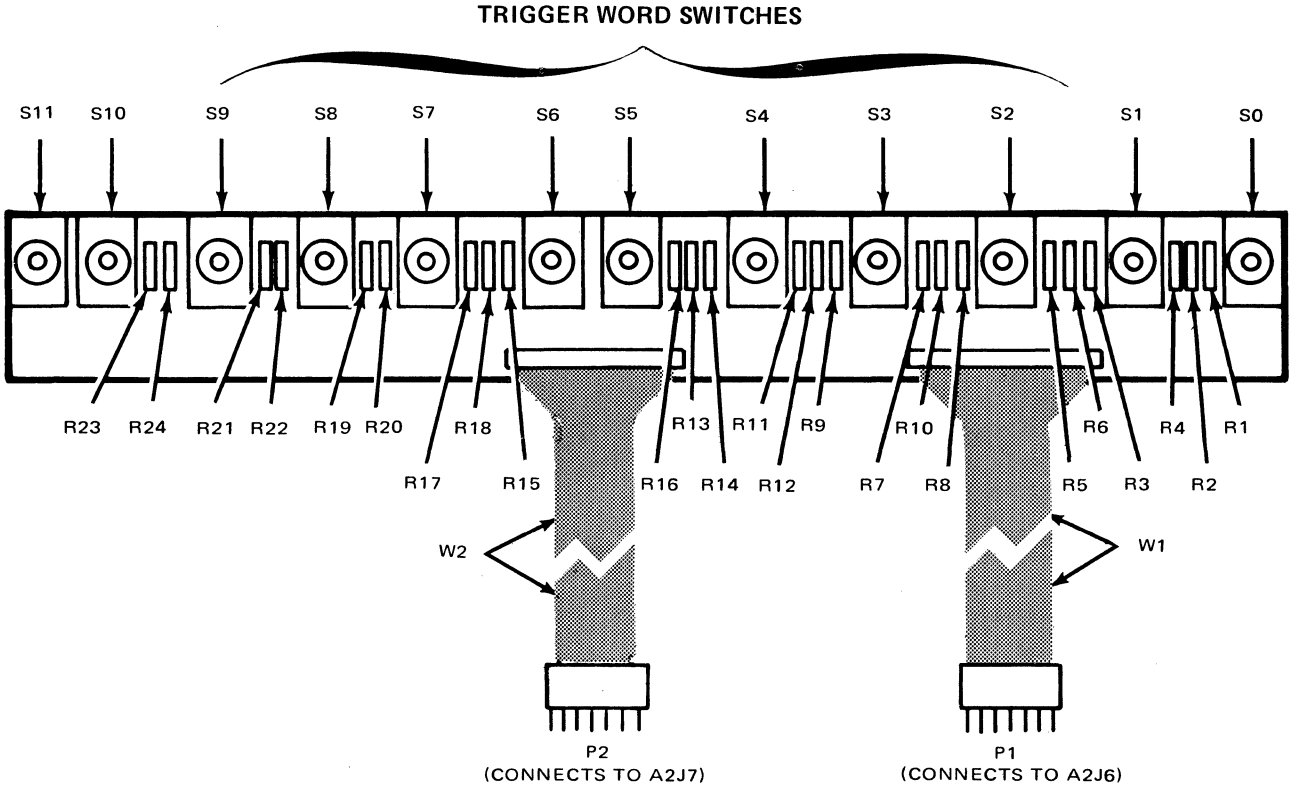


Figure 8-8.
Data Input Assembly Schematic 4



TRIGGER WORD SELECT ASSEMBLY - A6
(01601-66504)

CIRCUIT BOARDS HAVE PLATED THROUGH COMPONENT HOLES. THIS PERMITS SOLDERING FROM EITHER SIDE OF THE BOARD.

1-L-022

Figure 8-9. Trigger Word Assembly A6 Component Identification

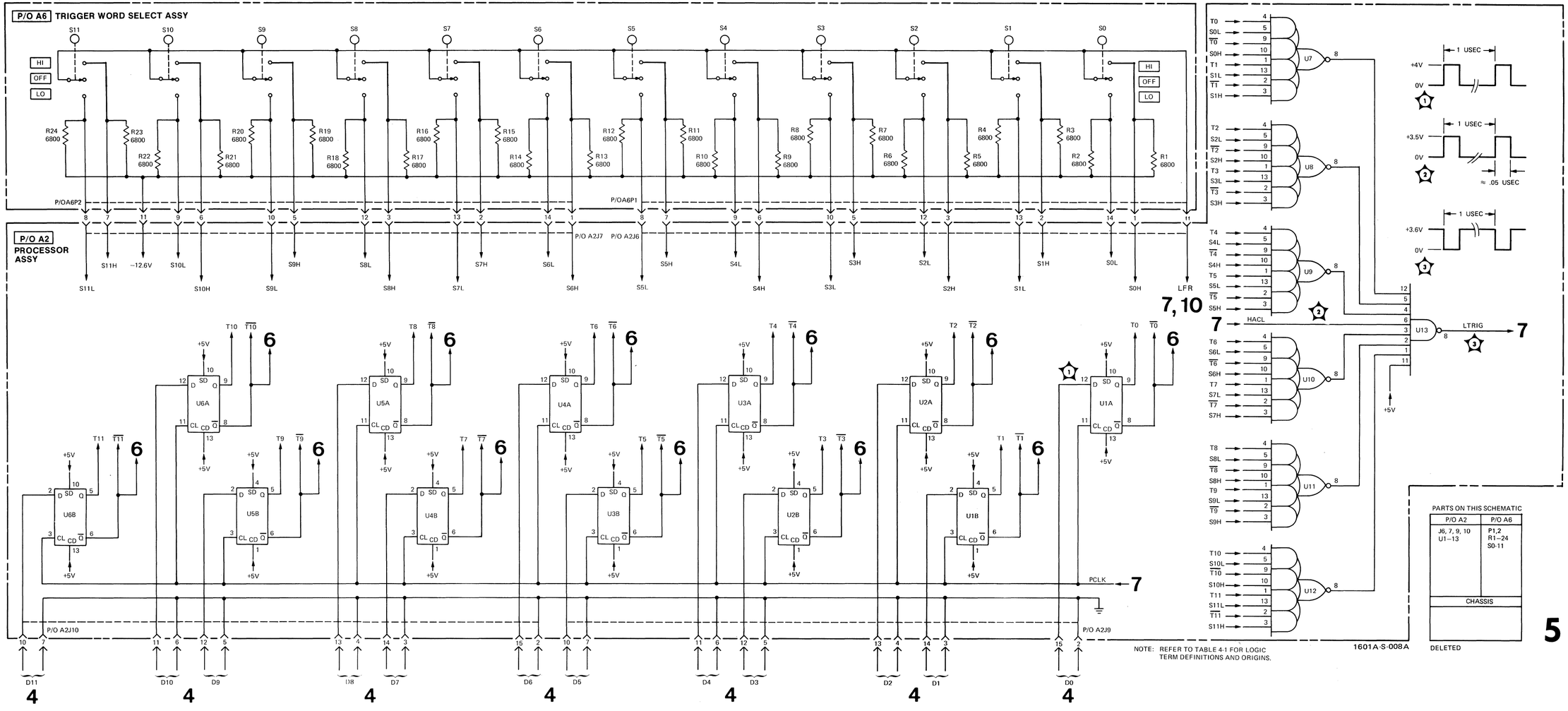


Figure 8-10.
Pattern Recognition Schematic 5

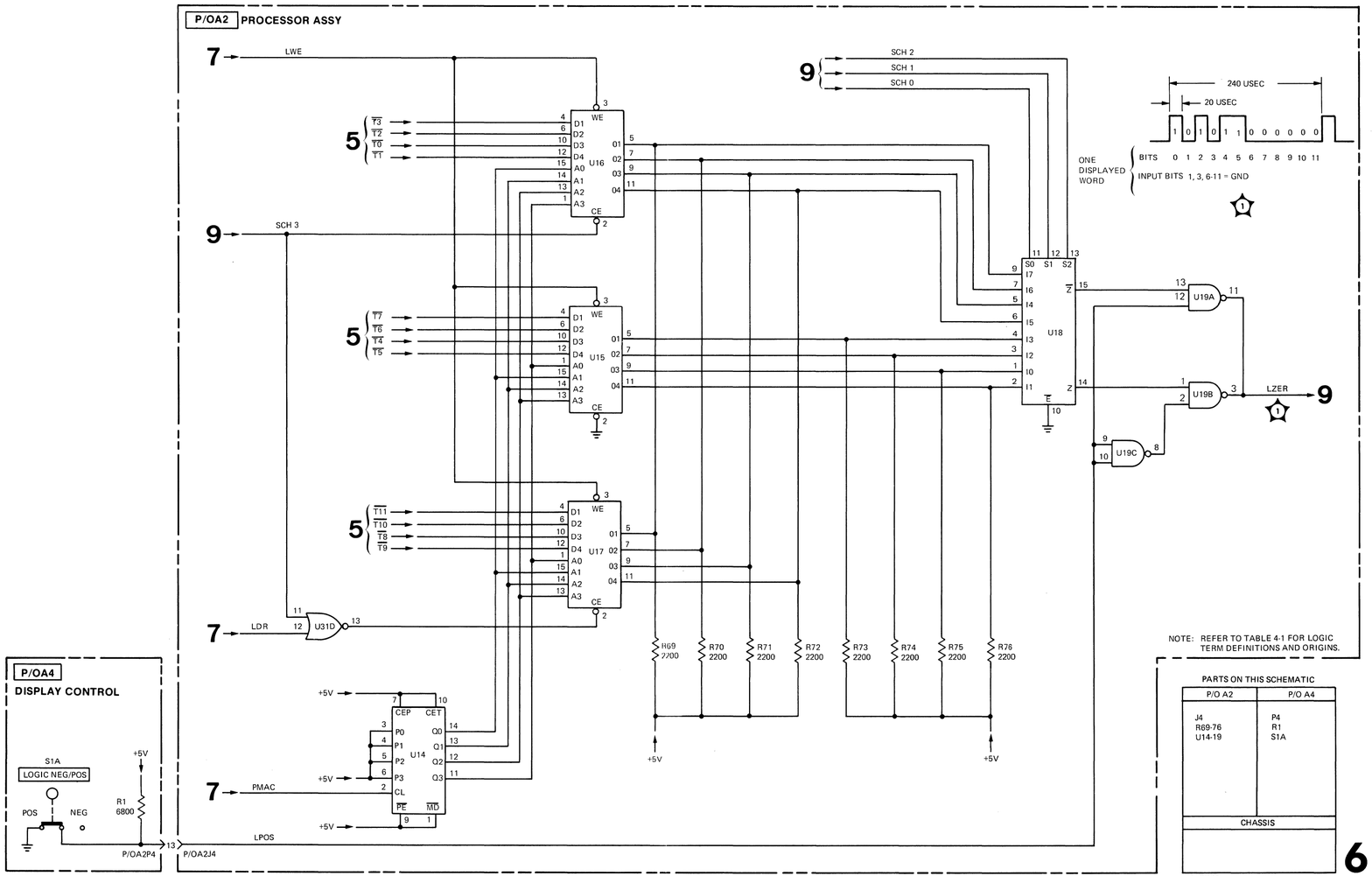


Figure 8-11.
Memory/Multiplexer Schematic 6

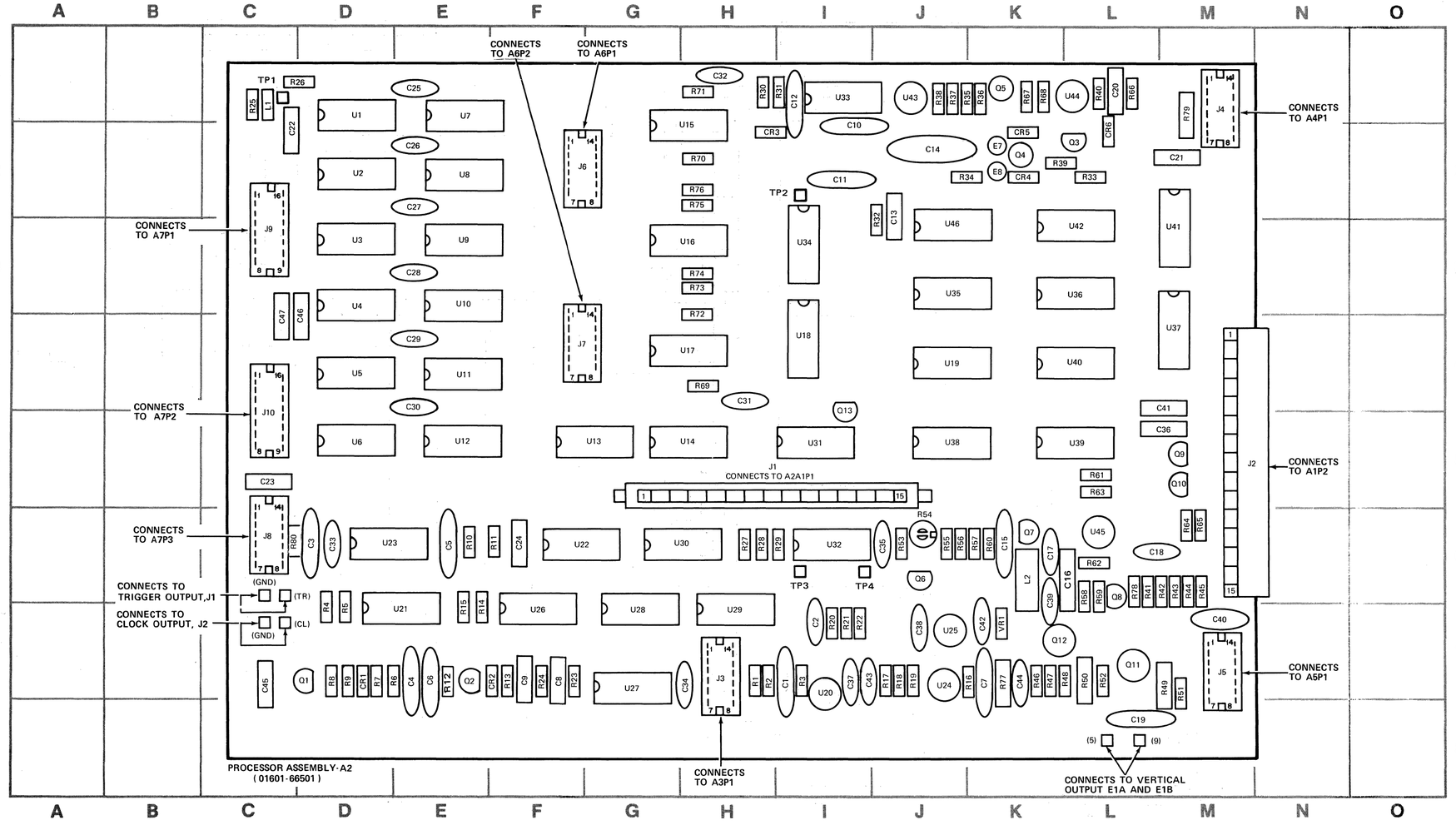
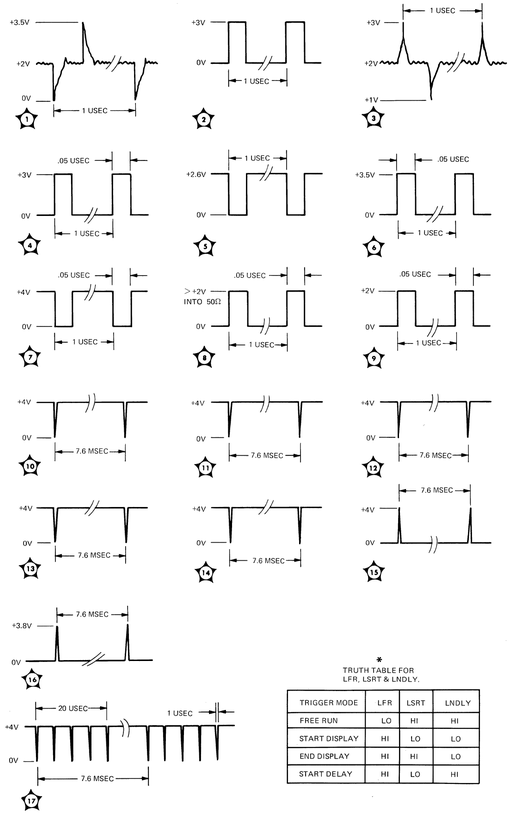


Figure 8-12. Processor Assembly A2 Component Identification

REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	I-7	C43	I-7	R5	D-7	R47	K-7	U5	D-5
C2	I-7	C44	K-7	R6	D-7	R48	L-7	U6	D-6
C3	D-6	C45	C-7	R7	D-7	R49	M-7	U7	E-1
C4	E-7	C46	C-4	R8	D-7	R50	L-7	U8	E-2
C5	E-6	C47	C-4	R9	D-7	R51	M-7	U9	E-3
C6	E-7	CR1	D-7	R10	E-6	R52	L-7	U10	E-3
C7	K-7	CR2	E-7	R11	F-6	R53	J-6	U11	E-4
C8	F-7	CR3	H-2	R12	E-7	R54	J-6	U12	E-5
C9	F-7	CR4	K-2	R13	F-7	R55	J-6	U13	G-5
C10	I-2	CR5	K-2	R14	E-7	R56	J-6	U14	H-5
C11	I-2	CR6	L-2	R15	E-7	R57	K-6	U15	H-2
C12	I-1	E7	K-2	R16	K-7	R58	L-6	U16	H-3
C13	J-2	E8	K-2	R17	J-7	R59	L-6	U17	H-4
C14	J-2	J1	H-5	R18	J-7	R60	K-6	U18	I-4
C15	K-6	J2	M-5	R19	J-7	R61	L-5	U19	J-4
C16	L-6	J3	H-7	R20	I-7	R62	L-6	U20	I-7
C17	K-6	J4	M-1	R21	I-7	R63	L-5	U21	F-7
C18	L-6	J5	M-7	R22	I-7	R64	M-6	U22	G-6
C19	L-8	J6	G-2	R23	F-7	R65	M-6	U23	E-6
C20	L-2	J7	G-4	R24	F-7	R66	L-1	U24	J-7
C21	M-2	J8	C-6	R25	C-1	R67	K-1	U25	J-7
C22	C-2	J9	C-3	R26	C-1	R68	K-1	U26	F-7
C23	C-5	J10	C-5	R27	H-6	R69	H-4	U27	G-7
C24	F-6	L1	C-1	R28	H-6	R70	H-2	U28	G-7
C25	E-1	L2	K-6	R29	I-6	R71	H-1	U29	H-7
C26	E-2	Q1	D-7	R30	H-1	R72	H-4	U30	H-6
C27	E-2	Q2	E-7	R31	I-1	R73	H-3	U31	I-5
C28	E-3	Q3	L-2	R32	J-3	R74	H-3	U32	I-6
C29	E-4	Q4	K-2	R33	L-2	R75	H-2	U33	I-1
C30	E-4	Q5	K-1	R34	K-2	R76	H-2	U34	I-3
C31	H-4	Q6	J-6	R35	K-2	R77	K-7	U35	J-3
C32	H-1	Q7	K-6	R36	K-2	R78	L-6	U36	L-3
C33	D-6	Q8	L-6	R37	J-2	R79	M-1	U37	M-4
C34	H-7	Q9	M-5	R38	J-2	R80	C-6	U38	J-5
C35	J-6	Q10	M-5	R39	L-2	TP1	C-1	U39	L-5
C36	M-5	Q11	L-7	R40	L-1	TP2	J-2	U40	L-4
C37	I-7	Q12	K-7	R41	L-6	TP3	I-6	U41	M-3
C38	J-7	Q13	I-5	R42	M-6	TP4	I-6	U42	L-3
C39	K-6	R1	H-7	R43	M-6	U1	D-1	U43	J-1
C40	M-7	R2	A-7	R44	M-6	U2	D-2	U44	L-1
C41	M-4	R3	I-7	R45	M-6	U3	D-3	U45	L-6
C42	K-7	R4	D-7	R46	K-7	U4	D-4	U46	J-3
								VR1	K-7

CIRCUIT BOARDS HAVE PLATED THROUGH COMPONENT HOLES. THIS PERMITS SOLDERING FROM EITHER SIDE OF THE BOARD.

1601A-L-023A



*
TRUTH TABLE FOR
LFR, LSRT & LNDLY.

TRIGGER MODE	LFR	LSRT	LNDLY
FREE RUN	LO	HI	HI
START DISPLAY	HI	LO	LO
END DISPLAY	HI	HI	LO
START DELAY	HI	LO	HI

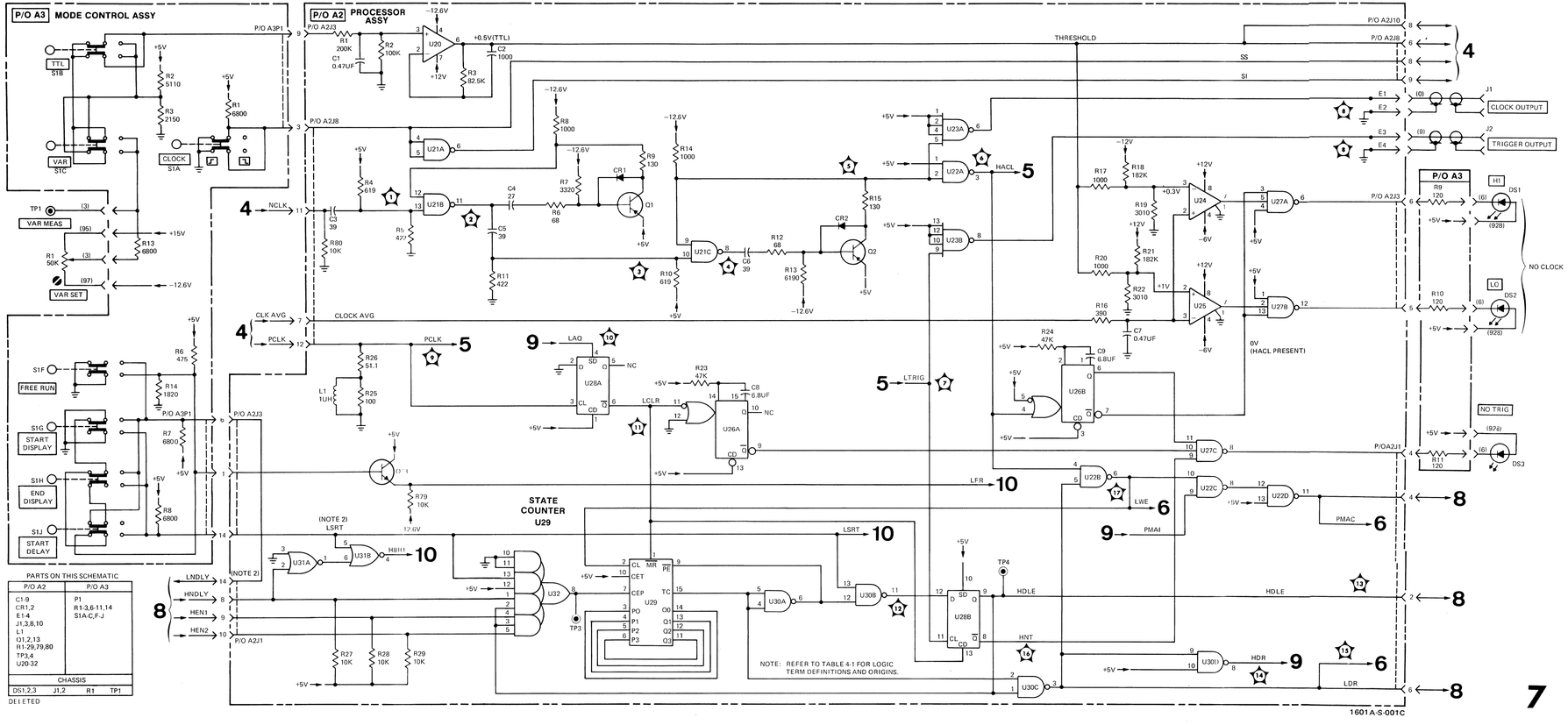
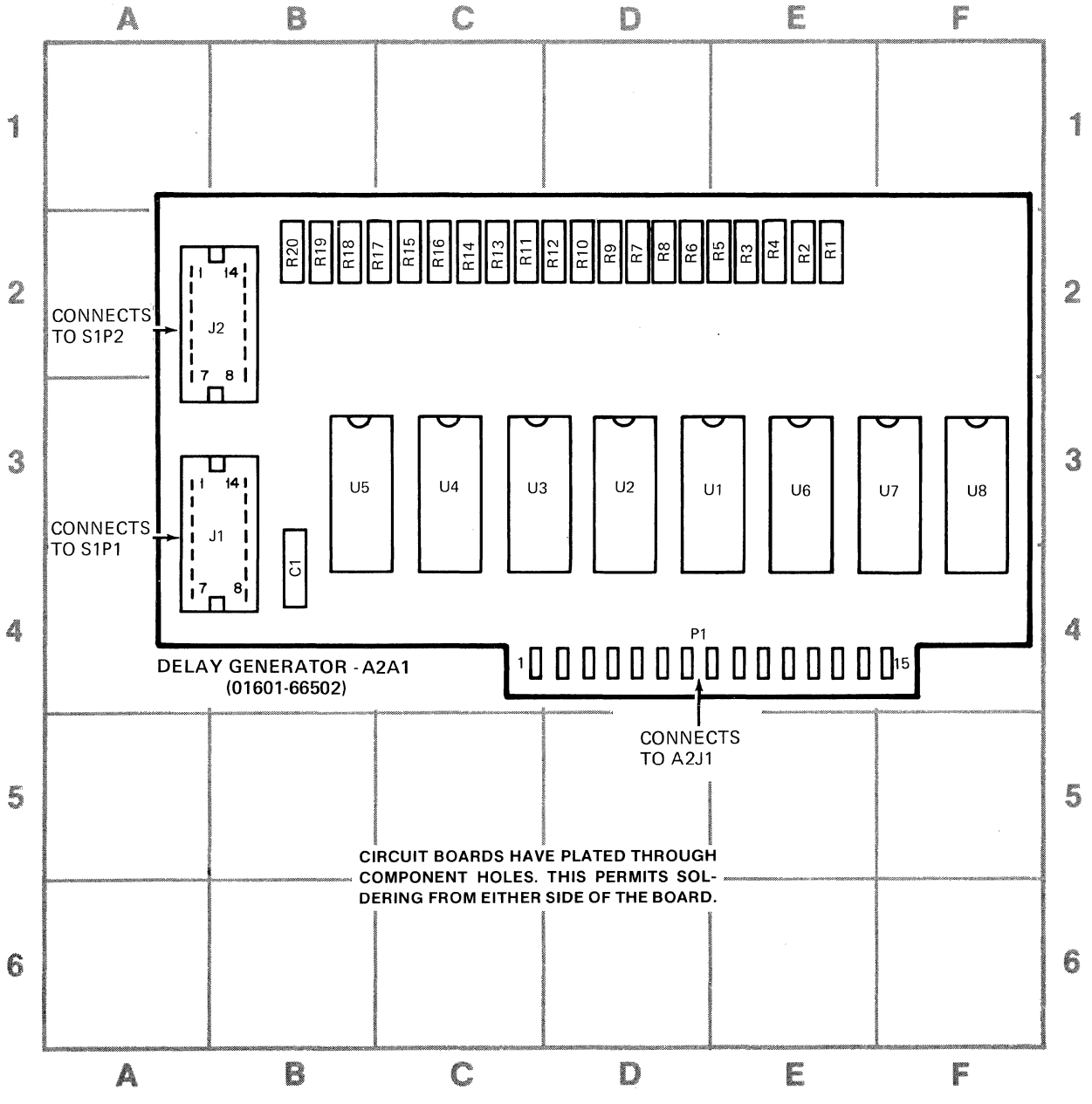


Figure 8-13.
Data Acquisition Control Schematic 7
8-23



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	B-4	R5	E-2	R13	C-2	U1	E-3
J1	B-4	R6	D-2	R14	C-2	U2	D-3
J2	B-2	R7	D-2	R15	C-2	U3	D-3
P1	D-4	R8	D-2	R16	C-2	U4	C-3
R1	E-2	R9	D-2	R17	C-2	U5	B-3
R2	E-2	R10	D-2	R18	B-2	U6	E-3
R3	E-2	R11	C-2	R19	B-2	U7	F-3
R4	E-2	R12	D-2	R20	B-2	U8	F-3

1-L-019

Figure 8-14. Delay Generator A2A1 Component Identification

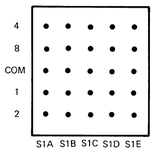
TRUTH TABLE FOR DELAY SET
(S1A THROUGH S1E)
OUTPUT TERMINALS

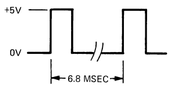
SWITCH POSITION	SWITCH OUTPUTS			
	8	4	2	1
0		•	•	
1		•	•	•
2	•			
3	•			•
4	•		•	
5	•		•	•
6	•	•		
7	•	•		•
8	•	•	•	
9	•	•	•	•

• = CONNECTED TO COMMON (GROUND)

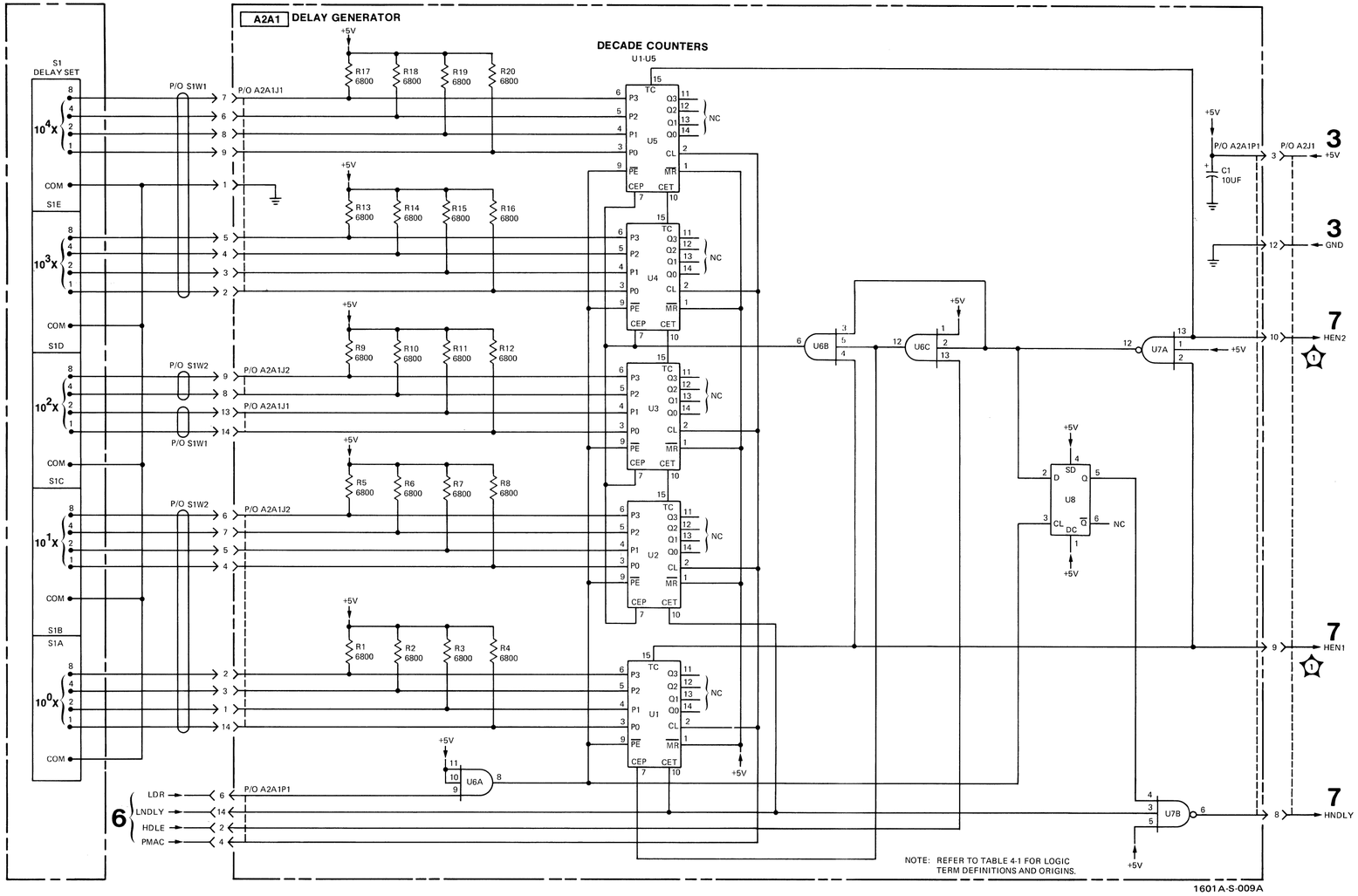
PIN LOCATOR FOR
S1A THROUGH S1E

(REAR VIEW)





(START DELAY OR FREE RUN
WITH DELAY SET OF 11000)



PARTS ON THIS SCHEMATIC

A2A1	CHASSIS
C1 J1, J2 P1 R1–R20 U1–U8	S1 P/O S1W1 P/O S1W2

DELETED

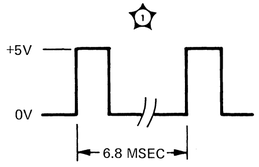
8

Figure 8-15.
Delay Generator Schematic 8
8-25

TRUTH TABLE FOR DELAY SET
(S1A THROUGH S1E)
OUTPUT TERMINALS

SWITCH POSITION	SWITCH OUTPUTS			
	8	4	2	1
0		●	●	
1		●	●	●
2	●			
3	●			●
4	●		●	
5	●		●	●
6	●	●		
7	●	●		●
8	●	●	●	
9	●	●	●	●

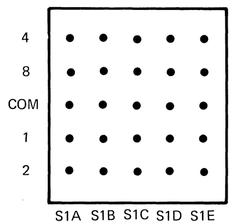
● = CONNECTED TO COMMON (GROUND)



(START DELAY OR FREE RUN
WITH DELAY SET OF 11000)

PIN LOCATOR FOR
S1A THROUGH S1E

(REAR VIEW)



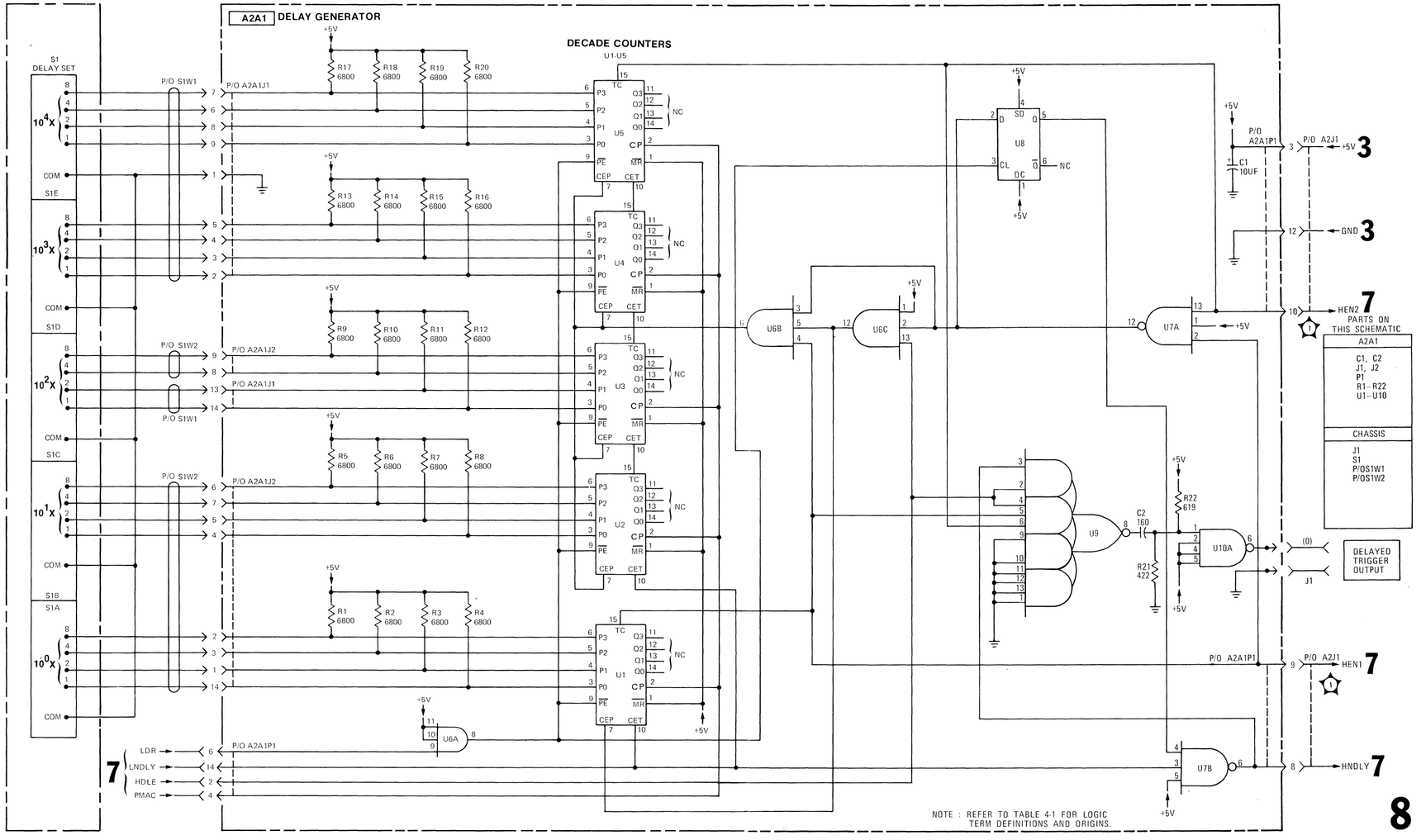
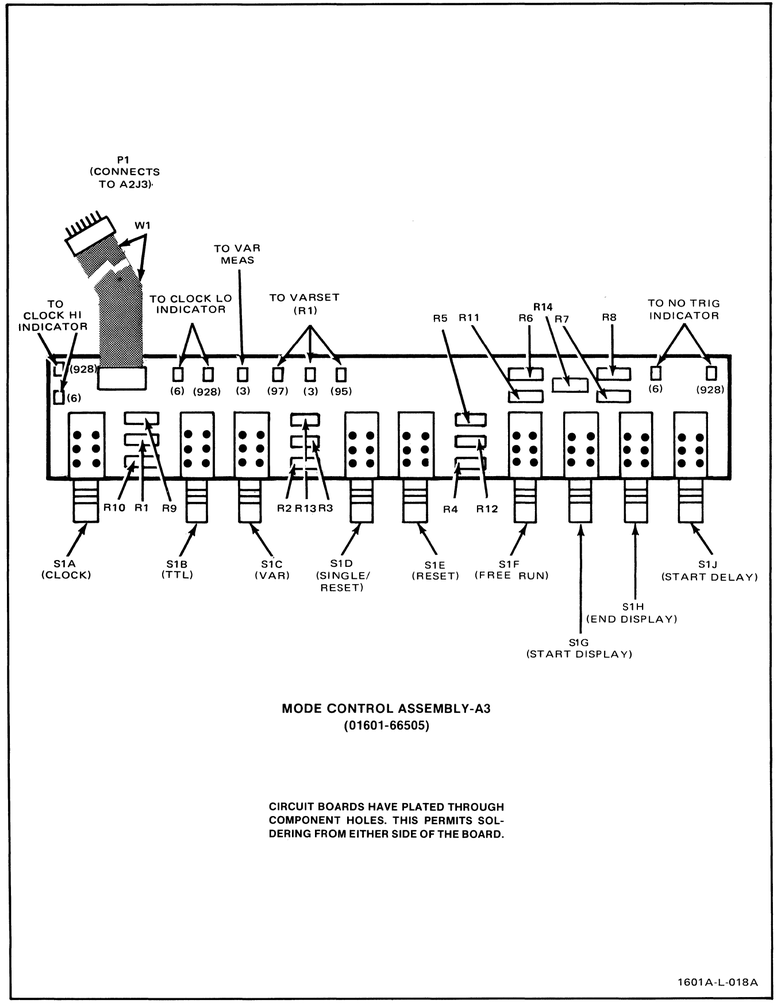


Figure 8-15.
Delay Generator Schematic 8



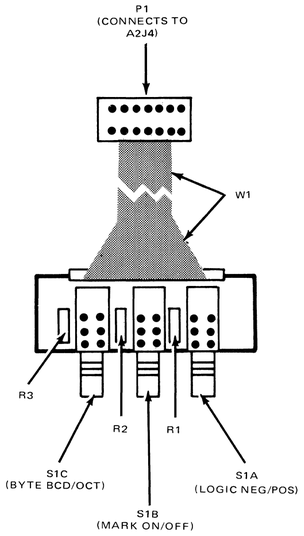
MODE CONTROL ASSEMBLY-A3
(01601-66505)

CIRCUIT BOARDS HAVE PLATED THROUGH COMPONENT HOLES. THIS PERMITS SOLDERING FROM EITHER SIDE OF THE BOARD.

1601A-L-018A

Figure 8-16. Mode Control Assembly A3 Component Identification

CIRCUIT BOARDS HAVE PLATED THROUGH COMPONENT HOLES. THIS PERMITS SOLDERING FROM EITHER SIDE OF THE BOARD.

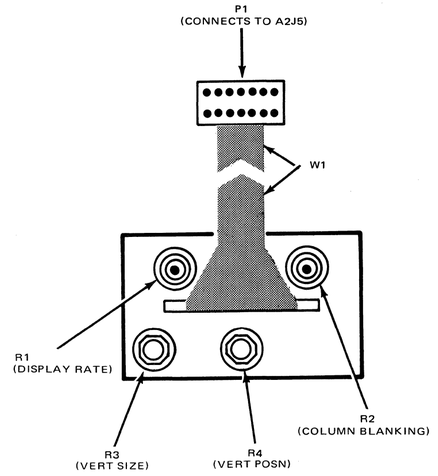


DISPLAY CONTROL ASSEMBLY - A4
(01601-66507)

1601A-L-017A

Figure 8-17. Display Control Assembly A4 Component Identification

CIRCUIT BOARDS HAVE PLATED THROUGH COMPONENT HOLES. THIS PERMITS SOLDERING FROM EITHER SIDE OF THE BOARD.



DISPLAY ADJUST ASSEMBLY - A5
(01601-66508)

1601A-L-016A

Figure 8-18. Display Adjust Assembly A5 Component Identification

Table 8-2. Horizontal/Vertical Waveform Timing

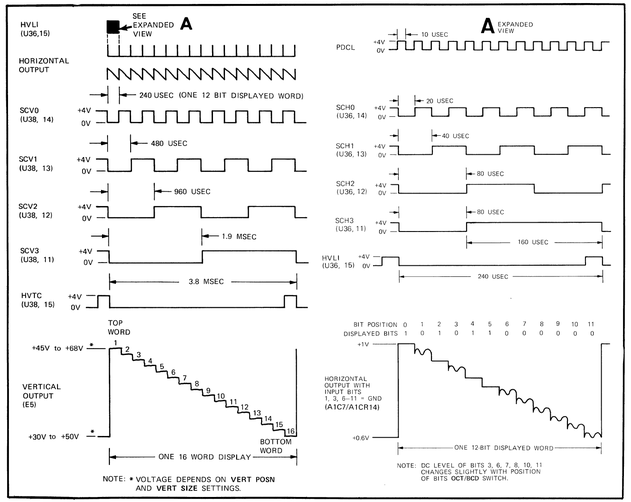
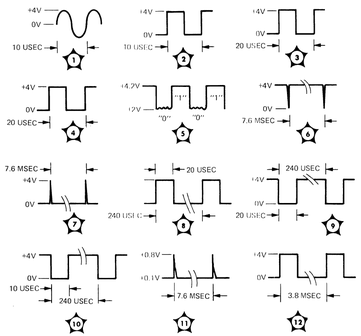


Table 8-3. A2U37 (ROM) Truth Table

DISPLAY FORMAT	BYTE OUTPUT	HORIZONTAL STATE COUNTER OUTPUTS				ROM OUTPUTS			
	LOCT	SCV3	SCV2	SCV1	SCV0	DEH3	DEH2	DEH1	DEH0
OCT	L	L	H	L	L	H	H	H	L
	L	L	H	L	H	H	H	L	H
	L	L	H	H	L	H	H	L	L
	L	L	H	H	H	H	L	H	H
	L	H	L	L	L	H	L	H	L
	L	H	L	L	H	H	L	L	H
	L	H	L	H	L	L	H	H	L
	L	H	L	H	H	L	H	L	H
	L	H	H	L	L	L	L	H	L
	L	H	H	L	H	L	L	L	H
	L	H	H	H	L	L	L	L	L
	L	H	H	H	H	L	L	L	L
BCD	H	L	H	L	L	H	H	H	L
	H	L	H	L	H	H	H	L	H
	H	L	H	H	L	H	H	L	L
	H	L	H	H	H	H	L	H	H
	H	H	L	L	L	H	L	H	L
	H	H	L	L	H	H	L	L	H
	H	H	L	H	L	L	H	H	L
	H	H	L	H	H	L	H	L	H
	H	H	H	L	L	L	L	H	L
	H	H	H	L	H	L	L	L	H
	H	H	H	H	L	L	L	L	L
	H	H	H	H	H	L	L	L	L



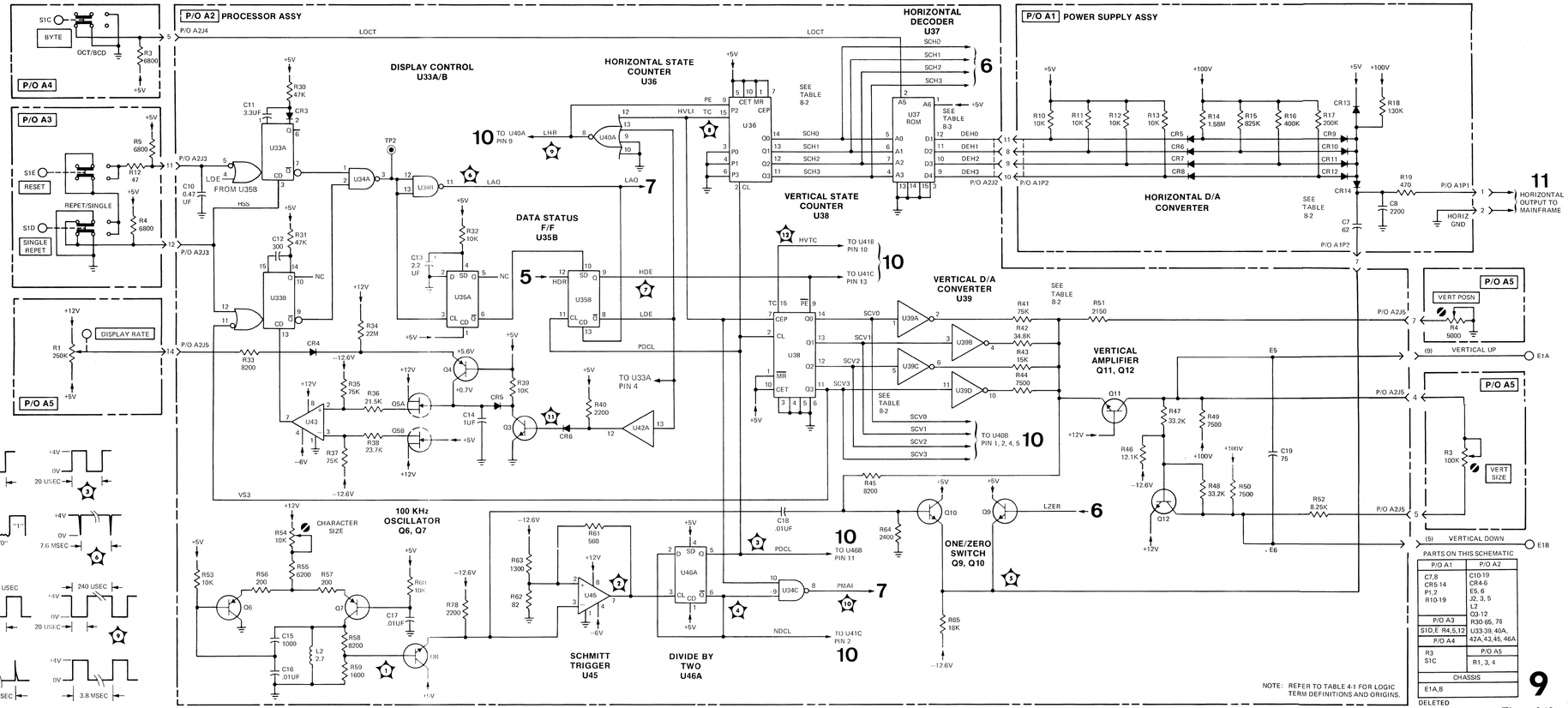
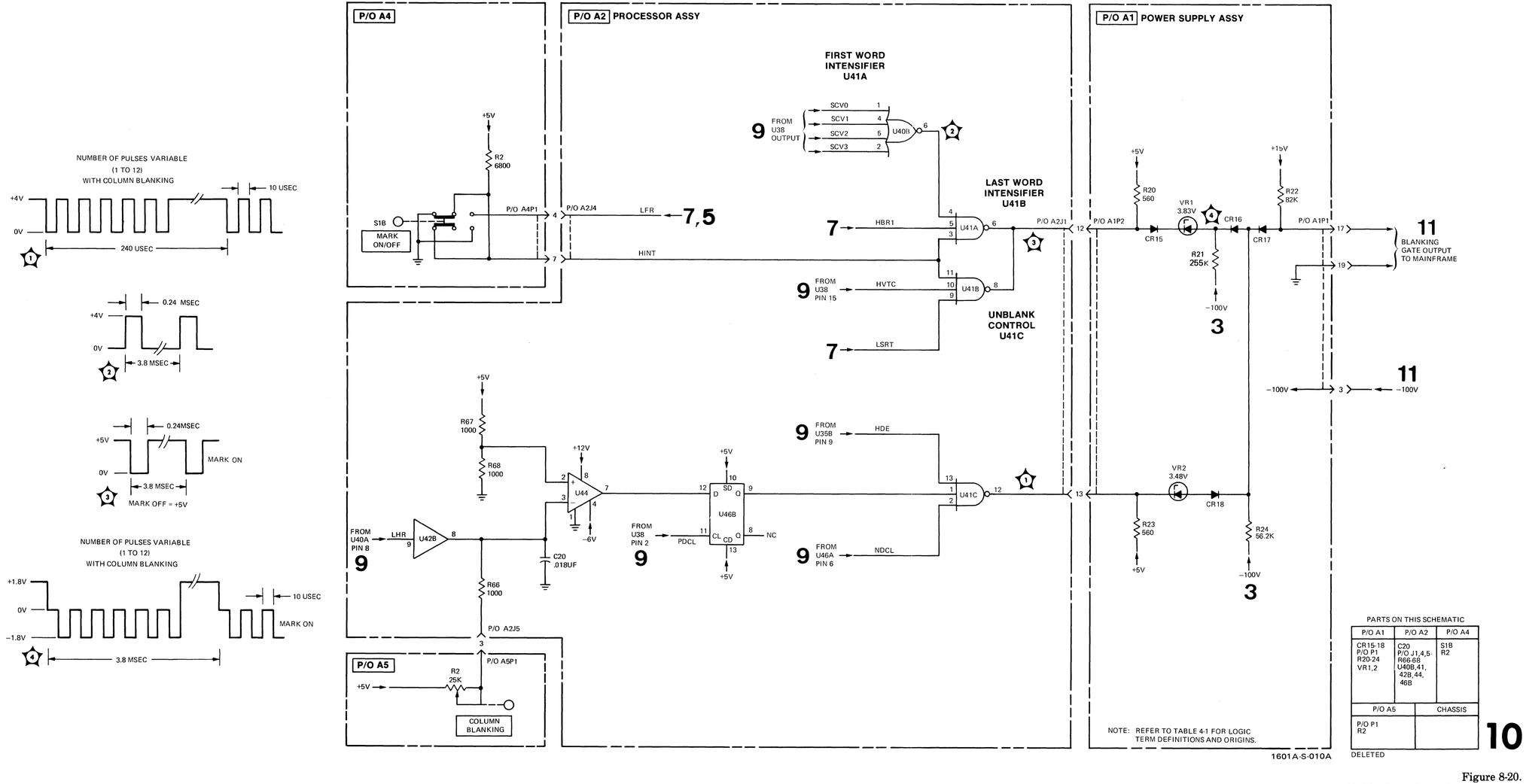


Figure 8-19. Display Control Schematic 9



PARTS ON THIS SCHEMATIC

P/O A1	P/O A2	P/O A4
CR15-18 P/O P1 R20-24 VR1,2	C20 P/O J1,4,5 R66-68 U40B,41, 42B,44, 46B	S1B R2
P/O A5		CHASSIS
P/O P1 R2		

DELETED

10

Figure 8-20.
Unblanking Control Schematic 10

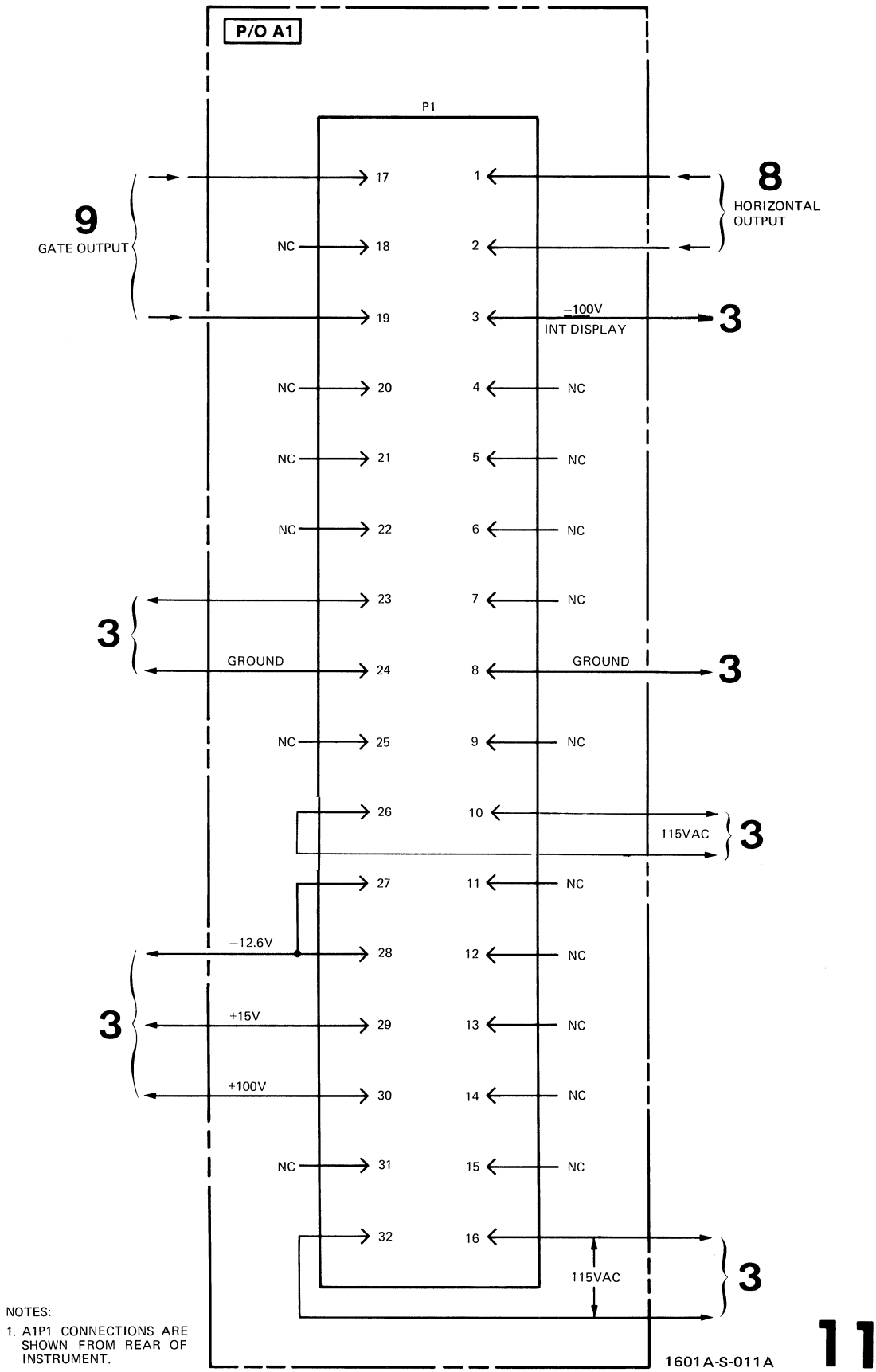
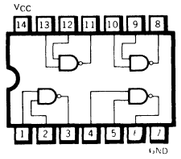
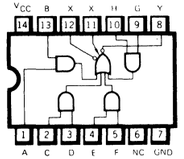


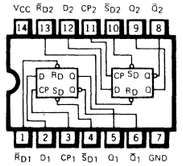
Figure 8-21. Mainframe Connector Schematic 11



1820-0054
1820-0094



1820-0074



1820-0077

Positive logic:

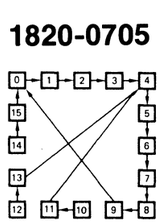
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

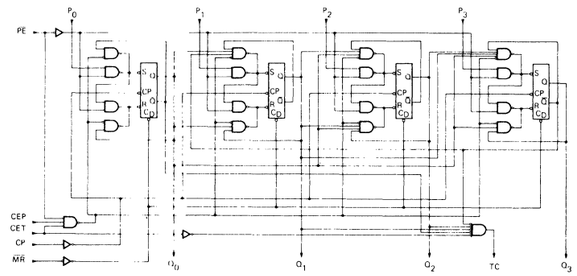
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

NOTES:
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

1820-0705

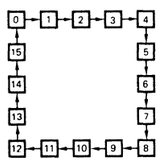


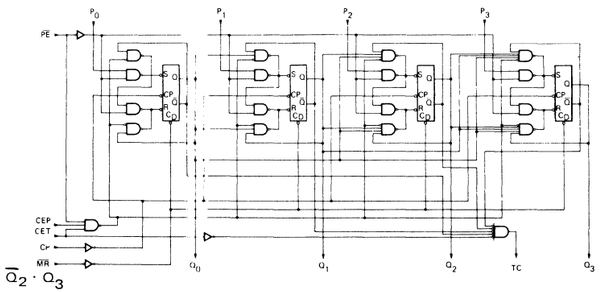


LOGIC EQUATIONS
Count Enable = CEP · CET · PE
TC for 1820-0705 = CET · $Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3$
Preset = $\overline{PE}$ · CP3 (rising clock edge)
Reset = $\overline{MR}$

NOTE:
The 1820-0705 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

1820-0231



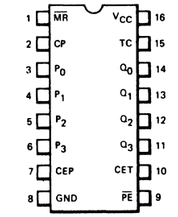


LOGIC EQUATIONS
Count Enable = CEP · CET · PE
TC for 1820-0231 = CET · $Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3$
Preset = $\overline{PE}$ · CP+ (rising clock edge)
Reset = $\overline{MR}$

MODE SELECTION

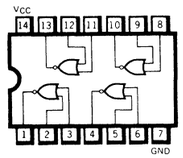
$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

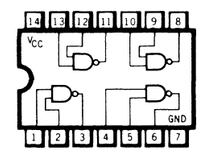


PIN NAMES

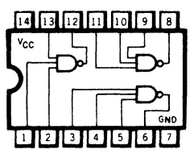
$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0, P_1, P_2, P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note b)
TC	Terminal Count Outputs



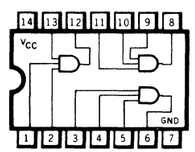
1820-0328



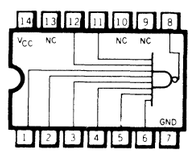
1820-0370



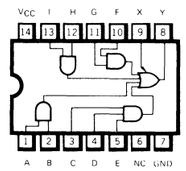
1820-0371



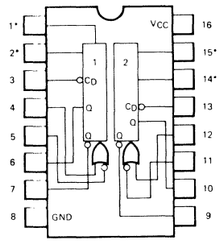
1820-0372



1820-0375

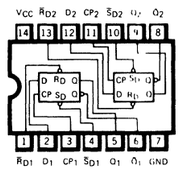


1820-0379



*Pins for external timing.

1820-0515



Asynchronous Inputs:
LOW input to preset sets Q to HIGH level
LOW input to clear sets Q to LOW level
Preset and clear are independent of clock

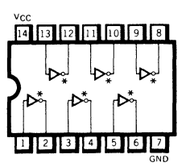
TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
L	L	H
H	H	L

H = HIGH Level, L = LOW Level

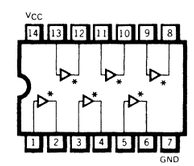
NOTES: t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

1820-0512



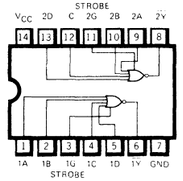
*OPEN COLLECTOR

1820-0577



*OPEN COLLECTOR

1820-0618



1820-0655

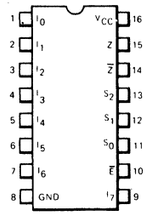
TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

H = HIGH level, L = LOW level, X = irrelevant

1-L-045

Figure 8-22.
Integrated Circuit (IC) Identification (Sheet 1)

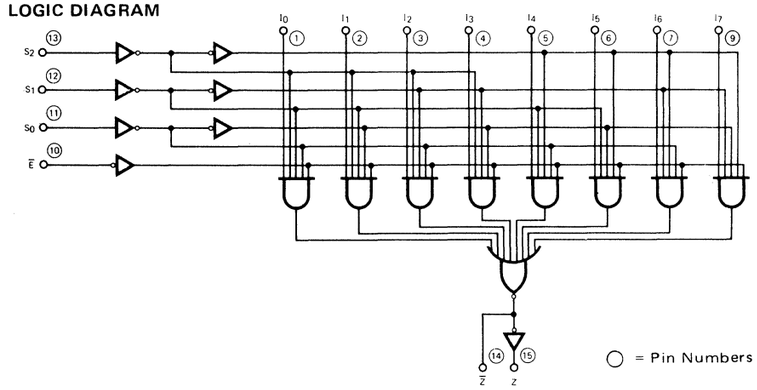


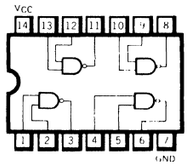
1820-0615

PIN NAMES

S_0, S_1, S_2	Select Inputs
$\bar{E}$	Enable (Active LOW) Input
I_0 to I_7	Multiplexer Inputs
Z	Multiplexer Output (Note b)
$\bar{Z}$	Complementary Multiplexer Output

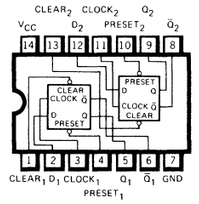
LOGIC DIAGRAM





1820-0681

1820-0693



Positive logic: LOW input to preset sets Q to HIGH level
LOW input to clear resets Q to LOW level
Preset and clear are independent of clock

SYNCHRONOUS TRUTH TABLE
(EACH FLIP-FLOP)

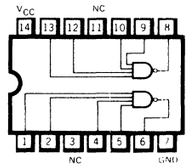
t_n	t_{n+1}	
INPUT	OUTPUT	
D	Q	$\bar{Q}$
L	L	H
H	H	L

H = HIGH level
L = LOW level
D = Data

NOTES:
A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

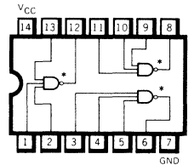
ASYNCHRONOUS TRUTH TABLE
(EACH FLIP-FLOP)

INPUT		OUTPUT	
Preset	Clear	Q	$\bar{Q}$
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	



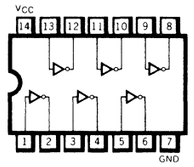
NC—No internal connection.

1820-0697

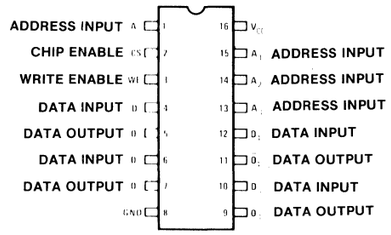


* Open collector

1820-0907



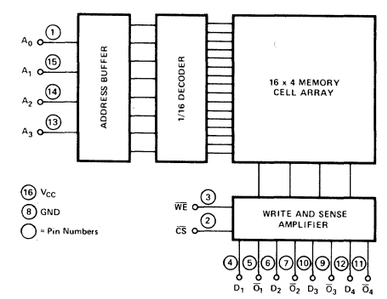
1820-1139



PIN NAMES

D_1–D_4	DATA INPUTS	$\overline{CS}$	CHIP SELECT INPUT
A_0–A_3	ADDRESS INPUTS	$\bar{O}_1$–$\bar{O}_4$	DATA OUTPUTS
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)

1820-1106



CE	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Input
L	H	Read	Complement of Selected Word
H	L	Inhibits Storage	Complement of Data Inputs
H	H	Do Nothing	High

1-L-046

Figure 8-22. Integrated Circuit (IC) Identification (Sheet 2)

MANUAL CHANGES

MODEL 1601A

LOGIC STATE ANALYZER

Manual Serials Prefixed: 1351A
Manual Printed: FEB 1974

Make all changes listed below as Errata. Check the following table for your instrument serial prefix and/or serial number and make listed change(s) to the manual:

Serial Prefix or Number	Make Changes	Serial Prefix or Number	Make Changes
1435A	1		

ERRATA

Page 2-1, paragraph 2-10,
Add following sentence: Model 1601A is not recommended for use in storage oscilloscope mainframes.

△ Page 5-2, table 5-1,
4-Bit Binary Counter: Change recommended Model number to read Integrated Circuit HP Part No. 1820-0231 (Fairchild Part No. 9316).

Page 5-6, paragraph 5-14,
Add step after step ad as follows:
ad(1). Set CLOCK to ⌐(in).

Page 5-7, figure 5-5,
0V (reference level): Change to 1.5 VDC (two places).
Change: statement 0.4V p-p (SYMMETRICAL ABOUT 0V) to read 3V p-p (SYMMETRICAL ABOUT 1.5 VDC) in two places.

△ Page 6-3, figure 6-1,
MP8: Change to read MP31 on upper, left-hand side of diagram.
MP9: Change to read MP8 on center, left-hand side of diagram.
TP1: Delete reference designator. This part is not separately replaceable.
MP8: Change to MP32 on bottom, left-hand side of diagram.
Add: MP28 to the undesignated knob shown in the upper, right-hand corner of the front panel.

Table 6-2,
△ A2A1: Change HP Part No. and Mfr Part No. to 01601-66512.
△ J1: Change to HP Part No. 1250-0118, CONNECTOR: BNC, Mfr Code 24931, Mfr Part No. 28JR 128-1.
△ J2: Change to HP Part No. 1250-0118, CONNECTOR: BNC, Mfr Code 24931, Mfr Part No. 28JR 128-1.
△ MP7: Change Qty to 3.
△ MP8: Change Qty to 3.
△ Delete: MP9.
△ MP10: Change Qty to 4.
△ MP11: Change Qty to 12.
△ MP15: Change HP Part No. and Mfr Part No. to 01822-67401, and change Qty to 1.
△ MP28: Change HP Part No. and Mfr Part No. to 01803-67401.
△ Add: MP31, HP Part No. 0370-0671, Qty 3, PUSH-BUTTON: SQUARE BLUE, Mfr Code 28480, Mfr Part No. 0370-0671.
△ Add: MP32, HP Part No. 0370-0684, Qty 2, PUSH-BUTTON: SQUARE GOLD, Mfr Code 28480, Mfr Part No. 0370-0684.
△ Delete: TP1.
△ A1C2: Change Qty to 1.
△ A1C3: Change Qty to 1.

10 February 1975
△ = Latest additions to this change sheet.
This change sheet supersedes all prior change sheets for this manual.

Supplement A for
01601-90903

ERRATA (Cont'd)

Table 6-2 (Cont'd),
Δ A1R9: Change Qty to 14.
Δ A2C3: Change Qty to 3.
Δ A2C13: Change to HP Part No. 0180-0309, C:FXD ELECT 4.7 UF 20% 10 VDCW, Mfr Code 56289, Mfr Part No. 150D475X0010A2-DYS.
Δ A2C21: Add Qty of 4.
Δ A2C24: Add Qty of 6.
Δ A2C37: Change reference designator to read A2C37 thru A2C39.
Δ Add: A2C40, HP Part No. 0160-3665, Qty 1, C:FXD CER 0.01 UF +80–20% 500 VDCW, Mfr Code 56289, Mfr Part No. C071A501K103ZS25-CD.
Δ A2J3: Change Qty to 9.
Add: A2J11, HP Part No. 1200-0441, SOCKET:IC 14-PIN MINATURE FOR A2U46, Mfr Code 28480, Mfr Part No. 1200-0441.
Δ A2R1: Add Qty of 1.
A2R32: Change to HP Part No. 0757-0959, R:FXD FLM 30K OHM 2% 1/8W, Mfr Code 28480, Mfr Part No. 0757-0959.
Δ A2R51: Change Qty to 3.
Δ A2R65: Change Qty to 1.
Add: A2R81, HP Part No. 0757-0912, R:FXD MET FLM 330 OHM 2% 1/8W, Mfr Code 28480, Mfr Part No. 0757-0912.
Δ A2U23: Change Qty to 2.
A2U37: Change to HP Part No. 1816-0352, IC:ROM 256X4, Mfr Code 28480, Mfr Part No. 1816-0352.
Δ A2A1: Change HP Part No. and Mfr Part No. to 01601-66512.
Δ Add: A2A1C1, HP Part No. 0140-0218, Qty 1, C:FXD MICA 160 PF 2%, Mfr Code 28480, Mfr Part No. 0140-0218.
Δ A2A1R1: Change Qty to 53.
Δ Add: A2A1U9, HP Part No. 1820-0691, Qty 1, IC:TTL SCHOTTKY 4 W(4-2-3-2) INPT, Mfr Code 01295, Mfr Part No. SN74S64N.
Δ Add: A2A1U10, HP Part No. 1820-0697, IC:TTL DUAL 4-INPT LINE DRIVER, Mfr Code 01295, Mfr Part No. SN74S140N.
Δ Delete: A3R14.
Δ A5R1: Change to HP Part No. 2100-0651, R:VAR COMP 250K 20% 0.5W LIN, Mfr Code 28480, Mfr Part No. 2100-0651.
Δ A5R2: Change to HP Part No. 2100-0643, R:VAR COMP 25K OHM 20% 0.5W LIN, Mfr Code 01121, Mfr Part No. WA4H052S253MZ.
Δ A6R1 thru A6R12: Change reference designators to A6R1 thru A6R24.
Δ Add: A7U2, HP Part No. 1820-1139, IC:TTL INVERTER, Mfr Code 28480, Mfr Part No. 1820-1139.

Δ Page 7-1/7-2,
Add: Paragraph 7-11 as follows:
7-11. Option 003. This is a standard option to allow operation from a source of 100V or 200V input power. Option 003 instruments are the same as the standard instruments except that transformer

Δ Page 7-1/7-2 (Cont'd),
T1 is replaced with a new transformer (HP Part No. 9100-3469).

Δ Schematic 3,
A1J1, pin 28: Delete connection labeled TO R24 on schematic 10.
Schematic 5,
U13, pin 1: Change to pin 2.
U13, pin 2: Change to pin 1.
Schematic 6,
A2U14, pin 1: Change $\overline{MD}$ to read $\overline{MR}$.
A2U18, pin 15: Change $\overline{Z}$ to read Z.
A2U18, pin 14: Change Z to read $\overline{Z}$.
A2U16: Change designator to A2U15.
A2U15: Change designator to A2U16.
Δ A2U15, pin 1: Change A0 to read A3.
Δ A2U15, pin 15: Change A1 to read A0.
Δ A2U15, pin 14: Change A2 to read A1.
Δ A2U15, pin 13: Change A3 to read A2.
Δ A2U17, pin 1: Change A0 to read A3.
Δ A2U17, pin 15: Change A1 to read A0.
Δ A2U17, pin 14: Change A2 to read A1.
Δ A2U17, pin 13: Change A3 to read A2.
Schematic 7,
LFR, 10: Add reference to schematic 5.
A2U29, pin 2: Change CL to read CP.
Δ Delete: A3R14.
Δ Add: A2R81 (330) in between A2J3, pin 1 and base of A2Q13.
Schematic 8,
A2A1U1 through A2A1U5, pin 2: Change CL to read CP.
6, LDR, LNDLY, HDLE, PMAC: Change schematic reference from 6 to 7.
Page 8-27/8-28, table 8-3,
SCV0: Change to read SCH0.
SCV1: Change to read SCH1.
SCV2: Change to read SCH2.
SCV3: Change to read SCH3.
Schematic 9,
A2U35B: Change 5 to read 7 as signal source on pin 12 (HDR).
A2U36, pin 5: Label as P2 and remove P2 from between pins 9 and 15.
A2R32: Change value to 30K.
A2U36, pin 9: Label as $\overline{PE}$.
A2U40A, pin 8: Change output notation to read 10 TO U42B PIN 9.
Δ A2C13: Change value to 4.7 UF.
Δ A2R32: Change value to 30K.
Page 8-31, figure 8-22,
1820-0705: Change Count Enable to equal CEP · CET · $\overline{PE}$, and change Preset to equal $\overline{PE}$ · CP + (rising clock edge).
1820-0231: Change Count Enable to equal CEP · CET · $\overline{PE}$, and change TC for 1820-0231 to equal CET · $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$.

ERRATA (Cont'd)

Page 8-32, figure 8-22,
1820-1106: Change $\overline{WE}$ to read WE, and change $\overline{CS}$ to read CE. Replace corresponding table with following table from this manual changes sheet:

CE	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	High
L	H	Read	Compliment of Written Data
H	L		High
H	H		High

CHANGE 1

Page 1-1, table 1-1,
Change CLOCK AND TRIGGER OUTPUTS to read PATTERN TRIGGER AND DELAYED TRIGGER OUTPUTS.

Page 3-0, figure 3-1,
Item 3: Change to DELAYED TRIGGER OUTPUT. Output connector for TTL level pulse generated when the input data meets triggering requirements and the count selected on DELAY SET (item 21) is completed.
Item 4: Change nomenclature to PATTERN TRIGGER OUTPUT. Same function as for TRIGGER OUTPUT.

Page 4-4, paragraph 4-27,
Change lines 6 and 7 to read: HACL (a 40-ns wide internal clocking signal). CLK AVG is . . . . .

Page 4-4, paragraph 4-28,
Change last two lines to read:
verted to produce the front panel PATTERN TRIGGER OUTPUT signal. The DELAYED TRIGGER OUTPUT on the front panel is a positive-going pulse which is approximately 40 ns wide. It occurs at the time that the delay generator count is completed in the START DELAY mode; in all other modes, the timing is the same as the PATTERN TRIGGER OUTPUT. The frequency of the PATTERN TRIGGER OUTPUT is derived from the frequency of the incoming clock. The frequency of the DELAYED TRIGGER OUTPUT is dependent on the selected display rate of the Model 1601A.

Page 4-8, table 4-1,
HACL: Delete last sentence in FUNCTION column.

Page 5-7, paragraph 5-20,
Change: paragraph title to read Pattern Trigger and Delayed Trigger Outputs.

Page 5-9, paragraph 5-20,
Add step after a as follows:
a(1). Set TRIGGER MODE to START DELAY and DELAY SET to all zeros.
CLOCK OUTPUT and TRIGGER OUTPUT:
Change to read PATTERN TRIGGER OUTPUT and DELAYED TRIGGER OUTPUT in step b.

Page 5-12, figure 5-9,
TIMER COUNTER, output 3: Label connection TO PATTERN TRIGGER OUTPUT.
TIMER COUNTER, output 4: Label connection TO DELAYED TRIGGER OUTPUT.

Table 6-2,
A2A1: Change HP Part No. and Mfr Part No. to 01601-66512.
Add: A2A1C2, HP Part No. 0140-0218, C:FXD MICA 160 PF 2%, Mfr Code 28480, Mfr Part No. 0140-0218.
Add: A2A1R21, HP Part No. 0698-3447, R:FXD MET FLM 422 OHM 1% 1/8W, Mfr Code 28480, Mfr Part No. 0698-3447.
Add: A2A1R22, HP Part No. 0757-0418, R:FXD MET FLM 619 OHM 1% 1/8W, Mfr Code 28480, Mfr Part No. 0757-0418.
Add: A2A1U9, HP Part No. 1820-0691, IC:TTL SCHOTTKY 4-2-3-2-INPUT AND-OR-INVERT GATE, Mfr Code 01295, Mfr Part No. SN74S64N.
Add: A2A1U10, HP Part No. 1820-0697, IC:TTL DUAL 4-INPT LINE DRIVER, Mfr Code 01295, Mfr Part No. SN74S140N.

Schematic 1,
TRIGGER OUTPUT: Relabel as PATTERN TRIGGER OUTPUT at top-center of page.
CLOCK OUTPUT: Delete connector at lower, left-hand side of schematic.

CHANGE 1 (Cont'd)

Schematic 1 (Cont'd),
DELAY GENERATOR TDR: Show output connection labeled DELAYED TRIGGER OUTPUT on schematic 8 portion in upper, right-hand area of schematic.
Schematic 2,
Delete: CLOCK OUTPUT on right-hand side.
TRIGGER OUTPUT: Change to PATTERN TRIGGER OUTPUT on right-hand side. Show wire color of (9).
A2A1 DELAY ASSY: Add output J1 connection labeled DELAYED TRIGGER OUTPUT. Show wire color of (0).

Page 8-22, figure 8-12,
Lower, left-hand side: Delete CONNECTS TO CLOCK OUTPUT, J2.
Schematic 7,
J2: Change TRIGGER OUTPUT to read PATTERN TRIGGER OUTPUT.
Delete: J1 and associated cable.
Schematic 8,
Replace with schematic 8 supplied with this manual changes sheet.

01601-90903

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