$(Ba,Sr)TiO_3$ dielectrics for future stacked-capacitor DRAM

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Thin films of barium–strontium titanate $(Ba,Sr)TiO_3$ (BSTO) have been investigated for use as a capacitor dielectric for future generations of dynamic random-access memory (DRAM). This paper describes progress made in the preparation of BSTO films by liquid-source metal-organic chemical vapor deposition (LS–MOCVD) and the issues related to integrating films of BSTO into a DRAM capacitor. Films of BSTO deposited on planar Pt electrodes meet the electrical requirements needed for future DRAM. The specific capacitance and charge loss are found to be strongly dependent on the details of the BSTO deposition, the choice of the lower electrode structure, the microstructure of the BSTO, the post-electrode thermal treatments, BSTO dopants, and thin-film stress. Films of BSTO deposited on patterned Pt electrodes with a feature size of 0.2 μm are found to have degraded properties compared to films on large planar structures, but functional bits have been achieved on a DRAM test site at 0.20-μm ground rules. Mechanisms influencing specific capacitance and charge loss of BSTO films are described, as are the requirements for the electrode and barrier materials used in stacked-capacitor structures, with emphasis given to the properties of the Pt/TaSi(N) electrode/barrier system. Major problems requiring additional investigation are outlined.

1. Introduction

The density of dynamic random-access memory (DRAM) has increased by a factor of 4× every three years during the past 25 years, and this trend continues today. This remarkable increase in density has been brought about by advances in various areas of technology, including lithography, dry patterning, and thin-film deposition techniques, and by improvements in the DRAM architecture resulting in a more efficient cell utilization. **Figure 1** shows the expected size of a DRAM cell for future generations of DRAM [1]. As the lithographic feature size decreases from 0.25 to 0.10 μm, the area of the DRAM cell is expected to decrease by a factor of more than 10×.

Since DRAM cells contain a single transistor and capacitor and each capacitor must be isolated from adjacent capacitors in the array, only a fraction of the cell area can be occupied by the capacitor. An estimate of the

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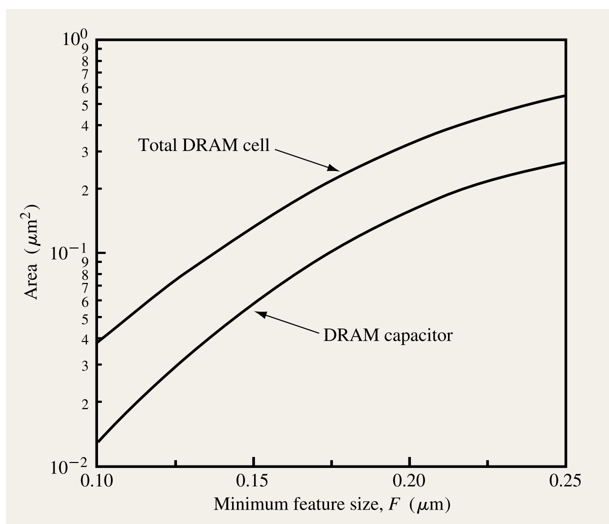

Figure 1

Expected area of a DRAM cell and the area available for the capacitor as a function of the minimum feature size.

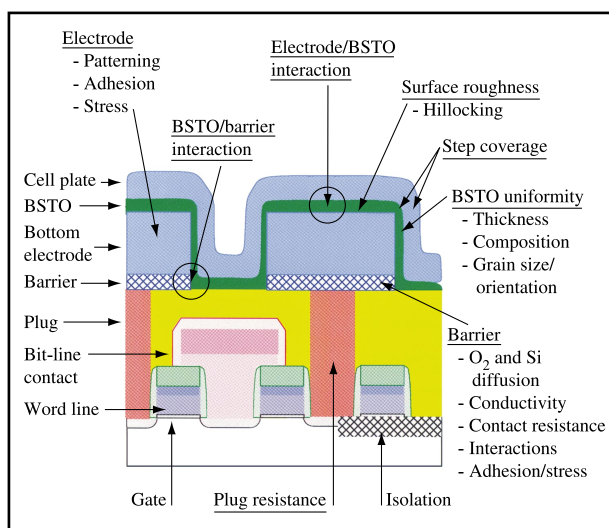

Figure 2

Schematic representation of a simple stacked-capacitor structure with the capacitor above the bit line.

area available for the capacitor is shown by the red line in Figure 1. Here, the capacitor was assumed to be rectangular in shape and separated from the adjacent capacitors by 0.8× the minimum lithographic feature size.

The minimum amount of charge that must be stored in the capacitor in order to obtain reliable operation of the DRAM is determined by the sensitivity limits of the sense amplifiers, parasitic capacitances, and alpha-particle considerations. This minimum charge has historically decreased by about a third per generation [2]. Similar decreases in operating voltage are expected for future DRAM generations, so that the required DRAM capacitance will remain nearly constant at 25–30 fF/cell. Achieving the required capacitance density while maintaining a charge loss of $<10\%$ after one second, corresponding to a current density of approximately 1 fA/cell, will be a major challenge in fabricating future generations of DRAM.

Higher capacitance density can be achieved by the use of 1) complex electrode structures providing a large surface area within a small lateral area; 2) thinner capacitor dielectrics; and 3) higher-permittivity capacitor dielectric materials. In general, increasing the surface area leads to increased complexity and hence increased cost; other papers in this issue discuss the limitations on the dielectric thickness of SiO_2 and SiN_x (see for example [3, 4]).

Much work in recent years has focused on the development of high-permittivity materials for a DRAM capacitor. DRAM chips manufactured to date contain primarily capacitors utilizing a thin dielectric containing a mixture of silicon dioxide and silicon nitride sandwiched between two electrodes made of doped crystalline or polycrystalline silicon. Modifying this materials set will break a 25-year precedent in which long-term dielectric performance and reliability have been firmly established. Incorporating a high-permittivity material into a DRAM capacitor drives the need not only for new dielectric materials, but also for new electrode and barrier materials. Thin-film barium–strontium titanate $(Ba,Sr)TiO_3$ (BSTO), with a permittivity in the range 200–350 and a specific capacitance exceeding 125 fF/μm^2, has emerged as the leading contender as a dielectric for future DRAMs.

This paper introduces the issues involved with integrating high-permittivity thin films of BSTO into a DRAM capacitor. The following section describes the capacitor structure. Section 3 focuses on electrode and barrier issues. Section 4 describes the deposition process for producing thin films of BSTO by liquid-source metal-organic chemical vapor deposition (LS–MOCVD). Sections 5 and 6 focus on the microstructure and electrical properties of Pt/BSTO/Pt capacitors. Conclusions and problem areas requiring additional investigation are described in Section 7.

2. Stacked-capacitor structure with $(Ba,Sr)TiO_3$ dielectrics

Various stacked-capacitor structures have been proposed for high-permittivity dielectrics. A simple stacked-capacitor structure, with the capacitor above the bit line,

is illustrated in **Figure 2**. Here, the bottom electrode of the capacitor is connected to the transfer device through a conductive plug. A conductive barrier material is used to separate the electrode from the plug material to prevent electrode–plug interdiffusion and reaction, and to protect the plug against oxygen exposure during the deposition of the BSTO dielectric, which normally occurs in an oxygen environment at temperatures in the range of 450–700°C. The high-permittivity dielectric conformally coats the bottom electrode, and the counter electrode forms a plate which is common to an array of capacitors. The major issues which must be addressed when integrating BSTO dielectrics in this type of DRAM structure are also presented in Figure 2.

Figure 3 shows a cross-sectional transmission electron micrograph (TEM) of a Pt/BSTO/Pt stacked-capacitor structure, similar to that illustrated in Figure 2. Here, the minimum feature size is 0.2 μm. The structure consists of a 250-nm-thick Pt bottom electrode on a 75-nm barrier of TaSiN, over a doped polycrystalline silicon plug embedded in a TEOS dielectric. The BSTO thickness is 27 nm, and the plate electrode is a 50-nm film of Pt. The barrier and electrode layers are deposited by physical vapor deposition (PVD), while the BSTO dielectric is deposited by MOCVD.

The bottom Pt electrode is patterned using dry etching with a hard mask, such as Ti, TiN, or SiO_2. After the bottom Pt electrode is etched, the remaining hard mask is removed and the TaSiN barrier layer is simultaneously etched to isolate the individual Pt electrodes. The etch rate of the hard mask is higher than the etch rate of TaSiN during the mask-removal step. As a result, the remaining hard mask is removed quickly and the bottom Pt electrode itself acts as a mask during most of the TaSiN-layer etch. Because of the low selectivity of Pt to TaSiN, corner rounding and erosion of Pt occur, leading to a curved shape of the bottom Pt electrode.

The BSTO film is amorphous on the surface of the TaSiN barrier but crystallized on the Pt surface. Microprobe analysis indicates that the amorphous BSTO layer has a higher Ti concentration than the crystallized BSTO film, but no variation in the BSTO composition can be detected along the Pt electrode. The interaction of the BSTO and the barrier layer reveals a drawback to this structure, and it will be beneficial to recess the barrier into the plug or use a spacer to cover the TaSiN surface to avoid direct exposure of the TaSiN to the BSTO film [5, 6].

The required height of such a simple stacked-capacitor structure as a function of the minimum feature size and specific capacitance of the dielectric layer is shown in **Figure 4**. Here, the structure was assumed to utilize the area for the capacitor described by the curve in Figure 1, and the bottom electrode was assumed to have vertical sidewalls. Only the surface area on the sides of the

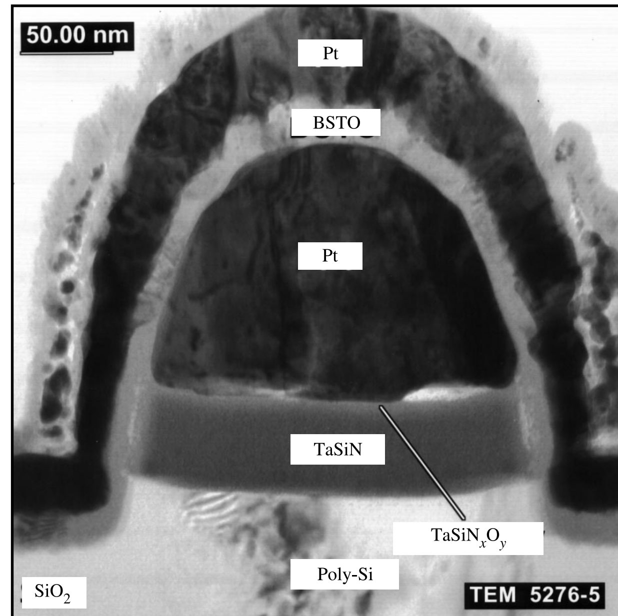

Figure 3

Cross-sectional TEM image of a stacked-capacitor structure with a BSTO dielectric, Pt electrodes, and a TaSiN barrier layer. The minimum feature size is 0.2 μm, and the BSTO dielectric thickness is 27 nm.

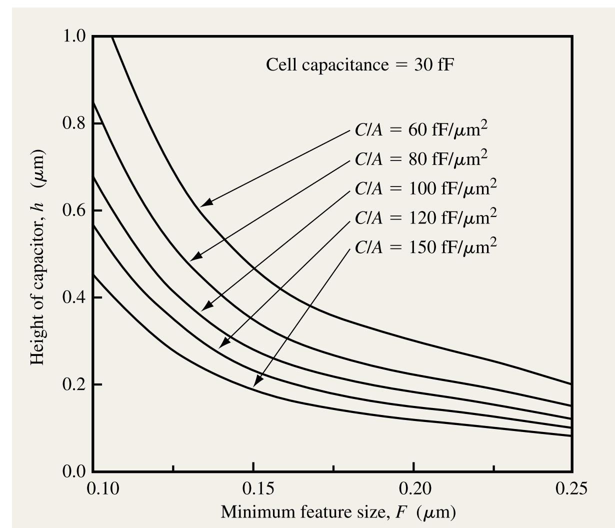

Figure 4

Required height of the bottom electrode in a stacked-capacitor structure as a function of the minimum feature size and the specific capacitance of the dielectric layer.

Table 1 Candidate materials which can be used as electrodes for BSTO and other high-permittivity dielectrics. Preparation method, permeability to oxygen, work function, and suitability for patterning into small features are indicated.

Electrode material	*Deposition methods*	*Permeability to oxygen*	*Work function* (eV)	*Dry etch*
Pt	PVD, CVD	High	5.6–5.7	Difficult
Ir	PVD	Moderate	5.0–5.8	Difficult
Ru	PVD		4.7	Easy/dangerous
Pd	PVD	Oxidizes readily	5.1–5.6	Difficult
IrO_2	Reactive sputtering	Low		Difficult
RuO_2	Reactive sputtering	Low		Easy/dangerous

Table 2 Candidate materials which can be used as a conductive plug between capacitor and the transfer device and their resistivity.

Plug material	*Resistivity* ($\mu\Omega$-cm)	*Reactivity with Pt*	*Oxidation resistance*
Doped polysilicon	500	High	Good
W	10	Low	Poor
WSi_x	60	High	Good

capacitor is considered in this calculation. As can be seen, to keep the height of the capacitor below 0.5 μm as the minimum feature size approaches 0.1 μm, a specific capacitance approaching 150 fF/μm^2 is required.

3. Electrode and barrier properties

Most integration schemes for perovskite dielectrics use noble-metal or noble-metal-oxide electrodes in combination with a deposited diffusion-barrier material at the electrode/plug interface. In this section we briefly survey electrode and barrier materials under consideration for use with these dielectrics, and focus on the properties of the TaSiN barrier used with Pt electrodes.

Table 1 lists materials potentially suitable for use as electrodes with BSTO and perovskite dielectrics, along with some of their relevant properties. Patterning of Pt (and Ir) electrode materials is complicated by the absence of any low-temperature readily formable volatile etch products. Pt is typically patterned by reactive ion etching (RIE) using a Cl-based chemistry and a patterned hard mask. Physical sputtering is believed to be the dominant etch mechanism when conventional dry-etching techniques are used. Fence-free Pt etching can be achieved with a Pt profile angle close to 70°, as shown in Figure 3. Here, the SEM image is taken after removal of the remaining TiN hard mask; the Pt thickness is 250 nm and the material underlying Pt is SiO_2.

The diffusion barrier must prevent plug oxidation and electrode/plug reactions and must remain conductive after the deposition and processing of the BSTO dielectric. The degree of oxidation resistance and oxygen diffusion-barrier function required of the diffusion-barrier material clearly depends on the severity of the oxygen exposure associated with the deposition and post-electrode anneals of the BSTO capacitor.

The choice of stacked-capacitor structure is also a factor. In the simple stacked-capacitor structure, the side of the barrier is directly exposed to the oxygen processing ambient, whereas in structures with a recessed barrier [5] or where the side of the barrier is covered with an insulating or noble-metal [6] layer, the barrier is primarily exposed to oxygen diffusing through the electrode grain boundaries [7].

The oxidation resistance required of the barrier material also depends on the properties of the barrier-material oxide that is formed. Some oxidation may be tolerable if the barrier oxide is not too resistive, but oxidation through the entire thickness of the barrier indicates that the barrier is not protecting underlying structures from exposure to oxygen. Finally, the demands on the barrier material also depend on the choice of electrode and plug materials. For example, an oxygen-permeable electrode material such as Pt would require a more oxidation-resistant barrier than the less oxygen-permeable electrode material IrO_2, and readily oxidizable plug materials such as W would be expected to be less tolerant to oxygen exposure than plug materials of doped polycrystalline Si. Some candidate plug materials are listed in **Table 2** along with their properties.

Another key requirement for the barrier material is that it prevent diffusion of plug material and/or silicon into the electrode. This is particularly important for plug materials of potentially "silicon-contributing" materials such as WSi_x or doped polycrystalline Si, which can react with noble-metal electrodes to form noble-metal silicides. In addition to forming a silicide, silicon may also diffuse to the electrode surface to form an SiO_2 layer which will lower the overall capacitance. These various barrier failure modes are illustrated in **Figure 5**.

Most candidate barrier materials are introduced to the structure as deposited layers. Some representative barrier materials are listed in **Table 3** and consist mostly of various metal nitrides and metal silicon nitrides. More

Table 3 Candidate materials which can be used as a barrier layer between the lower electrode and the conducting plug in a stacked-capacitor DRAM structure with a BSTO dielectric layer. These films can all be deposited by reactive ion sputtering.

Barrier material	Processability	Resistivity (mΩ-cm)	Oxidation resistance
TiN	Easy	0.2	Poor
TaN	Easy		Poor
TiAlN, TaAlN	Moderate		Good
TaSiN	Easy	1–10	Excellent

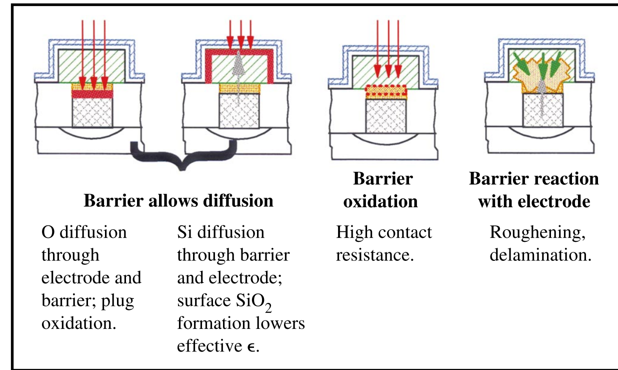

Figure 5

Schematic representation showing the possible failure modes of the barrier during thermal processing in an oxidizing ambient.

extensive listings can be found elsewhere [8]. Barriers used with doped polycrystalline Si plugs typically include a metal silicide layer at the barrier/plug interface to lower contact resistance (for example, the silicide $TiSi_2$ with the barrier TiN).

Barriers incorporated into the device structure in the nonrecessed geometry are typically patterned by RIE. With this patterning method, the barrier and electrode are perfectly aligned, since they are patterned in the same alignment step with the same hard mask. Barriers having the recessed geometry are typically patterned by planarization and self-aligned to recessed plugs. This self-aligned feature is advantageous in cases where a misaligned electrode does not completely cover an underlying plug, since the barrier material will be correctly in place over the plug even when the electrode is not. *In-situ*-formed barriers, a less explored alternative to deposited barriers, also have this self-aligned feature [9].

TaSiN is currently regarded as one of the more promising barrier materials [10–12]. Unlike the other barrier materials listed in Table 2, TaSiN remains amorphous (and thus free of fast-diffusion-path grain boundaries) over a wide range of compositions. Depending on the exact application, the TaSiN composition can be optimized for oxidation resistance, barrier properties, or low resistance. Increasing film nitrogen content typically improves Si diffusion-barrier performance but lowers conductivity, and decreasing Ta content typically improves barrier oxidation resistance.

The optimum TaSiN composition range for advanced dielectric barrier applications is indicated by the circled region on the ternary phase diagram of **Figure 6**, where the dots show compositions obtainable by reactive sputtering in Ar/N_2 with a $TaSi_2$ target. Resistance data for TaSiN films deposited on insulating substrates are given in **Table 4** for various compositions of TaSiN. Resistances were measured before and after oxidation anneals at 650°C in atmospheric-pressure O_2 ambients. As-deposited film resistance clearly increases with film nitrogen content, and the resistance of the annealed films clearly increases with oxygen exposure. However, it can

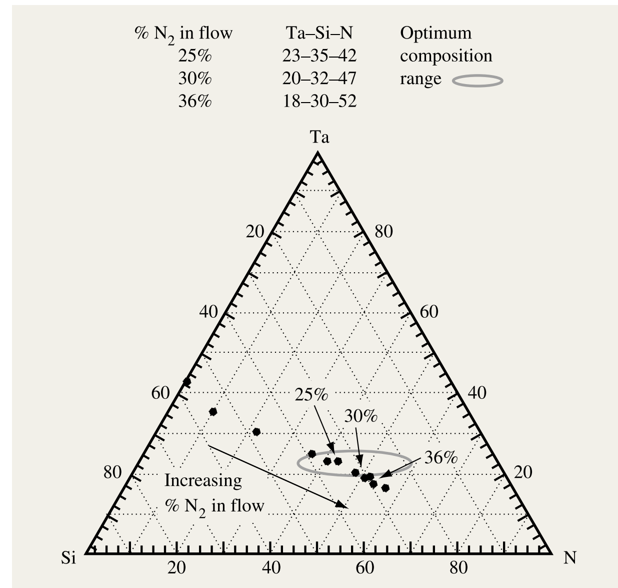

Figure 6

Ternary phase diagram showing the range of TaSiN compositions investigated for conductivity and oxidation properties. The compositions in the circled region were found to have the optimal compositions for a barrier application.

be seen that all films remain below 100 kΩ/□ even after 30-min anneals in an O_2 ambient.

Figure 7(a) shows patterned electrode structures as they would look immediately prior to BSTO deposition. The TaSiN is uniform in appearance and shows no oxidation. **Figures 7(b)** and **7(c)** show electrodes from the same wafer after 5- and 30-min anneals at 650°C in

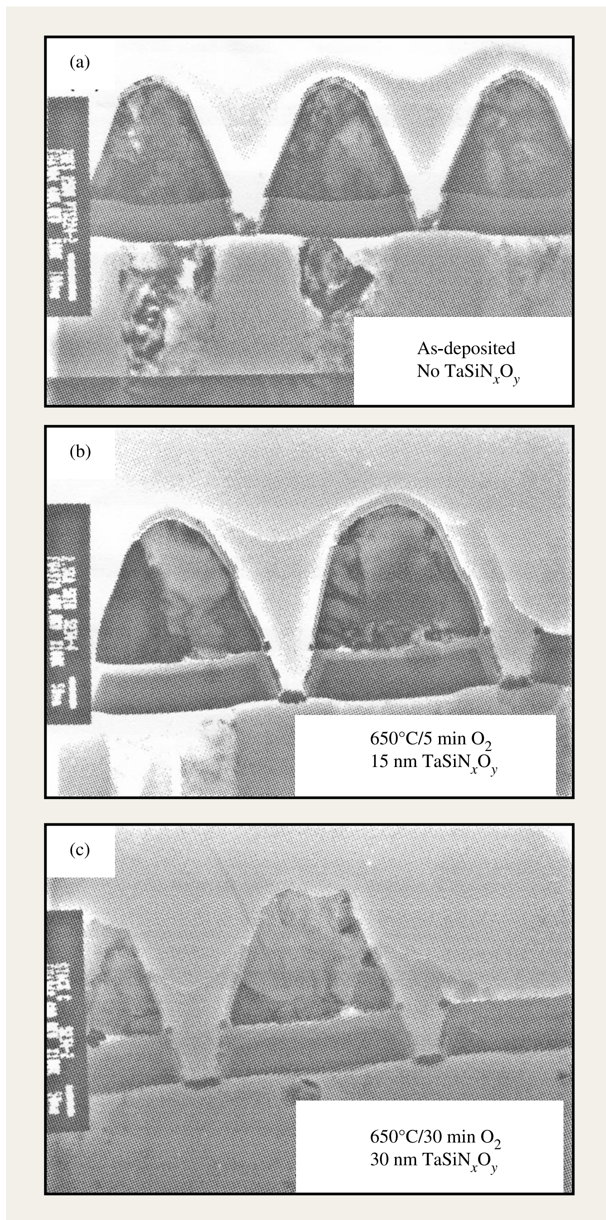

Figure 7

TEM micrographs showing patterned electrode structures (a) on a TaSiN barrier prior to BSTO deposition; (b) after a 650°C anneal in oxygen at atmospheric pressure for 5 min; (c) after a 650°C anneal in oxygen at atmospheric pressure for 30 min. An oxidized surface layer is observed on the top and sides of the TaSiN after the anneals.

atmospheric-pressure O_2 ambients. A uniformly thick oxidized $TaSiN_xO_y$ layer is clearly present at the sides and top of the TaSiN structure after both anneals. The thickness of this layer is estimated to be about 15 nm for the 5-min anneal and 30 nm for the 30-min anneal. Its uniform thickness suggests that oxygen diffusion through the Pt electrode grain boundaries and/or along the Pt/TaSiN interface is extremely rapid. The oxidized layer can also be observed in the TEM micrograph of Figure 3. The absence of an oxidized layer at the bottom TaSiN surface indicates that the TaSiN is an excellent barrier to oxygen diffusion. However, these micrographs clearly indicate that lower-temperature processing or an improved electrode/barrier material is needed if the oxidized $TaSiN_xO_y$ material has a high resistance.

Table 4 Sheet resistance (kΩ/□) of TaSiN as a function of the composition and oxidation treatment. The samples are 15 nm $TaSiN/SiO_2/Si$. All oxidation treatments were performed in an atmospheric pressure of oxygen.

Ta–Si–N composition	*Oxidation treatment*		
	As-deposited	*650°C/5 min RTA*	*650°C/30 min furnace*
23–34–44	1.2	3.3	10
20–30–49	2.4	6.8	20
18–30–52	12	38	94

4. Deposition of BSTO by MOCVD

Because of the three-dimensional nature of the bottom electrode, metal-organic chemical vapor deposition (MOCVD) is the method of choice for preparing a conformal coating of BSTO. In this study, films of $(Ba,Sr)TiO_3$ are deposited by MOCVD using liquid delivery of the precursors. $Ba(thd)_2$(4-glyme), $Sr(thd)_2$(4-glyme), and $Ti(O\text{-}iPr)_2(thd)_2$ are used as the organic sources. Liquid precursors are volumetrically mixed, metered, and delivered to a vaporization zone. The volumetric control of room-temperature liquids allows for high accuracy of mixing, provides precision in tuning the composition of the BSTO, and provides high wafer-to-wafer reproducibility [13].

The BSTO CVD reactor is a single-wafer warm-wall reactor, with the wall temperature maintained at 235°C. During deposition, the vaporized precursor liquid and oxidizer gases, consisting of O_2 and N_2O, are mixed and transported through a showerhead into the reaction chamber. The wafer is held at a temperature between 550°C and 700°C, and the total gas pressure is maintained at 0.5–1.0 Torr. The BSTO films are deposited at a rate of approximately 0.1 nm/s. The nominal composition of the BSTO films used in this study is $Ba_{0.65}Sr_{0.35}Ti_xO_3$, where x is slightly greater than unity, producing a Ti/(Ba + Sr) ratio of 1.02–1.05. The excess Ti is needed to produce BSTO films with low leakage. Film thickness and composition are measured by wavelength-dispersion X-ray fluorescence. The thickness nonuniformity is $<5\%$ across a 200-mm-diameter wafer, while the compositional

nonuniformity is within the accuracy of the WDXRF measurement at <0.25 at.%.

5. Microstructure of BSTO thin films

Two distinct microstructures are observed in the MOCVD-grown BSTO films. Examples of typical microstructures are shown in **Figure 8**. In Figure 8(a) the film has a strong (110) fiber texture, with the ⟨110⟩ directions aligned normal to the substrate. In this plan-view image it can be seen that many of the grain boundaries are inclined in the film and thus have an appreciable twist component to their grain-boundary structure. The grains also contain many (111) twin boundaries. In Figure 8(b) the film has a strong (100) fiber texture, with the ⟨100⟩ direction aligned normal to the substrate. In this image it can be seen that the grain boundaries lie almost normal to the substrate; the grain boundaries are thus predominantly tilt boundaries. In several instances the dislocation arrays that make up the tilt boundaries are clearly visible in the image. The grain sizes in the two microstructures are similar, with an average grain size of about 15 nm. Measurements of the grain size of films having different thicknesses and cross sections through the films show that grains grow in a columnar fashion, keeping an almost constant diameter [14].

Studies of microstructure development during early stages of deposition have shown that strong texture is present in the films even before BSTO grains have coalesced to form a continuous film. X-ray diffraction studies indicate that both (110) and (100) textures are present in the film at this stage of growth, and only in the later stages of film development does a dominant texture develop. This suggests that it is the factors that favor the preferential growth of one orientation over the other that control the final texture of the film. One proposal is that faceting of the BSTO on (100) planes could result in sideways spreading of the (110)-oriented grains, occluding the (100) grains. This would result in inclined grain boundaries in the film, as observed in the (110)-textured films. However, the processing factors that control the competitive growth between the two textures are poorly understood.

The underlying bottom Pt electrode has a strong (111) texture and a grain size of about 80 nm. Thus, many BSTO grains nucleate and grow on each Pt grain. Examination of the diffraction from individual grains shows that there was no preferred orientation relationship between the Pt and BST grains. High-resolution imaging of cross sections through the Pt BST interface shows that the BST perovskite lattice extends right up to the Pt grains, indicating that no intermediate phase formed at the electrode interfaces.

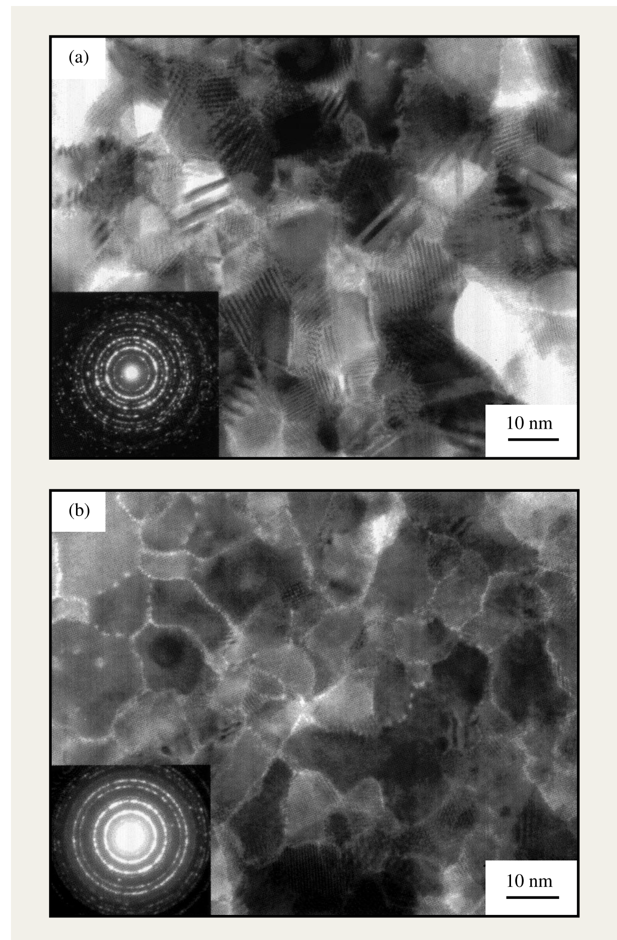

Figure 8

Plan-view TEM images of (a) (110)- and (b) (100)-textured 30-nm BSTO films.

Measurements of the capacitance of different MOCVD-grown films indicate that texture and microstructural differences have only a secondary effect on the permittivity of the films. Other factors such as composition, electrode heat treatment, and stress tend to dominate the variations in capacitance that are observed from film to film. Studies of fine-grained barium titanate have recently shown that the grain boundaries can act as low-dielectric-constant capacitive elements in series with the capacitance of the grains [15]. However, in the columnar grain structure produced by the MOCVD process, most grain boundaries lie perpendicular to the electrodes and hence do not act in series with the BSTO grains. The main factor reducing the capacitance of the thin films is the electrode interface capacitance, which results in strong thickness dependence to the effective dielectric constant of the films (discussed in Section 6).

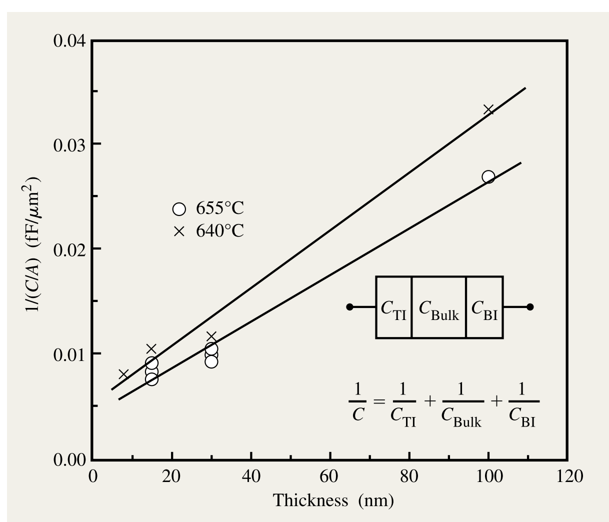

Figure 9

Plots of $1/(C/A)$ vs. thickness for MOCVD BSTO thin films deposited at substrate temperatures of 655°C and 640°C. The terms C_{TI} and C_{BI} respectively indicate top and bottom interfacial layer capacitance.

Leakage currents in the films are also dominated by the electrode interface properties. Small- and large-grained films show similar leakage currents. Grain boundaries in the films have only a minor effect on leakage. If anything, grain boundaries are thought to have the beneficial effect of depleting the grains of free charge and hence reducing the leakage of the films [15]. One effect of the grain structure that has been observed is that (100)-textured films show evidence of a time dependence to the leakage currents at high fields. This behavior is characterized by a steady decrease in leakage with time. In (110)-textured films, the effect is greatly reduced or absent. Preliminary studies of this phenomenon suggest that the time dependence is caused by charge trapping in the films, and it is possible that the effect grain texture has on this behavior is due to changes in trap density at the grain boundaries in the different films [16].

6. Electrical properties of BSTO thin-film capacitors

Before BSTO can be used as a storage-node dielectric in high-density DRAMs, electrical properties such as capacitance density, dielectric relaxation, leakage current, and resistance degradation must be characterized and understood. It may also be necessary to optimize the electrical properties by doping. Another important issue is determining the impact of these electrical properties, which differ from those found in conventional silicon oxide/nitride dielectrics, on DRAM performance.

- *Specific capacitance*

In addition to processing and microstructure considerations, the capacitance of BSTO thin films depends on film thickness, applied electric field, frequency, and temperature. **Figure 9** shows the capacitance density plotted as $1/(C/A)$ vs. thickness for MOCVD BSTO thin films deposited at substrate temperatures of 655°C and 640°C. Pt electrodes were used for the electrical measurements. The decrease in capacitance is well described by a model in which an interfacial capacitance acts in series with the bulk of the film. Such a model predicts a linear relationship of $1/(C/A)$ vs. thickness, with the intercept corresponding to the effective capacitance of the interface. This model is seen to hold for films as thin as 8 nm, indicating that any interfacial layer present is thinner than 4 nm. The capacitance density in thin films is limited by the interfacial capacitance, making it an important factor in obtaining high-capacitance-density thin films. The origin of the interfacial layer is not currently understood. TEM images of the interface rule out the possibility that a thin layer of low-permittivity material is formed at the interface. An interfacial capacitance could result from depletion layers formed at the Pt/BSTO Schottky barrier, but photoemission measurements by Copel et al. [18] indicate depletion depths of 70 nm for MOCVD BSTO films; thus, as proposed by Waser [19], the films in this thickness range are completely depleted. Mechanisms other than a series-connected capacitance, such as finite size effects and stress, can also give rise to the behavior shown in Figure 9. BSTO thin films are under a biaxial stress due to different thermal expansion coefficients between the film and electrodes [20–21] and intrinsic deposition stress. A biaxial tensile stress shifts the Curie temperature (T_c) to lower values. Increasing stress in thinner films would then result in decreasing capacitance density with decreasing film thickness. Measurements of the stress in BSTO thin films on Pt electrodes reveal that the observed shift in T_c, determined from extrapolation of the Curie–Weiss behavior, for different thicknesses of BSTO is greater than that expected on the basis of stress alone. The postulation of a series barrier capacitance, probably between electrode and film, is required to account for the data.[1] It has also been shown that residual porosity in the film cannot account for the large shift in T_c [22]. Such an interfacial layer may result from an intrinsic subpolarized layer ("dead layer") at the surface of a thin ferroelectric film [23], but further studies are needed to establish the precise cause.

[1] T. M. Shaw, J. D. Baniecki, and R. B. Laibowitz, unpublished results.

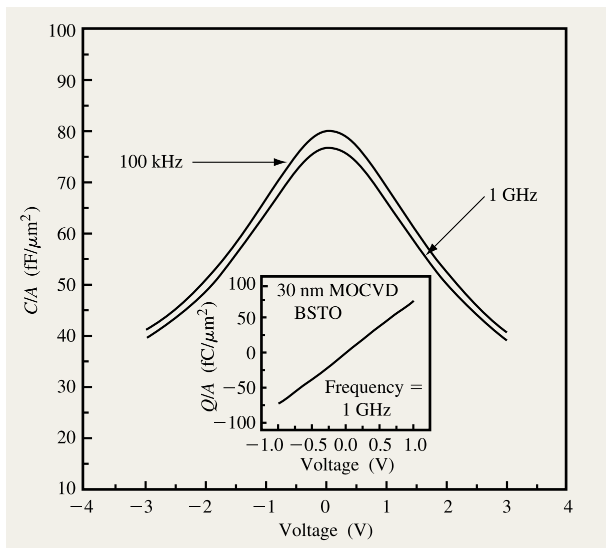

Figure 10

Capacitance density vs. voltage for 30-nm BSTO films with Pt electrodes at 100 kHz and 1 GHz. The inset shows the charge density vs. voltage obtained by integrating the small-signal *C–V* characteristic at 1 GHz.

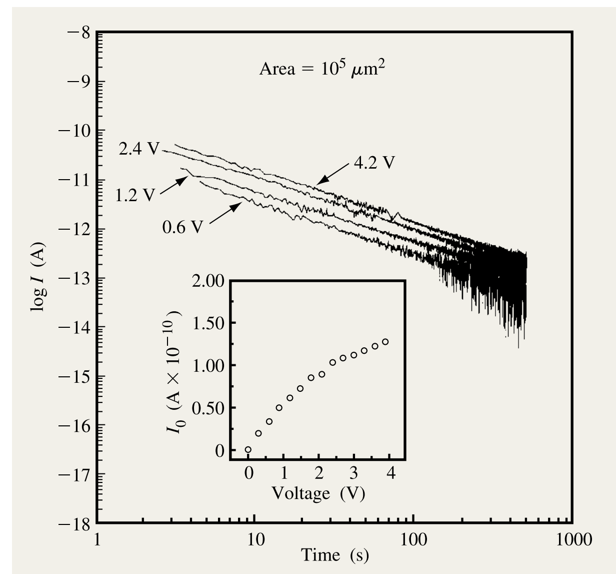

Figure 11

Depolarization currents *I* for 100-nm BSTO films with Pt electrodes. The inset shows the voltage dependence of the magnitude of the relaxation currents.

Figure 10 shows the capacitance density vs. voltage for 30-nm BSTO with Pt electrodes at 100 kHz and 1 GHz. The variation of capacitance with voltage is not a thin-film property, but an intrinsic property of the material resulting from the soft-phonon characteristics [24]. The field and temperature dependence of BSTO thin films is well described in terms of the Landau–Ginzberg–Devonshire theory of ferroelectrics [20]. Owing to the nonlinearity in capacitance, the available charge for DRAM applications is less than that determined at zero volts from the small-signal *C–V* characteristic. The available charge at a given capacitor voltage can be found by integrating the *C–V* characteristic, as shown in the inset in Figure 10. A slight nonlinearity is observed in the *Q–V* characteristic, resulting in less charge at a given voltage than would be obtained with a linear capacitor. For 30-nm MOCVD BSTO (assuming that V_{CC} = 2 V and half of V_{CC} is dropped across the capacitor) this results in about 4% less charge.

- *Dielectric relaxation*

In addition to an instantaneous dielectric response, BSTO thin films have a slow polarization component which follows a power-law dependence in both the time [$J_R(t) = J_0 t^{-n}$] and frequency ($C_T - C_\infty = C_0 f^{n-1}$) domains [25, 26]. **Figure 11** shows the depolarization currents for 100-nm MOCVD BSTO with Pt electrodes. A voltage step technique [27] was used to record the charging and discharging transients, with the voltage being stepped in 0.1-V increments. A subset of voltages is shown in the figure for clarity. As shown in Figure 11, the depolarization currents follow a power-law time dependence known as the Curie–von Schweidler law [28], with an exponent slightly less than 1. The power-law time dependence of the relaxation currents has been measured to times as short as 10 μs [26, 29]. The inset in Figure 11 shows the voltage dependence of the magnitude of the relaxation current after 1 s; for low voltages it is approximately linear, but a marked departure from linearity occurs at higher voltages. The relaxation currents are sensitive to doping [30], deposition temperature [31], annealing conditions [32], and stoichiometry [31]. Acceptor doping (Mn), lower deposition temperatures, and post-top-electrode annealing in forming gas (95% Ar 5% H_2) were shown to increase relaxation currents, while a decrease in the relaxation currents was observed for films with increasing Ti concentration. **Figure 12** shows the capacitance density and loss tangent for 30-nm MOCVD BSTO from 1 mHz to 20 GHz. The capacitance follows a power-law frequency dependence, as indicated by the dotted lines, over the entire measurement range. Because the frequency and time domains are related through Fourier transformation, the data in Figure 12 imply that

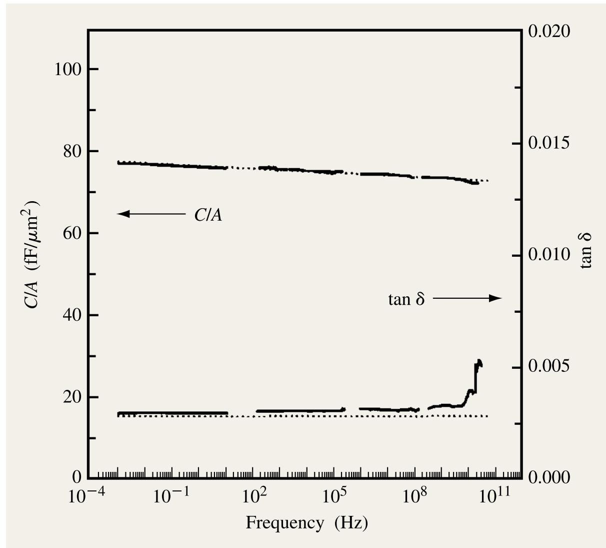

Figure 12

Capacitance density and loss tangent for 30-nm BSTO films from 1 mHz to 20 GHz.

the power-law relaxation currents extend back to the nanosecond regime of DRAM read/write pulses.

A power-law time dependence of polarization currents has been observed in a wide range of disordered solids, both crystalline and glassy [28]. Often the relaxation mechanism invoked to explain this behavior is the hopping of charge carriers between localized sites, where a distribution of hopping times, energies, or distances accounts for the distribution of relaxation times necessary for the power-law dependence. Localization of charge carriers can occur because of impurities, defects, disorder (Anderson localization), and electron–phonon coupling (polarons) [33]. The origin of localized charge carriers in BSTO thin films is currently under debate. Fukuda et al. [34] have proposed that electrons being thermally trapped/detrapped from oxygen vacancies (with a defect level of about 0.3 eV below the conduction band edge) in an interfacial depletion region is the origin of the phenomena. This explanation does not appear to apply to completely depleted MOCVD BSTO thin films, where the temperature dependence of the relaxation currents is different from that expected on the basis of thermal trapping/detrapping from a single defect level. Arrhenius plots of the magnitude of the relaxation currents reveal a break in the slope of $\log(J_R)$ versus reciprocal temperature. At high temperatures ($T \gtrsim 300$ K), activation energies of 0.3–0.76 eV as determined by the slope of the Arrhenius plot have been reported [31, 34, 35]; however, at low temperatures ($T \lesssim 300$ K) the activation energy drops to the meV range, and the relaxation currents persist down to 4.2 K [35]. Schumacher has suggested a model based on electronic hopping between localized states arising from impurity defects and disorder as the origin for the Curie–von Schweidler law in BSTO thin films [31]. At low temperatures the polarization currents result from hopping of carriers between localized states near the Fermi level, while hopping by carriers thermally excited into localized states near the conduction band edge occurs at higher temperatures.

- *Leakage*

Care must be taken when interpreting *I–V* data in BSTO thin films, since the slow polarization currents can mask the true leakage behavior. The best method of separating polarization and leakage currents is the use of a voltage step technique. The conduction mechanism for charge transport through metal–BSTO–metal thin-film capacitors is dominated by thermionic emission of electrons from the cathode [36]. This model is strongly supported by the dependence of the barrier height on the cathode metal work function and deposition conditions. The completely depleted nature of films less than about 140 nm leads to leakage currents that are relatively independent of film thickness. The temperature and field dependence for thermionic emission over a reverse-biased Schottky barrier are given by

$$J_L = A^*T^2 \exp\left(\frac{-W_B}{kT}\right) \exp\left(\frac{q}{kT}\sqrt{\frac{q}{4\pi\varepsilon}E}\right), \quad (1)$$

where A^* is the effective Richardson's constant, which incorporates carrier mobility, q is the electronic charge, ε is the permittivity (which may be different from the static permittivity), and k is Boltzmann's constant. If the conduction mechanism is thermionic emission, plots of $\log(J/T^2)$ vs. $1000/T$ and $\log(J)$ vs. $E^{1/2}$ yield straight lines. The barrier height, W_B, is then extracted from either the slope or the intercepts of the plots. **Figures 13(a)** and **13(b)** show the field and temperature dependence of the leakage current for as-deposited and annealed 30-nm MOCVD BSTO with Pt electrodes. The sample was annealed at 550°C for 15 minutes in O_2. In both films, as-deposited and annealed, good linear fits are obtained above a threshold voltage, even though the leakage through the films differs by as much as eight orders of magnitude. The leakage current at 1 V in the annealed film is 1.7×10^{-9} A/cm^2. Below the knee in the Schottky plot, the field dependence is approximately ohmic. Dietz and Waser [37] have reported a similar low-field behavior in $SrTiO_3$ thin films and used the more general quantum-mechanical charge injection model of Murphy and Good to predict both the low- and high-field behavior and to

extend the theory to cover all temperature ranges. The data in Figure 13 yield a barrier height of about 0.64 eV in the as-deposited state and 1.22 eV after a rapid thermal anneal at 550°C for 15 minutes in O_2. The lower barrier height in the as-deposited state may result from a high density of surface states in the as-deposited film, although further studies are needed to determine the precise cause. If the standard Schottky expression [Equation (1)] is used, parameters other than the barrier height extracted from the data analysis are typically unrealistic. As discussed by Simmons [38], the standard Schottky expression [Equation (1)] is valid for long electron mean free paths in the insulator. The condition of long electronic mean free paths in BSTO thin films may not be valid owing to a high density of surface states, traps in the film bulk, or strong electron–phonon coupling. A modified Schottky expression derived by Simmons, taking into account short mean free path, has been used which yielded better values for the Richardson constant and permittivity for sputter-deposited BSTO thin films on Pt electrodes [39]. The modified Schottky expression does not appear to yield better results for MOCVD BSTO thin-film capacitors with Pt electrodes after a post-top-electrode anneal in oxygen.[2]

- *Influence of dopants*

The electrical properties of BSTO thin films, such as leakage and resistance degradation, are significantly affected by the addition of dopants. Nominally undoped MOCVD BSTO thin films are n-type. The addition of lower-valence substitutions, such as Mn or Fe on Ti sites, compensates the charge density in undoped films, leading to greatly increased depletion depths. Higher-valence substitutions, such as La on Ba or Sr sites, act as donors. Small doses of Mn (<0.5 at.%) have been found to reduce leakage currents in BSTO thin films by up to an order of magnitude while increasing relaxation currents and dielectric loss only slightly. At higher doses, the leakage and relaxation currents were found to increase. There is also evidence that acceptor-doped films have an increased barrier to thermionic emission, which may explain the decrease in leakage observed in Mn-doped BSTO thin films [40]. The addition of donor (La) or acceptor (Mn, Fe) impurities to $SrTiO_3$ thin films leads to reduced resistance degradation [41].

- *Slow polarization as a charge-loss mechanism*

The slow polarization currents in BSTO thin films are a charge-loss mechanism that must be considered in addition to the dc leakage through the film [32, 42–44]. Only polarization components that are able to respond within the read/write times projected for future DRAMs

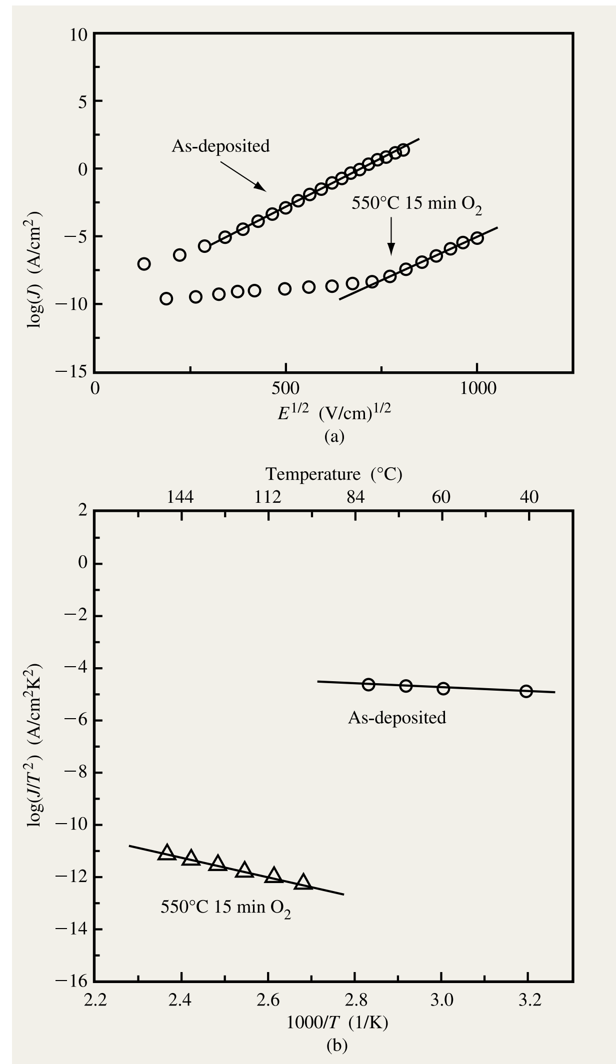

Figure 13

(a) Field dependence of the leakage current density for as-deposited and annealed 30-nm BSTO films with Pt electrodes at 23°C. The sample was annealed at 550°C for 15 min in O_2. (b) Temperature dependence of the leakage current density for as-deposited and annealed 30-nm BSTO films with Pt electrodes. The sample was annealed at 550°C for 15 min in O_2. A voltage of 1.4 V was applied to the as-deposited sample and 2.2 V to the annealed sample.

($t_{write} \approx t_{refresh} \leq 10$ ns) result in usable charge storage. Polarization components that cannot respond within the read/write time result in charge loss. The greatest charge loss due to the relaxation currents occurs during the first read after a refresh time following a write to the opposite state for a capacitor that has been written to the same state for many refresh cycles (steady state) [44]. This can be estimated by calculating the ratio of usable free charge

[2] J. D. Baniecki, R. B. Laibowitz, and T. M. Shaw, unpublished results.

Table 5 Worse-case charge loss due to the relaxation currents for BSTO films with thicknesses of 15, 30, and 100 nm, assuming $V_{CC} = 2$ V, $t_{write} = 10$ ns, and $t_{refresh} = 1$ s. The value of C_{HF}/A is that at $f = 1/t_{write} = 0.1$ GHz and is 4% smaller than that measured at 0 V, owing to the nonlinearity of the C–V characteristic (see Figure 10).

BSTO thickness (nm)	a $(\mathrm{fF}/\mu\mathrm{m}^2)\mathrm{s}^{n-1}$	n	C_{HF}/A $(\mathrm{fF}/\mu\mathrm{m}^2)$	Q_{lost} (%)
100	0.14	0.99	40.41	10.9
30	0.26	0.99	80.01	10.3
15	0.21	0.99	92.39	7.3

(free charge on the capacitor plate that has not been compensated by slow polarization currents) after a refresh time, to the initial usable charge just following the opposite-state write [32]:

$$\%\, Q_{lost} \approx \frac{2a[(t_{refresh})^{1-n} - (t_{write})^{1-n}]}{C_{HF}(1-n) + a[(t_{refresh})^{1-n} - (t_{write})^{1-n}]} \times 100, \quad (2)$$

where a and n are the magnitude and exponent of the power-law relaxation current defined by $J_R(t) = aVt^{-n}$, and C_{HF} is the capacitance per unit area measured at a frequency of $1/t_{write}$. For $t_{write} \le 10$ ns, this frequency is in the low microwave region. In deriving Equation (2), the capacitor has been assumed to be perfectly isolated, and the leakage currents through the film have been neglected. In addition, the relaxation currents are assumed to be linear. **Table 5** shows the charge loss due to the relaxation currents for MOCVD BSTO capacitors with film thicknesses of 100, 30, and 15 nm, assuming $V_{CC} = 2$ V, $t_{write} = 10$ ns, and $t_{refresh} = 1$ s. It is important to note that the calculated charge loss due to dielectric relaxation is for large (10^4 $\mu\mathrm{m}^2$) planar capacitors and may not reflect the charge loss for submicron stack BSTO capacitors in actual DRAM circuits. It is interesting to compare the loss due to the relaxation currents to that due to leakage. For 30-nm MOCVD BSTO capacitors, the steady-state leakage is in the range of 10^{-9}–10^{-8} A/cm^2. The voltage drop (proportional to charge loss) can be estimated by $\Delta V \approx J\Delta t/(C/A)$, which gives a drop of 0.0125%–0.125% for $V_{CC} = 2$ V and $C/A = 80$ fF/μm^2, with a refresh time Δt of 1 s. This is well below the 7–10% worst-case charge loss due to dielectric relaxation.

- *Reliability issues*

In addition to a high capacitance density and low leakage, a BSTO thin-film capacitor must be reliable. There are various failure modes possible for BSTO thin-film devices, including time-dependent dielectric breakdown (TDDB) and resistance degradation. Most experimental studies show that the onset of resistance degradation occurs before TDDB [45–47]. Resistance degradation is a slow increase in leakage under a prolonged dc voltage stress [48–50] and is influenced by parameters such as doping, stoichiometry [51], and grain size [52]. The predicted lifetimes reported in the literature vary, but recent data on MOCVD BSTO thin films predict lifetimes ≫ ten years for 24-nm films under the operating conditions of 85°C and 1.6 V. For DRAM applications, the voltage stress conditions on the capacitor are dynamic rather than static; thus, the reliability of the material should be tested under dynamic stress conditions. Horikawa et al. [47] have reported that the degradation in BSTO thin films is greater under a bipolar voltage stress than under a dc stress, and therefore bipolar stress conditions should be used to evaluate BSTO reliability. The estimated breakdown time for 30-nm MOCVD BSTO under a bipolar voltage stress under the operating conditions of 85°C and 1 V was reported to be in excess of ten years.

7. Conclusions

Much progress has been made in the development of processes for generating high-quality dielectric films of BSTO, and in the development of suitable electrode and barrier materials needed for integrating the BSTO dielectric in a DRAM capacitor. Planar capacitors of BSTO with Pt electrodes have been fabricated with a specific capacitance greater than 90 fF/μm^2 and a total charge loss of less than 10% after 1 s. Though the interrelationships among the details of the process parameters and integration sequence, the microstructure of the BSTO films, and the mechanisms which affect the specific capacitance and charge loss of a BSTO capacitor are becoming better understood, additional work is required to refine and optimize the details of the processes and integration scheme to achieve three-dimensional stacked-capacitor structures which meet the performance objectives for future generations of DRAM. Particular emphasis must be placed on elimination of interfacial layers, reduction of defects caused by plasma processing and hydrogen annealing after BSTO capacitor formation, and a more detailed investigation of the reliability of stacked-capacitor structures with a dielectric of BSTO.

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