Plasma processing damage in etching and deposition

by S. J. Fonash

Plasma-based etching and deposition are key processes in macroelectronics and microelectronics. The energetic species, the time-changing magnetic fields, and the fluxes inherent in these processes give them their flexibility and functionality but also their potential for process damage. The basic causes of the damage are 1) process-induced current flow and 2) direct exposure to the plasma. The impact of plasma-based etching and deposition damage is very much dependent on process flow as well as on device and circuit layout.

Introduction

Plasma etching and deposition are basic tools in the fabrication of the large-area thin-film structures of macroelectronics and the submicron structures of microelectronics. Plasma-based etching allows the attainment of both selective and anisotropic processing in subtractive steps; plasma-based deposition allows the attainment of film stoichiometry and morphology control in additive steps. In both plasma-based etching and deposition, electromagnetic energy rather than thermal energy creates energetic atoms and radicals. In addition, plasma–substrate voltage differences can be set up, thereby creating charged-particle fluxes for anisotropy control in etching and film morphology control in deposition. This presence of both highly reactive species and bombarding fluxes in plasma-based processing makes possible the creation of reaction paths for highly tailored subtractive or additive functions even at relatively low temperatures.

While plasma-based processing enables relatively low-temperature, versatile etching and deposition, its use requires careful consideration of the full process flow and of device and circuit layout. This is necessary because plasma-based processing can produce damage that can be exacerbated or mitigated by subsequent processing and by device and circuit design. The various types of damage which are possible with plasma-based processing are listed in **Table 1**. They can be broadly classified as 1) impurity contamination from residual reaction products; 2) impurity contamination of semiconductors and dielectrics from plasma species permeation; 3) bonding disruption in semiconductors and dielectrics due to photon and particle bombardment; and 4) current damage due to charging and induced EMF currents [1].

As indicated in Table 1, the basic cause of damage in all of these cases is either 1) current flow due to charging or induced EMFs or 2) direct exposure to the plasma with

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Table 1 Potential damage inherent in plasma-based processing.

Damage type	*Basic cause*	*Present in etching or deposition*	*Materials affected*
Residue contamination	Exposure to plasma	Usually only in etching due to reaction by-products remaining on surfaces	All
Plasma-caused species permeation	Exposure to plasma	Both	Dielectrics and semiconductors
Bonding disruption	Exposure to plasma Particle and/or photon bombardment	Both	Dielectrics and semiconductors
Current flow damage	Current flow during plasma processing due to charging or induced EMFs	Both	Dielectrics

Table 2 Impact of processing flow and of device and circuit layout.

Impact category	*Plasma damage type affected*	*Example*
Processing flow—passivation	Bonding disruption due to bombardment Wear-out damage	Hydrogen released in subsequent processing such as a postmetallization anneal or a hydrogen-laden plasma step can passivate damage
Processing flow—activation	Bonding disruption due to bombardment Current flow damage	Charging current of a subsequent plasma-based step can activate dielectric damage passivated in an earlier step
Processing flow—cumulative effects	Bonding disruption due to bombardment Current flow damage	Dielectric current flow damage of a plasma-based step can augment current flow damage of an earlier plasma-based step
Layout—antenna effects	Current flow damage	Interconnects can collect charge that must pass through a dielectric to dissipate
Layout—EMF loop effects	Current flow damage	Interconnect loops can induce EMFs from time-changing magnetic fields, thereby setting up currents across dielectrics
Layout—edge effects	Bonding disruption due to bombardment Current flow damage	Device edge exposure to plasmas can cause damage due to bombardment and/or increased current flow damage arising from edge conduction

its highly reactive species and bombarding particles and photons. Processing flow and device and circuit layout very strongly influence the impact of the potential damage effects seen in Table 1. This synergism is outlined in **Table 2**. Here the impact of processing flow on plasma-based etching and deposition is divided into three categories: passivation effects, activation effects, and cumulative effects. Passivation effects can be particularly insidious because they can mask damage which can then later affect reliability [2, 3]. The impact of layout can also be divided into three categories: antenna effects, EMF loop effects, and edge effects, as noted in Table 2.

Residue contamination

This form of damage is found in plasma-based etching processes and arises from the presence of etching reaction products that remain on exposed surfaces. The reaction product residues may be purposely or inadvertently present. In the former case they may be designed into the process, e.g., to create anisotropy by covering sidewalls during the etching. In the latter case they may be present because of inefficient reaction product removal or inadvertent chemical attack, such as etching of masking photoresist.

Process flow is very important in handling residues. Subsequent processing must be tailored to include their

removal, as necessary. Prior processing steps must be tailored to enhance or mitigate against their presence, as necessary.

Plasma-caused species permeation

Exposure to a plasma can also result in the inadvertent permeation of dielectrics and semiconductors by plasma-related species. One example of this is permeation of dielectrics and semiconductors by hydrogen during plasma exposures [4]. This hydrogen permeation can, in some cases, increase dielectric/semiconductor defect densities [5], while in other cases it can decrease them. The latter possibility is exploited in plasma-based hydrogenation of polysilicon [6]. Another example of permeation is found in studies that have demonstrated that interstitials and vacancies can be generated at surfaces undergoing etching and then diffuse into the substrate below [1].

Depending on the species involved, permeation may or may not lead to problems. As noted in Table 2, the impact of permeation can depend very much on process flow and on layout. For example, inadvertent hydrogen permeation resulting in passivation of defects can be a problem if it causes the presence of damage to go unobserved [2], or if subsequent thermal or plasma processing can modify the state of this hydrogen, resulting in depassivation and even enhanced damage [5]. Layout can affect the state of this hydrogen because hydrogen-passivated defects can be reactivated by electrical stressing currents produced in subsequent processing or in device operation. Layouts causing large currents during plasma processing due to effective "antenna" charge collection from interconnects [1–3] or due to time-changing magnetic-field-induced EMFs in interconnect loops [7] are detrimental.

Bonding disruption

Inadvertent bonding disruption in dielectrics and semiconductors due to plasma particle and/or photon fluxes can occur during etching or deposition, as noted in Table 1. Such damage can cause gap states in semiconductors that affect lifetimes and band bending [1, 4]; it can cause fixed charge and traps in dielectrics [1–3, 5].

As indicated in Table 2, process flow and layout can affect the impact of bonding disruption damage. Hydrogen permeation during the offending plasma processing step or a subsequent one can passivate bonding damage in dielectrics and semiconductors, giving the illusion that such damage is not present. However, the damage can be present and passivated and perhaps latent (i.e., not cured but easily reactivated). If passivation occurs, it may be undone in another plasma-based step (because of current flow stressing) or thermal processing step. It may also be undone by stress during device operation [1, 5].

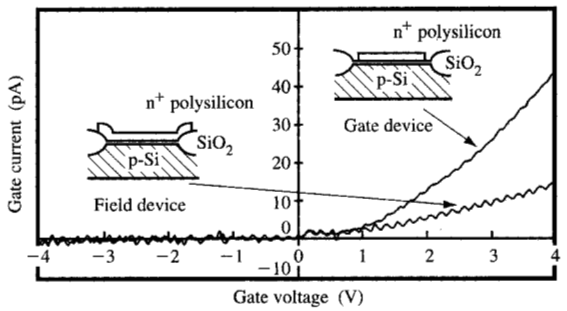

Figure 1

Current–voltage characteristics of capacitors on p-type silicon substrates. Higher generation currents were observed at positive gate voltages (depletion) for the "gate device" capacitor because of the "edge-type" damage. The capacitors had the same area ($10^5\ \mu m^2$) and oxide thickness (70 Å). The technique of [10] is used to elucidate generation current.

Current damage

It is well known that dielectrics degrade (wear out) when subjected to high-density currents. Such degradation is a type of dielectric bonding disruption caused by current flow through these materials [1]. We use the term "current damage" here to characterize this degradation as it occurs in plasma-based processing [8]. The dielectric can be exposed directly to the plasma-caused current. However, this is not necessary. The dielectric could be protected from direct exposure but forced to carry the charging current collected by some antenna or to carry the EMF-induced current set up by some loop in the layout.

Obviously, layout has a considerable effect on this type of damage, since it affects the current-density stress levels experienced by dielectric layers. Processing flow has an equally important impact on this type of damage. For example, damage from dielectric current flow can be passivated by hydrogen. However, it has been shown that such damage is only rendered latent; it can subsequently be activated by another current stress or even by some forms of thermal cycling [9]. The layout of device edges on active area can also affect dielectric current flow damage. For example, **Figure 1** shows the current–voltage characteristics observed for capacitors on p-type silicon substrates having the same gate oxide area, but with the edges defined on the field oxide (field devices) or the gate oxide (gate devices). The voltage used was a step-ramp and the current shown was that measured at a fixed sampling time after each step [10]. It can be seen that the transient gate current at positive voltages (depletion) was larger in the gate devices; this is due to higher generation currents due to the "edge-type" damage. The damage

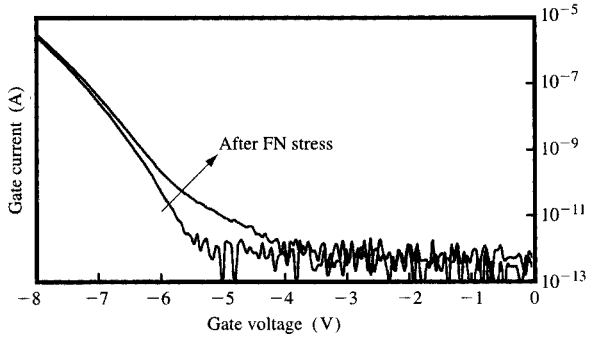

Figure 2

Stress-induced leakage currents (SILC) observed after high-field FN stressing of a nonvolatile memory device having a 70-Å-thick oxide. The indicated degradation may have resulted from current-induced damage during processing.

results from the direct exposure of the gate oxide at the device edges during the polysilicon-gate-etching step, in contrast to field devices, in which only the current damage is possible [10].

Current damage can also cause stress-induced leakage currents (SILC), which are one of the main reliability concerns in nonvolatile memory devices that use tunnel oxides [11]. Such an increase in leakage current in the medium-gate-field range is shown in **Figure 2** for a 70-Å-thick oxide sample after Fowler–Nordheim (FN) stressing. Soft breakdown (or quasi-breakdown) also comes into play in the ultrathin oxide regime, again due to current flow damage [12, 13]. This phenomenon is observed as additional noise in the current–voltage characteristics and the deviation of the oxide currents from the "intrinsic" level [14] at low fields.

Conclusions

Plasma-based processing damage is currently of serious concern in macroelectronic and microelectronic processing. Its seriousness will only increase as interconnections become more complex and new materials become more prevalent in both macroelectronics and microelectronics. Of special concern will be the impact of plasma processing on organic materials, on low-dielectric-constant insulators, and on stacked-gate dielectrics. Organic LED materials require careful consideration of plasma-processing sequencing. Several low-dielectric-constant insulators of current interest are either organics or porous materials. In the latter case, permeation can be of particular concern. Stacked dielectrics will probably involve the deposition of at least one high-dielectric-constant material. This deposition may have to be a plasma-deposition step, necessitating great care to avoid damaging other constituents of the stack.

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