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Safe Operating Area for Bipolar Transistors

Abstract: A mathematical model is utilized to predict the safe operating area (SOA) for proper circuit applications of bipolar transistors in the forward as well as reverse operating regions. Nonuniformity of the temperature within the transistor structure due to internal self-heating and the avalanche multiplication effect in the reverse operating region, which cause second breakdown failure, are taken into account. Steady-state electrical and time-dependent thermal problems are solved to establish stability of a specified operating condition. Safe operating area curves for three transistor designs of similar power handling capability are presented. Current density and temperature distributions within the transistor structure for various operating conditions in the stable as well as unstable regions are presented. Suitability of V_{BE} to estimate peak temperature within the device is discussed.

Introduction

The operation of bipolar transistors in high-power circuits is limited, due to second breakdown failure mode in both forward ($I_B > 0$, $V_{CE} < BV_{CE0}$) and reverse ($I_B < 0$, $BV_{CE0} \leq V_{CE} \leq BV_{CB0}$) operating regions. For many switching applications of n-p-n^--n^+ power transistors, second breakdown failures have been observed in turn-on as well as turn-off transients where the device is subjected to high-voltage high-current operating conditions for part of the switching time. Avalanche multiplication in the collector region and the nonuniformity of the temperature within the transistor structure are believed to be causes of second breakdown [1–4]. By use of a two-dimensional mathematical model, which includes avalanche multiplication and internal self-heating effects, the internal behavior of a high-voltage power transistor design has been obtained by the author [3–5] for various operating conditions of the transistor. This detailed numerical solution of Poisson's equation, electron and hole continuity equations, and the heat flow equation for a transistor design (without assuming internal junctions and other conventional approximations) has provided a clear understanding of the electrical and thermal stresses within the device that cause second breakdown failure at high-voltage high-current operating conditions. However, due to the complexity of the model, the computational cost is rather high.

This paper [6] presents a technique for predicting the safe operating area (SOA) for transistor applications in forward as well as reverse operating regions by a two-dimensional analysis that is somewhat simpler than that described in [3–5]. Only the thermal mode second breakdown is treated in this paper. The parameter which is used to establish stability of an operating point in the forward or reverse region is the temperature distribution in the base of the transistor. A distributed model of the transistor, similar to one introduced by Ghosh [7], has been developed and used by Navon and Lee [8] and Gaur et al. [9] to obtain nonuniform current density and temperature distributions within p-n-p power transistor structures, and the effect of design parameters on second breakdown in the forward operating region has been predicted [9]. This paper modifies that analysis [9] for n-p-n^--n^+ high-voltage power transistor structures and includes the effect of avalanche multiplication [10] when analyzing transistor operation in the reverse as well as forward operating regions. Steady-state electrical and time-dependent thermal problems, which are described in the following section, are solved to establish the stability of specified operating conditions (V_{CE}, I_C or V_{CE}, V_{BE}) for a specific transistor design. An iterative procedure is used to obtain compatible current density and temperature distributions within the device. For a given operating condition, a stable solution is obtained, or the temperature and current density increase beyond bound, indicating unstable behavior. The SOA curve is obtained by considering a number of points on the V_{CE}, I_C plane and by drawing a boundary between the stable and unstable points. Additional boundaries are drawn in the unstable region corresponding to different time values, so that the operating points on the left of a boundary are stable for a time interval shorter than the specified time.

SOA curves for three different power transistors of similar power handling capability are presented for their circuit applications in both forward and reverse operating regions. The computation time required to establish the stability of one operating point is about two to three minutes on an IBM 370/168 computer. Both current density and temperature distributions within these transistors, for various operating conditions in the stable region, are presented. For unstable operating points, the

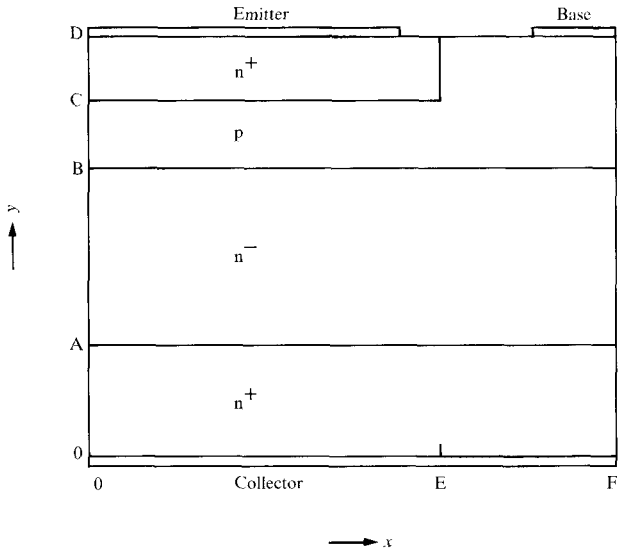


Figure 1 Two-dimensional n-p-n^--n^+ transistor structure.

current density and temperature distributions are sketched at various time intervals to illustrate their localization before failure. Variations of both peak temperature within the device and external base-emitter voltage with time are presented for stable as well as unstable operating points; use of V_{BE} to estimate peak temperature within the device [11–13] is discussed. The effect of temperature drop in the package of a transistor on its SOA is also illustrated.

As mentioned earlier, the stability of specified operating conditions is established by solving steady-state electrical and time-dependent thermal problems. Therefore, this model is applicable to the analysis of transistor failures occurring after a delay time greater than about 0.1 μs. Analysis of failures occurring in a time period of the order of nanoseconds would require solution of the time-dependent electrical transport equations. The criterion of instability in this analysis is based on the temperature distribution in the base region of the transistor. Localization of current density and temperature cause transistor failure in forward and reverse operating regions. Device failure is indicated when the temperature reaches a value such that silicon becomes intrinsic. To analyze second breakdown failure occurring in a time period of the order of nanoseconds (current mode second breakdown), a criterion for failure may be based on the carrier concentration distribution in the lightly doped n^- collector region. In their analysis, Koyanagi et al. [14] indicate that current mode second breakdown failure occurs when the mobile electron concentration at the collector n^--n^+ interface becomes equal to the doping of the n^- region. The present analysis excludes this second breakdown failure mode. Therefore, the predicted SOA in the reverse operating region is on the optimistic side. Current mode second breakdown has been reported to be the dominant triggering mechanism in the reverse operating region [1], and occurs at a voltage less than breakdown voltage due to thermal effect [14].

As described in detail in the following section, the change in the electric field distribution in the lightly doped collector region of the transistor with increasing current levels [4, 14] is approximated by three idealized cases to simplify the calculations as compared to the analysis of [4]. Also, in this analysis the temperature at the base-collector junction is assumed to be identical to the temperature at the emitter-base junction, and the internal heat generated within the transistor is assumed to occur mainly at the base-collector junction. In switching applications of n-p-n^--n^+ high-voltage power transistors in circuits with inductive loads, internal heat generated at the n^--n^+ interface may be higher than the heat generated at the base-collector junction [15] for certain operating conditions. The SOA curve is generated by a point-by-point stability analysis of the V_{CE}, I_C operating points. The applicability of this model to analysis of the stability of time-varying voltage and current operating conditions is discussed in the results and discussion section. The effect of the third dimension (variation of current density and temperature along the length of the emitter fingers) can also be incorporated by considering a variable emitter active area which changes with voltage and current operating conditions.

Theory

The internal behavior of multi-emitter high-voltage power transistor designs is obtained by analyzing the two-dimensional region shown in Fig. 1. Only half of an emitter finger is analyzed, on the assumption that all the emitter fingers are identical, and the variation in electrical parameters along the length of the emitter finger is ignored. The stability of any specified operating condition (V_{CE}, I_C or V_{CE}, V_{BE}) is established by solving the steady-state electrical and time-dependent thermal problems.

• *Electrical model*

The set of mathematical equations governing the internal behavior of bipolar transistors is listed in [4]. This set of equations is solved in the base region of the transistor shown in Fig. 1 by using a distributed model [8, 9] of the transistor. The two-dimensional region of Fig. 1 is represented by a number of one-dimensional transistors separated by resistors as shown in Fig. 2. The value of each resistor is inversely proportional to the modulated conductivity of each increment [9]. The transverse potential

drop in the base region from the emitter center to the emitter edge is obtained by summing the incremental voltage drops across the resistors [8, 9], which are given as

$$\Delta V = m\, I_R R, \tag{1}$$

where m is a fraction of the transverse base current that is drift current. The results of a two-dimensional analysis have shown that the emitter crowding predicted by the distributed model is much greater than the crowding predicted by the two-dimensional model (providing the transverse base current is assumed to be completely drift current). By taking into account the diffusion component of the transverse base current as shown in Eq. (1), the discrepancy between the emitter crowding predictions of the two models is very small [16].

The term m in Eq. (1) is given by

$$m = \frac{J_{hx}\ \text{drift}}{J_{hx}} \tag{2}$$

$$= \frac{n(x, C) + p_0}{2\, n(x, C) + p_0}, \tag{3}$$

where J_{hx} is the transverse hole current density in the base region, $n(x, C)$ is the electron concentration at the emitter-base junction, and p_0 is the equilibrium hole concentration in the base region. The term I_R in Eq. (1) is the current flowing in the resistor of value R. Electron concentration $n(x, C)$ is obtained as follows:

$$n(x, C) = \left(\frac{n_i^2}{p_0}\right) \exp\left(\frac{qV_J}{kT}\right), \tag{4}$$

where n_i is the intrinsic carrier concentration. The temperature dependence of n_i for silicon is as follows [5]:

$$n_i(T) = 3.88 \times 10^{16} T^{1.5} \exp(-7000/T). \tag{5}$$

The term V_J in Eq. (4) is the base-emitter junction voltage and T is the temperature. The longitudinal electron current density in the base region for each one-dimensional transistor is given by

$$J_{ey} = qD_e n(x, y)\, \frac{\partial}{\partial y} \ln[p(x, y)\, n(x, y)], \tag{6}$$

where D_e is the electron diffusion coefficient. Equation (6) is further simplified by assuming a linear distribution of electrons in the base region and quasi-neutrality approximation [8, 16].

The base current per unit length along the emitter width for each one-dimensional transistor is composed of three terms:

$$I_b = I_{be} + I_{br} - I_g, \tag{7}$$

where I_{be} is the portion of the base current per unit length due to holes injected into the emitter, and is given by the expression [16]

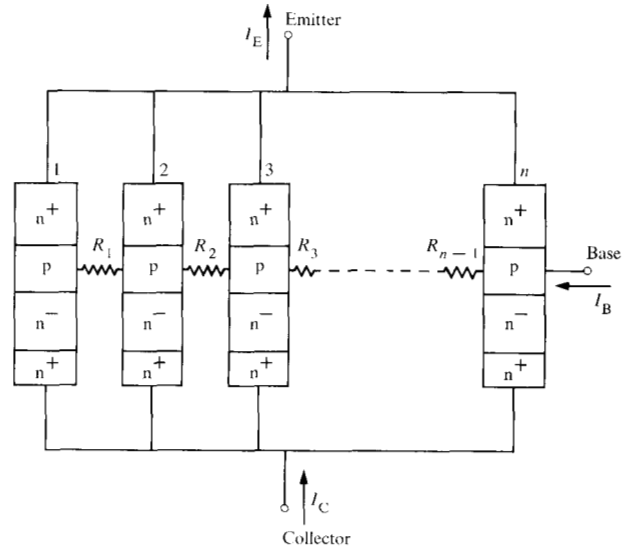


Figure 2 Distributed transistor model.

$$I_{be} = \Delta x\, q\, d_{he} p(x, C)\ n(X, C) / n_{e0} L_{he}, \tag{8}$$

where Δx is the width of each increment in the base, D_{he} is the diffusion coefficient for holes in the emitter, n_{e0} is the equilibrium electron concentration in the emitter, L_{he} is the diffusion length of holes in the emitter [$L_{he} = (D_{he}\tau_h)^{\frac{1}{2}}$], τ_h is the hole lifetime in the emitter, and $p(x, C)$ is the hole concentration at the emitter-base junction. Einstein's relation [$D_e/\mu_e = D_h/\mu_h = kT/q$] is assumed valid to relate diffusion coefficients and mobilities. The term I_{br} in Eq. (7) is the portion of the base current per unit length due to hole recombination with electrons in the base region, and is expressed as follows [16]:

$$I_{br} = W_B \Delta x\, q\, n(x, C)/2\tau_e, \tag{9}$$

where τ_e is electron lifetime in the base and W_B is the electrical base thickness. Term I_g in Eq. (7) is the portion of the base current per unit length due to holes injected into the base from the collector region resulting from avalanche multiplication. Generation of carriers depends on the electric field and current density, and the avalanche-generated current density can be written as [10]

$$J_g = \int J_{ey} \alpha_n \exp(-b/|E|)\, dy, \tag{10}$$

where α_n is the ionization coefficient, b_n the critical field, J_{ey} the longitudinal electron current density, and E the electric field. Values of α_n and b_n used are as follows [10]:

$\alpha_n = 2.4 \times 10^6\ \text{cm}^{-1}$, and

$b_n = 1.6 \times 10^6\ \text{V/cm}$.

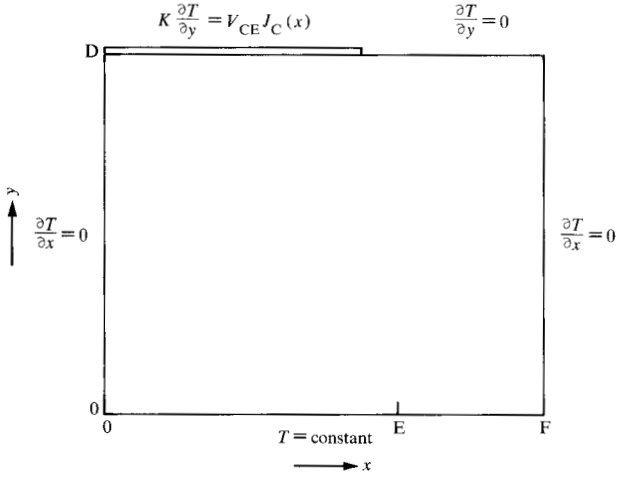


Figure 3 Region of analysis with assumed boundary conditions for the time-dependent heat flow problem.

The electric field distribution in the n^- collector region changes with current and voltage operating conditions [3, 4], and is approximated by one of the following three idealized cases:

1. A linear distribution of the electric field with a maximum value at the base-collector junction and a zero electric field at the n^--n^+ interface. Avalanche-generated current density for this electric field distribution can be approximated as [10]

$$J_g = \frac{J_{ey}\alpha_n E_m Y_c}{b_n} \exp\left(\frac{-b_n}{E_m}\right), \tag{11}$$

where E_m is the magnitude of the electric field value at the base-collector junction, given as

$$E_m = \left(\frac{2qN_0V_{CB}}{\varepsilon}\right)^{\frac{1}{2}} \left(1 - \frac{J_{ey}}{qv_sN_0}\right)^{\frac{1}{2}}, \tag{12}$$

and Y_c is the distance from the base-collector junction to a point of zero electric field in the n^- collector region ($Y_c < W_c$, the n^- collector thickness). It is expressed as [10]

$$Y_c = \left(\frac{2\varepsilon V_{CB}}{qN_0}\right)^{\frac{1}{2}} \left(1 - \frac{J_{ey}}{qv_sN_0}\right)^{-\frac{1}{2}}. \tag{13}$$

V_{CB} is the collector-to-base applied voltage, v_s is the saturated velocity of carriers, and N_0 is the doping of the n^- collector region.

2. A constant electric field of magnitude E_m from the base-collector junction to the n^--n^+ interface. Avalanche-generated current density can be written as

$$J_g = J_{ey}\alpha_n W_c \exp\left(\frac{-b_n}{E_m}\right), \text{ and} \tag{14}$$

$$E_m = V_{CB}/W_c, \tag{15}$$

where W_c is the n^- collector thickness.

3. A linear distribution of the electric field with zero value at the base-collector junction and a maximum value E_m at the n^--n^+ interface. Avalanche-generated current density for this case can be written as

$$J_g = \frac{J_{ey}\alpha_n W_c E_m}{b_n} \exp\left(\frac{-b_n}{E_m}\right), \text{ and} \tag{16}$$

$$E_m = 2V_{CB}/W_c. \tag{17}$$

Present analysis does not include the base widening effect with increasing current level of operation which depends on the doping and thickness of the n^- collector region and causes the electric field localization at the n^--n^+ interface [3, 4]. The total collector current density for each one-dimensional transistor is given by

$$J_c = J_{ey} + (\beta + 1)\, J_g, \tag{18}$$

where

$$\beta = \frac{\Delta x J_{ey}}{I_{be} + I_{br}}. \tag{19}$$

•• *Thermal model*

Internal self heating is taken into account by solving the heat flow equation

$$\nabla \cdot K\nabla T + Q = \rho C_p \frac{\partial T}{\partial t}, \tag{20}$$

where K is the thermal conductivity, Q is the heat generated per unit volume, ρ is the mass density and C_p is the specific heat. Figure 3 shows the region of analysis for the heat flow equation with assumed boundary conditions. Temperature along $y = 0$ in Fig. 1 is assumed to be a constant. Lines $x = 0$ and $x = F$ in Fig. 1 are assumed to be lines of symmetry and there is no heat flow across them. Heat generated due to reverse biased collector-to-base voltage is represented by the boundary condition along $y = D$, from $x = 0$ up to $x = E$. Along $y = D$ from $x = E$ to $x = F$, $\partial T/\partial y = 0$, assuming that no heat is radiated or convected from the emitter surface.

The finite difference method is used to solve Eq. (20) for the region of analysis shown in Fig. 3. Discrete representations of Eq. (20) at every node, with four neighbors, of a square grid of spacing h gives the following explicit formulation of the finite difference method [9]:

Table 1 Device design parameters.

Parameter	*Device A*	*Device B*	*Device C*
Base thickness (μm)	12.5	18.0	28.8
Collector thickness (μm)	33.5	45.5	102.0
Emitter width (μm)	177.8	127.0	101.6
Chip thickness (μm)	203.2	228.6	177.8
Emitter area (cm^2)	0.0432	0.0692	0.1429
Emitter doping (cm^{-3})	1.0×10^{20}	1.0×10^{20}	2.0×10^{20}
Base doping (cm^{-3})	1.15×10^{16}	1.5×10^{16}	2.0×10^{15}
Collector doping (cm^{-3})	1.8×10^{14}	1.5×10^{14}	8.0×10^{13}
Electron lifetime in base (s)	1.0×10^{-6}	1.0×10^{-6}	1.0×10^{-6}
Hole lifetime in emitter (s)	2.0×10^{-9}	2.0×10^{-9}	2.0×10^{-9}
Hole mobility in base ($cm^2/V \cdot s$)	385.4	375	496
Electron mobility in base ($cm^2/V \cdot s$)	925	900	1250
Hole mobility in emitter ($cm^2/V \cdot s$)	15	15	10

$$T(x, y, t + h_t) = \frac{4}{M(K_1 + K_2 + K_3 + K_4)} \times [K_1 T(x - h, y, t) + K_2 T(x + h, y, t) + K_3 T(x, y - h, t) + K_4 T(x, y + h, t)] + [1 - (4/M)]\, T(x, y, t),$$

where

$$M = \frac{4\rho C_p h^2}{h_t(K_1 + K_2 + K_3 + K_4)}. \quad (22)$$

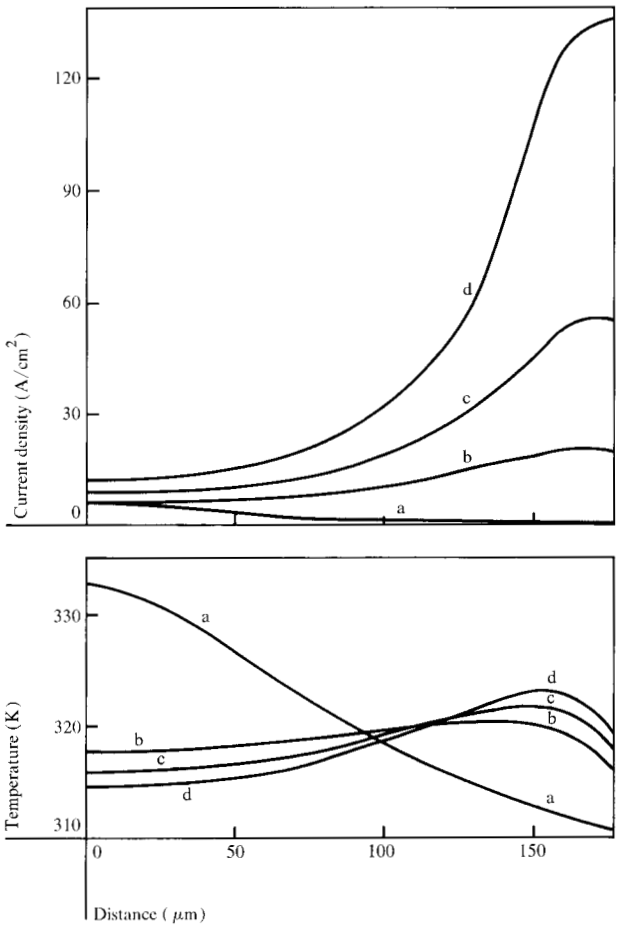
The temperature dependence of the thermal conductivity for silicon is approximated by the expression [5]

$$K = 3110/T^{1.33}\ (\mathrm{W/cm \cdot K}). \quad (23)$$

Term K_1 is the thermal conductivity at $[T(x - h, y) + T(x, y)]/2$, K_2 is the thermal conductivity at $[T(x + h, y) + T(x, y)]/2$, etc. The value of spatial interval h is specified, and the time interval h_t is chosen such that the coefficient $[1 - (4/M)]$ in Eq. (21) is always positive.

At time $t = 0$, collector current density for each one-dimensional transistor is calculated assuming a constant temperature T_0. The values of emitter-base junction voltages V_J are adjusted such that the total collector current of the device I_C or the external base-emitter voltage V_{BE} correspond to the specified operating condition. The time-dependent heat flow equation is solved for a specified V_{CE} and a nonuniform collector current density J_C to obtain a temperature distribution due to internal self heating after a small time interval h_t. By using this temperature distribution, carrier concentration and collector current values for each one-dimensional transistor are recalculated. Since the electrical time constant is much shorter than the thermal time constant, it

Figure 4 Current density and temperature distributions along the emitter-base junction (line $y = C$ in Fig. 1) for device A of Table 1 for $V_{CE} = 800$ V, $I_C = 0.1$ A (curves a); $V_{CE} = 160$ V, $I_C = 0.5$ A (curves b); $V_{CE} = 80$ V, $I_C = 1.0$ A (curves c); and $V_{CE} = 40$ V, $I_C = 2.0$ A (curves d) operating conditions.



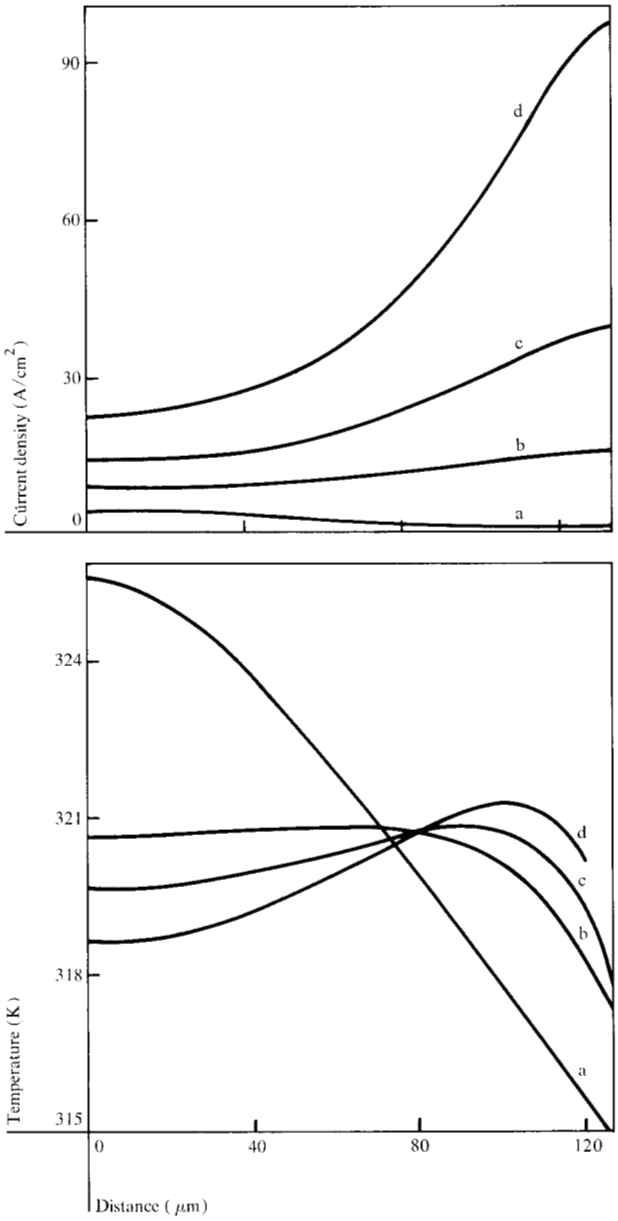


Figure 5 Current density and temperature distributions along the emitter-base junction (line $y = C$ in Fig. 1) for device B of Table 1 for $V_{CE} = 800$ V, $I_C = 0.16$ A (curves a); $V_{CE} = 160$ V, $I_C = 0.8$ A (curves b); $V_{CE} = 80$ V, $I_C = 1.6$ A (curves c); and $V_{CE} = 40$ V, $I_C = 3.2$ A (curves d) operating conditions.

is assumed that electrical parameters reach their steady-state values during the time interval h_t. This new current distribution is again used to calculate new temperature distribution and this iterative procedure is continued. Either a compatible solution is obtained, indicating the stable operation for specified operating conditions, or the temperature and current density increase beyond bound in a certain localized region of the device, indicating unstable behavior. For unstable operating points, calculations are stopped when the temperature reaches a value at which silicon becomes intrinsic, and the time to reach this temperature is noted. The SOA curve is obtained by considering a number of points on the V_{CE}, I_C plane and by drawing a boundary between stable (on the left) and unstable (on the right) operating points. Additional boundaries are drawn in the unstable region corresponding to different time values, so that the operating points on the left are stable for a time shorter than the specified time. The effect of the package on the SOA curve is analyzed by introducing a lumped thermal resistance between the collector contact and the ambient. This thermal resistance increases the constant temperature T_0 of the collector contact (Fig. 3) with increasing power dissipation in the device.

Results and discussions

The design parameters for three high-voltage power transistors of n-p-n$^-$-n$^+$ structure as shown in Fig. 1 are listed in Table 1. Figures 4–6 depict the current density and temperature distributions along the emitter-base junction (line $y = C$ in Fig. 1) for various stable operating conditions (1 mil = 25.4 μm). The temperature T_0 along the line $y = 0$ in Fig. 1 is assumed to be 300 K. For device A (Fig. 4), the current and voltage operating conditions are arranged (800 V, 0.1 A; 160 V, 0.5 A; 80 V, 1.0 A; 40 V, 2.0 A) so that the power dissipation within the device is 80 W. Constant power dissipation for the curves of Fig. 5 (device B) is 128 W while for the curves of Fig. 6 (device C), the power dissipation is 248 W. For the curves of Figs. 4–6, voltage levels are constant while the current levels increase in proportion to the total emitter area, so that the power density for all three devices is constant. It is seen from Figs. 4–6 that for each device, there are higher temperature gradients in the longitudinal (y direction in Fig. 1) as well as the transverse (x direction in Fig. 1) direction for the high-voltage low-current operating condition, as compared to the high-current low-voltage operating condition, for which the current crowding toward the edge of the emitter is higher. The temperature gradient in the longitudinal direction is estimated from Figs. 4–6, where the temperature along $y = C$ in Fig. 1 is sketched, and from the fact that the temperature along the collector contact is assumed to be 300 K. The low-current high-voltage condition is experienced in the turn-off transient, while the high-current low-voltage condition occurs in the turn-on transient condition. For the same power density, current crowding toward the edge of the emitter and temperature gradients in longitudinal and transverse directions decrease from device A to device B to device C. The predicted SOA curves for these three transistor designs are sketched in Fig. 7. It is clearly seen from

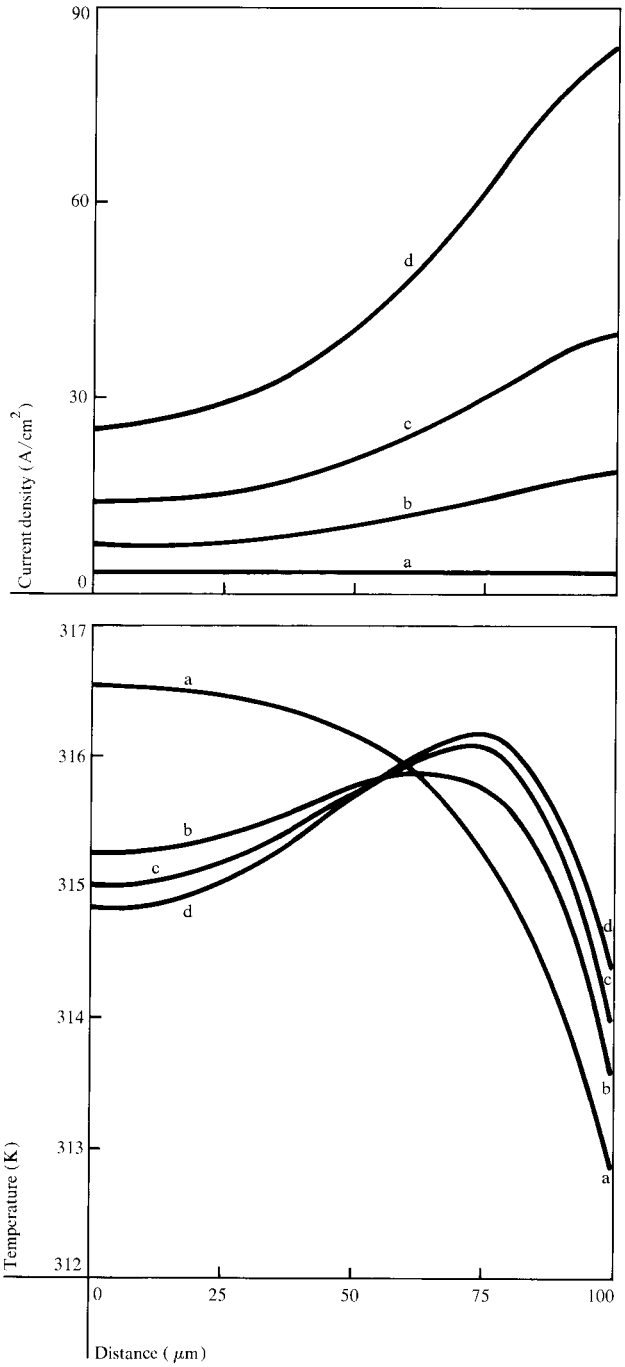


Figure 6 Current density and temperature distributions along the emitter-base junction (line $y = C$ in Fig. 1) for device C of Table 1 for $V_{CE} = 800$ V, $I_C = 0.33$ A (curves a); $V_{CE} = 160$ V, $I_C = 1.65$ A (curves b); $V_{CE} = 80$ V, $I_C = 3.31$ A (curves c); and $V_{CE} = 40$ V, $I_C = 6.62$ A (curves d) operating conditions.

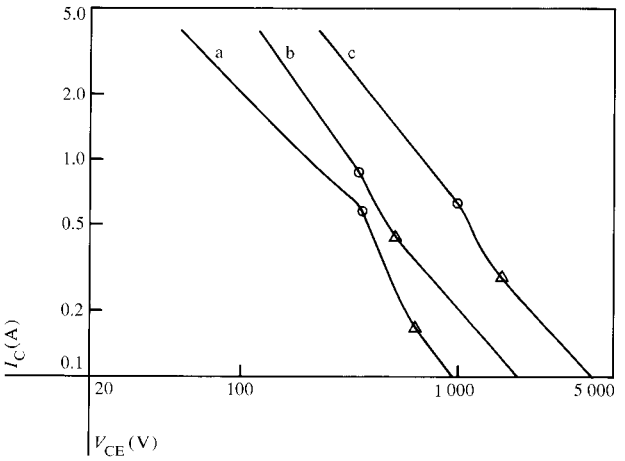


Figure 7 Predicted SOA curves for device A (curve a), device B (curve b), and device C (curve c) of Table 1.

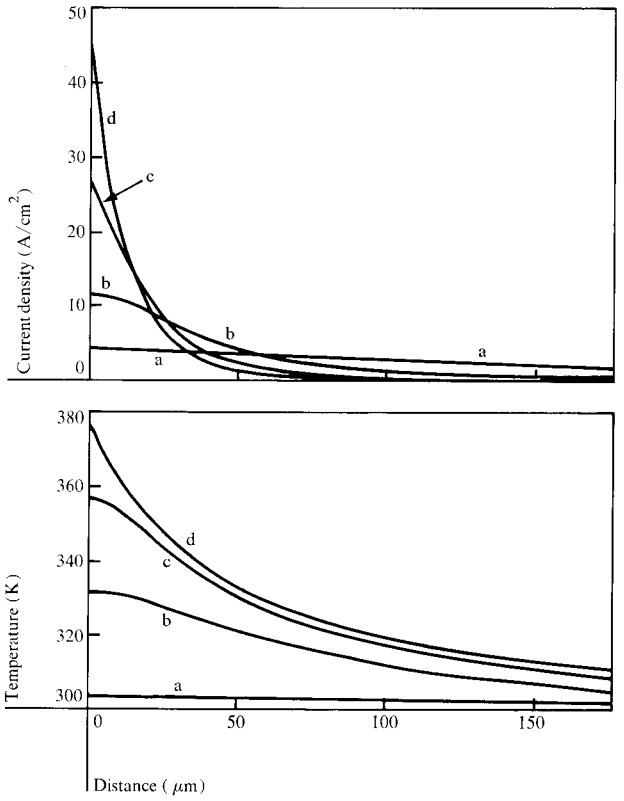


Figure 8 Current density and temperature distributions along the emitter-base junction (line $y = C$ in Fig. 1) for device A for $V_{CE} = 685$ V, $I_C = 0.15$ A operating condition after time intervals $t = 0.86$ μs (curves a), $t = 0.086$ ms (curves b), $t = 0.26$ ms (curves c), and $t = 0.43$ ms (curves d). At $t = 0.50$ ms, the temperature reaches a value for which the base region becomes intrinsic.

Fig. 7 that the power handling capability of device B is superior to that of device A, while device C has a higher power handling capability than either device A or B. For voltage levels less than the voltage marked by circles on the SOA curves of Fig. 7, the device failure is due to thermal instability. For voltage levels within the range marked by circles and triangles, the total base current is positive ($I_B > 0$) for points in the stable region.

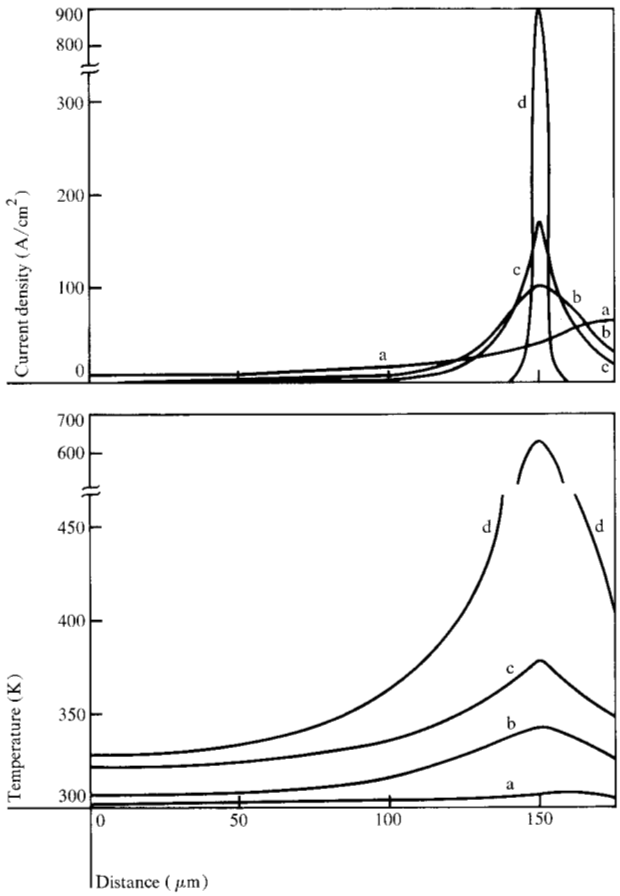


Figure 9 Current density and temperature distributions along the emitter-base junction (line $y = C$ in Fig. 1) for device A for $V_{CE} = 205$ V, $I_C = 1.0$ A operating condition after time intervals $t = 0.86$ μs (curves a), $t = 0.043$ ms (curves b), $t = 0.27$ ms (curves c), and $t = 0.34$ ms (curves d). At $t = 0.35$ ms, the temperature reaches a value for which the base region becomes intrinsic.

In the unstable region, avalanche injection from the collector region causes current crowding at the center of the emitter, and the total base current is negative ($I_B < 0$) when the temperature under the center of the emitter reaches intrinsic value. For voltage levels higher than the voltage marked by triangles, avalanche-generated carriers cause the total base current to be negative ($I_B < 0$) for operating points in the stable region. Avalanche injection from the collector initates failure in the unstable region.

Figures 8 and 9 depict the localization of current density and temperature at the emitter-base junction of device A as a function of time for unstable operating points. At $V_{CE} = 685$ V and $I_C = 0.15$ A (Fig. 8), current density and temperature increase under the center of the emitter, and at $t = 0.50$ ms, the temperature under the center of the emitter reaches the intrinsic range. For a $V_{CE} = 205$ V, $I_C = 1.0$ A operating point (Fig. 9), the current density and temperature buildup is at the edge of the emitter where the device becomes unstable at $t = 0.35$ ms. Figure 10 shows the increase of the peak temperature within device A as a function of time for the unstable operating points of Figs. 8 and 9 as well as for the stable operating points at $V_{CE} = 800$ V, $I_C = 0.1$ A and $V_{CE} = 80$ V, $I_C = 1.0$ A depicted in Fig. 4. A sharp increase in peak temperature is observed (after an initial value of temperature) for the unstable operating points in Fig. 10. As the current density is localized to the single, almost one-dimensional, transistor of Fig. 2, the rate of increase of current density and peak temperature reduces due to the finite number of one-dimensional transistors used in the analysis. In a real device, localization of the current density continues and the peak temperature continues to increase until the failure of the device.

For switching applications of transistors with inductive loading in the collector circuit, collector-to-emitter voltage V_{CE} may exceed the breakdown voltage BV_{CE0} [1], and therefore the current density and temperature buildup within the device can correspond to those shown in Fig. 8, and the failure of the device should be under the center of the emitter.

Figure 11 shows the variation of the external base-emitter voltage V_{BE} as a function of time for the stable and unstable operating points of Fig. 10 (voltage drop in the inactive base region is assumed to be negligible). For a constant collector current I_C at a certain value of V_{CE}, the base-emitter voltage V_{BE} decreases as the peak temperature within the device increases. As mentioned earlier, the rate of increase of the peak temperature decreases as the current density is localized to a small region of the device (Fig. 10). Curves c and d of Fig. 11 reflect this decrease in the rate of peak temperature increase by a corresponding reduction in the rate of decrease of V_{BE}. From Figs. 10 and 11, it is concluded that V_{BE} is a good indicator of the peak temperature variation along the emitter-base junction [11–12]. In certain switching applications, the temperature at the n^--n^+ interface may be much higher than the temperature along the emitter-base junction [15].

Figure 12 shows the effect of the temperature drop in the package of device A on its power handling capability. A lumped thermal resistance between the collector contact and the ambient simulates the temperature difference in the package, and the temperature value T_0 at the collector contact increases with power dissipation. It is seen from Fig. 12 that thermal resistance values of 0.25 K/W and 1 K/W (curves a and b) have a rather small effect on the power handling capability of the device. Curves d and e in Fig. 12 are additional boundaries in the unstable region so that the operating points on the left of these curves are stable for time values less than 1.0×10^{-4} s (curve d) and 1.0×10^{-5} s (curve e).

The predicted SOA curves of Figs. 7 and 12 compare favorably with the experimental observations of reverse second breakdown voltage in a test circuit with a collector inductive load. The variation of external base-emitter voltage with hot spot formation in the device in the forward operating region, as observed by an infrared microscanner, correlates well with the predictions of Figs. 10 and 11 [13]. The total time for temperature to reach the steady-state distribution for the stable operating points shown in Fig. 10 is smaller than lab observations. (This is expected since the heat flow in the package has not been taken into account for Fig. 10.)

The SOA curves of Figs. 7 and 12 have been obtained by a point-by-point stability analysis of V_{CE}, I_C operating conditions. The stability analysis of time varying V_{CE}, I_C operating conditions can be made with this model by changing V_{CE}, I_C values after small nonuniform time intervals. As mentioned earlier, when the time interval is of the order of nanoseconds, predictions resulting from this model can be very approximate since the assumption of electrical parameters reaching their steady-state values in this time interval may not be valid. The effect of the third dimension (variation of current density and temperature along the length of the emitter fingers), which has been ignored in the present analysis, can be incorporated into the model by empirical relationships between the active emitter area and the voltage and current operating conditions.

Summary

A mathematical model was utilized to predict the safe operating area (safe from second breakdown failure) for proper circuit applications of bipolar transistors in the forward ($I_B > 0$, $V_{CE} < BV_{CE0}$) as well as reverse ($I_B < 0$, $BV_{CE0} \leq V_{CE} \leq BV_{CB0}$) operating regions. This model takes into account the nonuniformity of the temperature within the transistor structure due to internal self-heating, and the avalanche multiplication effect in the reverse operating region, which cause second breakdown failure. Steady-state electrical and time-dependent thermal problems are solved to establish stability of a specified operating condition. The SOA curve is obtained by considering a number of operating points and by drawing a boundary between stable and unstable points. Predicted SOA curves for three high-voltage power transistors with similar power handling capability are presented. Additional boundaries are drawn in the unstable region for the pulsed operation of the device. Current density and temperature distributions within the transistor for various operating conditions in the stable region are presented. Localization of current density and temperature before failure for unstable operating points is illustrated by sketching them at various time intervals. The variations of peak temperature within the

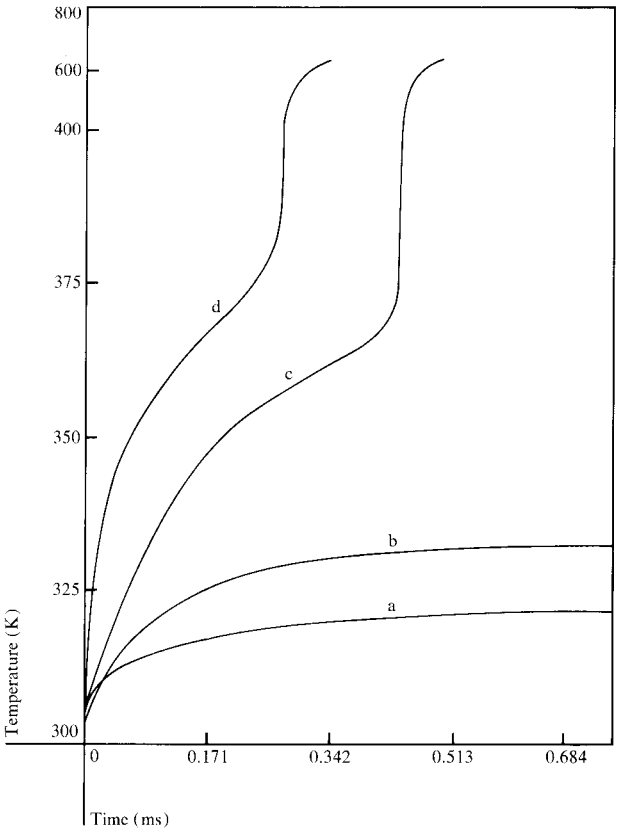
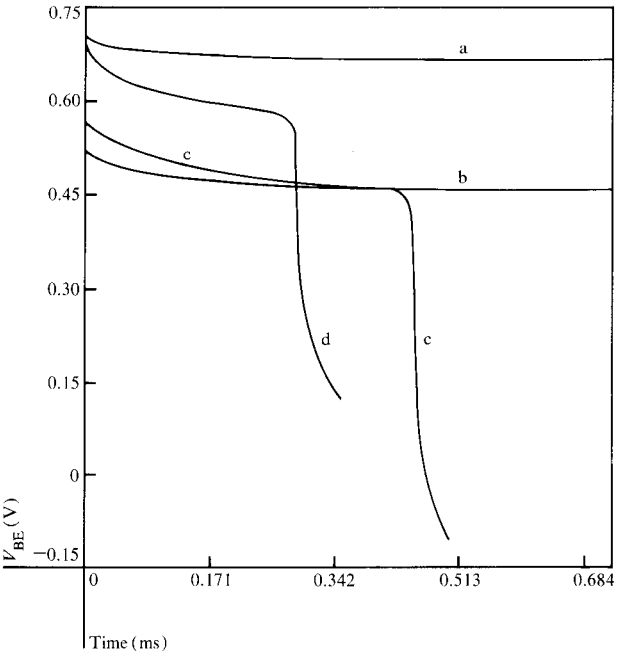


Figure 10 Variation of the peak temperature within device A with time for $V_{CE} = 80$ V, $I_C = 1.0$ A (curve a); $V_{CE} = 800$ V, $I_C = 0.1$ A (curve b); $V_{CE} = 685$ V, $I_C = 0.15$ A (curve c); and $V_{CE} = 205$ V, $I_C = 1.0$ A (curve d).

Figure 11 Variation of the external base-emitter voltage of the device A with time for $V_{CE} = 80$ V, $I_C = 1.0$ A (curve a); $V_{CE} = 800$ V, $I_C = 0.1$ A (curve b); $V_{CE} = 685$ V, $I_C = 0.15$ A (curve c); and $V_{CE} = 205$ V, $I_C = 1.0$ A (curve d).



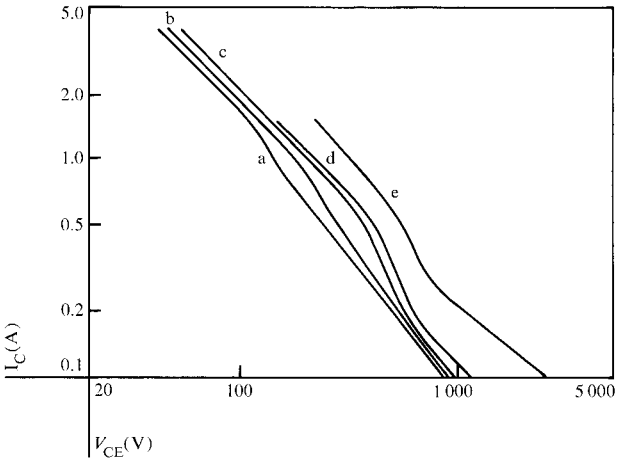


Figure 12 Predicted SOA curves for device A of Table 1 for $t = \infty$, thermal resistance between collector contact to the ambient (θ) = 1 K/W (curve a); $t = \infty$, $\theta = 0.25$ K/W (curve b); $t = \infty$, $\theta = 0$ (curve c); $t = 1.0 \times 10^{-4}$ s, $\theta = 0$ (curve d); and $t = 1.0 \times 10^{-5}$ s, $\theta = 0$ (curve e).

device and external base-emitter voltage with time are provided, and the effect of the temperature drop in the package of the transistor on its power handling capability is discussed.

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