G. Constantine, Jr.

New Developments in Load-Sharing Matrix Switches

The load-sharing matrix switch described previously[1] combines the power from fast, low-power drivers into a fast, high-power memory drive pulse. Although the matrix switch provides larger, faster drive pulses than were available previously, it requires a comparatively large number of drivers as inputs. Marcus[2] has already shown that it is possible to reduce the number of drivers by a factor of two except for memories with binary addresses. This note shows the minimum number of drivers required to provide a specified amount of noise cancellation. A method for constructing orthogonal matrices to obtain a minimum number of input drivers is given in the accompanying note by Chien.[3] Load-sharing matrix switches will be described which have low (but not zero) excitation on nonselected cores, as well as switches with ideally zero net excitation.

It should be pointed out that this letter deals with the logical design of matrix switches rather than with the design of the matrix switch transformers. The size of the cores, the core material, the number of turns, et cetera, must be chosen according to the methods of pulse transformer design to fit the requirements of the matrix switch logic.

Conventions

The logical design of a matrix switch is described in terms of the relative magnitude and direction of excitation applied by each input driver. For convenience, the windings excited by a driver are arranged in a column and the windings on a core are arranged in a row. Thus a matrix may be formed of elements A_{ij} which describe the excitation on a particular core caused by a particular driver. The opposite polarities of drive are indicated by $+$'s and $-$'s. The magnitude of drive is indicated by A, the relative number of turns on the winding. Therefore a $+3$ winding gives 50% more excitation in the opposite direction from a -2 winding. For simplicity the symbols $+1$ and -1 will be replaced by $+$ and $-$, respectively.

Plus excitation, by definition, gives a plus (or READ) output. Conversely, minus excitation gives a minus (or WRITE) output.

Noiseless, load-sharing matrix switches

A noiseless, load-sharing matrix switch is defined as one having no net excitation applied to any nonselected core. Therefore, equal plus and minus excitation must be applied to any core as a result of selecting any other core. An equal number of $+$ and $-$ windings must be excited on each nonselected core when another core is selected by pulsing all of its $+$ windings (or $-$ windings). Also, each matrix switch core generally has an equal number of $+$ and $-$ windings to provide equal READ and WRITE pulse amplitudes. Therefore, one-fourth of the total windings on a core are $+$ windings in series with $+$ windings on any other core. Thus the number of inputs n must equal 4 times some integer m, and exactly half of the windings excite any pair of cores in the same direction.

$$\sum_{i=0}^{n-1} A_{ij} \times A_{ij'} = 0 .$$

This is equivalent to requiring that the A matrix describing the switch be an orthogonal matrix,[3] except that the row of all $+$'s is not usable for a matrix switch.

R.E.A.C. Paley[4] has already described the method of constructing most of the orthogonal matrices of $n=4m$ inputs where n is less than 200. He lacks a method of construction only where $m=92$, 116, 156, 172, 184, or 188. Paley's Table 1 lists a method to be used for each constructable size of matrix.

A matrix switch with a particular number of outputs is constructed using the next larger multiple of four inputs which is constructable. For instance, Fig. 1 contains the A_{ij} matrix for a 20-input, 19-output, noiseless load-sharing switch. Sixteen of the outputs can be used to replace the older 16-output switch (for a 2 μsec memory[1]) with a significant reduction in the number of inputs from 32 to 20. With 20 inputs available, only 10 contribute to each output pulse. It seems wise to use a larger size of switch because ten drivers cannot furnish sufficient power to operate the memory. The 20-input, 19-output switch may be doubled in size, using techniques described previously,[1] or a 36-input, 35-output switch may be constructed; either method will yield a 32-output switch. However, for one particular application considered, the saving of four drivers was less than the additional logic required to decode into the 36-input rather than the 40-input switch.

It is also interesting to note that the A matrix may be considered as a group of code sequences with N bits per

Core number	Driver number 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
0	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−	−
1	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−
2	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	−
3	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	−
4	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−
5	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−
6	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−
7	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−
8	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	−
9	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−
10	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	−
11	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−
12	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	−
13	+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	−
14	+	+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	−
15	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	−
16	−	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−
17	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−
18	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−	+	−

Figure 1 **A 20-input, 19-output, load-sharing matrix switch.**

sequence, a maximum distance of $n/2$, and a minimum distance of $n/2$:

$d_{max}=d_{min}=n/2$.

Plotkin[5] has described the construction of such code sequences.

Decoding load-sharing matrix switches

There is a class of load-sharing matrix switches which have more outputs for a given number of inputs than the noiseless, load-sharing switch. This class is characterized by some unselected cores driven into saturation by an excitation comparable with the excitation of a selected core. Although it is in the saturated direction, excitation of a nonselected core may result in appreciable spurious outputs which, in general, are larger in amplitude and more numerous for switches with more outputs.

This class of load-sharing switch also can be described by an A_{ij} matrix of excitation on a particular core by a particular driver. The A_{ij} matrix can be formed by the proper interpretation of any binary code with any amount of redundancy. Each code sequence corresponds to a row in the A_{ij} matrix. Each bit position in the code (a column in a set of code sequences) corresponds to *two* columns in the A_{ij} matrix. A "1" in a bit position of the code corresponds to + excitation and a "0" corresponds to − excitation in one column of a A_{ij} matrix pair. The correspondence is reversed for the other A_{ij} matrix column of the pair. These columns are called *normal* or *complement*, depending on whether the correspondence to the code bits is normal or reversed. The normal or the complement winding of a pair is pulsed at READ time depending on whether the code sequence has a "1" or "0" in the corresponding bit position. Pulsing the input windings in this manner results in applying only + excitation to the core corresponding to the pattern of drivers pulsed. Any other core has at least one winding providing negative excitation. The minimum negative excitation on a nonselected core must be large enough to cancel the maximum positive excitation to prevent a READ output.

The relative positive and negative excitation applied to the cores is determined by the number of turns on the + and − windings, $N+$ and $N-$,

$$N- = \left(\frac{n-d_{\min}}{d_{\min}}\right) N+ .$$

If $d_{\max}$ is larger than $d_{\min}$ for a particular pair of cores, then one will receive negative excitation when the other core is selected. In general,

$$NI \text{ nonselected} = \left(1-\frac{d}{d_{\min}}\right) NI \text{ selected} .$$

The amount of noise at the output of the matrix switch depends on the flux change caused by exciting a nonselected core in the saturated direction. Therefore, the characteristics of the core limit the amount of saturation excitation which can be tolerated and thus limit the amount of decoding which can be built into this class of switch.

Rajchman[6] has already described one such decoding load-sharing matrix. By adding a parity check bit, a new matrix switch with reduced negative excitations can be constructed as shown in Fig. 2. The addition of input pairs with the same number of outputs results in a larger minimum distance between code sequences and thus lower noise outputs. The modified load-sharing switch described previously (Fig. 4 in Reference 1) is a type of decoding load-sharing switch with only one noise-generating core.

Figure 2 **The code, winding pattern and operation of a 5-input-pair, 16-output, decoding load-sharing matrix switch.**

Core No.	*Code* A	B	C	D	P	A_{ij} *Matrix* A $\bar{A}$	B $\bar{B}$	C $\bar{C}$	D $\bar{D}$	P $\bar{P}$	*Net Excitation*	
0	0	0	0	0	1	−3+2	−3+2	−3+2	−3+2	+2−3	0	
1	0	0	0	1	0	−3+2	−3+2	−3+2	+2−3	−3+2	−10	
2	0	0	1	0	0	−3+2	−3+2	+2−3	−3+2	−3+2	0	
3	0	0	1	1	1	−3+2	−3+2	+2−3	+2−3	+2−3	0	
4	0	1	0	0	0	−3+2	+2−3	−3+2	−3+2	−3+2	−10	
5	0	1	0	1	1	−3+2	+2−3	−3+2	+2−3	+2−3	−10	
6	0	1	1	0	1	−3+2	+2−3	+2−3	−3+2	+2−3	0	
7	0	1	1	1	0	−3+2	+2−3	+2−3	+2−3	−3+2	−10	
8	1	0	0	0	0	+2−3	−3+2	−3+2	−3+2	−3+2	0	
9	1	0	0	1	1	+2−3	−3+2	−3+2	+2−3	+2−3	0	
10	1	0	1	0	1	+2−3	−3+2	+2−3	−3+2	+2−3	+10	*Selected Core*
11	1	0	1	1	0	+2−3	−3+2	+2−3	+2−3	−3+2	0	
12	1	1	0	0	1	+2−3	+2−3	−3+2	−3+2	+2−3	0	
13	1	1	0	1	0	+2−3	+2−3	−3+2	+2−3	−3+2	−10	
14	1	1	1	0	0	+2−3	+2−3	+2−3	−3+2	−3+2	0	
15	1	1	1	1	1	+2−3	+2−3	+2−3	+2−3	+2−3	0	
						↑	↑	↑	↑	↑		
						Drivers Operated						

$$n- = \left(\frac{N-d_{\min}}{d_{\min}}\right) n+$$

$$n- = \left(\frac{5-2}{2}\right) \times 2 = 3$$

$$NI \text{ nonselected} = \left(1-\frac{d}{d_{\min}}\right) NI \text{ selected}$$

$$NI \text{ nonselected} = \left(1-\frac{4}{2}\right) \times 10 = -10$$

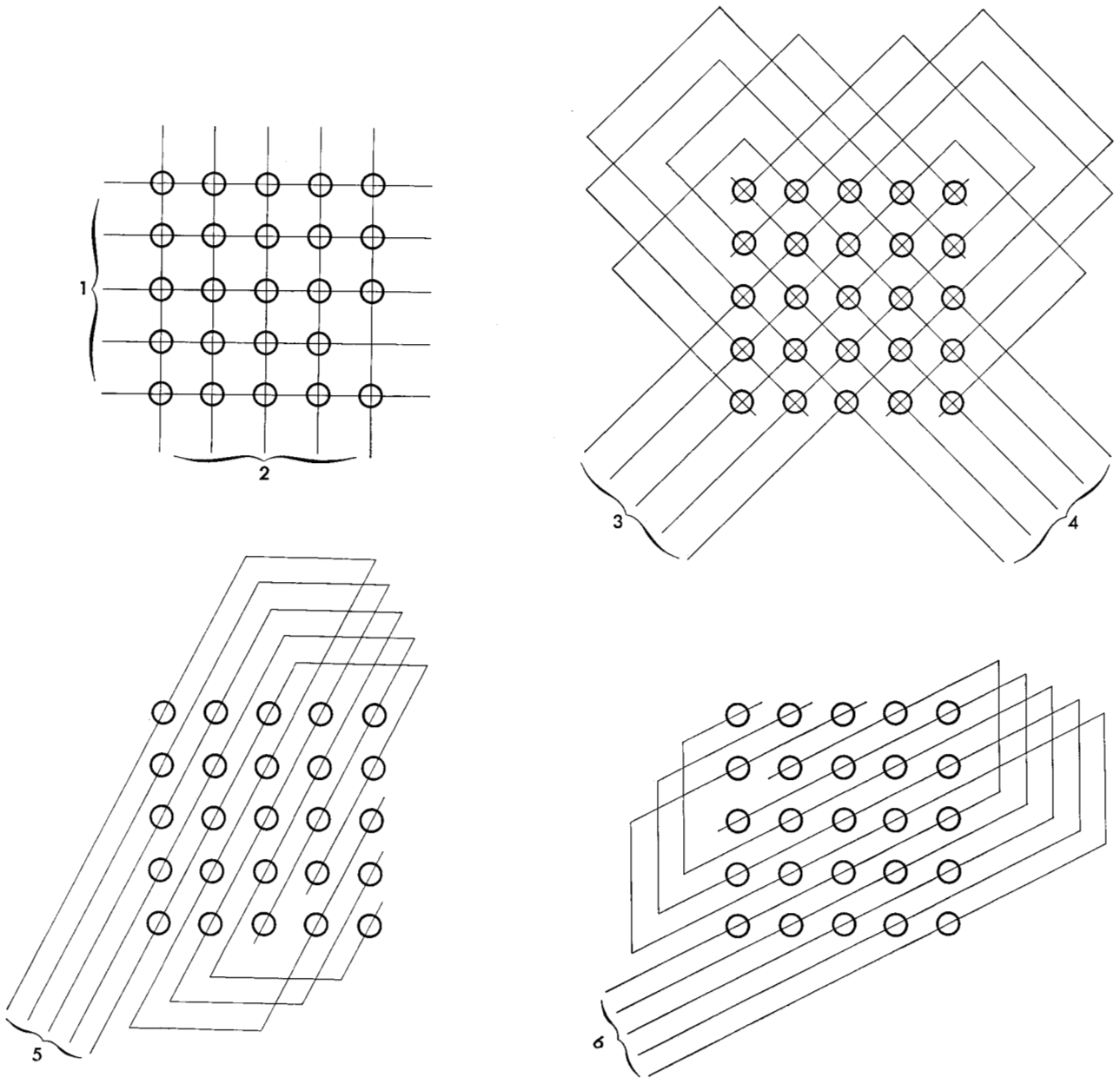

Figure 3 **The six sets of drive lines for a 5×5, coincident-current load-sharing matrix switch.**

The selected core cannot be reset by the drivers corresponding to negative excitation on the core because some nonselected cores would then receive uncancelled positive excitation and be set. One technique for resetting the selected core is to provide a single, large reset drive current to all cores simultaneously. Another is to provide a resetting bias on all cores which is roughly equal to one-half of the excitation applied to select the core. The bias will reset the core when the inputs are turned off.

Coincident-current, load-sharing matrix switch

The coincident-current matrix switch described by Rajchman[7] depends on exciting one row and one column of an array of switch cores. Drive currents which are each equal to an opposing bias on all cores are only able to switch the core excited by both of them simultaneously.

Minnick and Ashenhurst[8] have shown how to wire a plane for multiple-coincidence selection. Combining multiple-coincidence selection techniques with the coinci-

dent-current matrix switch gives load sharing with low-noise outputs. Figure 3 shows the sets of drive lines which may be used to select a 5×5 coincident-current, load-sharing matrix switch. One core receives six units of drive and each other core receives one unit of drive if one line in each group is pulsed. The bias current for the matrix switch may be made equal to the excitation from three drivers to obtain equal output amplitudes at READ and WRITE time. The relative amplitude of the READ and WRITE pulses may be varied over a wide range by changing the bias.

Assuming, in our example, a bias equal to one half of the input drive on the selected core, then the excitation on each other core in the plane is one-third of the bias. The noise output is small and the series impedance of the partially excited cores is low.

Conclusion

Noiseless, load-sharing matrix switches usually may be built with almost any multiple of four inputs and one fewer outputs. Paley has described methods of forming the A_{ij} matrix for this switch. By means of Chien's modification of these techniques,[3] the number of drivers required for a 16,384 word core memory x-y drive system can be reduced from 512 to 320.

In the use of the class of decoding load-sharing matrix switches many compromises between the size of noise excitation and the amount of decoding are available. As core materials are improved, larger amounts of noise excitation will still give acceptably low-noise outputs. Thus additional decoding can be done in the matrix switch.

The coincident-current, load-sharing matrix switch permits unequal READ and WRITE output amplitudes with fewer windings on each switch core. Although noise outputs are generated, they tend to be uniform for all partially excited cores. Noise cancellation techniques, such as not connecting the common ground of the secondary windings to the common ground for the ends of the memory drive lines, are very effective.

Acknowledgment

Many people have contributed the ideas summarized here. Robert Chien worked out the relationship between noiseless, load-sharing matrix switches, orthogonal matrices, and error-correcting codes suggested by John Gibson. Burke Fontaine contributed techniques for constructing error-correcting codes. Mitchell Marcus independently worked out the application of error-correcting codes to matrix switches. Norbert Vogl worked out many of the limitations of coincident-current type load-sharing matrix switches.

References

1. G. Constantine, Jr., *IBM Journal,* **2,** No. 3, 204 (July, 1958).
2. M. P. Marcus, *IBM Journal,* **3,** No. 2, 194 (April, 1959).
3. R. T. Chien, this issue, p. 414.
4. R. E. A. C. Paley, *J. Math. and Phys.,* **12,** 311 (1933).
5. M. Plotkin, "Binary Codes with Specified Minimum Distance," *Research Division Report 51-20,* University of Pennsylvania, January, 1951.
6. J. A. Rajchman, *RCA Review,* **13,** 183 (June, 1953).
7. J. A. Rajchman, *Proc. IRE,* **41,** No. 10, 1047 (October, 1953).
8. R. C. Minnick and R. L. Ashenhurst, *J. Appl. Phys.,* **26,** No. 5, 575 (May, 1955).

Received October 15, 1959