

[illegible]

```

LL          IIIIII      SSSSSSSS
LL          IIIIII      SSSSSSSS
LL          II         SS
LL          II         SS
LL          II         SS
LL          II         SS
LL          II         SSSSSS
LL          II         SSSSSS
LL          II         SS
LL          II         SS
LL          II         SS
LL          II         SS
LLLLLLLLLLL IIIIIIII   SSSSSSSS
LLLLLLLLLLL IIIIIIII   SSSSSSSS

```

MPLOAD
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- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00

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(1)	228	MPDCL - Multi-processing DCL command line handling
(1)	641	MPSSUNLOAD - STOP/CPU DCL command
(1)	719	MPSSUNHOOK - Unhook multi-processing code from system


```
0000 1 : Version: 'V04-000'
0000 2 :
0000 3 :
0000 4 :
0000 5 : .MCALL MFPR
0000 6 : .TITLE MPLOAD - LOAD AND CONNECT CODE FOR MULTIPROCESSING
0000 7 : .IDENT 'V04-000'
0000 8 :
0000 9 : *****
0000 10 : *
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0000 28 : *
0000 29 : *****
0000 30 : ++
0000 31 : Facility: Executive , Hardware fault handling
0000 32 : Abstract:
0000 33 :
0000 34 : MPLOAD is the main control module for the installation of
0000 35 : the code required for multiprocessing. It changes mode to kernel,
0000 36 : acquires sufficient pool space and moves the code into it.
0000 37 : With all interrupts disabled, the necessary hooks are inserted
0000 38 : into the exec to connect several replacement routines.
0000 39 :
0000 40 : Environment: MODE=Kernel
0000 41 :
0000 42 : Author: RICHARD I. HUSTVEDT, Creation date: 15-MAY-1979
0000 43 :
0000 44 : Modified by:
0000 45 :
0000 46 : V03-009 KDM0024 Kathleen D. Morse 10-Oct-1982
0000 47 : Alter CHMx vectors in secondary SCB if system service
0000 48 : inhibit was requested at boot time.
0000 49 :
0000 50 : V03-008 KDM0020 Kathleen D. Morse 04-Oct-1982
0000 51 : Create a subroutine that unhooks the multi-processing
0000 52 : code from the system, that can be invoked from the
```



```
0000 53 : primary's invalidate time-out logic.
0000 54 :
0000 55 : V03-007 KDM0003 Kathleen D. Morse 06-Aug-1982
0000 56 : Make STOP/CPU provide correct address to EXES$DEANONPAGED
0000 57 : when the pool block was < 32 bytes off a page boundary.
0000 58 :
0000 59 : 01 -
0000 60 : --
0000 61 :
0000 62 :
0000 63 : INCLUDE FILES:
0000 64 :
0000 65 :
0000 66 :
0000 67 : MACROS:
0000 68 :
0000 69 :
0000 70 : .MACRO HOOK,LOC,TARGET :
0000 71 : .LONG LOC :
0000 72 : JMP @#TARGET :
0000 73 : .BLKB 6 ; Normal VMS contents of hook location
0000 74 : .ENDM HOOK ;
0000 75 :
0000 76 : .MACRO HOOKJSB,LOC,TARGET
0000 77 : .LONG LOC
0000 78 : JSB @#TARGET
0000 79 : .BLKB 6 ; Normal VMS contents of hook location
0000 80 : .ENDM HOOKJSB
0000 81 :
0000 82 :
0000 83 : EQUATED SYMBOLS:
0000 84 :
0000 85 :
0000 86 : $CLIMSGDEF ; Define CLI error messages
0000 87 : $DSCDEF ; Define string descriptor fields
0000 88 : $DYNDEF ; Define dynamic structure types
0000 89 : $IPLDEF ; Define interrupt priority levels
0000 90 : $IRPDEF ; Define structure header fields
0000 91 : $LCKDEF ; Lock bit definitions
0000 92 : $MPMDEF ; Define MA780 registers
0000 93 : $MPSDEF ; Define secondary processor states
0000 94 : $NDTDEF ; Define nexus type codes
0000 95 : $PCBDEF ; Process control block definitions
0000 96 : $PHDDEF ; Process header definitions
0000 97 : $PRDEF ; Define processor register numbers
0000 98 : $PTEDEF ; Define page table entry format
0000 99 : $RPBDEF ; Define restart param block offsets
0000 100 : $SSDEF ; Define system error messages
0000 101 : $STATEDEF ; State definitions
0000 102 : $VADEF ; Define virtual address fields
0000 103 :
0000 104 :
0000 105 :
0000 106 : OWN STORAGE:
0000 107 :
0000 108 : .PSECT $$$$$$BEGIN,PAGE ; Base PSECT
0000 109 MP$$BEGIN:: ;
```

```
00000000 0000 110 MPSS$GL_POOLDSC:: ; Structure descriptor for MP code
000001F0' 0000 111 .LONG 0 ; Adr of non-paged pool alloc for MP
000001F0' 0004 112 .LONG <<<<MPSS$END-MPSS$BEGIN>+511>a-4>a4> ; Size of pool used
01F0' 0008 113 .WORD <<<<MPSS$END-MPSS$BEGIN>+511>a-4>a4> ; Structure size
62 000A 114 .BYTE DYN$C_LOADCODE ; Structure type of loadable code
03 000B 115 .BYTE DYN$C_LC_MP ; Structure sub-type of multi-processing
000000AC'00000014' 000C 116 MPSS$HOOKTBL:: ; Addresses to be locked in WS
0014 117 .LONG HOOKBASE,HOOKEND ;
0014 118 :
0014 119 : The convention for the following logical names is:
0014 120 :
0014 121 : 1) All hooks in the exec are prefixed by MPH$
0014 122 : 2) If the entire routine is replaced, then the
0014 123 : rest of the hook name is the same as the normal
0014 124 : routine name
0014 125 : 3) If there are only a few lines of new MP code to
0014 126 : be inserted, the hook name ends with HK and the
0014 127 : continuation point (if any) hook name ends with CONT
0014 128 : 4) All MP routines are prefixed with MPSS$
0014 129 : 5) If the MP routine entirely replaces an exec routine,
0014 130 : then the rest of the MP routine name is the same as
0014 131 : the normal routine name
0014 132 : 6) If there are only a few lines of new MP code, then
0014 133 : the rest of the MP routine name is a new name
0014 134 :
0014 135 HOOKBASE: ; Base of hook table
0014 136 HOOK MPH$SCHED,MPSS$SCHED ;
0024 137 HOOK MPH$RESCHED,MPSS$RESCHED ; Reschedule interrupt
0034 138 HOOK MPH$QAST,MPSS$QAST ; Queue AST
0044 139 HOOK MPH$INVALIDHK,MPSS$INVALID ; Invalidate TB
0054 140 HOOKJSB MPH$BUGCHKHK,MPSS$BUGCHECK ; Check for 2ndary during bugchk
0064 141 HOOK MPH$ASTDELHK,MPSS$ASTSCHEDCHK ; Resched process to 2ndary chk
0074 142 HOOK MPH$NEWLVLHK,MPSS$ASTNEWLVL ; Set new PR ASTLVL
00000000 0084 143 .LONG 0 ; End of JMP/JSB type hooks
0088 144 SCB_IPL14: ; Hook for SCB IPL=14 vector
00000000 0088 145 .LONG 0 ; Adr of longword
00000000 008C 146 .LONG 0 ; Old contents of longword
0090 147 SCB_IPL16: ; Hook for SCB IPL=16 vector
00000000 0090 148 .LONG 0 ; Adr of longword
00000000 0094 149 .LONG 0 ; Old contents of longword
0098 150 SCB_VEC94: ; Hook for XDELTA (SOFTINT 5)
00000000 0098 151 .LONG 0 ; Adr of longword
00000000 009C 152 .LONG 0 ; Old contents of longword
00A0 153 SCB_VECBC: ; Hook for SOFTINT F
00000000 00A0 154 .LONG 0 ; Adr of longword
00000000 00A4 155 .LONG 0 ; Old contents of longword
00000000 00A8 156 .LONG 0 ; Empty hook at ends table
00AC 157 HOOKEND: ;
00000000 158 .PSECT _END,PAGE ; End PSECT
0000 159 MPSS$END:: ;
0000 160 ;
00000000 161 .PSECT __MPLOAD, LONG ;
0000 162 ;
0000 163 LOCKRANGE: ; Addresses to be locked in WS
00000525'000004E1' 0000 164 .LONG LOCKSTART,LOCKEND ;
0008 165 ;
0008 166 STOPRANGE: ; Addresses to be locked in WS
```



```
000005DC'00000555' 0008 167 .LONG STOPSTART,STOPEND ;
0010 168
0010 169 :
0010 170 : Output buffer for SHOW CPU displays.
0010 171 :
00000000 0010 172 OUTPUT_LENGTH: .LONG 0
0014 173
0014 174 OUTPUT_BUFFER:
0000005A 0014 175 .BLKB 70
005A 176
005A 177 OUTPUT_BUF_DSC:
00000046 005A 178 .LONG 70
00000014' 005E 179 .ADDRESS OUTPUT_BUFFER
0062 180
0062 181 DCL_LINE_DSC:
00000000 0062 182 .LONG 0
00000000 0066 183 .LONG 0
006A 184
006A 185 STATE_VALUE:
00000000 006A 186 .LONG 0
006E 187
006E 188
006E 189 :
006E 190 : Array of ascid descriptor addresses for secondary
006E 191 : processor states. Ordered from minimum to maximum
006E 192 : value of the state. Indexed via numeric state value - 1.
006E 193 :
006E 194 STATES:
000000CB' 006E 195 .ADDRESS IDLE_STATE_DSC
000000BF' 0072 196 .ADDRESS DROP_STATE_DSC
000000A4' 0076 197 .ADDRESS BUSY_STATE_DSC
000000B0' 007A 198 .ADDRESS EXEC_STATE_DSC
00000086' 007E 199 .ADDRESS INIT_STATE_DSC
00000098' 0082 200 .ADDRESS STOP_STATE_DSC
0086 201
0086 202 INIT_STATE_DSC:
41 49 54 49 4E 49 0000008E'010E0000' 0086 203 .ASCID /INITIALIZE/
45 5A 49 4C 0094
0098 204 STOP_STATE_DSC:
50 4F 54 53 000000A0'010E0000' 0098 205 .ASCID /STOP/
00A4 206 BUSY_STATE_DSC:
59 53 55 42 000000AC'010E0000' 00A4 207 .ASCID /BUSY/
00B0 208 EXEC_STATE_DSC:
54 55 43 45 58 45 000000B8'010E0000' 00B0 209 .ASCID /EXECUTE/
45 00BE
00BF 210 DROP_STATE_DSC:
50 4F 52 44 000000C7'010E0000' 00BF 211 .ASCID /DROP/
00CB 212 IDLE_STATE_DSC:
45 4C 44 49 000000D3'010E0000' 00CB 213 .ASCID /IDLE/
00D7 214 GET_VERB_DSC:
42 52 45 56 24 000000DF'010E0000' 00D7 215 .ASCID /$VERB/
00E4 216 GET_LINE_DSC:
45 4E 49 4C 24 000000EC'010E0000' 00E4 217 .ASCID /$LINE/
00F1 218
00F1 219 STATE_CTL_DSC:
74 41 5F 21 2F 21 000000F9'010E0000' 00F1 220 .ASCID \!/_Attached processor is in the !AS state.\
65 63 6F 72 70 20 64 65 68 63 61 74 00FF
```


MPLOAD
V04-000

- LOAD AND CONNECT CODE FOR MULTIPROCESS ^{F 7} 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

Page 5
(1)

74 20 6E 69 20 73 69 20 72 6F 73 73 010B
65 74 61 74 73 20 53 41 21 20 65 68 0117
2E 0123
0124
0124
74 41 5F 21 2F 21 0000012C'010E0000' 0124
65 63 6F 72 70 20 64 65 68 63 61 74 0132
61 20 6E 69 20 73 69 20 72 6F 73 73 013E
74 73 20 6C 61 67 65 6C 6C 69 20 6E 014A
4C 58 21 20 66 6F 20 65 74 61 0156
0160
0160
0160

221
222 ILSTATE_CTL_DSC:
223 .ASCID \!/_Attached processor is in an illegal state of !XL\

.LIST MEB

; Show macro expansions

```
0160 228 .SBTTL MPDCL - Multi-processing DCL command line handling
0160 229 :++
0160 230 : Functional Description:
0160 231 :
0160 232 : This routine contains the entry point for MP.EXE, MP$DCL. This code
0160 233 : determines which command verb was requested (START, STOP, or SHOW)
0160 234 : and branches to the appropriate code. It reports an error if the
0160 235 : invocation was not via one of these three verbs.
0160 236 :
0160 237 : Calling Sequence:
0160 238 :
0160 239 : CALLx MP$DCL
0160 240 :
0160 241 : Input Parameters:
0160 242 :
0160 243 : None
0160 244 :
0160 245 : Environment:
0160 246 :
0160 247 : Executed by the primary processor.
0160 248 :
0160 249 : Return Status:
0160 250 :
0160 251 : $$$_NORMAL - normal completion
0160 252 : $$$_DEVOFFLINE - device is not in configuration (returned if not
0160 253 : on an 11/780, or secondary is not started)
0160 254 : $$$_SHMNOTCNCT - shared memory not connected (returned if no MA780
0160 255 : is found for START/CPU)
0160 256 : CLIS_ABVERB - unrecognized command (returned if MP.EXE is not invoked
0160 257 : via START, STOP, or SHOW DCL commands)
0160 258 :
0160 259 :--
0160 260 ERRORX2:
0160 261 MOVZBL #$$$_DEVOFFLINE,R0 ; Report device not in configuration
0164 262 ERRORX5:
0164 263 RET ; Exit with error status
0165 264 MP$DCL::
0165 265 .WORD 0 ; Entry mask
0167 266 .ENABL LSB
0167 267 CMPB #1,G^EX$GB_CPUTYPE ; Is this an 11/780?
016E 268 BNEQ ERRORX2 ; Br if not, error exit
0170 269 MOVB #DSC$K_CLASS_D,DSC$B_CLASS+DCL_LINE_DSC ; Initialize descriptor
0175 270 PUSHAB DCL_LINE_DSC ; Buffer dsc adr for command line
0179 271 PUSHAB GET_LINE_DSC ; Dsc adr of callback item requested
017D 272 CALLS #2,G^CLISGET_VALUE ; Request command line
0184 273 BLBC R0,ERRORX5 ; Br if error
0187 274 :
0187 275 : Determine which DCL command was issued: SHOW/CPU, START/CPU, or SHOW/CPU.
0187 276 : If none of these was issued, then exit with an error status.
0187 277 :
0187 278 MOVL DCL_LINE_DSC+DSC$A_POINTER,R2 ; Get address of DCL command line
0187 279 CMPB (R2),#^A\S\ ; First character must be an S
018C 280 BNEQ ERRORX3 ; Br if unrecognized verb
0190 281 CMPB (R2),#^A\H\ ; Check for SHOW verb
0192 282 BEQL SHOW_CPU ; Br to execute SHOW/CPU command
0196 283 CMPB (R2),#^A\T\ ; Check for STOP or START verbs
0198 284 BNEQ ERRORX3 ; Br if unrecognized verb
```


Line	Address	Hex	Op	Op2	Op3	Op4	Op5	Op6	Op7	Op8	Op9	Op10	Op11	Op12	Op13	Op14	Op15	Op16	Op17	Op18	Op19	Op20	Op21	Op22	Op23	Op24	Op25	Op26	Op27	Op28	Op29	Op30	Op31	Op32	Op33	Op34	Op35	Op36	Op37	Op38	Op39	Op40	Op41	Op42	Op43	Op44	Op45	Op46	Op47	Op48	Op49	Op50	Op51	Op52	Op53	Op54	Op55	Op56	Op57	Op58	Op59	Op60	Op61	Op62	Op63	Op64	Op65	Op66	Op67	Op68	Op69	Op70	Op71	Op72	Op73	Op74	Op75	Op76	Op77	Op78	Op79	Op80	Op81	Op82	Op83	Op84	Op85	Op86	Op87	Op88	Op89	Op90	Op91	Op92	Op93	Op94	Op95	Op96	Op97	Op98	Op99	Op100	Op101	Op102	Op103	Op104	Op105	Op106	Op107	Op108	Op109	Op110	Op111	Op112	Op113	Op114	Op115	Op116	Op117	Op118	Op119	Op120	Op121	Op122	Op123	Op124	Op125	Op126	Op127	Op128	Op129	Op130	Op131	Op132	Op133	Op134	Op135	Op136	Op137	Op138	Op139	Op140	Op141	Op142	Op143	Op144	Op145	Op146	Op147	Op148	Op149	Op150	Op151	Op152	Op153	Op154	Op155	Op156	Op157	Op158	Op159	Op160	Op161	Op162	Op163	Op164	Op165	Op166	Op167	Op168	Op169	Op170	Op171	Op172	Op173	Op174	Op175	Op176	Op177	Op178	Op179	Op180	Op181	Op182	Op183	Op184	Op185	Op186	Op187	Op188	Op189	Op190	Op191	Op192	Op193	Op194	Op195	Op196	Op197	Op198	Op199	Op200	Op201	Op202	Op203	Op204	Op205	Op206	Op207	Op208	Op209	Op210	Op211	Op212	Op213	Op214	Op215	Op216	Op217	Op218	Op219	Op220	Op221	Op222	Op223	Op224	Op225	Op226	Op227	Op228	Op229	Op230	Op231	Op232	Op233	Op234	Op235	Op236	Op237	Op238	Op239	Op240	Op241	Op242	Op243	Op244	Op245	Op246	Op247	Op248	Op249	Op250	Op251	Op252	Op253	Op254	Op255	Op256	Op257	Op258	Op259	Op260	Op261	Op262	Op263	Op264	Op265	Op266	Op267	Op268	Op269	Op270	Op271	Op272	Op273	Op274	Op275	Op276	Op277	Op278	Op279	Op280	Op281	Op282	Op283	Op284	Op285	Op286	Op287	Op288	Op289	Op290	Op291	Op292	Op293	Op294	Op295	Op296	Op297	Op298	Op299	Op300	Op301	Op302	Op303	Op304	Op305	Op306	Op307	Op308	Op309	Op310	Op311	Op312	Op313	Op314	Op315	Op316	Op317	Op318	Op319	Op320	Op321	Op322	Op323	Op324	Op325	Op326	Op327	Op328	Op329	Op330	Op331	Op332	Op333	Op334	Op335	Op336	Op337	Op338	Op339	Op340	Op341	Op342	Op343	Op344	Op345	Op346	Op347	Op348	Op349	Op350	Op351	Op352	Op353	Op354	Op355	Op356	Op357	Op358	Op359	Op360	Op361	Op362	Op363	Op364	Op365	Op366	Op367	Op368	Op369	Op370	Op371	Op372	Op373	Op374	Op375	Op376	Op377	Op378	Op379	Op380	Op381	Op382	Op383	Op384	Op385	Op386	Op387	Op388	Op389	Op390	Op391	Op392	Op393	Op394	Op395	Op396	Op397	Op398	Op399	Op400	Op401	Op402	Op403	Op404	Op405	Op406	Op407	Op408	Op409	Op410	Op411	Op412	Op413	Op414	Op415	Op416	Op417	
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MPLOAD
V04-000

I 7
- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
MPDCL - Multi-processing DCL command lin 5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

Page 8
(1)

FE3F	CF	9D	50	E9	0211	334	BLBC	RO,ERRORX4	; Exit with error status
		FDF8	CF	D0	0214	335	MOVL	OUTPUT_LENGTH,OUTPUT_BUF_DSC	; Initialize output buffer dsc
		FE3B	CF	7F	021B	336	PUSHAQ	OUTPUT_BUF_DSC	; Dsc adr for output buffer
00000000	'GF		01	FB	021F	337	CALLS	#1,G^LIB\$POT_OUTPUT	; Output secondary processor state
		88	50	E9	0226	338	BLBC	RO,ERRORX4	; Exit with error status
					0229	339			
					0229	340	EXIT:		
50	01			9A	0229	341	MOVZBL	#SS\$_NORMAL,RO	; Exit with success code
				04	022C	342	RET		; Exit
					022D	343	.DSABL	LSB	

```
022D 345 .SBTTL
022D 346 :++
022D 347 : Functional Description:
022D 348 :
022D 349 : MPSS$LOAD is linked together with all of the code required for multi-
022D 350 : processing. The necessary amount of non-paged pool is allocated
022D 351 : and rounded up to page boundary. Code is then moved into this
022D 352 : block of pool. All of this code must be PIC although a limited
022D 353 : amount of relocation will be done on data cells and the SCB for
022D 354 : the secondary processor.
022D 355 :
022D 356 : Calling Sequence:
022D 357 :
022D 358 : BRW MPSS$LOAD
022D 359 :
022D 360 : Input Parameters:
022D 361 :
022D 362 : None
022D 363 :
022D 364 : Environment:
022D 365 :
022D 366 : Executed by the primary processor.
022D 367 :
022D 368 :
022D 369 :--
022D 370 :
022D 371 MPSS$LOAD::
022D 372 $LKWSET_S INADR=LOCKRANGE ; Load multi-processing code for START
                                PUSHL #0 ; Lock critical code into WS
                                PUSHL #0
                                PUSHQA LOCKRANGE
                                CALLS #3,G^SYSS$LKWSET
                                RO,ERRORX1 ; Exit if unable to lock pages
022D 373 BLBC
022D 374 $LKWSET_S INADR=MPSS$HOOKTBL ; Lock critical data into WS
                                PUSHL #0
                                PUSHL #0
                                PUSHQA MPSS$HOOKTBL
                                CALLS #3,G^SYSS$LKWSET
                                RO,ERRORX1 ; Br if error
022D 375 BLBC
022D 376 $CMKRNL S W^MPSS$LOADK ; Execute kernel routine
                                PUSHL #0
                                PUSHAL W^MPSS$LOADK
                                CALLS #2,G^SYSS$CMKRNL
022D 377 ERRORX1:
022D 378 RET ; Return
022D 379
022D 380
022D 381 LOCAL_MEM_ERR:
022D 382 MOVL #ERR$_LCLMEMUSED,R0 ; Local memory cannot be used for MP
022D 383 RET
022D 384
022D 385 MA780_NOT_USED:
022D 386 MOVL #ERR$_MA780_REQ,R0 ; MA780 memory required for MP
022D 387 RET
022D 388
022D 389 MA780_CNCT_ERR:
022D 390 MOVL #ERR$_SHMDBLUSE,R0 ; MA780 memory used for MP and MA780
```

00 DD 022D
00 DD 022F
FDCB CF 7F 0231
00000000'GF 03 FB 0235
21 50 E9 023C 373
023F 374
00 DD 023F
00 DD 0241
00000000C'EF 7F 0243
00000000'GF 03 FB 0249
0D 50 E9 0250 375
0253 376
00 DD 0253
0279'CF DF 0255
00000000'GF 02 FB 0259
04 0260 377
0260 378
0261 379
0261 380
0261 381
50 00000000'8F D0 0261 382
04 0268 383
0269 384
0269 385
50 00000000'8F D0 0269 386
04 0270 387
0271 388
0271 389
50 00000000'8F D0 0271 390


```
04 0278 391 RET ; system interconnect at same time
0279 392
0279 393
0279 394
OFFC 0279 395 MPSS$LOADK:: .WORD ^M<R2,R3,R4,R5,R6,R7,R8,R9,R10,R11> ; Entry mask
027B 396 .ENABL LSB
00000000'GF D5 027B 397 TSTL G^EXE$GL_MP ; Is secondary already started?
A6 12 0281 398 BNEQ EXIT ; Br on yes, don't do anything
00000000'GF D5 0283 399 TSTL G^EXE$GL_SHBLIST ; Is MA780 in use as sys intercnc?
E6 12 0289 400 BNEQ MA780 CNCT ERR ; Br if MA780 already in use
50 00000000'GF D0 028B 401 MOVL G^EXE$GL_RPB,R0 ; Get address of RPB
CA 30 A0 OC E0 0292 402 BBS #RPB$V_USEMPM,RPB$L_BOOTR5(R0),LOCAL MEM ERR ; Br if booted with
CD 30 A0 OB E1 0297 403 BBC #RPB$V_MPM,RPB$L_BOOTR5(R0),MA780 NOT_USED ; wrong memory
51 0008'CF 3C 029C 404 MOVZWL W^MPSS$GL_POOLDSC+IRPSW_SIZE,R1 ; Size of loadable code
00000000'GF 16 02A1 405 JSB G^EXE$ALONONPAGED ; Allocate necessary block
02A7 406
02A7 407 .IF DF,MPDBGSWT
02A7 408 SETIPL #0 ;***** Drop IPL for debugging
02A7 409 .ENDC
02A7 410
B6 50 E9 02A7 411 BLBC R0,ERRORX1 ; Exit if none available
50 52 D0 02AA 412 MOVL R2,R0 ; Remember starting address of pool
0000'CF 52 D0 02AD 413 MOVL R2,W^MPSS$GL_POOLDSC ; Assume nothing to return to pool
52 01FF C2 9E 02B2 414 MOVAB 511(R2),R2 ; Round up to page boundary
52 00001FF 8F CA 02B7 415 BICL #^X1FF,R2 ; Set to page boundary
SA 52 D0 02BE 416 MOVL R2,R10 ; Save address of block
00000000'GF 52 D0 02C1 417 MOVL R2,G^EXE$GL_MP ; Set exec pointer to MP code
51 52 50 C3 02C8 418 SUBL3 R0,R2,R1 ; Compute size of unused piece of pool
08 A0 51 B0 02CE 419 BEQL 10$ ; Br if piece of pool was page-aligned
OA A0 0362 8F B0 02D2 420 MOVW R1,IRPSW_SIZE(R0) ; Set size of unused piece
20 51 D1 02D8 421 MOVW #<DYN$C[_C_MP28+DYN$C_LOADCODE],IRPSB_TYPE(R0) ; Set type
40 15 02DB 422 CML R1,#32 ; Is piece too small to bother returning
0000'CF 52 D0 02DD 423 BLEQ 10$ ; Br if too small
0004'CF 51 C2 02E2 424 MOVL R2,W^MPSS$GL_POOLDSC ; Set page-aligned pool adr
0008'CF 51 C2 02E7 425 SUBL2 R1,W^MPSS$GL_POOLDSC+4 ; Set page-aligned pool size
02EC 426 SUBL2 R1,W^MPSS$GL_POOLDSC+IRPSW_SIZE ; Set page-aligned size
427 ASSUME IRPSW_SIZE [E 10]
62 0000'CF D0 02EC 428 MOVL W^MPSS$GL_POOLDSC,(R2) ; Initialize enough of pool block
04 A2 0004'CF D0 02F1 429 MOVL W^MPSS$GL_POOLDSC+4,4(R2) ; to allow its deallocate if an
08 A2 0008'CF D0 02F7 430 MOVL W^MPSS$GL_POOLDSC+8,8(R2) ; error exit is required
00000000'GF 16 02FD 431 JSB G^EXE$DEANONPAGED ; Return unused piece of pool
17 50 E8 0303 432 BLBS R0,10$ ; Br if successful
0306 433 DEA_ERR_EXIT:
50 DD 0306 434 PUSHL R0 ; Save error exit status
50 0000'CF D0 0308 435 MOVL W^MPSS$GL_POOLDSC,R0 ; Get address of pool allocated
00000000'GF 16 030D 436 JSB G^EXE$DEANONPAGED ; Release block of pool
50 8ED0 0313 437 POPL R0 ; Restore exit status
00000000'GF D4 0316 438 CLRL G^EXE$GL_MP ; Indicate no MP code loaded
04 031C 439 RET ; Exit with error status
031D 440
031D 441 10$:
50 0000'CF 9E 031D 442 MOVAB W^MPSS$BEGIN,R0 ; Address of start of code segment
59 SA 50 C3 0322 443 SUBL3 R0,R10,R9 ; Relocation offset is difference
0326 444 ;
0326 445 ; The addresses in the SCB for the secondary processor are now relocated
0326 446 ; by adding the relocation value. Any SCB pointer already a system space
0326 447 ; address is correct and need not be relocated.
```



```
51 0200'CF 9E 0326 448 :  
50 80 8F 9A 0326 449 : MOVAB W*SCB$AL_BASE+512,R1 ; Get base of SCB  
032B 450 : MOVZBL #128,R0 ; Do all 128 vectors  
032F 451 : .DSABL LSB  
032F 452 SCB_LOOP: :  
71 D5 032F 453 : TSTL -(R1) ; Is vector in system space?  
03 19 0331 454 : BLSS 10$ ; Yes, skip it  
61 59 C0 0333 455 : ADDL R9,(R1) ; Other wise relocate pointer to point  
F6 50 F5 0336 456 10$: SOBGTR R0,SCB_LOOP ; to code segment. Do all 128 vectors  
0339 457 :  
0339 458 : Locate all the multiport memory controllers and initialize the SCB  
0339 459 : vectors for the inter-processor interrupts. The first MA780 is used for  
0339 460 : the multi-processing scheduling interrupt while the other MA780s are  
0339 461 : vectored to an unexpected interrupt logging routine. The error interrupt  
0339 462 : vectors for the MA780s are initialized for the secondary also, while  
0339 463 : those for the primary were initialized in the normal VMS boot procedures.  
0339 464 :  
0339 465 LOC_MPM: : Initialize vectors for MA780 memories  
50 D4 0339 466 : CLRL R0 ; Initialize index  
52 0000'CF 9E 033B 467 : MOVAB W*MPSS$INT58,R2 ; Get adr of error interrupt logger  
52 59 C0 0340 468 : ADDL R9,R2 ; Relocate for eventual location  
52 01 C8 0343 469 : BISL #1,R2 ; Set interrupt stack bit in vector  
53 00000000'GF D0 0346 470 : MOVL G*MMG$GL_SBICONF,R3 ; Get address of SBI config array  
54 0000'CF 9E 034D 471 : MOVAB W*MPSS$AL_MPMBASE,R4 ; Get address of first MA780 base  
55 00000000'GF D0 0352 472 : MOVL G*EXE$GL_SCB,R5 ; Base address for primary SCB  
56 00000000'GF D0 0359 473 : MOVL G*EXE$GL_RPB,R6 ; Get base of RPB  
57 0000'CF DE 0360 474 : MOVAL W*SCB$AL_BASE,R7 ; Base address for secondary SCB  
0365 475 :  
10 00000000'GF 00' E1 0365 476 : BBC S*#EXE$V SSINHIBIT,G*EXE$GL_FLAGS,5$ ; If sys srv are being  
44 A7 00000000'GF DE 036D 477 : MOVAL G*EXE$CMODEXECX,^X44(R7) ; inhibited, then revector the  
40 A7 00000000'GF DE 0375 478 : MOVAL G*MPSS$CMODKRN LX,^X40(R7) ; entry points for CHMK and CHME  
037D 479 5$:  
037D 480 :  
51 0090 C640 03 8B 037D 481 10$: BICB3 #3,RPB$B CONFREG(R6)[R0],R1 ; Get a type byte  
51 40 8F 91 0384 482 : CMPB #NDT$_MPM0,R1 ; Is it a multiport memory?  
7D 12 0388 483 : BNEQ 15$ ; Br if not an MA780  
038A 484 :  
58 0100 C740 DE 038A 485 : MOVAL 256(R7)[R0],R8 ; Compute address of first vector  
40 A8 52 D0 0390 486 : MOVL R2,64(R8) ; Set IPL=X15 vector (error interrupt)  
00C0 C8 52 D0 0394 487 : MOVL R2,192(R8) ; Set IPL=X17 vector (error interrupt)  
0399 488 :  
0000'CF D5 0399 489 : TSTL W*MPSS$AL_MPMBASE ; Is this the first MA780?  
51 12 039D 490 : BNEQ 12$ ; Br if not  
039F 491 :  
51 0000'CF 9E 039F 492 : MOVAB W*MPSS$SINTSR,R1 ; Get adr of secondary interrupt rtn  
51 59 C0 03A4 493 : ADDL R9,R1 ; Relocate for eventual location  
51 01 C8 03A7 494 : BISL #1,R1 ; Set interrupt stack bit in vector  
68 51 D0 03AA 495 : MOVL R1,(R8) ; Set IPL=X14 vector (inter-proc intrpt)  
0080 C8 51 D0 03AD 496 : MOVL R1,128(R8) ; Set IPL=X16 vector (inter-proc intrpt)  
03B2 497 :  
51 0000'CF 9E 03B2 498 : MOVAB W*MPSS$PINTSR,R1 ; Get adr of primary interrupt routine  
51 59 C0 03B7 499 : ADDL R9,R1 ; Relocate for eventual location.  
51 01 C8 03BA 500 : BISL #1,R1 ; Set interrupt stack bit in vector  
58 0100 C540 DE 03BD 501 : MOVAL 256(R5)[R0],R8 ; Compute address of first vector  
00000088'EF 58 D0 03C3 502 : MOVL R8,SCB_IPL14 ; Remember adr for unload logic  
0000008C'EF 68 D0 03CA 503 : MOVL (R8),SCB_IPL14+4 ; Remember contents for unload  
68 51 D0 03D1 504 : MOVL R1,(R8) ; Set IPL=X14 vector (inter-proc intrpt)
```

```
00000090'EF 0080 C8 9E 03D4 505 MOVAB 128(R8),SCB_IPL16 ; Remember adr for unload logic
00000094'EF 0080 C8 D0 03DD 506 MOVL 128(R8),SCB_IPL16+4 ; Remember contents for unload
0080 C8 51 DC 03E6 507 MOVL R1,128(R8) ; Set IPL=X16 vector (inter-proc intrpt)
16 11 03EB 508 BRB 14$ ; Continue with common code
FF8D 31 03ED 509 ;
51 0000'CF 9E 03F0 510 11$: BRW 10$ ; Branch assist
51 51 59 C0 03F5 511 12$: MOVAB W'MPSS$UNEXPINT,R1 ; Get adr of unexpected interrupt rtn
51 01 C8 03F8 512 ADDL R9,R1 ; Relocate for eventual location
68 51 D0 03FB 513 BISL #1,R1 ; Set interrupt stack bit in vector
0080 C8 51 D0 03FE 514 MOVL R1,(R8) ; Set IPL=X14 vector (inter-proc intrpt)
84 6340 D0 0403 515 MOVL R1,128(R8) ; Set IPL=X16 vector (inter-proc intrpt)
E2 50 10 F2 0407 516 ;
50 0000'CF D0 040B 517 14$: MOVL (R3)[R0],(R4)+ ; Remember adr for this MA780s registers
08 12 0410 518 AOBLS #16,R0,11$ ; Try all 16
50 037C 8F 3C 0412 519 MOVL W'MPSS$AL_MPMBASE,R0 ; Get base of MA780 registers
FEED 31 0417 520 15$: BNEQ FOUND_MPM ; Found at least one MA780
51 0000'CF 9E 041A 521 MOVZWL #SS$ SHMNOTCNCT,R0 ; Indicate failure to find an MA780
00000098'EF 0094 C5 9E 0422 522 BRW DEA_ERR_EXIT ; Error exit with pool deall
0000009C'EF 0094 C5 D0 042B 523 FOUND_MPM:
000000A0'EF 00BC C5 9E 0434 524 MOVAB W'MPSS$RESCHEDIPL5,R1 ; Get address of primary fork rtn
000000A4'EF 00BC C5 D0 043D 525 BISL #1,R1 ; Set interrupt stack bit in vector
00BC C5 0094 C5 D0 0446 526 MOVL ^X94(R5),SCB_VEC94 ; Remember adr for unload logic
0094 C5 51 59 C1 044D 527 MOVL ^X94(R5),SCB_VEC94+4 ; Remember contents for unload
0000'CF 0000'CF C1 0453 528 MOVL ^XBC(R5),SCB_VECBC ; Remember adr for unload logic
52 60 D0 045B 529 MOVL ^XBC(R5),SCB_VECBC+4 ; Remember contents for unload
00 00 EF 045E 530 MOVL ^X94(R5),^XBC(R5) ; Make XDELTA respond to softint ^XF
52 52 02 0460 531 ADDL3 R9,R1,^X94(R5) ; Relocate for eventual location & store
0000'CF 0000'CF C1 0463 532 ADDL3 #MPM$IIR,W'MPSS$AL_MPMBASE,- ; Compute address of
53 52 10 C1 0467 533 W'MPSS$GL_MPMIIR ; interrupt request register
8F 53 78 047A 534 MOVAB MPMSL_CSR(R0),R2 ; Interrupt routines
0000'CF 0000'CF 0F 52 78 047A 535 EXTZV #MPMSV_CSR_PORT,- ; Read configuration register
53 52 10 C1 047A 536 #MPMS$CSR_PORT,R2,R2 ; Get port number
0000'CF 0000'CF 0F 52 78 047A 537
53 52 10 C1 047A 538 ADDL3 #MPMSV_IIR_CTL,R2,R3 ; Set to control field
0000'CF 0000'CF 0F 52 78 047A 539 ASHL R3,#^XT111,W'MPSS$GL_PRIMSKT ; Generate interrupt trigger mask
0000'CF 0000'CF 0F 52 78 047A 540 MULL #4,R2 ; Compute bit position for trigger
0000'CF 0000'CF 0F 52 78 047A 541 ASHL R2,#^XF,W'MPSS$GL_PRIMSKC ; Align and store mask for clear
0000'CF 0000'CF 0F 52 78 047A 542
0000'CF 0000'CF 0F 52 78 047A 543 ; Compute the physical addresses for the secondary SCB and the Secondary
0000'CF 0000'CF 0F 52 78 047A 544 ; initialization routine starting address.
0000'CF 0000'CF 0F 52 78 047A 545
0000'CF 0000'CF 0F 52 78 047A 546
0000'CF 0000'CF 0F 52 78 047A 547
0000'CF 0000'CF 0F 52 78 047A 548
0000'CF 0000'CF 0F 52 78 047A 549
0000'CF 0000'CF 0F 52 78 047A 550 SET_PHYS:
55 00000000'GF D0 047A 551 MOVL G'MMG$GL_SPTBASE,R5 ; Get base of SPT
51 0000'CF 9E 0481 552 MOVAB W'SCBS$AL_BASE,R1 ; VA of Secondary processor SCB
51 51 59 C0 0486 553 ADDL R9,R1 ; Relocate to eventual location
51 51 15 09 EF 0489 554 EXTZV #VASV_VPN,#VASS_VPN,R1,R1 ; Get virtual page number
50 50 50 6541 D0 048E 555 MOVL (R5)[R1],R0 ; Fetch PTE for it
50 50 15 00 EF 0492 556 EXTZV #PTESV_PFN,#PTESS_PFN,R0,R0 ; Isolate page number
0000'CF 50 09 78 0497 557 ASHL #9,R0,W'MPSS$GL_SCBB ; Save physical SCB address
51 0000'CF 9E 049D 558 MOVAB W^EXE$MPSTART,R1 ; VA of initialization routine
51 51 59 C0 04A2 559 ADDL R9,R1 ; Relocate to eventual location
51 51 15 09 EF 04A5 560 EXTZV #VASV_VPN,#VASS_VPN,R1,R1 ; Get virtual page number
50 6541 D0 04AA 561 MOVL (R5)[R1],R0 ; Fetch PTE for it
```



```
50 50 15 00 EF 04AE 562 EXTZV #PTESV PFN,#PTES PFN,R0,R0 ; Isolate page number
10 A6 50 09 78 04B3 563 ASHL #9,R0,RPB$HALTPC(R6) ; Save starting physical address
04B8 564
04B8 565 ; Relocate some stray locations
04B8 566
00000000'EF 59 C0 04B8 567 MISC_RELOC: ;
00000000'EF 59 C0 04BF 568 ADDL R9,XDELIBRK ; Address for initial breakpoint
00000000'EF 59 C0 04C6 569 ADDL R9,MPSS$GL_STRTVA ; Address for jump into S0 space
04CD 570 ADDL R9,MPSS$GL_ISP ; Interrupt stack for secondary
04CD 571
04CD 572 ; Remember the time and date that this code was loaded. This field
04CD 573 ; is used by the MONITOR utility to determine if the multi-processing
04CD 574 ; code has been reloaded during its last sampling interval (and therefore,
04CD 575 ; the cpu time accumulation cells have been re-initialized).
04CD 576
0000'CF 00000000'GF 7D 04CD 577 MOVQ G^EXES$GQ_SYSTIME,W^MPSS$GQ_MPSTRTIM ; Get time in 64 bits
04D6 578
04D6 579 ; Now move the code into the pool segment after all relocation is done.
04D6 580
04D6 581 MOVE_CODE:
6A 5B 0000'8F 3C 04D6 582 MOVZWL #<MPSS$END-MPSS$BEGIN>,R11 ; Size of MP code in bytes
0000'CF 5B 28 04DB 583 MOVCL R11,W^MPSS$BEGIN,(R10) ; Move code to allocated pool space
04E1 584
04E1 585 .IF DF,MPDBGSWT
04E1 586 NOP ;***** Instruction for debug breakpoint
04E1 587 .ENDC
04E1 588
04E1 589
04E1 590 ; Begin locked down code that will execute at IPL=31 to actually
04E1 591 ; install needed hooks into the running system.
04E1 592
04E1 593 LOCKSTART:
04E1 594 SETIPL #31
04E1 595 MTPR #31,S^#PRS_IPL
00000000'GF 12 1F DA 04E1 596 JSB G^INIS$WRITABLE ; Set writable for installing hooks
55 00000014'EF 16 04E4 597 MOVAB HOOKBASE,R5 ; Get base of hook table
51 55 59 C1 04F1 598 ADDL3 R9,R5,R1 ; Get address of loaded mp code
50 85 D0 04F5 599 10$: MOVL (R5)+,R0 ; Fetch address to install hook
0A A1 60 B0 04F8 600 BEQL 20$ ; Done if address is zero
80 80 85 B0 04FA 601 MOVW (R0),10(R1) ; Save normal VMS contents for STOP/CPU
OC A1 60 D0 04FE 602 MOVW (R5)+,(R0)+ ; Move JMP opcode + operand specifier
80 85 59 C1 0501 603 MOVL (R0),12(R1) ; Save normal VMS contents for STOP/CPU
55 06 C0 0505 604 ADDL3 R9,(R5)+,(R0)+ ; Set address
51 10 C0 0509 605 ADDL2 #6,R5 ; Point to next hook
E4 11 050F 606 ADDL2 #16,R1 ; Point to next hook
0003 31 0511 607 BRB 10$ ; Continue installing hooks
0514 608 BRW HOOKS_DONE ; Branch assist for hooks completed
0514 609 ; This code is loaded into the RPB. It is used as a safe place for
0514 610 ; the secondary to wait while the primary does a bugcheck. The first
0514 611 ; longword is modified by the primary after it reboots.
0514 612
00000510 0514 613 .ALIGN LONG
0514 614 RPB_BUGCHK=-4 ; Address of longword that is modified
0514 615 ; by primary and secondary
F9 BF 17 0514 616 MPSS$RPB_WAIT::
0514 617 JMP @RPB_BUGCHK ; RPB loop for secondary to execute
```



```
00000003 0517 618 RPB_LOOPSIZ = .-MPSSRPB_WAIT ; Number of bytes for code for RPB loop
0517 619
0517 620
0517 621 ;
0517 622 ; Now load loop code into the RPB for bugcheck. This must be loaded
0517 623 ; in two steps. First, the loop code is loaded and then the loop address.
0517 624 ;
0517 625 HOOKS_DONE:
0517 626 MOVCL #RPB_LOOPSIZ,W^MPSSRPB_WAIT,RPB$B_WAIT(R6) ; Load JMP loop
0517 627 MOVL RPB$C_HALT(PC(R6),RPB$L_BUGCHK(R6) ; Now start the secondary
0525 628 ; executing at EXE$MPSTART (phys. adr)
0525 629 ;
0525 630 LOCKEND: ; End of locked code
0525 631 ;
0525 632 ; Installation of the multi-processing code is now complete
0525 633 ;
0525 634 INSTALL_DONE:
0525 635 JSB G^INISRDONLY ; Reset protection on system pages
0528 636 SETIPL #0 ; Drop IPL
12 00 DA 0528 MTPR #0,S^#PRS_IPL ; Initialize MA780 for interrupts
50 01 D0 052E 637 BSBW MPSS$MAINIT ; Set status to success
04 0531 638 MOVL #1,R0 ; and return
0534 639 RET
```

```
0535 641 .SBTTL MPSS$UNLOAD - STOP/CPU DCL command
0535 642
0535 643 :++
0535 644 : Functional Description:
0535 645 :
0535 646 : MPSS$UNLOAD is linked together with all of the code required for
0535 647 : multi-processing. This routine causes the secondary processor
0535 648 : to halt and then unloads the multi-processing code (i.e., restores
0535 649 : all the executive hook locations to their original values and
0535 650 : restores the SCB to its single processor VMS values.
0535 651 :
0535 652 : Calling Sequence:
0535 653 :
0535 654 : BRW MPSS$UNLOAD
0535 655 :
0535 656 : Input Parameters:
0535 657 :
0535 658 : EXE$GL_MP - Points to multi-processing code loaded in pool
0535 659 : EXE$GL_RPB - Points to RPB
0535 660 :
0535 661 : Environment:
0535 662 :
0535 663 : Executed by the primary processor.
0535 664 :
0535 665 :
0535 666 :--
0535 667
0535 668 MPSS$UNLOAD::
0535 669 $LKWSET_S INADR=STOPRANGE ; Unload multi-processing code for STOP
                                ; Lock critical code into WS
                                PUSHL #0
                                PUSHL #0
                                PUSHAQ STOPRANGE
                                CALLS #3,G^SYSS$LKWSET
                                BLBC R0,EXIT2 ; Exit if unable to lock pages
                                $CMKRNL_S W^MPSS$UNLOADK ; Execute kernel routine
                                PUSHL #0
                                PUSHAL W^MPSS$UNLOADK
                                CALLS #2,G^SYSS$CMKRNL
                                EXIT2:
                                RET ; Return
                                STOPSTART:
                                OFFC
                                0555 672
                                0555 673
                                0555 674
                                0555 675
                                0555 676
                                0555 677
                                0555 678 MPSS$UNLOADK:: .WORD ^M<R2,R3,R4,R5,R6,R7,R8,R9,R10,R11> ; Entry mask
                                0557 679 SETIPL #IPL$_SYNCH ; Synchronize on primary
                                                MTPR #IPL$_SYNCH,S^#PR$ IPL
                                                #SS$ NORMAL,R0 ; Assume success
                                                G^EXE$GL_MP,R10 ; Is multi-proc code loaded?
                                                5$ ; Br on yes, continue unloading
                                                100$ ; Branch assist
                                                4$: BRW 100$ ; Set STOP request flg
                                                5$: BBSSI #MPSS$V_STOPREQ,MPSS$GL_STOPFLAG(R10),4$ ; Flush cache
                                                10$: BBSSI #LCK$V_INTERLOCK,MPSS$GL_INTERLOCK(R10),15$ ; Is secondary active?
                                                15$: CMPL MPSS$GL_STATE(R10),#MPSS$R_INITSTATE ; Br if not active, no process to return
                                                50$ ; Interrupt secondary with STOP request
                                                MPSS$INTSCND(R10) ; Wait for secondary
                                                20$: JSB #MPSS$V_STOPACK1,MPSS$GL_STOPFLAG(R10),20$ ; Wait for secondary
                                12 08 DA 0557
                                50 01 9A 055A 680 MOVZBL
                                5A 00000000'GF 03 12 055D 681 MOVL
                                006F 31 0564 682 BNEQ
                                F7 0000'CA 00 E6 0566 683 4$: BRW
                                00 0000'CA 00 E6 0569 684 5$: BBSSI
                                05 0000'CA D1 056F 685 10$: BBSSI
                                3F 18 0575 686 15$: CMPL
                                0000'CA 16 057A 687 BGEQ
                                FA 0000'CA 01 E7 057C 688 JSB
                                0580 689 20$: BBCCI #MPSS$V_STOPACK1,MPSS$GL_STOPFLAG(R10),20$ ; Wait for secondary
```



```
00 0000'CA 00 E6 0586 690 BBSSI #LCK$V_INTERLOCK,MPSS$GL_INTERLOCK(R10),30$ ; Flush cache
01 0000'CA D1 058C 691 30$: CMPL MPSS$GL_STATE(R10),#MPSS$R_IDLESTATE ; Is secondary active?
28 13 0591 692 BEQL 50$ ; Br if not active, no process to return
0593 693 ;
0593 694 ; Return process executing on the secondary to the scheduling queues.
0593 695 ;
51 0000'CA D0 0593 696 MOVL MPSS$GL_CURPCB(R10),R1 ; Get PCB address for process
52 0B A1 9A 0598 697 MOVZBL PCB$B_PRI(R1),R2 ; Get current priority of process
00 00000000'GF 52 E2 059C 698 BBSS R2,G^SCH$GL_COMQS,40$ ; Indicate something in sched queue
2C A1 0C B0 05A4 699 40$: MOVW #SCH$C_COM,PCB$W_STATE(R1) ; Indicate process is computable
53 00000000'GF 42 7E 05A8 700 MOVAQ G^SCH$AQ_COMTER2],R3 ; Get tail of queue
93 61 0E 05B0 701 INSQUE (R1),a(R3)+ ; Place process in scheduling queue
0000'CA 06 D0 05B3 702 MOVL #MPSS$K_STOPSTATE,MPSS$GL_STATE(R10) ; Set secondary stopped
14 03 DA 05B8 703 SOFTINT #IPL$_SCHED ; Request primary reschedule
05B8 704 MTPR #IPL$_SCHED,S^#PR$_SIRR
05BB 705 ; Now unload the multi-processing code.
05BB 706 ;
0000'CA 06 D0 05BB 707 50$: MOVL #MPSS$K_STOPSTATE,MPSS$GL_STATE(R10) ; Change INIT state to STOP
0000'CA 16 05C0 708 JSB MPSS$UNHOOK(R10) ; Call routine to unhook MP code
12 02 DA 05C4 709 SETIPL #IPL$_ASTDEL ; Lower IPL for deallocate of pool
50 0000'CA D0 05C7 710 MTPR #IPL$_ASTDEL,S^#PR$_IPL
00000000'GF 16 05CC 711 MOVL MPSS$GL_POOLDSC(R10),R0 ; Set address of block to return
03 50 E9 05D2 712 JSB G^EXE$DEANONPAGED ; Return block of nonpaged pool
50 01 9A 05D5 713 BLBC R0,100$ ; Branch if error
12 00 DA 05D8 714 100$: MOVZBL #SS$_NORMAL,R0 ; Return success code
04 05DB 715 SETIPL #0 ; Restore IPL
05DC 716 MTPR #0,S^#PR$_IPL
05DC 717 RET ;
STOPEND:
```

```
05DC 719 .SBTTL MPSS$UNHOOK - Unhook multi-processing code from system
05DC 720
05DC 721 :++
05DC 722 : Functional Description:
05DC 723 :
05DC 724 : MPSS$UNHOOK is a part of the loadable multi-processing code.
05DC 725 : It unhooks the multi-processing code from the VMS system and
05DC 726 : resets the system to be a single processor 11/780, executing
05DC 727 : a vanilla VMS system.
05DC 728 :
05DC 729 : This code is invoked for two reasons: 1) a STOP/CPU DCL command
05DC 730 : and 2) an invalidate request time-out. It must be loaded into
05DC 731 : pool due to the latter usage.
05DC 732 :
05DC 733 : Calling Sequence:
05DC 734 :
05DC 735 : JSB MPSS$UNHOOK
05DC 736 :
05DC 737 : Input Parameters:
05DC 738 :
05DC 739 : R10 - address of multi-processing code in non-paged pool
05DC 740 :
05DC 741 : Environment:
05DC 742 :
05DC 743 : Executed by the primary processor.
05DC 744 :
05DC 745 : Side-effects:
05DC 746 :
05DC 747 : R0,R1 destroyed. EXE$GL_MP is cleared.
05DC 748 :
05DC 749 :--
05DC 750
00000000 751 .PSECT $AEXNONPAGED, LONG
0000 752 MPSS$UNHOOK::
0000 753 DSBINT
7E 12 DB 0000 MFPR S^#PRS IPL, -(SP) ; Prevent all system events
12 1F DA 0003 MTPR #31, S^#PRS IPL
50 00000000 GF 9E 0006 754 MOVAB G^SCH$GL NULLPCB, R0 ; Get address of null process PCB
50 6C AO DO 000D 755 MOVL PCB$ PHD(R0), R0 ; Get address of null process PHD
38 AO 0000 CA C2 0011 756 SUBL MPSS$GL NULLCPU(R10), PHD$ CPU$TIM(R0) ; Del secondary null time
00000000 GF 16 0017 757 JSB G^INIS$WRITABLE ; Make executive writable
51 0014 CA 9E 001D 758 MOVAB HOOKBASE(R10), R1 ; Get address of exec hook table
50 61 DO 0022 759 60$: MOVL (R1), R0 ; Get address of a hook
50 OD 13 0025 760 BEQL 70$ ; 0 ends the JMP/JSB type hooks
80 0A A1 B0 0027 761 MOVW 10(R1), (R0)+ ; Replace the JMP/JSB opcode
80 0C A1 DO 002B 762 MOVL 12(R1), (R0)+ ; Replace the longword destination
51 10 CO 002F 763 ADDL2 #16, R1 ; Point to next hook in table
51 EE 11 0032 764 BRB 60$ ; Repeat for each hook
51 04 CO 0034 765 70$: ADDL #4, R1 ; Skip the end indicator
50 81 DO 0037 766 80$: MOVL (R1)+, R0 ; Get address of SCB vector changed
60 05 13 003A 767 BEQL 90$ ; 0 ends the SCB vector changes
60 81 DO 003C 768 MOVL (R1)+, (R0) ; Replace SCB vector
00000000 GF D4 0041 769 BRB 80$ ; Repeat for each SCB change
00000000 GF 16 0047 770 90$: CLRL G^EXE$GL_MP ; Reset pointer to multi-proc code
12 8E DA 004D 771 JSB G^INIS$RDONLY ; Restore protection on executive pages
004D 772 ENBINT ; Lower IPL for deallocate of pool
MTPR (SP)+, S^#PRS_IPL
```


MPLOAD
V04-000

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- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
MPSS\$UNHOOK - Unhook multi-processing cod 5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

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05	0050	773	RSB	
	0051	774		
	0051	775		
	0051	776	.END	MPSS\$DCL

; Return to caller

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MPLOAD
Symbol table

G 8

- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

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\$ST2	= 00000004			LOCKRANGE	00000000 R	04
BUSY_STATE_DSC	000000A4	R	04	LOCKSTART	000004E1 R	04
CLISGET_VALUE	*****	X	04	LOC MPM	00000339 R	04
CLIS_IVVERB	= 00038090			MA780_CNCT_ERR	00000271 R	04
DCL_LINE_DSC	00000062	R	04	MA780_NOT_USED	00000269 R	04
DEA-ERR_EXIT	00000306	R	04	MISC_RELOC	000004B8 R	04
DROP_STATE_DSC	000000BF	R	04	MMG\$GL-SBICONF	*****	X 04
DSC\$A_POINTER	= 00000004			MMG\$GL-SPTBASE	*****	X 04
DSC\$B_CLASS	= 00000003			MOVE_CODE	000004D6 R	04
DSC\$K_CLASS_D	= 00000002			MPH\$ASTDELHK	*****	X 02
DYN\$C-LC-MP	= 00000003			MPH\$BUGCHKHK	*****	X 02
DYN\$C-LOADCODE	= 00000062			MPH\$INVALIDHK	*****	X 02
ERR\$-CLMEMUSED	*****	X	04	MPH\$NEWLVLHK	*****	X 02
ERR\$-MA780_REQ	*****	X	04	MPH\$QAST	*****	X 02
ERR\$-SHMDBCUSE	*****	X	04	MPH\$RESCHED	*****	X 02
ERRORX1	00000260	R	04	MPH\$SCHED	*****	X 02
ERRORX2	00000160	R	04	MPM\$-CSR	= 00000000	
ERRORX3	000001AA	R	04	MPM\$-IIR	= 00000020	
ERRORX4	000001B1	R	04	MPM\$-CSR-PORT	= 00000002	
ERRORX5	00000164	R	04	MPM\$V-CSR-PORT	= 00000000	
EX\$ALONONPAGED	*****	X	04	MPM\$V-IIR-CTL	= 00000010	
EX\$CMODEXECX	*****	X	04	MP\$SAC-MPMBASE	*****	X 04
EX\$DEANONPAGED	*****	X	04	MP\$ASTNEWLVL	*****	X 02
EX\$GB-CPUTYPE	*****	X	04	MP\$ASTSCHEDCHK	*****	X 02
EX\$GL-FLAGS	*****	X	04	MP\$S-BEGIN	00000000 RG	02
EX\$GL-MP	*****	X	04	MP\$S-BUGCHECK	*****	X 02
EX\$GL-RPB	*****	X	04	MP\$S-CMODKRN LX	*****	X 04
EX\$GL-SCB	*****	X	04	MP\$S-DCL	00000165 RG	04
EX\$GL-SHBLIST	*****	X	04	MP\$S-END	00000000 RG	03
EX\$GQ-SYSTIME	*****	X	04	MP\$S-GL-CURPCB	*****	X 04
EX\$MP-START	*****	X	04	MP\$S-GL-INTERLOCK	*****	X 04
EX\$V-SSINHIBIT	*****	X	04	MP\$S-GL-ISP	*****	X 04
EXEC_STATE_DSC	000000B0	R	04	MP\$S-GL-MPMIIR	*****	X 04
EXIT	00000229	R	04	MP\$S-GL-NULLCPU	*****	X 05
EXIT2	00000554	R	04	MP\$S-GL-POOLDSC	00000000 RG	02
FOUND-MPM	0000041A	R	04	MP\$S-GL-PRIMSKC	*****	X 04
GETDATA	000001B8	R	04	MP\$S-GL-PRIMSKT	*****	X 04
GET_LINE_DSC	000000E4	R	04	MP\$S-GL-SCBB	*****	X 04
GET-VERB-DSC	000000D7	R	04	MP\$S-GL-STATE	*****	X 04
HOOKBASE	00000014	R	02	MP\$S-GL-STOPFLAG	*****	X 04
HOOKEND	000000AC	R	02	MP\$S-GL-STRIVA	*****	X 04
HOOKS_DONE	00000517	R	04	MP\$S-GQ-MPSTRIM	*****	X 04
IDLE_STATE_DSC	000000CB	R	04	MP\$S-HOOKTBL	0000000C RG	02
ILSTATE-CTL-DSC	00000124	R	04	MP\$S-INT58	*****	X 04
INISRDONLY	*****	X	04	MP\$S-INTSCND	*****	X 04
INISWRITABLE	*****	X	04	MP\$S-INVALID	*****	X 02
INIT_STATE_DSC	00000086	R	04	MP\$S-K-IDLESTATE	= 00000001	
INSTALL_DONE	00000525	R	04	MP\$S-K-INITSTATE	= 00000005	
IPL\$-ASTDEL	= 00000002			MP\$S-K-STOPSTATE	= 00000006	
IPL\$-SCHED	= 00000003			MP\$S-LOAD	0000022D RG	04
IPL\$-SYNCH	= 00000008			MP\$S-LOADK	00000279 RG	04
IRP\$B-TYPE	= 0000000A			MP\$S-MAINIT	*****	X 04
IRP\$W-SIZE	= 00000008			MP\$S-PINTSR	*****	X 04
LCK\$V-INTERLOCK	= 00000000			MP\$S-QAST	*****	X 02
LIB\$PDT-OUTPUT	*****	X	04	MP\$S-RESCHED	*****	X 02
LOCAL_MEM_ERR	00000261	R	04	MP\$S-RESCHEDIPL5	*****	X 04
LOCKEND	00000525	R	04	MP\$S-RPB-WAIT	00000514 RG	04

MPLOAD
Symbol table

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- LOAD AND CONNECT CODE FOR MULTIPROCESS 16-SEP-1984 02:05:53 VAX/VMS Macro V04-00
5-SEP-1984 02:06:41 [MP.SRC]MPLOAD.MAR;1

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MPSS\$SCHED	*****	X	02
MPSS\$INTSR	*****	X	04
MPSS\$UNEXPINT	*****	X	04
MPSS\$UNHOOK	00000000	RG	05
MPSS\$UNLOAD	00000535	RG	04
MPSS\$UNLOADK	00000555	RG	04
MPSS\$V_STOPACK1	= 00000001		
MPSS\$V_STOPREQ	= 00000000		
NDTS\$MPMO	= 00000040		
OUTPUT_BUFFER	00000014	R	04
OUTPUT_BUF_DSC	0000005A	R	04
OUTPUT_LENGTH	00000010	R	04
PCBS\$B_PRI	= 0000000B		
PCBS\$L_PHD	= 0000006C		
PCBS\$W_STATE	= 0000002C		
PHDS\$L_CPUTIM	= 00000038		
PR\$ IPL	= 00000012		
PR\$ SIRR	= 00000014		
PTE\$S_PFN	= 00000015		
PTE\$V_PFN	= 00000000		
RPBS\$B_CONFREG	= 00000090		
RPBS\$B_WAIT	= 00000100		
RPBS\$L_BOOTR5	= 00000030		
RPBS\$L_BUGCHK	= 000000FC		
RPBS\$L_HALTPC	= 00000010		
RPBS\$V_MPM	= 0000000B		
RPBS\$V_USEMPM	= 0000000C		
RPB_BUGCHK	= 00000510	R	04
RPB_LOOPSIZ	= 00000003		
SCB\$AL_BASE	*****	X	04
SCB_IPC14	00000088	R	02
SCB_IPL16	00000090	R	02
SCB_LOOP	0000032F	R	04
SCB_VEC94	00000098	R	02
SCB_VECBC	000000A0	R	02
SCH\$AQ_COMT	*****	X	04
SCH\$C_COM	= 0000000C		
SCH\$GL_COMQS	*****	X	04
SCH\$GL_NULLPCB	*****	X	05
SET_PHYS	0000047A	R	04
SHOW_CPU	000001CE	R	04
SS\$_DEVOFFLINE	= 00000084		
SS\$_NORMAL	= 00000001		
SS\$_SHMNOTCNCT	= 0000037C		
START_CPU	000001B2	R	04
STATES	0000006E	R	04
STATE_CTL_DSC	000000F1	R	04
STATE_VALUE	0000006A	R	04
STOPEND	000005DC	R	04
STOPRANGE	00000008	R	04
STOPSTART	00000555	R	04
STOP_CPU	000001B5	R	04
STOP_STATE_DSC	00000098	R	04
SYSS\$CMKRN	*****	GX	04
SYSS\$FAO	*****	X	04
SYSS\$LKWSET	*****	GX	04
VAS\$VPN	= 00000015		

VAS\$ VPN
XDELIBRK

= 00000009
***** X 04

+-----+
! Psect synopsis !
+-----+

PSECT name	Allocation	PSECT No.	Attributes
ABS	00000000 (0.)	00 (0.)	NOPIC USR CON ABS LCL NOSHR NOEXE NORD NOWRT NOVEC BYTE
\$AB\$\$	00000000 (0.)	01 (1.)	NOPIC USR CON ABS LCL NOSHR EXE RD WRT NOVEC BYTE
\$\$\$\$\$BEGIN	000000AC (172.)	02 (2.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC PAGE
END	00000000 (0.)	03 (3.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC PAGE
MPLOAD	000005DC (1500.)	04 (4.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC LONG
\$EXNONPAGED	00000051 (81.)	05 (5.)	NOPIC USR CON REL LCL NOSHR EXE RD WRT NOVEC LONG

+-----+
! Performance indicators !
+-----+

Phase	Page faults	CPU Time	Elapsed Time
Initialization	35	00:00:00.08	00:00:00.80
Command processing	136	00:00:00.87	00:00:05.33
Pass 1	464	00:00:17.71	00:00:43.37
Symbol table sort	0	00:00:02.80	00:00:05.53
Pass 2	165	00:00:03.78	00:00:08.57
Symbol table output	22	00:00:00.22	00:00:00.84
Psect synopsis output	3	00:00:00.03	00:00:00.03
Cross-reference output	0	00:00:00.00	00:00:00.00
Assembler run totals	827	00:00:25.49	00:01:04.47

The working set limit was 1800 pages.
101303 bytes (198 pages) of virtual memory were used to buffer the intermediate code.
There were 100 pages of symbol table space allocated to hold 1786 non-local and 25 local symbols.
781 source lines were read in Pass 1, producing 26 object records in Pass 2.
37 pages of virtual memory were used to define 35 macros.

+-----+
! Macro library statistics !
+-----+

Macro library name	Macros defined
-\$255\$DUA28:[MP.OBJ]MP.MLB;1	4
-\$255\$DUA28:[SYS.OBJ]LIB.MLB;1	15
-\$255\$DUA28:[SYSLIB]STARLET.MLB;2	12
TOTALS (all libraries)	31

1914 GETS were required to define 31 macros.

There were no errors, warnings or information messages.

MACRO/LIS=LIS\$:MPLOAD/OBJ=OBJ\$:MPLOAD MSRC\$:MPPREFIX/UPDATE=(ENH\$:MPPREFIX)+MSRC\$:MPLOAD/UPDATE=(ENH\$:MPLOAD)+EXECMLS/LIB+LIB\$:MP.ML

0248 AH-BT13A-SE
VAX/VMS V4.0

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