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Military electronics

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DRAM-controller ICs

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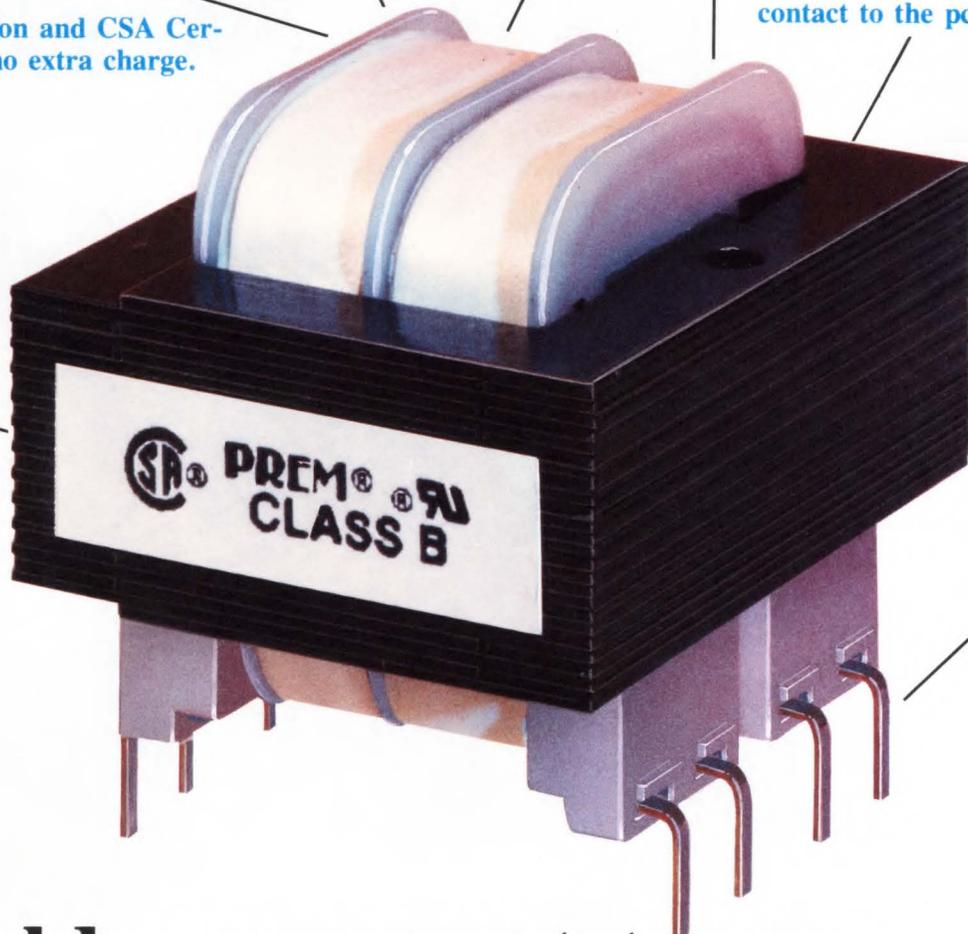
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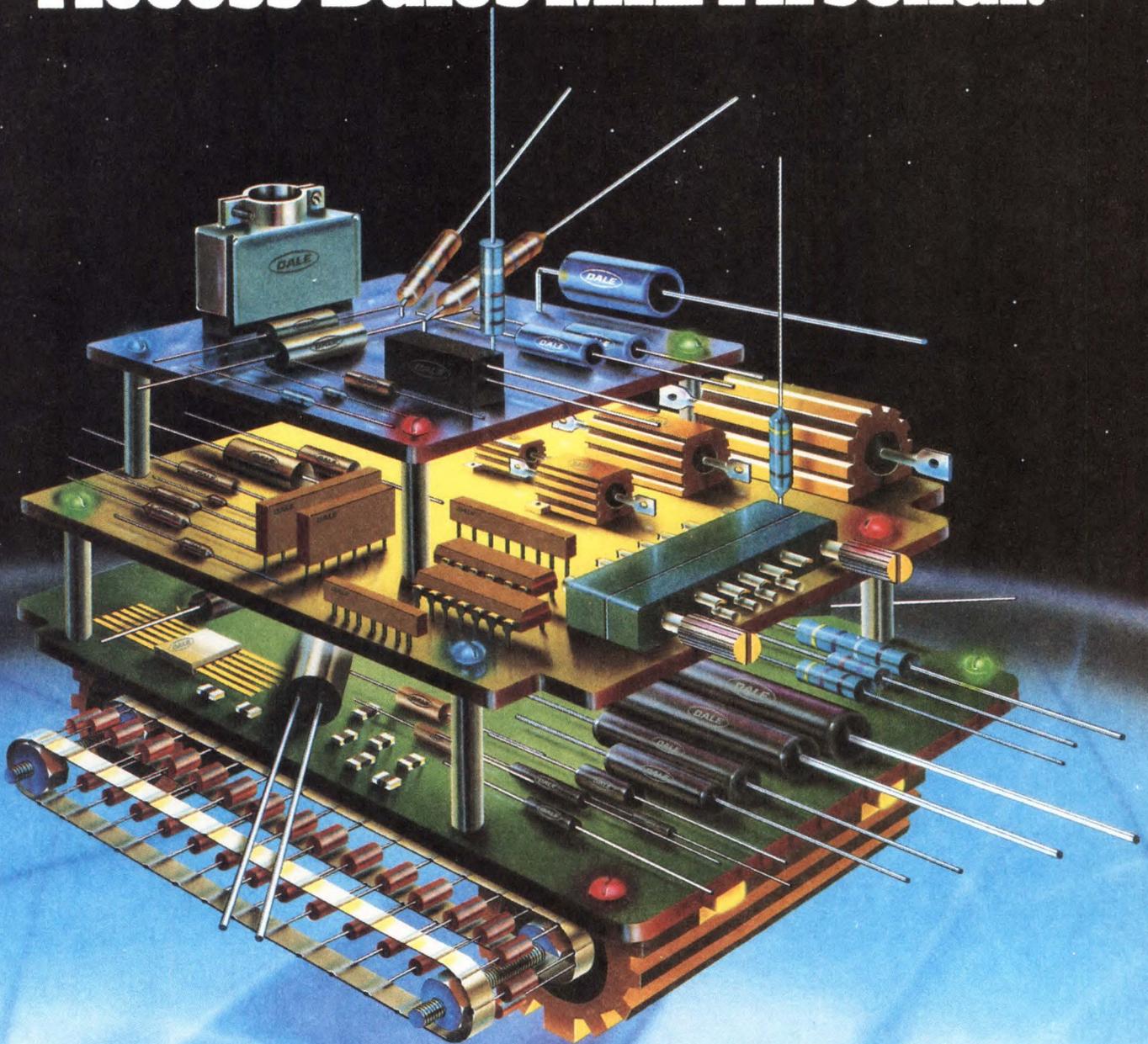
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SPECIFICATIONS

Pin. Model	KSW-2-46	KSWA-2-46
Connector Version	ZFSW-2-46	ZFSWA-2-46
FREQ. RANGE	dc-4.6 GHz	dc-4.6 GHz
INSERT. LOSS (db)	typ max	typ max
dc-200MHz	0.9 1.1	0.8 1.1
200-1000MHz	1.0 1.3	0.9 1.3
1-4.6GHz	1.3 1.7	1.5 2.6
ISOLATION (dB)	typ min	typ min
dc-200MHz	60 50	60 50
200-1000MHz	45 40	50 40
1-4.6GHz	30 23	30 25
VSWR (typ)	ON 1.3:1 OFF —	1.3 1.4
SW. SPEED (nsec)		
rise or fall time	2(typ)	3(typ)
MAX RF INPUT (bBm)		
up to 500MHz	+17	+17
above 500MHz	+27	+27
CONTROL VOLT.	-5V on, 0V off	-5V on, 0V off
OPER./STOR TEMP.	-55° to +125°C	-55° to +125°C
PRICE (1-24)	\$32.95 \$72.95	\$48.95 \$88.95

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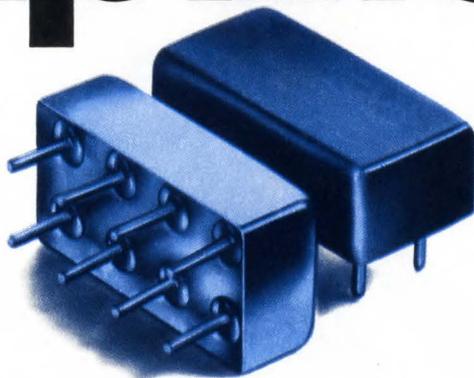
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MODEL	FREQ. RANGE (MHz) f_L to f_U	GAIN dB min flatness ^{††}	MAX. OUT/PWR [†] dBm	NF dB (typ)	DC PWR 12V, mA	PRICE \$ ea. (5-24)
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MAN-2	0.5-1000	19 1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28 1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10 0.8	15	3.7	70	15.95

^{††}Midband $10f_L$ to $f_U/2$, $\pm 0.5\text{dB}$ [†]1dB Gain Compression ◇Case Height 0.3 in.
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C118 REV. B



On the cover: Manufacturers are working to make flat-panel displays that are suitable for more and more complex applications, while improving performance levels and lowering their cost. See pg 138. (Photo courtesy Cherry Electrical Products)

SPECIAL ISSUE: MILITARY ELECTRONICS

SPECIAL REPORT

Flat-panel displays 138

The technology and manufacturing processes for flat-panel displays are changing fast—particularly for large-area displays with expanded information content. In choosing a model, however, you need to consider other aspects too.—*Dave Pryce, Associate Editor*

DESIGN FEATURES

Simulation helps you design radiation-hard circuits for space 161

You no longer need to use guesswork, rules of thumb, or prohibitively expensive test protocols to predict the effects of manmade and naturally occurring radiation on spaceborne electronic assemblies.—*Kevin Walsh, Electrical Engineering Software Inc and Gary Lum, PhD, Lockheed Missiles and Space Co Inc*

Peer-to-peer protocol facilitates real-time communications 179

The low communications overhead of the CSMA/DCR peer-to-peer protocol makes it desirable for real-time network applications.—*Deif N Atallah, Intel Corp*

Testability is crucial in PLD-circuit design 191

Compared with standard logic parts, PLDs tend to have higher defect rates and require a larger investment in test-program development. As a result, engineers must make testability a prime design goal.—*Peter de Bruyn Kops, Anvil Software*

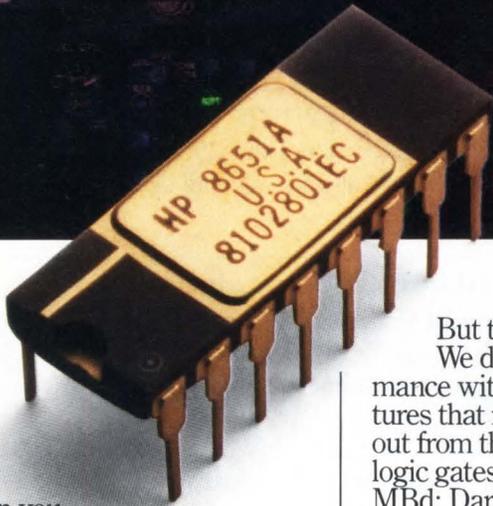
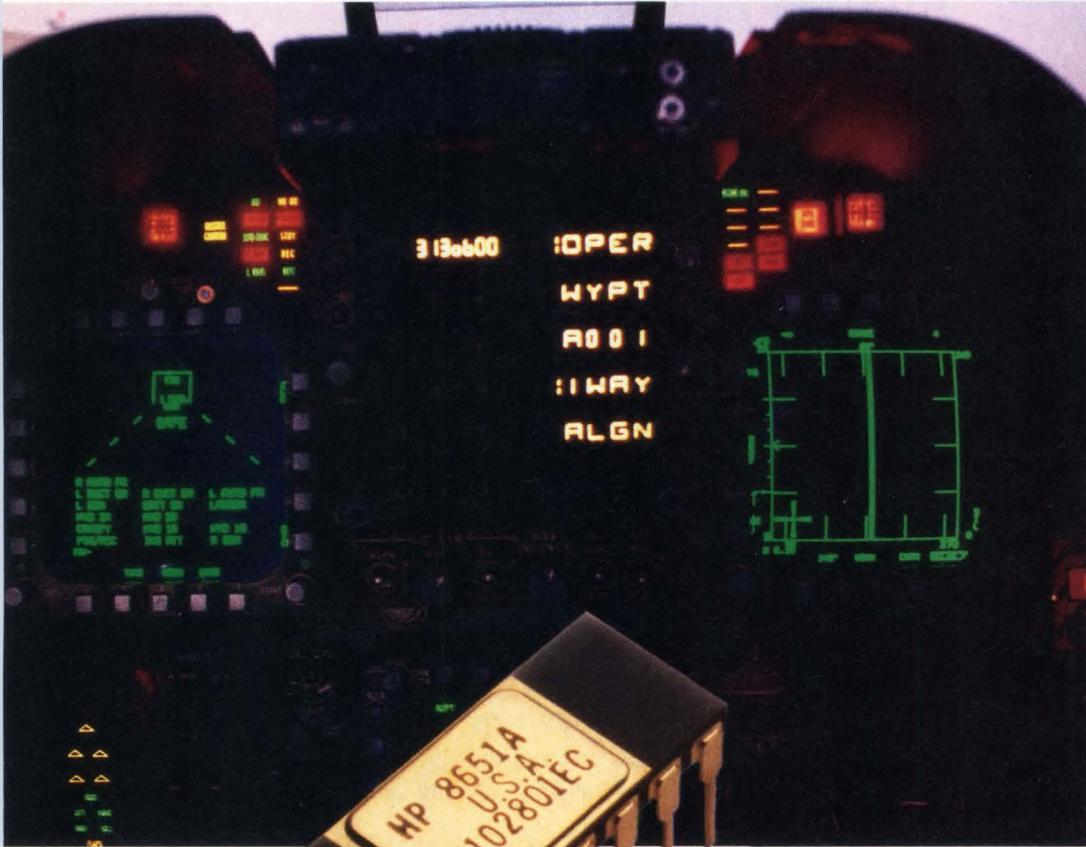
Retargetable tools ease microprogramming of SIMD processors 205

You can improve your single-instruction, multiple-data processors dramatically by using effective organization and management techniques. Retargetable tool sets help you program these massively concurrent processors conveniently and inexpensively.—*Robert A Mueller and Daniel R Benua, Quantitative Technology Corp*

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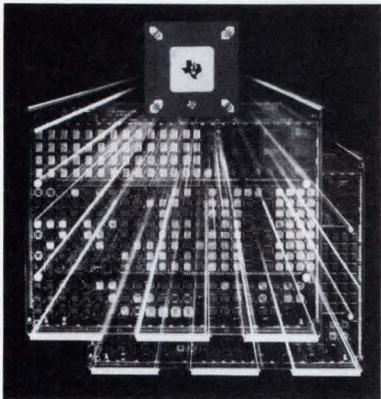
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You no longer need a supercomputer to run AI-related programs: many such programs will run on modest machines such as the IBM PC/AT and compatibles (pg 71).

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TECHNOLOGY UPDATE

PC-based development products move AI out of the classroom, into the workplace 71

Artificial intelligence (AI) was the dreamchild of the 50s—or perhaps it was Aladdin's lamp, which would release a genie of unlimited power and wisdom.—Chris Terry, Associate Editor

Dynamic-RAM-controller ICs squeeze maximum performance from DRAMs 91

Despite this year's acute parts shortage and the subsequent price increase, dynamic RAMs (DRAMs) still cost less than static RAMs (SRAMs) on a bit-by-bit basis, and they still take up less room on your pc board.—Steven H Leibson, Regional Editor

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else Count := 0;
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International trade problems may force us to give our Asian trade partners a taste of their own medicine.

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Design firms: A little bit of engineering heaven.—*Deborah Asbrand, Associate Editor*

LOOKING AHEAD

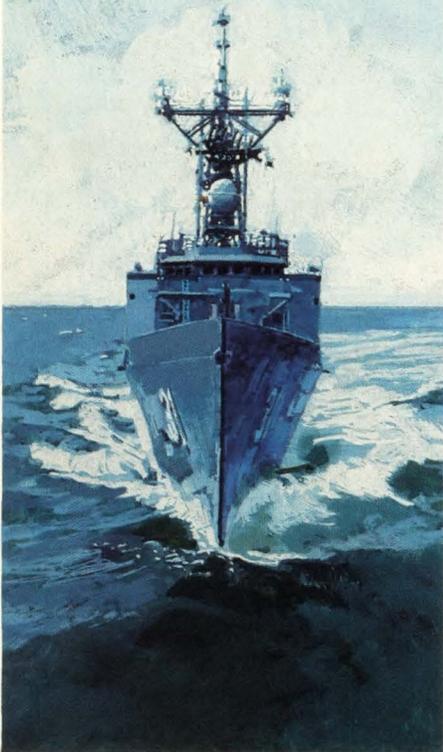
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Manufacturers praise JIT logistics . . . \$20B market predicted for smart network equipment.

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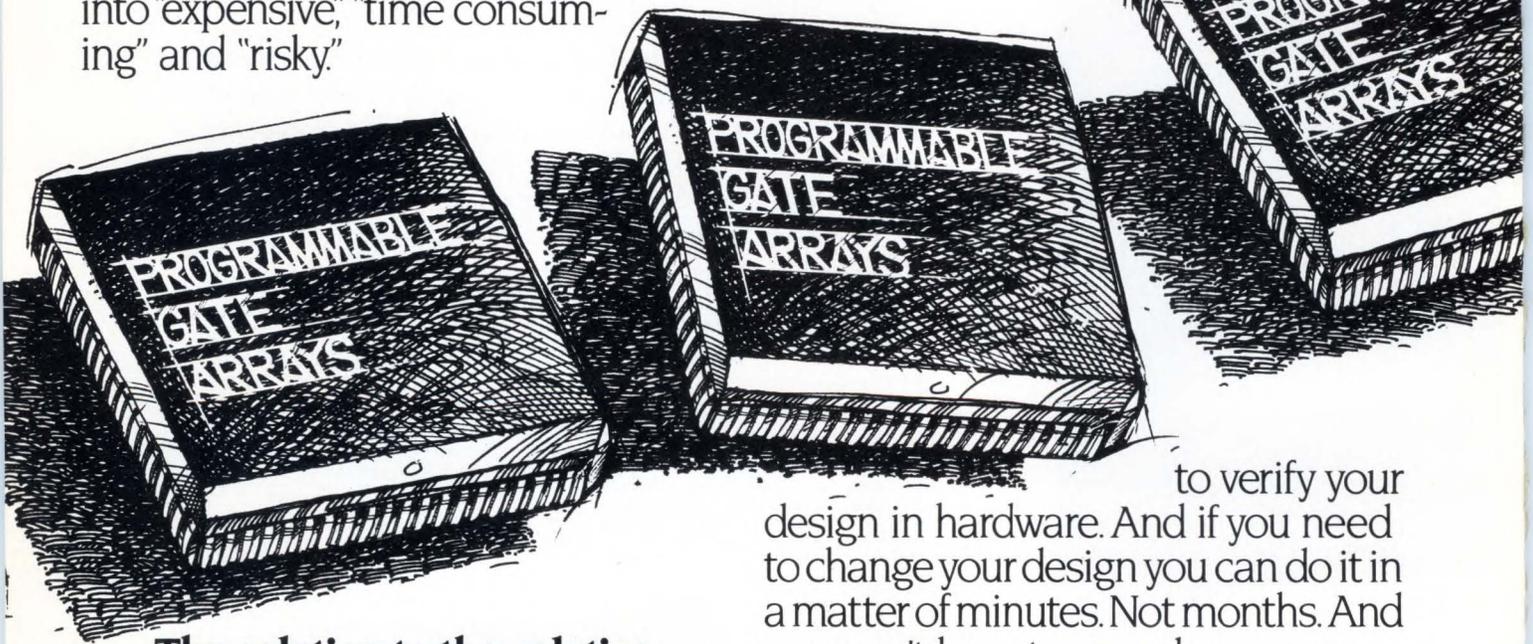
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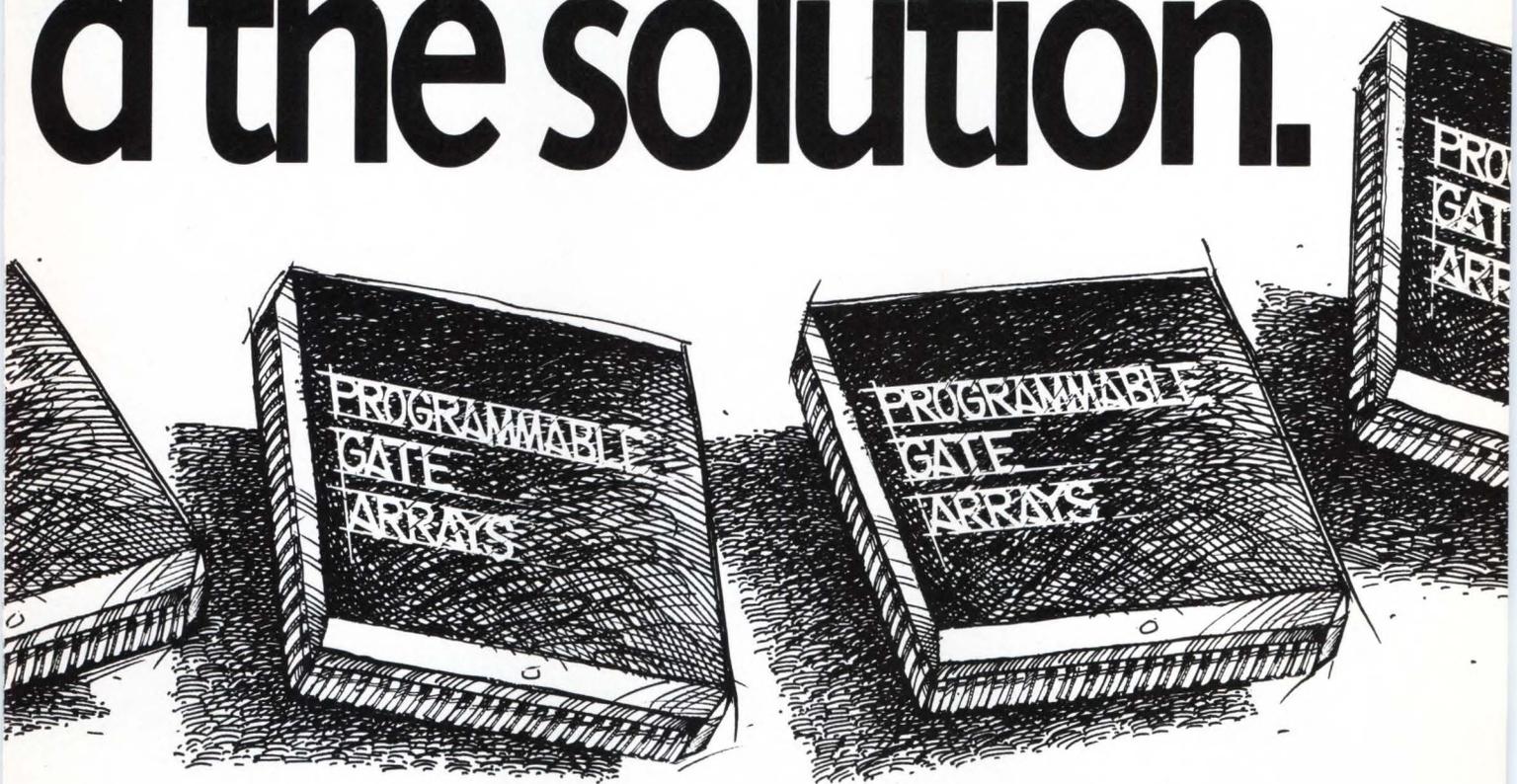
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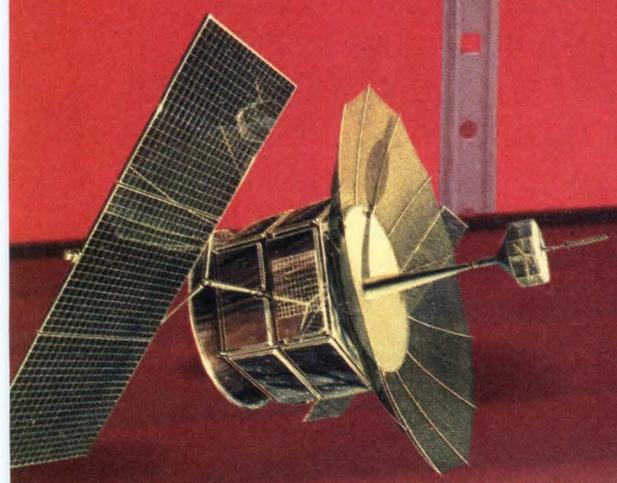
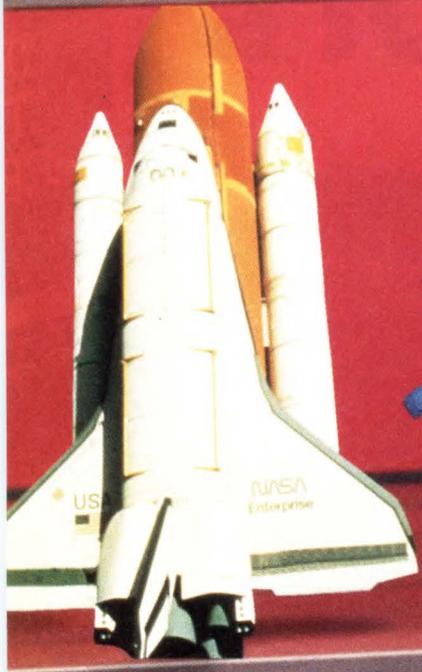
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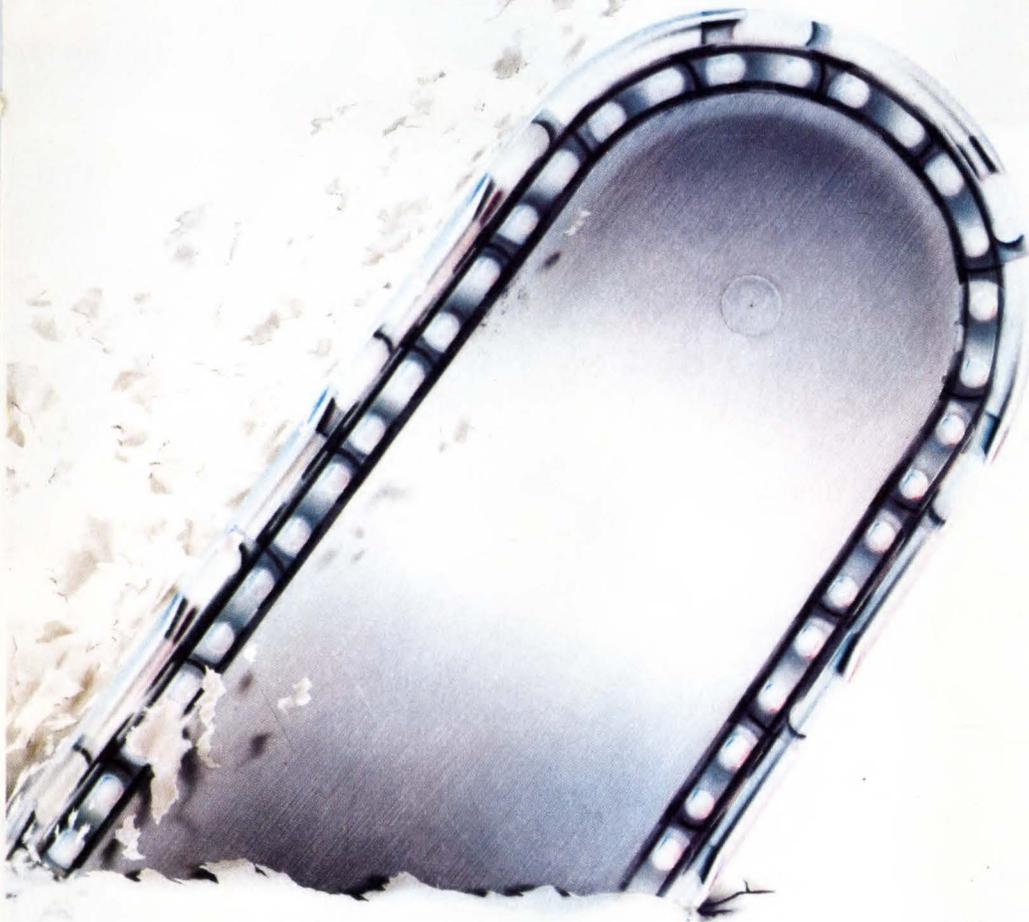
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* Sometimes called Rocky Mountain BASIC or BASIC 5.0.

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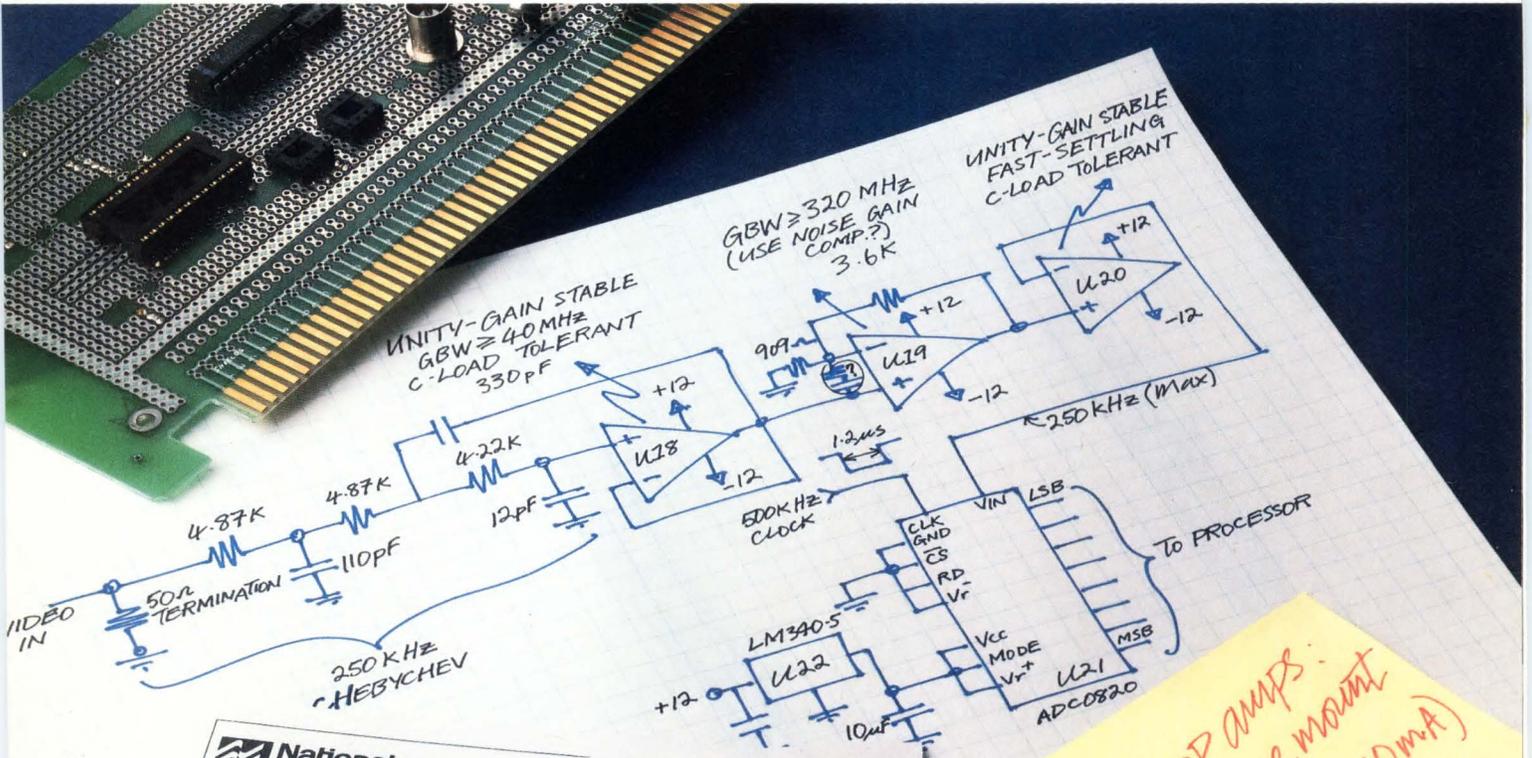
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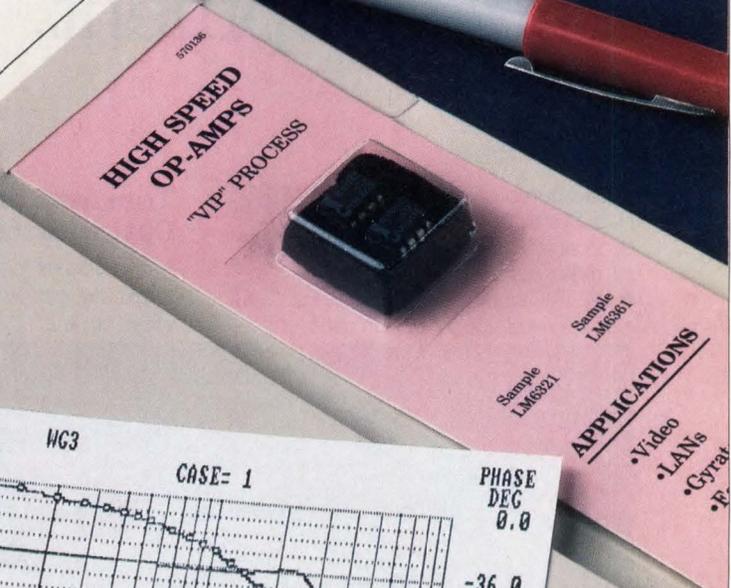
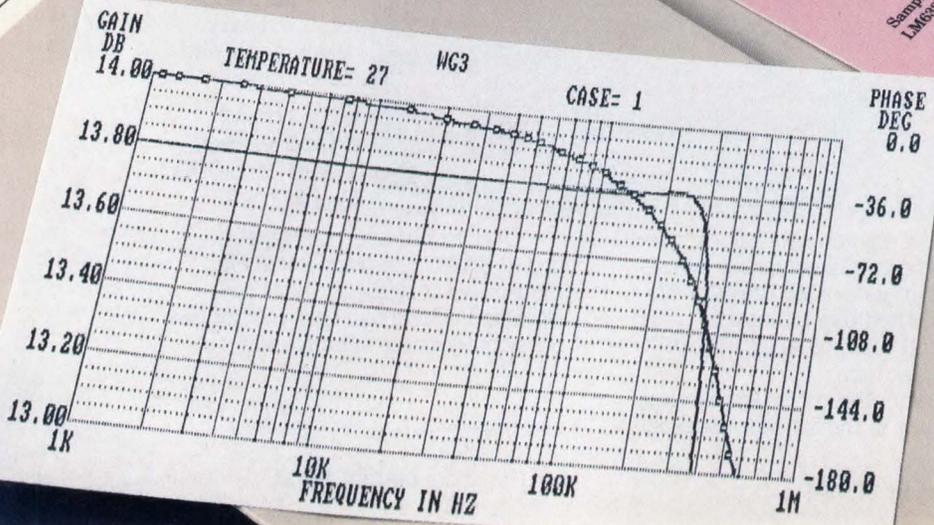


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General Description
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These new op amps feature slew rates of 300 V/μs and gain-bandwidth products up to 750 MHz.

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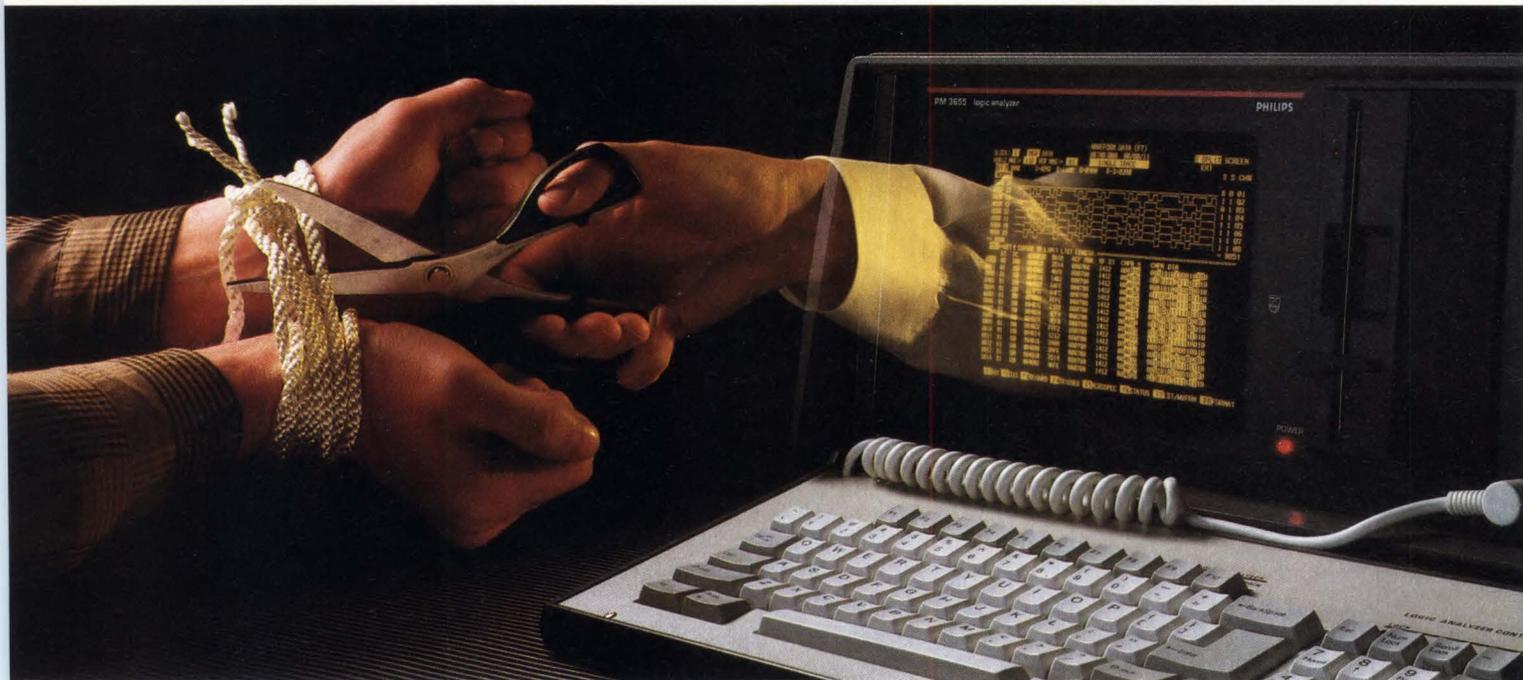
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NEWS BREAKS

EDITED BY JOANNE CLAY

MOSFET COMBINES HIGH POWER WITH LOW DRIVE REQUIREMENTS

The APT5010FN, a 500V power MOSFET from Advanced Power Technology (Bend, OR, (503) 382-8028), delivers 50A of usable current and features input capacitance of 6000 pF—about half the drive requirement of conventional MOSFETs configured for comparable currents, according to the manufacturer. Designed for power-supply and motor-control circuits in military and commercial systems, the device features 0.1 Ω on-resistance. The MOSFET is fabricated on a 338 \times 588-mil die and is available in a hermetically sealed package and in a die version (APT5010DN). The units are available with full military screening. The packaged and die versions cost \$149.88 (1000) and \$66.20, respectively. Delivery is four to six weeks.—Tom Ormond

POWER RECTIFIERS FEATURE 50-NSEC RECOVERY TIME

The 5A USC130X power rectifier from Semtech (Newbury Park, CA, (805) 498-2111) features a 50-nsec reverse recovery time at 200V, 300V, and 400V. (The X in the part number can be 4, 5, or 6, designating 200V, 300V, or 400V, respectively.) The hermetically sealed, subminiature, axially leaded parts are also available in a 2A version, the USC110X. Prices start at \$4 (OEM qty).—Margery S Conner

RF GENERATOR SENDS LONG-WAVE SIGNALS THROUGH UHF

Priced at only \$195 and providing an output range from 100 kHz to 150 MHz, the Model 2005 RF Signal Generator from B&K Precision (Chicago, IL, (312) 889-1448) offers you six fundamental bands and 450 MHz on harmonics. You can modulate the amplitude of the generator's output via an internal 1-kHz source, or you can do it externally by using any audio frequency. The 2005 can perform step and variable output attenuation to 40 dB, as well as variable amplitude modulation from 0 to 100%. The unit has a separate output for an external frequency counter and an RF connection. An antibacklash vernier dial gives you output-frequency control to within 3%.—J D Mosley

JFET OP-AMP FAMILY YIELDS HIGH SPEED AND LOW POWER

Texas Instruments' (Dallas, TX, (800) 232-3200) TL050 Enhanced-JFET op amps reduce input-offset voltage (V_{IO}) shifts to 60 μ V (typ) without resorting to metal packaging. They provide higher slew rates and lower input-bias-current requirements than do standard bipolar devices. The devices are pin-compatible with industry-standard JFET op amps, and you can choose a 15 or 2V/ μ sec minimum slew rate with a maximum V_{IO} ranging from 0.8 to 4.0 mV.—J D Mosley

8-BIT HALF-FLASH ADC INCLUDES TRUE SAMPLE/HOLD AMPLIFIER

The LTC1099 from Linear Technology Corp (Milpitas, CA, (800) 637-5545) is a half-flash 8-bit A/D converter that converts in 2.5 μ sec. A true sample/hold amplifier is included on the chip; it allows the ADC to convert 5V p-p signals at as much as 167 kHz, or signals with slew rates as high as 20V/ μ sec. The LTC1099 is pin compatible with the AD7820 and the ADC0820; these older devices can complete the A/D conversion in 1.5 μ sec, but have pseudo-S/H amplifiers that can accept signals with a maximum slew rate of 0.1V/ μ sec or a bandwidth limit of 7 kHz. (To acquire signals with higher frequencies, these older devices require an external S/H amplifier, which is usually expensive.) The LTC1099 costs \$8 (100).—David Shear

NEWS BREAKS

VME BUS SINGLE-BOARD COMPUTER INTEGRATES PERIPHERAL CONTROL

The Liberator-SBC single-board VME Bus computer is the only one to include so many functions on a single board, claims its vendor, Integrated Solutions (San Jose, CA, (408) 943-1902). Other products require as many as five boards to implement the same functions. The board includes a 16- or 20-MHz 68020 coupled with a 68851 paged memory-management unit and a 68881 floating-point unit. Its memory comprises 4M bytes of 1-wait-state RAM, 64k bytes of 2-wait-state EPROM, and 32 bytes of EEPROM. The board also includes an Ethernet interface, two synchronous/asynchronous serial ports, a synchronous or asynchronous SCSI port, 1024x768-pixel graphics with 16 colors, an 8-bit DAC with a 20-kHz bandwidth, and a battery-backed clock/calendar function. The board costs \$5995.—Doug Conner

STANDARD CREATES SET OF COMMON CALLS FOR 88000 OPERATING SYSTEMS

A trial-use binary compatibility standard (BCS) published by the 88open Consortium Ltd (Stratham, NH, (603) 778-3001) establishes a common set of basic, system-level calls for executable and binary programs written for systems based on Motorola's 88000 μ P. The 66 BCS calls define standard services an operating system can provide to an application program, including file I/O, process creation, and interprocess communications. The consortium's BCS defines a subset of calls taken from AT&T's proposed Unix application binary interface (ABI); AT&T has informally indicated to the 88open BCS committee that it intends to use the BCS as the basis for an 88000- μ P Unix ABI. Copies of 88open's BCS publication cost \$100.—Steven H Leibson

FLOATING-POINT MATH CHIP HELPS BREAK I/O BOTTLENECKS

The ADSP-3264 64-bit floating-point math chip from Analog Devices (Norwood, MA, (617) 329-4700) will incorporate an architecture that permits either eight 32-bit or four 64-bit internal data transfers per cycle. The transfers involve moving data to and from an internal register file, an arithmetic-logic unit (ALU), and a multiplier-divider unit. Packaged in a 280-pin ceramic pin-grid array (PGA), the chip will run at 15.6 MHz. That clock frequency translates into a 31M-flops rate—one floating-point operation per clock cycle in the ALU and one operation in the chip's multiplier. A 64-bit double-precision division operation requires 768 μ sec.

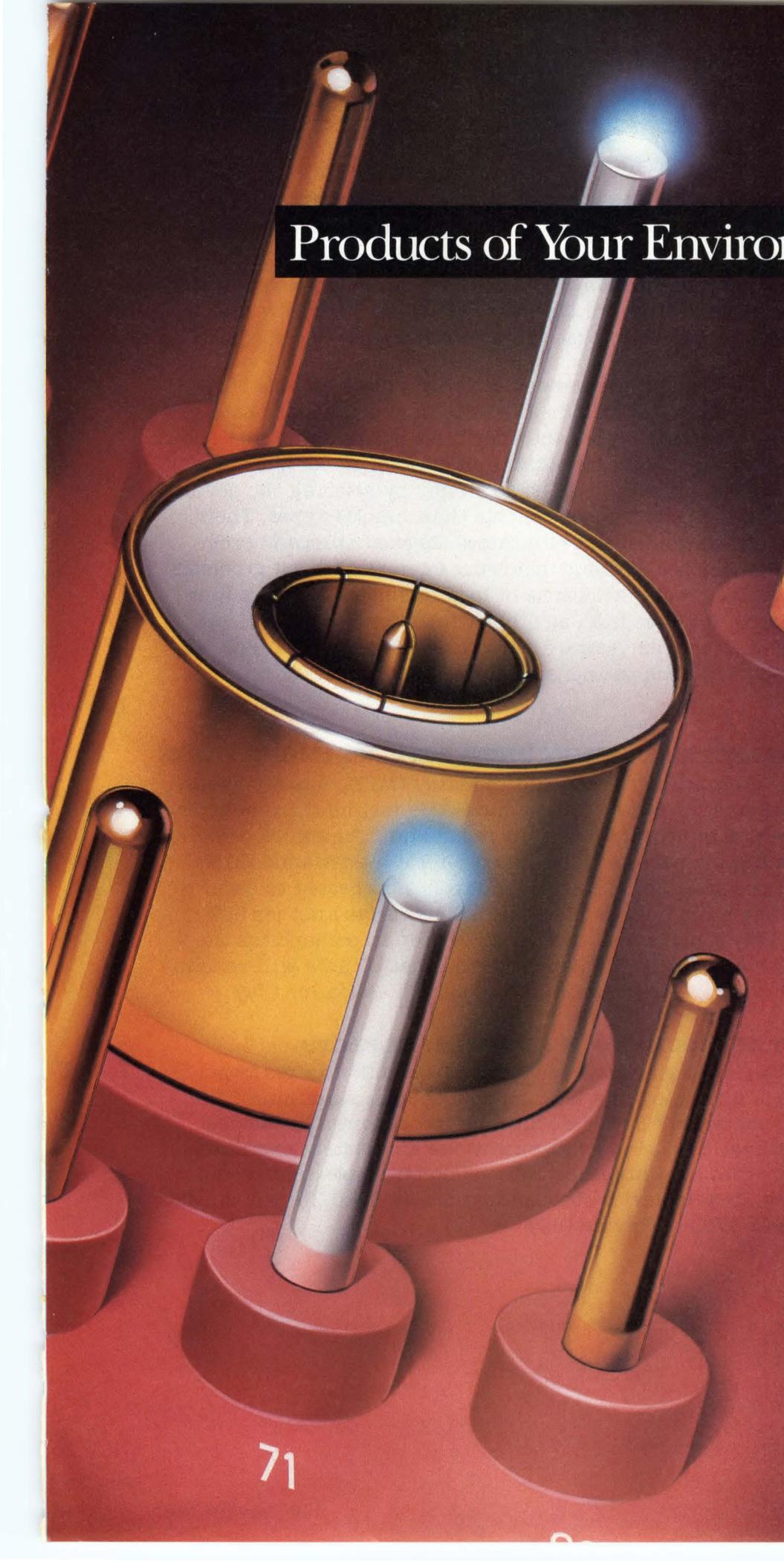
The chip performs standard IEEE-754 single- and double-precision floating-point math operations as well as 32-bit 2's-complement and 32-bit unsigned fixed-point manipulations. Samples are \$545 (1000); they should be available in October. The manufacturer expects to offer production quantities during the second quarter of 1989.—Jon Titus

PLD-DEVELOPMENT TOOL GETS NEW PRIMARY SOURCE

CUPL, the PLD-development software heretofore marketed by Personal CAD Systems, is now a product of Logical Devices Inc (LDI) (Fort Lauderdale, FL, (305) 974-0975). LDI will assume all of P-CAD's existing CUPL maintenance agreements. CUPL, which lists for \$1250, runs under MS-DOS, Unix, and VMS.—Dan Strassberg

DIGITAL ENCODERS PROVIDE DIRECT μ P INTERFACE

Available in 2-, 4-, or 5-bit versions, the EV and EH Series encoders from Allen-Bradley (El Paso, TX, (800) 592-4888 or (800) 292-4888) may eliminate the need for A/D conversion in your design application. The devices offer panel potentiometer capabilities, continuous rotation, and as many as 36 electrical positions per revolution; they range in price from \$1.39 to \$1.51 (1000).—J D Mosley



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CIRCLE NO 36

NEWS BREAKS: INTERNATIONAL

RF MOS POWER TRANSISTORS OUTPERFORM BIPOLAR TYPES

Offering significant performance advantages in comparison with high-frequency bipolar power transistors, the BLF series of MOS power transistors from Philips Components Div (Eindhoven, The Netherlands, TLX 51573) is suitable for use in the output stages of HF and VHF transmitters. In the near future, the company plans to extend the range with power transistors that can operate at UHF.

Among the currently available transistors are devices with power ratings of between 2 and 300W. These transistors feature noise figures in duplex mode that are typically 7 dB less than those of bipolar types, and they offer power gains that are as much as 4 dB higher than bipolar types. In addition, it's easier to control the power level of a MOS transistor because you can do so simply by altering the device's gate bias voltage. MOS transistors are also more reliable than bipolar types. Their negative drain-current temperature coefficient eliminates thermal runaway problems and allows you to parallel devices without incurring current-sharing problems. In addition, the MOS devices have greater tolerance of load mismatch (lower-power devices withstand an all-phases VSWR as high as 50:1 at full rated power without damage), and they have less of a tendency toward parasitic oscillation. The BLF145, an 8W, 28-MHz device in a SOT-123 package, sells for around gld 60 (100).

—Peter Harold

DEMAND FOR DRAMs EXPECTED TO SHIFT FROM 256k- TO 1M-BIT PARTS

The Japanese Ministry of International Trade and Industry (MITI) has reportedly predicted a decline in the demand for 256k-bit dynamic RAMs for the third quarter of 1988. The demand is expected to drop 1% from the second-quarter figure. Meanwhile, MITI also predicted a big increase in the demand for 1M-bit dynamic RAMs. The 40-million-part demand projected for the second quarter is expected to swell to almost 53 million pieces in the third quarter. The ministry expects another 35% increase in demand for the 1M-bit parts and another 3.3% drop in demand for the 256k-bit DRAMs in the fourth quarter. MITI also projected that DRAMs will remain in short supply even though vendors are increasing production.—Joanne Clay

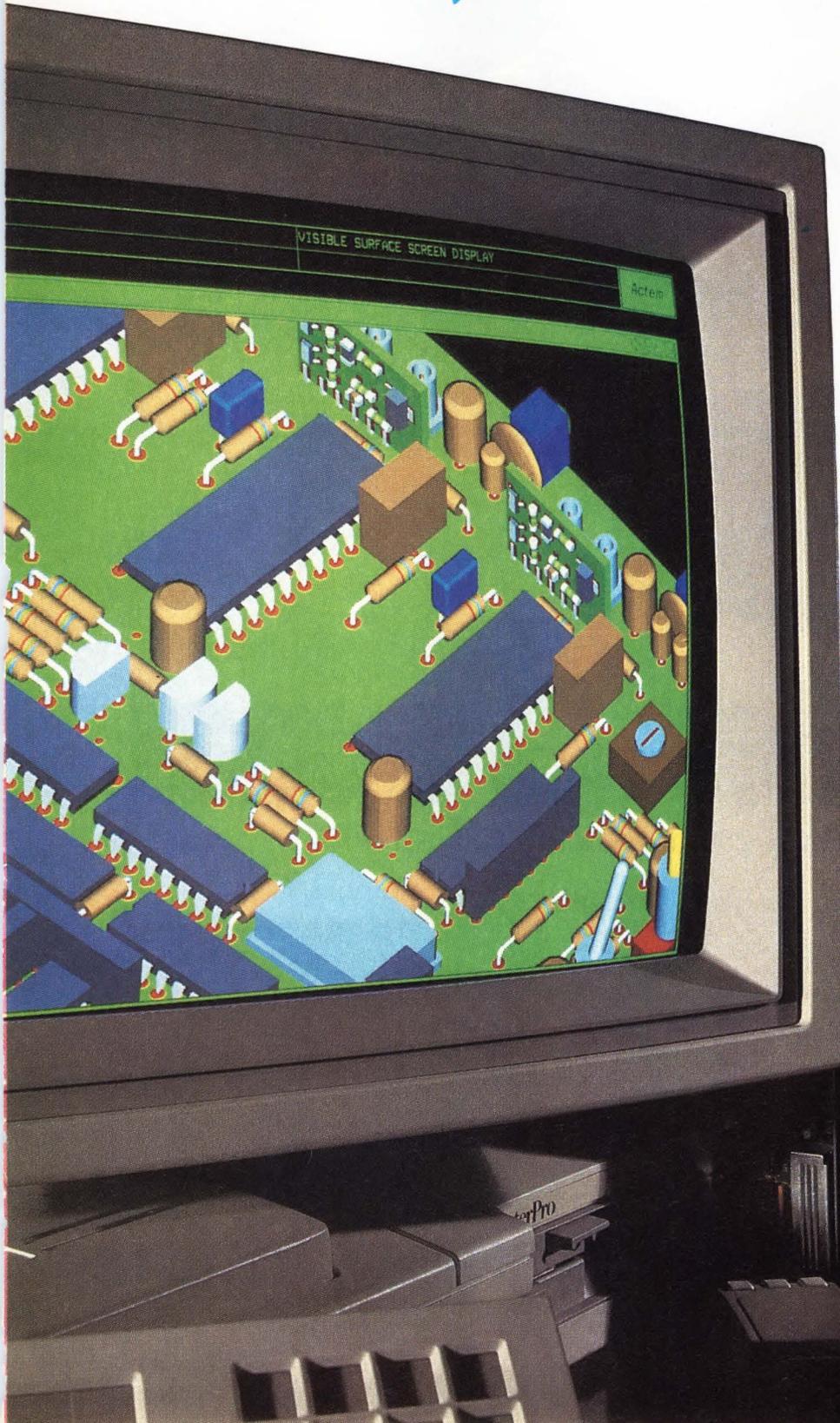
32-BIT FLOATING-POINT COPROCESSOR REACHES 6.7M FLOPS

The MuPD72691 32-bit floating-point math coprocessor from NEC can perform 6.7M flops. The chip, which is fabricated in a 1.2- μ m, double-layer-aluminum CMOS process, operates with the company's V Series 32-bit microprocessors. The device can perform high-speed arithmetic floating-point operations and matrix operations in one command, a capability that's essential for 3-dimensional-image display and manipulation. Samples of the 16-MHz device cost approximately \$615; for the 20-MHz part, the sample price is about \$769.—Joanne Clay

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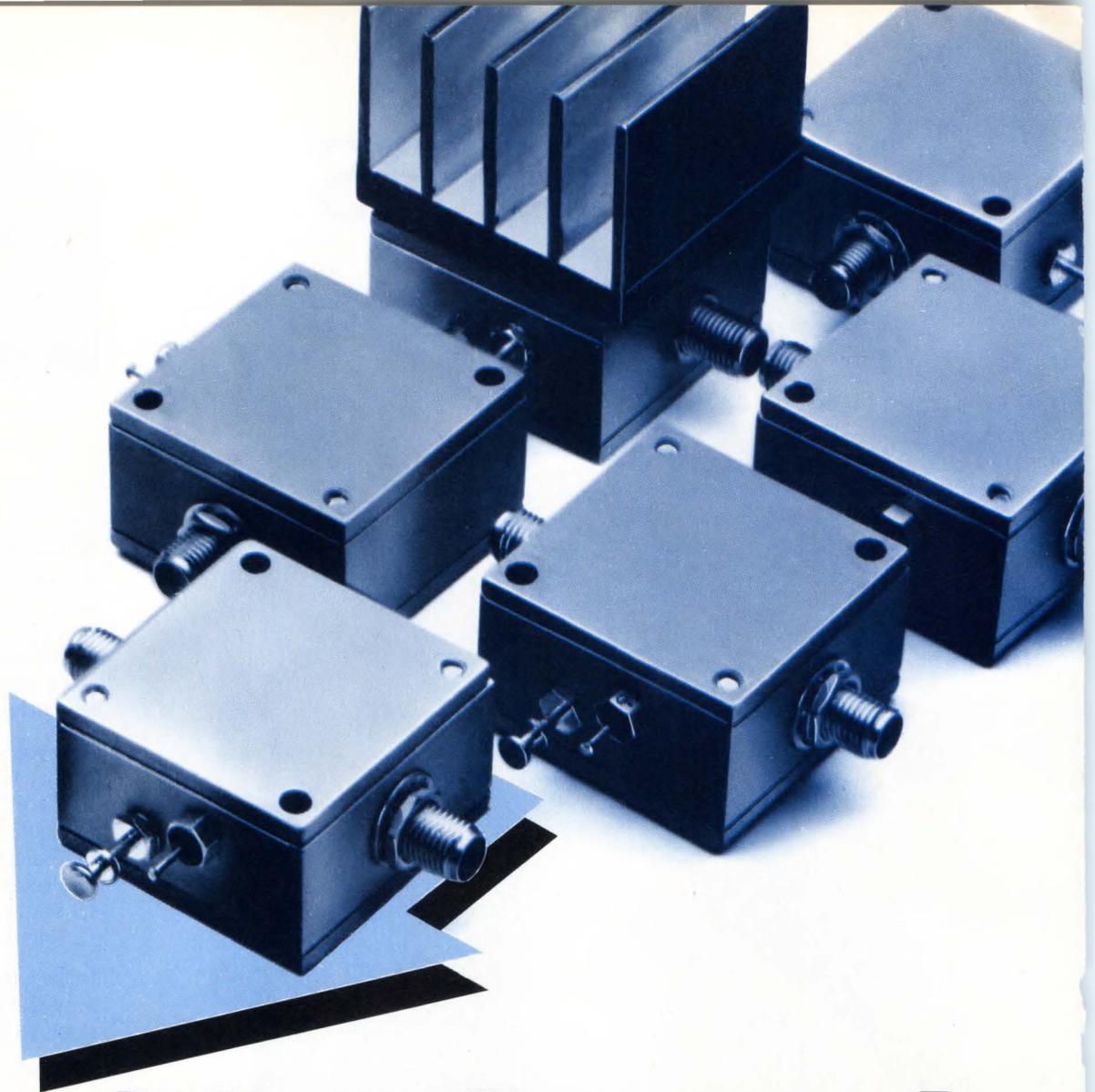
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ZFL-500LN	0.1-500	24	+5	2.9	79.95	1-24
ZFL-750	0.2-750	18	+9	6.0	74.95	1-24
ZFL-1000	0.1-1000	17	+9	6.0	79.95	1-24
ZFL-1000G*	10-1000	17	+3	12.0	199.00	1-9
ZFL-1000H	10-1000	28	+20	5.0	219.00	1-9
ZFL-500HLN	10-500	19	+16	3.8	99.95	1-24
ZFL-1000LN	0.1-1000	20	+3	2.9	89.95	1-24
ZFL-1000VH	10-1000	20	+25	4.5	229.00	1-9
ZFL-2000	10-2000	20	+17**	7.0	219.00	1-9

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LOW PASS	Model	*LP-	10.7	21.4	30	50	70	100	150	200	300	450	550	600	750	850	1000
Min. Pass Band (MHz) DC to			10.7	22	32	48	60	98	140	190	270	400	520	580	700	780	900
Max. 20dB Stop Frequency (MHz)			19	32	47	70	90	147	210	290	410	580	750	840	1000	1100	1340

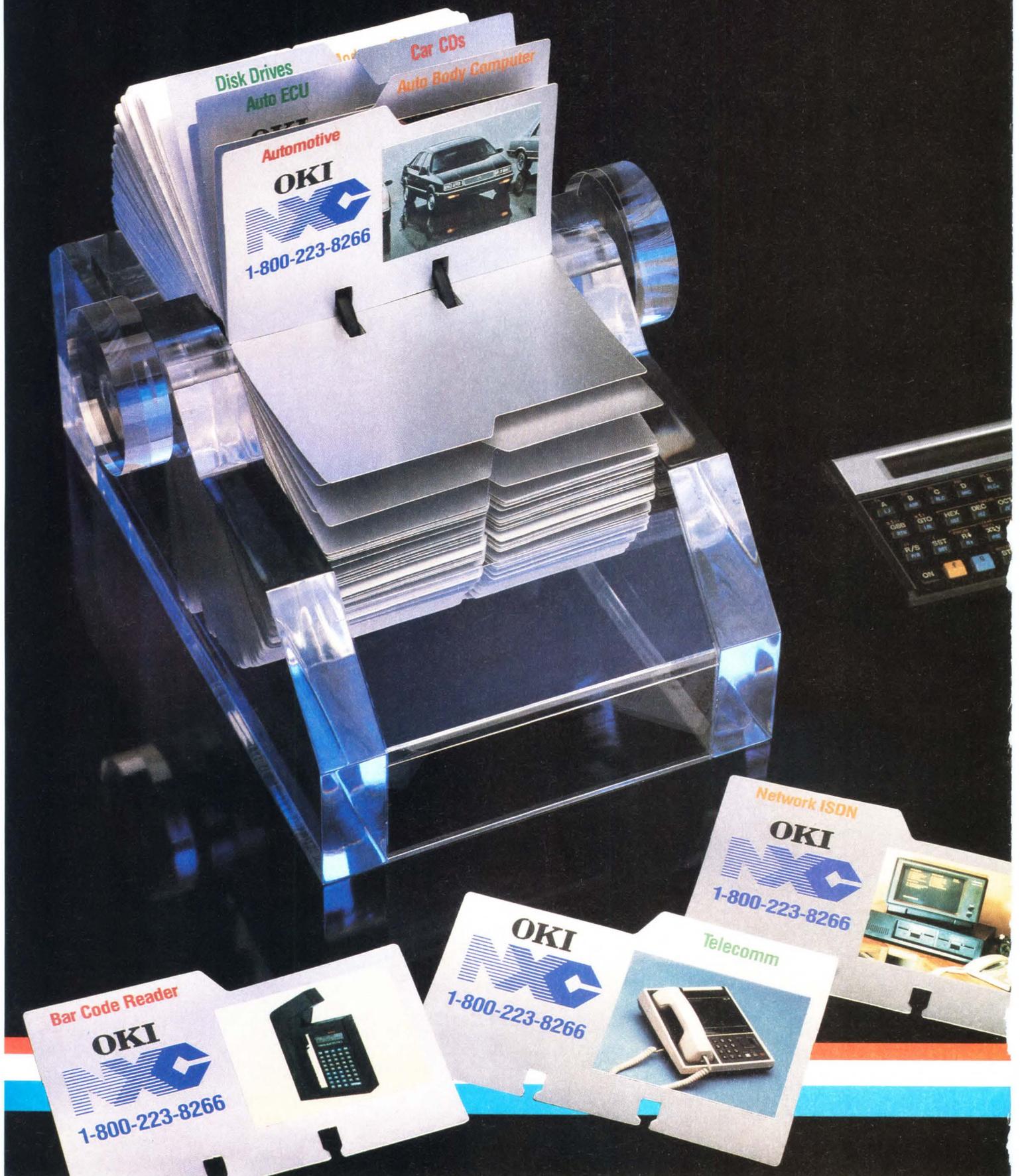
Prices (ea.): P \$9.95 (6-49), B \$24.95 (1-49), N \$27.95 (1-49), S \$26.95 (1-49)

HIGH PASS	Model	*HP-	50	100	150	200	250	300	400	500	600	700	800	900	1000
Pass Band (MHz)			41	90	133	185	225	290	395	500	600	700	780	910	1000
	start, max.		41	90	133	185	225	290	395	500	600	700	780	910	1000
	end, min.		200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
Min. 20dB Stop Frequency (MHz)			26	55	95	116	150	190	290	365	460	520	570	660	720

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*Prefix P for pins, B for BNC, N for Type N, S for SMA *example: PLP-10.7*

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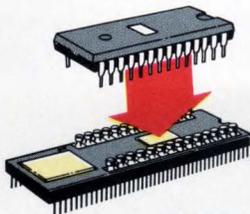
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SIGNALS & NOISE

Swap amplifier leads to make thermocouple work

I'd like to correct some errors in the schematic I submitted with the Design Idea "Electronic thermometer has 10-mV/°F output" (EDN, April 28, 1988, pg 237). To make the thermocouple thermometer work correctly, you must swap the leads to the amplifier: You hook the thermocouple lead to pin 3 and connect the other wire from the bridge circuit to ground. The accompanying figure shows a corrected version of the circuit.

If you reduce the gain of the amplifier to 100 (by changing R_2 from 1 M Ω to 100 k Ω), the output of the thermometer will be 1 mV/°F, so the thermometer will be able to read temperatures as high as 1800°F. Note, however, that there will be a 2% error in the temperature readings above 660°F.

Bill Donofrio
Moore Research Center
Grand Island, NY

Self-modifying code poses unacceptable risk

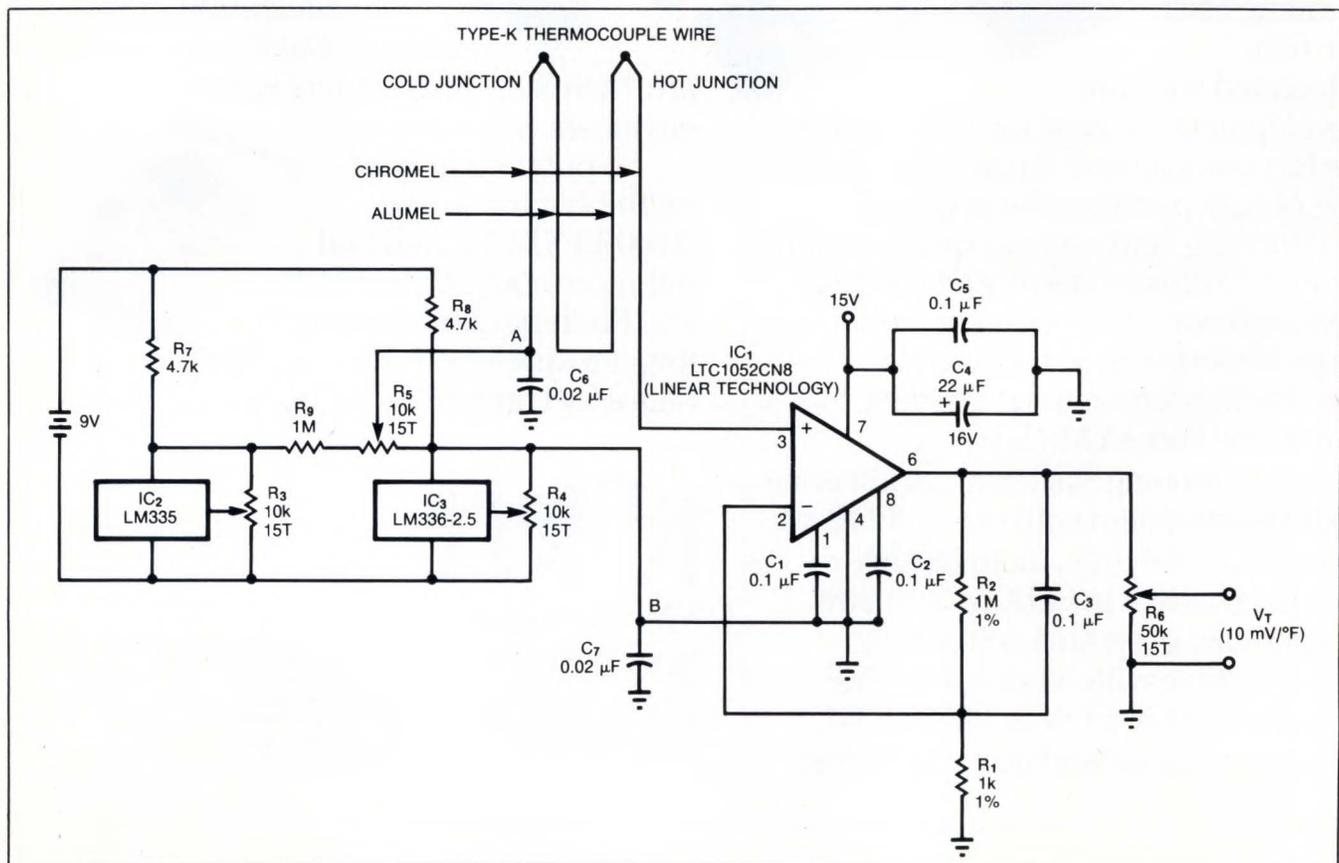
I am writing to express my shock at the Design Idea "Alterable code enhances instructions" by Noor Singh Khalsa (EDN, May 12, 1988, pg 210). I hope that Mr Khalsa takes what follows as criticism of his assumptions and ideas rather than as criticism of him as a person or as a professional engineer. In fact, my criticism is most sharply pointed to the editors of EDN for admitting the design to the magazine's pages.

The very heart of Mr Khalsa's Design Idea is self-modifying code —on a microprocessor that seems to be designed to prevent just that. Do engineers who attempt this practice realize that code and data have been separated by the designers of the 8031 because they are two entirely different kinds of things? Code acts and data is acted upon. To confuse the two by executing data or by modifying code as it runs is to commit an error so grave as to destroy

the very possibility of software design.

What automated design tool, what paper-and-pencil formal design could possibly have been used to generate this kind of code? Do engineers who add that little OR gate in Mr Khalsa's design realize what horrors lie behind the door they've just opened? Are they certain that the next line of code, or the next, or the next will not, under some untested machine state, unintentionally clobber some other line of code?

And to what effect? Will I be a passenger on an aircraft whose avionics software incorporates this design? Are missiles now being prevented from destroying my family by this kind of software? In fact, outside of school, is there any software these days that does not have a serious intent? And if there isn't, should we not simply and firmly state that this design poses an unacceptable risk?



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CIRCLE NO 49

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SIGNALS & NOISE

Let me ask another question from a purely selfish standpoint. As a software designer whose job sometimes requires me to interface assembly code to a high-order language, what kind of questions am I likely to get from my customer now that you've revealed self-modifying code as the latest state of the art?

I can't help thinking that our customer, on reading this Design Idea, not realizing the profound sense of outrage it causes for professional software designers, will use it as a justification for making life more difficult for us.

Self-modifying code indeed! EDN should realize that the third digit of this year is an 8 and not a 6.

*Bob Crispin
Decatur, AL*

Design Idea corrections

I'd like to thank you for your acceptance of my Design Idea "Signal-powered switch connects devices" (EDN, April 14, 1988, pg 227) and point out a few errors in the published schematic:

- The signal ground on the DTE side should be labeled pin 7;
- V⁺ of the MBR2045CT is pin 2;
- Pin 8 of the Si7661 should be connected to V⁺.

In response to inquiries I've received, I'd like to mention that the DG509s are bidirectional analog switches, so it's possible to operate the circuit in the opposite direction (that is, to connect one printer to four PCs) if you make appropriate changes to the diode connections. Also, the diode packs are Motorola parts, and the voltage inverter is from Siliconix.

*James Dean
Herzberg Institute of Astrophysics
National Research Council
Canada
Ottawa, Ontario, Canada*

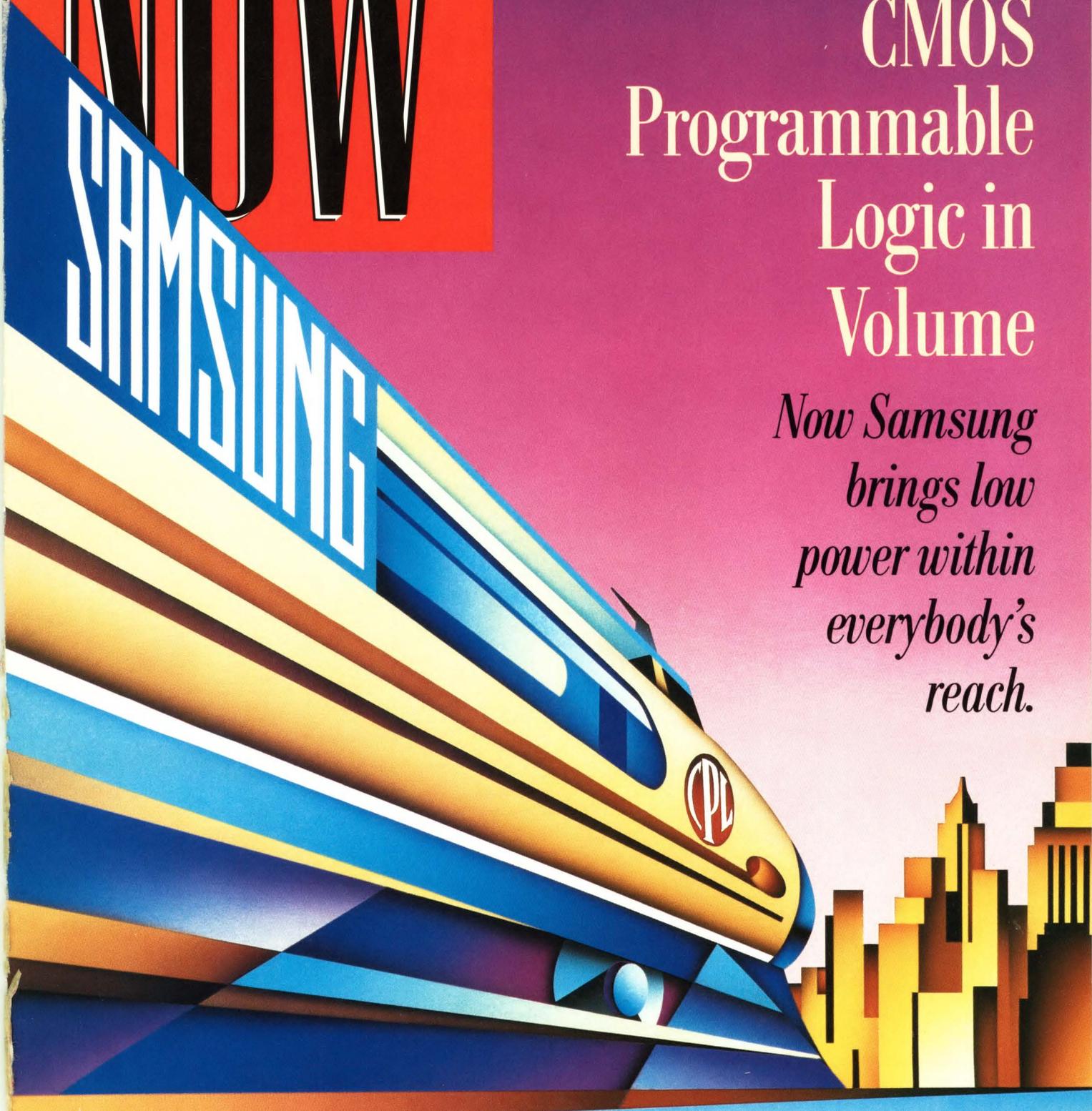
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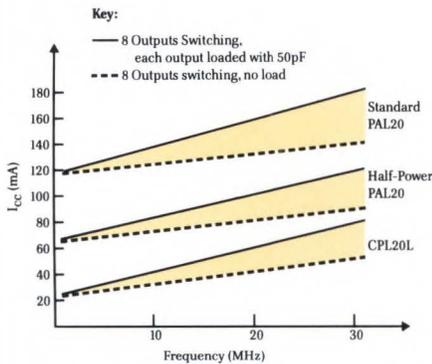
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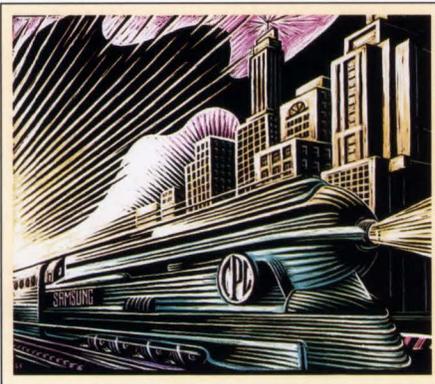
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126	244	368	468*
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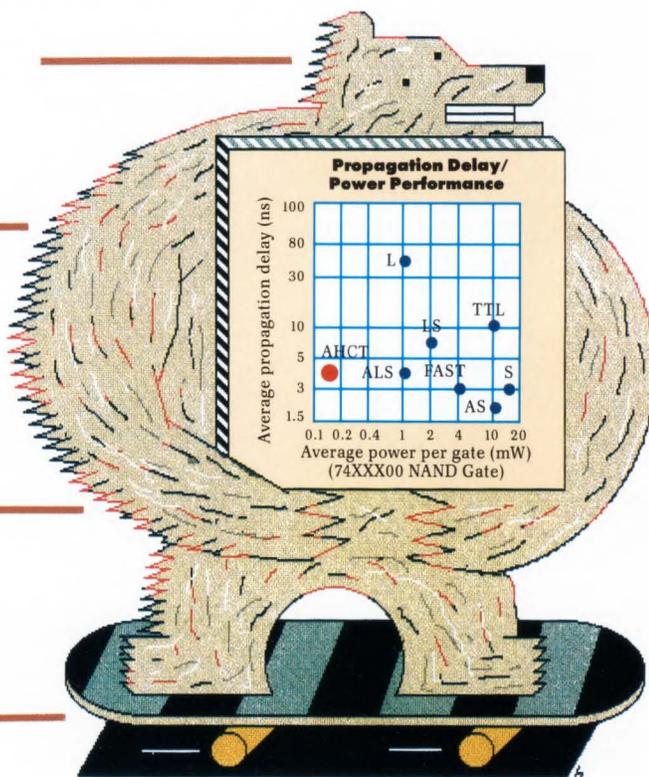
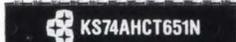
164	194	299	596*
165	195	595	597
166			

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TRC (read cycle time)	200 ns	200 ns
TWC (write cycle time)	2-5 ms/byte	2-5 ms/byte
VCC	5V \pm 10%	5V \pm 10%
Page mode	Yes	Yes
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Data retention	10 years	10 years
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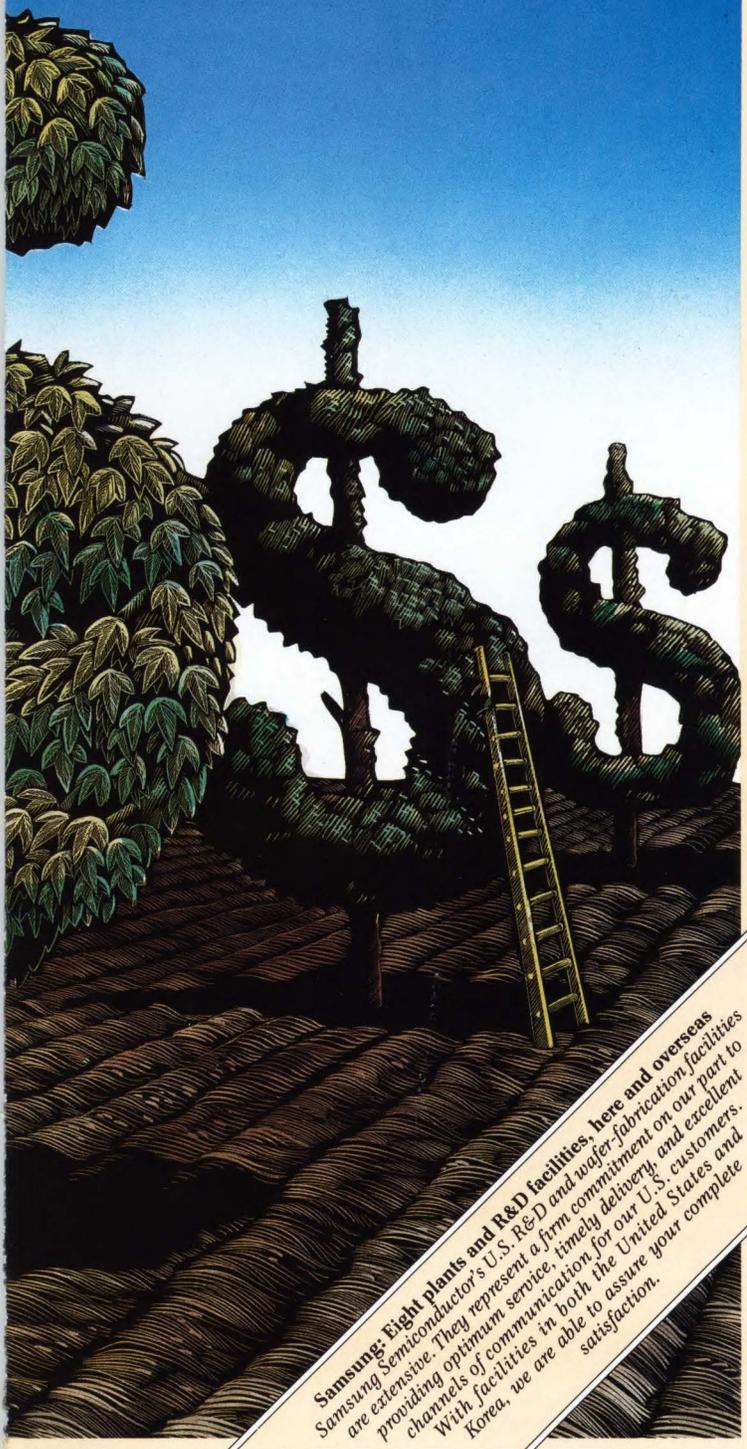
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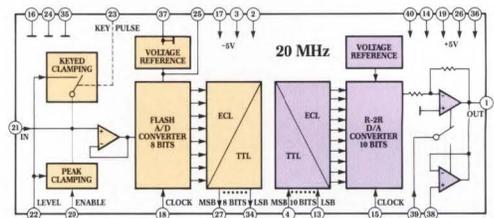
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KSV3110N-9	8 bits	10 bits	±1/2 LSB	±1 LSB	20 MSPS	
KSV3110N-8	8 bits	10 bits	±1/2 LSB	±2 LSB	20 MSPS	
KSV3110N-7	8 bits	10 bits	±1/2 LSB	±4 LSB	20 MSPS	
KSV3100AN-8	8 bits	10 bits	±1/2 LSB	±2 LSB	20 MSPS	UVC3101
KSV3100AN-7	8 bits	10 bits	±1/2 LSB	±4 LSB	20 MSPS	UVC3101

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KAD0820ACN	8 bits		±1/2 LSB		1.5 μsec	ADC0820BCN
KAD0820AIN	8 bits		±1/2 LSB		1.5 μsec	ADC0820BCJ
KAD0820BCN	8 bits		±1 LSB		1.5 μsec	ADC0820CCN
KAD0820BIN	8 bits		±1 LSB		1.5 μsec	ADC0820CCJ
KAD0808IN	8 bits		±1/2 LSB		100 μsec	ADC0808CCN
KAD0809IN	8 bits		±1 LSB		100 μsec	ADC0809CCN
KDA0800CN		8 bits		±1/2 LSB	*100 nsec	DAC0800LCN
KDA0801CN		8 bits		±1 LSB	*100 nsec	DAC0801LCN
KDA0802CN		8 bits		±1/4 LSB	*100 nsec	DAC0802LCN
KDA0806CN		8 bits		±2 LSB	*150 nsec	DAC0806LCN
KDA0807CN		8 bits		±1 LSB	*150 nsec	DAC0807LCN
KDA0808CN		8 bits		±1/2 LSB	*150 nsec	DAC0808LCN
KS7126CN	3-1/2 digit		±1/2 LSB		333 msec	TSC7126
KS25C02		CMOS 8-bit successive approx. register				DM2502
KS25C03		CMOS 8-bit successive approx. register				DM2503
KS25C04		CMOS 12-bit successive approx. register				DM2504

*Settling Time

AND IN OP AMPS, REGULATORS, COMPARATORS, TIMERS, AND MORE.



Across the entire spectrum of high-volume linear devices, in fact, Samsung—being a manufacturing leader—offers a combination of reliability and competitiveness in price that has given these devices tremendous acceptance in the marketplace.

It's a market we're strongly committed to, and we have more than 250 industry-standard ICs available for immediate delivery now.

If by chance you *aren't* buying linear devices from Samsung, it will make sense for you to look into us.

SOLUTIONS TAILORED TO SPECIFIC HIGH-VOLUME NEEDS. FOR THOSE WHO SIMPLY NEED MORE.



A particular specialty that Samsung offers in linear is in the area of specific, rather simple solutions tailored to certain very high-volume applications.

We have developed devices for use in such high-volume areas as telephones, car stereo, and household appliances—among many others.

If you have a need for a high-volume, tailored linear device on this order, we may have the device you need—and if we don't, we'd like to talk about making

it for you.

Our line of simple speech synthesis chips—designed for use primarily in electronic toys and answering machines—is one particular example of the kind of low-cost solution we can offer.

To learn about others, please contact us.

Our Speech Synthesizers.

Part	Function	Application
KS5901A	Voice synthesizer (external ROM)	Sound information answering machines
KS5902XX	Voice synthesizer (internal ROM)	Toys; simple sound generation
KS5911	Voice recording and reproducing (talking back type)	Talk-back answering machines
KS5912XX	Natural sound generation	Toys; natural sound effect

Major Linear ICs

Regulators

3T Positive

KA78TXXCF	3 Amp
KA78TXXCT	3 Amp
LM317T	1.5 Amp
MC78XXCT	1 Amp
MC78MXXCT	0.5 Amp
MC78LXXACZ	0.1 Amp
LM723CN	0.1 Amp

3T Negative

KA337T	1.5 Amp
MC79XXCT	1 Amp
MC79MXXCT	0.5 Amp
MC79LXXACZ	0.1 Amp

Switching

KA78S40CN	KA3524N
-----------	---------

REF Voltage

KA431CZ (TL431CLP)	KA336Z-2.5,5
KA431N (TL431CP)	KA385Z-1.2

Comparators

KA319N (LM319N)	LM2903N
KA361N (LM361N)	LM311N*
KA710CN (LM710N)	LM3302N
KS374N (TLC374N)	LM339N/AN*
LM2901N	LM393N/AN*

Op Amplifiers

KA301N/AN (LM301N)*	LM348N*
KA733CN (LM733CN)	LM358N/AN*
KA9256 (POWER AMP)	LM741CN*
KF351N (LF351N)	MC1458N*
LM2902N	MC3303N
LM2904N	MC3403N*
LM324N/AN*	MC4558N*

Telecommunication ICs

KA2410N	Tone Ringer
KA2411N	Tone Ringer
KA2418N	Tone Ringer/bridge diode
KA2412FN	Speech Network
KA2413N	DTMF
KS5808N	DTMF (MK5089)
KS5805AN	Pulse (MK50992)
KS5805BN	Pulse (MK50993)
KS5820N	DTMF/Pulse
KT3040J	CODEC Filter
KT5116J	CODEC
LM567N*	Tone Decoder
LM567LN	Tone Decoder (Low Power)
KS5812N	Quad UART

Timers

KS555N (CMOS)*	NE555CN*
KS555HN (CMOS)*	NE556CN*
KS556N (CMOS)*	NE558CN

RS-232 Interfaces

MC1488N*	MC1489/AN*
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Audio ICs

LM386N	0.5 Watt Power Amp
KA2201N	1.2 Watt Power Amp
KA2206	2.3 Watt Dual Power Amp
KA22062	4.6 Watt Dual Power Amp
KA2210	5.8 Watt Dual Power Amp
KA22101	23 Watt Power Amp
KA2243	AM/FM IF & DET
KA22441	FM IF & DET
KA22495	FM Front End
KA2263	FM MPX

45 other audio ICs available

Video ICs

KA2914A	Color TV VIF/SIF
KA2153	NTSC Chroma & Deflection
KA6101	Video R.G.B. Interface
KA6102	Video R.G.B. Interface

40 other video ICs available

Others

KA2580AN (UDN2580AN)	
KA2588AN (UDN2588AN)	
KA2651N (UCN5815AN)	
KA2615	LED/Lamp Driver
KA2616	LED/Lamp Driver
KA2284	5 Dot LED Meter Driver
KA2286	5 Dot LED Meter Driver
KA2288	7 Dot LED Meter Driver
KA2181	Infrared Amp
KA8301	Motor Driver IC
KS5803AN	Infrared Transmitter
MC3361N	FM IF Amp

*Also available in surface mount package (SOIC)

TRANSISTORS

We Launch a New 1500 volt Power Transistor

**With over 500 transistors,
Samsung is among the world's
largest producers.
Our 1500-volt parts break
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As a producer of transistors, Samsung sits squarely among the very largest in the world.

There is virtually no transistor need we can't fill—with a high-quality part, and at an advantageous price.

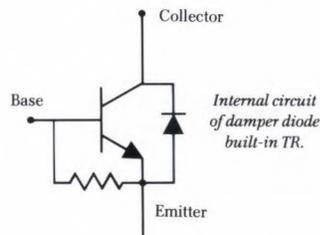
Our entire line of more than 500 transistors, in fact, is in full production and available from stock.

You can order anything from our list *now*, and get immediate delivery.

At present, we are introducing state-of-the-art, 1500-volt power transistors—transistors so difficult to produce that only one other company makes them.

We also provide 100 types of SOT-23s, ideal for both hybrid and surface-mount applications, plus TIP Series, MJE Series, and TO-92 transistors.

Many are listed here, but for a complete list of Samsung transistors, please turn to the back of this issue and request it.



Designed for high-voltage switching systems and industrial motor controls, the eight new Samsung 1500-volt power transistors utilize the TO-3PF fully isolated plastic package.

Transistors From Samsung

1500-Volt Power TR

2.5 amps	5 amps	6 amps
KSD5010*	KSD5012*	KSD5013*
KSD5014	KSD5016	KSD5017

3.5 amps
KSD5011*
KSD5015

*Damper diode built-in transistor

SOT-23

BCX70G	MMBT4403	MMBTA43
BCX71G	MMBT5087	MMBTA55
MMBR5179	MMBT5088	MMBTA56
MMBT2222A	MMBT5089	MMBTA63
MMBT2484	MMBT5401	MMBTA64
MMBT2907A	MMBT5550	MMBTA70
MMBT3904	MMBT6428	MMBTA92
MMBT3906	MMBTA05	MMBTA93
MMBT4123	MMBTA06	MMBTH10
MMBT4124	MMBTA13	MMBTH17
MMBT4125	MMBTA14	MMBTH24
MMBT4126	MMBTA20	
MMBT4401	MMBTA42	

66 other types also available.

TIP SERIES

TIP29 Family	TIP106	TIP140F
TIP30 Family	TIP107	TIP140T
TIP31 Family	TIP110	TIP141F
TIP32 Family	TIP111	TIP141T
TIP41 Family	TIP112	TIP142F
TIP42 Family	TIP115	TIP142T
TIP47	TIP116	TIP145F
TIP48	TIP117	TIP145T
TIP59	TIP120	TIP146F
TIP50	TIP121	TIP146T
TIP100	TIP122	TIP147F
TIP101	TIP125	TIP147T
TIP102	TIP126	
TIP105	TIP127	

MJE SERIES

MJE170	MJE210	MJE800
MJE171	MJE340	MJE801
MJE172	MJE350	MJE802
MJE180	MJE700	MJE803
MJE181	MJE701	MJE2955T
MJE182	MJE702	MJE3055T
MJE200	MJE703	

TO-92

2N3904	2N5210	MPSA42
2N3906	2N5400	MPSA43
2N4123	2N5401	MPSA55
2N4124	2N5550	MPSA56
2N4125	2N5551	MPSA70
2N4126	2N6427	MPSA92
2N4400	2N6428	MPSA93
2N4401	2N6515	MPSH10
2N4402	2N6517	MPSH17
2N4403	2N6520	MPSH20
2N5086	MPSA05	MPSH24
2N5087	MPSA06	PN2222A
2N5088	MPSA14	PN2907A
2N5089	MPSA20	

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Samsung: One of the world's largest corporations
As a unit of one of the world's largest corporations, Samsung Semiconductor is here to stay. Last year, the Samsung Group enjoyed revenues of \$2.4 billion—which would put us in 15th place on the list of the Forbes 500. We have the resources to make things happen technologically, and we have the strength to be a partner in whom you may have absolute confidence.

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MOSFETS

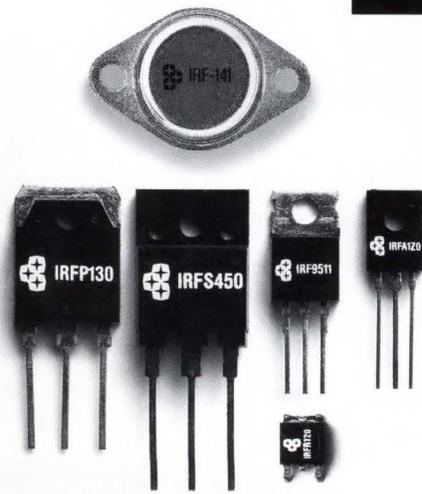
THE WORD IS Rugged

Power MOSFETs just don't come any more rugged than ours.

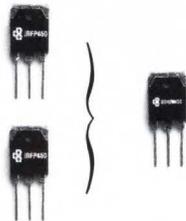
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xhaustive testing has proven Samsung's line of over 400 industry-standard power MOSFETs to be unsurpassed anywhere in ruggedness. They've been shown to withstand 2J at 500V, and in addition, each part has been screened to MIL-STD-750 specifications.

Our recently published ruggedness application note thoroughly documents the superior ruggedness of these parts, and we invite you to complete the coupon at the back of this insert to request a copy. We'll rush it to you.



The single MOSFET that does the job of two.



Samsung's SSH20N50 - available only from us - improves reliability, simplifies assembly, and minimizes mounting hardware, because it's a direct replacement for two IRFP450's. There's less to go wrong, and less to mount.

TURN
to coupon on back page to request MOSFET samples and ruggedness application note.

Samsung Power MOSFETs

TO-247 Full Pack N-Channel Types	IRF430	SSM4N50	
IRFS130	IRFS450	IRF432	SSM20N50
IRFS140	SSS4N70	IRF433	SSM4N45
IRFS150	SSS6N70	IRF440	SSM20N45
IRFS230	SSS10N70	IRF441	SSM5N40
IRFS240	SSS4N60	IRF442	SSM5N35
IRFS250	SSS6N60	IRF443	SSM7N20
IRFS330	SSS8N60	IRF450	SSM8N20
IRFS340	SSS15N60	IRF451	SSM7N18
IRFS350	SSS20N50	IRF452	SSM8N18
IRFS430	SSS25N40	IRF453	SSM7N15
IRFS440		SSM3N70	SSM8N15
		SSM4N70	SSM7N12
		SSM6N70	SSM8N12
TO-3P Package N-Channel Types	SSM10N70	SSM12N10	
IRFP120	IRFP422	SSM6N60	SSM10N10
IRFP121	IRFP423	SSM8N60	SSM12N08
IRFP122	IRFP430	SSM15N60	SSM10N08
IRFP123	IRFP431	SSM4N55	SSM12N06
IRFP130	IRFP432	SSM6N55	SSM10N06
IRFP131	IRFP433	SSM8N55	SSM12N05
IRFP132	IRFP440	SSM15N55	SSM10N05
IRFP133	IRFP441		
IRFP140	IRFP442		
IRFP141	IRFP443		
IRFP142	IRFP450		
IRFP143	IRFP451		
IRFP150	IRFP452		
IRFP151	IRFP453		
IRFP152	SSH3N70		
IRFP153	SSH4N70		
IRFP220	SSH6N70		
IRFP221	SSH10N70		
IRFP222	SSH4N60		
IRFP223	SSH6N60		
IRFP230	SSH8N60		
IRFP231	SSH15N60		
IRFP232	SSH4N55		
IRFP233	SSH6N55		
IRFP240	SSH8N55		
IRFP241	SSH15N55		
IRFP242	SSH4N50		
IRFP243	SSH20N50		
IRFP250	SSH4N45		
IRFP251	SSH20N45		
IRFP252	SSH5N40		
IRFP253	SSH25N40		
IRFP320	SSH5N35		
IRFP321	SSH25N35		
IRFP322	SSH7N20		
IRFP323	SSH8N20		
IRFP330	SSH7N18		
IRFP331	SSH8N18		
IRFP332	SSH7N15		
IRFP333	SSH8N15		
IRFP340	SSH7N12		
IRFP341	SSH8N12		
IRFP342	SSH12N10		
IRFP343	SSH10N10		
IRFP350	SSH12N08		
IRFP351	SSH10N08		
IRFP352	SSH12N06		
IRFP353	SSH10N06		
IRFP420	SSH12N05		
IRFP421	SSH10N05		
TO-3P Package P-Channel Types			
IRFP9120	IRFP9220		
IRFP9121	IRFP9221		
IRFP9122	IRFP9222		
IRFP9123	IRFP9223		
IRFP9130	IRFP9230		
IRFP9131	IRFP9231		
IRFP9132	IRFP9232		
IRFP9133	IRFP9233		
IRFP9140	IRFP9240		
IRFP9141	IRFP9241		
IRFP9142	IRFP9242		
IRFP9143	IRFP9243		
TO-3 Package N-Channel Types			
IRF120	IRF242		
IRF121	IRF243		
IRF122	IRF250		
IRF123	IRF251		
IRF130	IRF252		
IRF131	IRF253		
IRF132	IRF320		
IRF133	IRF321		
IRF140	IRF322		
IRF141	IRF323		
IRF142	IRF330		
IRF143	IRF331		
IRF150	IRF332		
IRF151	IRF333		
IRF152	IRF340		
IRF153	IRF341		
IRF220	IRF342		
IRF221	IRF343		
IRF222	IRF350		
IRF223	IRF351		
IRF230	IRF352		
IRF231	IRF353		
IRF232	IRF420		
IRF233	IRF421		
IRF240	IRF422		
IRF241	IRF423		
TO-220 Package P-Channel Types			
IRF9510	IRF9610		
IRF9511	IRF9611		
IRF9512	IRF9612		
IRF9513	IRF9613		
IRF9520	IRF9620		
IRF9521	IRF9621		
IRF9522	IRF9622		
IRF9523	IRF9623		
IRF9530	IRF9630		
IRF9531	IRF9631		
IRF9532	IRF9632		
IRF9533	IRF9633		
IRF9540	IRF9640		
IRF9541	IRF9641		
IRF9542	IRF9642		
IRF9543	IRF9643		
TO-126 Package N-Channel Types			
IRFA120	IRFA123		

DRAMS

1Mb DRAMs!



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As the latest DRAM addition to our line of leadership memory products, Samsung now offers several 1-megabit DRAMs. Thanks to our internally developed CMOS technology, they are low in power consumption, offer extremely fast access

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KM41C1002	1M x 1	Static Column mode	100,120	DIP,ZIP,SOJ	3Q '88*
KM44C256	256K x 4	Fast Page mode	100,120	DIP,ZIP,SOJ	3Q '88
KM44C258	256K x 4	Static Column mode	100,120	DIP,ZIP,SOJ	3Q '89
KM41256	256K x 1	Page mode	120,150	DIP,ZIP,PLCC	Now
KM41257	256 x 1	Nibble mode	120,150	DIP,ZIP,PLCC	Now
KM41464	64K x 4	Page mode	120,150	DIP,ZIP,PLCC	Now
KM4164	64K x 1	Page mode	120,150	DIP	Now

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- Samples

- Ruggedness application note

DRAMs

- Data sheets

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EDN



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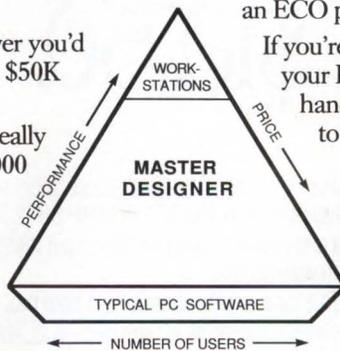
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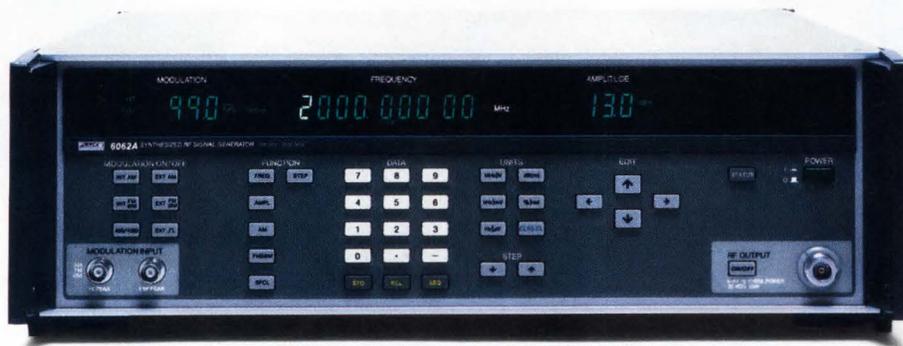
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Two Gigahertz.



Fluke 6062A Signal Generator.

\$10,750.

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Choosing the right 2GHz programmable RF signal generator doesn't have to be a painful decision. You have two good choices... at two very different prices.

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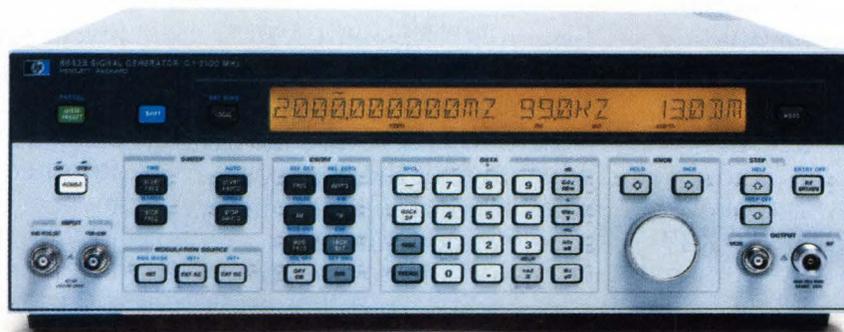
Where pulse modulation performance is important, the 6062A simply leaves the HP 8642B behind. With a rise/fall time of 15ns and on/off ratio of 80dB at all frequencies, the 6062A has what it takes to meet your most demanding system requirements.

And when you need both repeatability and confidence in your measurements, the 6062A holds steady with level



PHILIPS

Two Gigahurts.



Hewlett-Packard 8642B Signal Generator.

\$31,500.

accuracy and linearity performance that is simply outstanding.

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				Harris: 80C86 80C88	NEC: V20 V40 V30 V50
				National: NSC800	Signetics: 8X300 8X305

...AND MORE

*Assumes EZ-PRO Development Station connected to MSDOS host.

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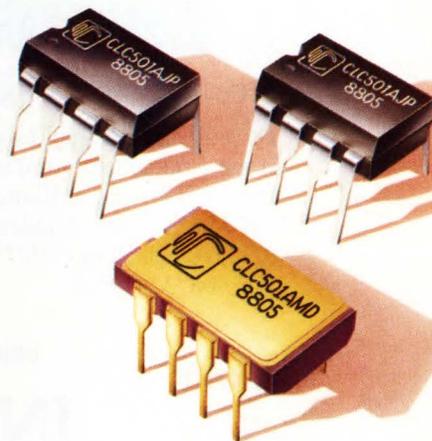
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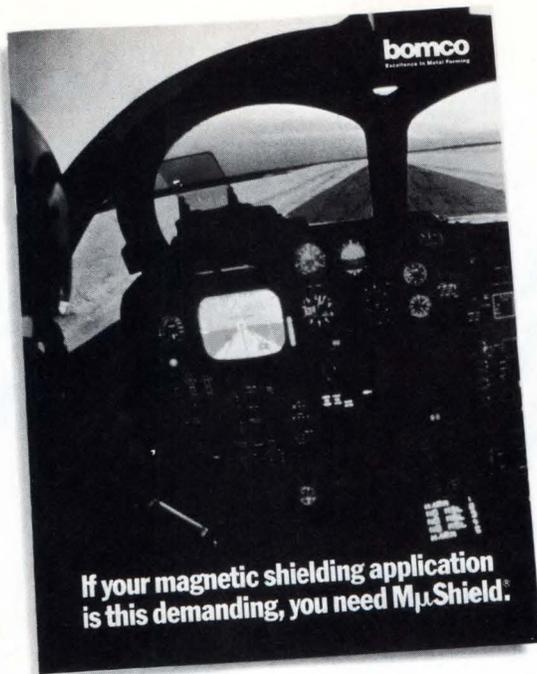
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Midcon, Dallas, TX. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (800) 421-6816; in CA, (213) 772-2965. August 30 to September 1.

Surface Mount '88, Marlborough, MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. August 30 to September 1.

Modern Electronic Packaging (seminar), Santa Clara, CA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. September 7 to 9.

International Test Conference, Washington, DC. Doris Thomas, ITC, Box 264, Mount Freedom, NJ 07970. (201) 267-7120. September 12 to 14.

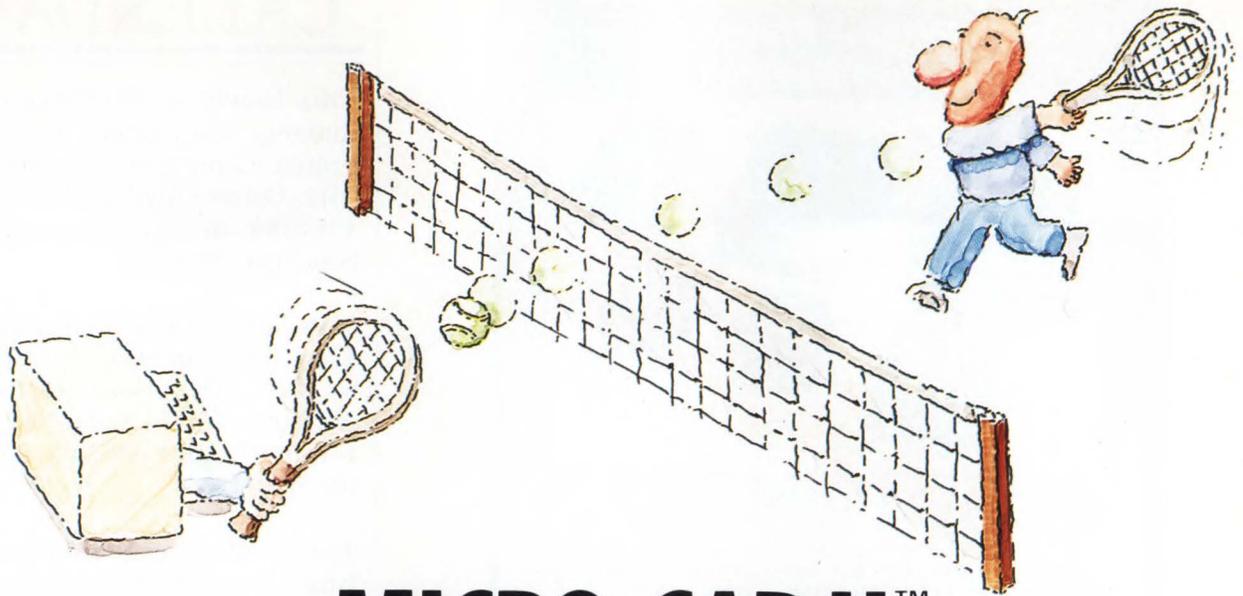
Worst-Case Circuit Analysis (seminar), Boston, MA. Design and Evaluation, 1000 White Horse Rd, Suite 304, Voorhees, NJ 08043. (609) 770-0800. September 12 to 14.

C Programming Workshop (short course), Seattle, WA. SSC, Box 55549, Seattle, WA 98155. (206) 527-3385. September 12 to 15.

12th International Fiber Optic Communications and Local Area Networks Exposition, Atlanta, GA. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (800) 323-1088; in MA, (617) 232-3111. September 13 to 16.

Unix Hands-on Workshop (short course), Montreal, Canada. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 13 to 16.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. September 19 to 22.

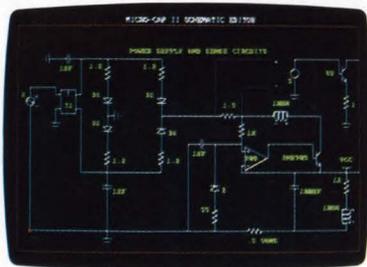


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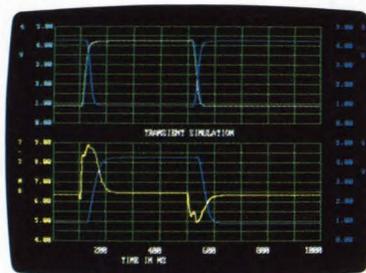
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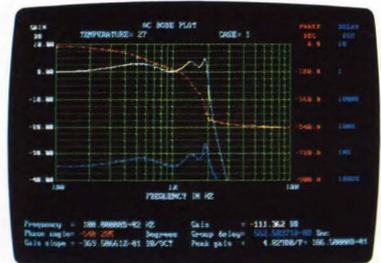
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Unix Hands-on Workshop (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 20 to 23.

34th IEEE Holm Conference on Electrical Contacts, San Francisco, CA. IEEE Holm Conference Registrar, 345 E 47th St, New York, NY 10017. (212) 705-7405. September 26 to 29.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Chicago, IL. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. September 27 to 30.

Unix Hands-on Workshop (short course), San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 27 to 30.

Connector and Interconnection Technology Symposium, Dallas, TX. Electronic Connector Study Group, 104 Wilmot Rd, Suite 201, Deerfield, IL 60015. (312) 940-8800. October 3 to 5.

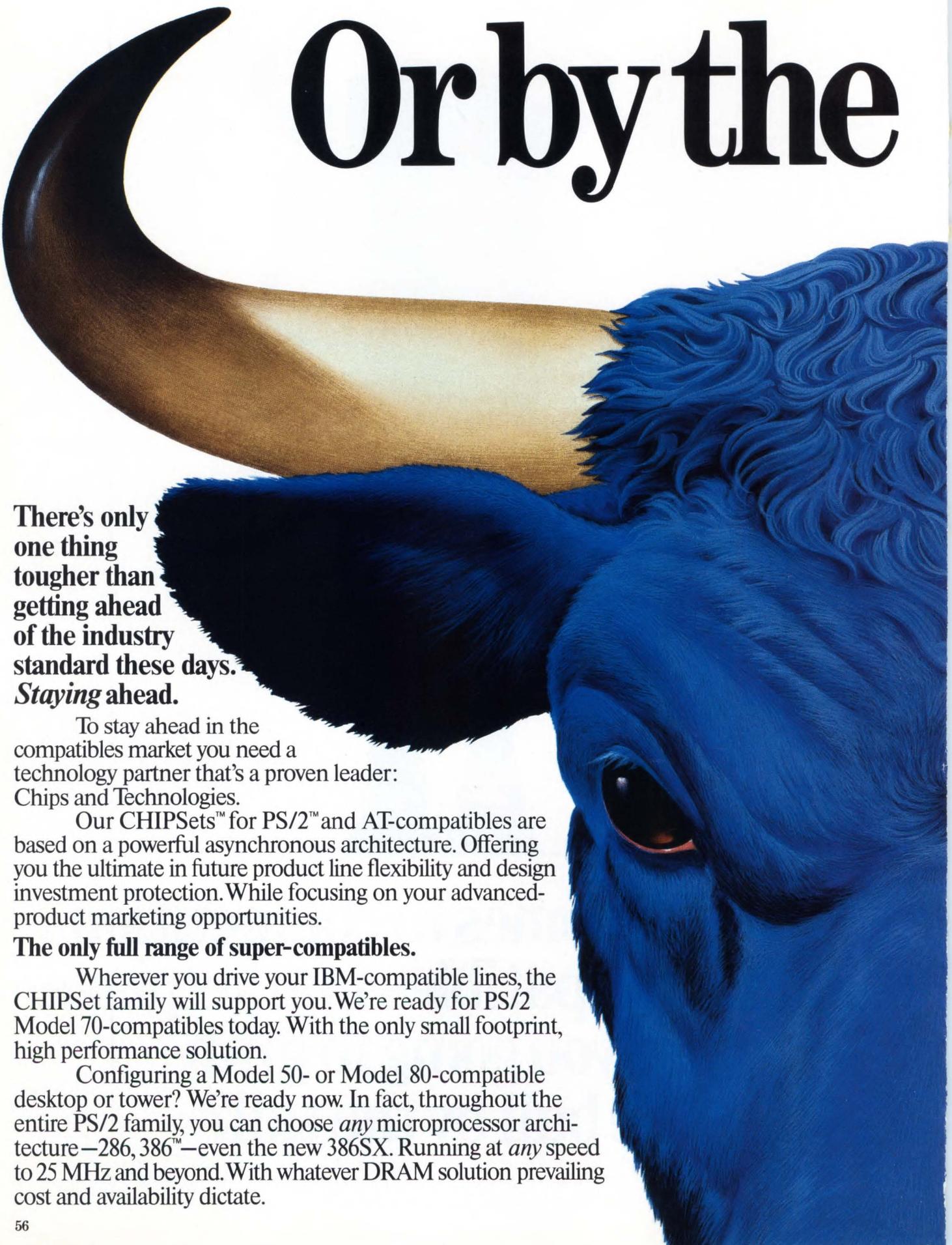
IEEE International Conference on Computer Design: VLSI in Computers and Processors, Port Chester, NY. Gail Clanton, IEEE, 1730 Massachusetts Ave NW, Washington, DC 20036. (202) 371-1013. October 3 to 5.

Autotestcon, Minneapolis, MN. Steve Palmer, Unisys, 3333 Pilot Knob Rd, Eagan, MN 55121. (612) 456-2349. October 4 to 6.

Buscon/88 East, New York, NY. Conference Management Corp, 200 Connecticut Ave, Norwalk, CT 06856. (203) 852-0500. October 4 to 6.



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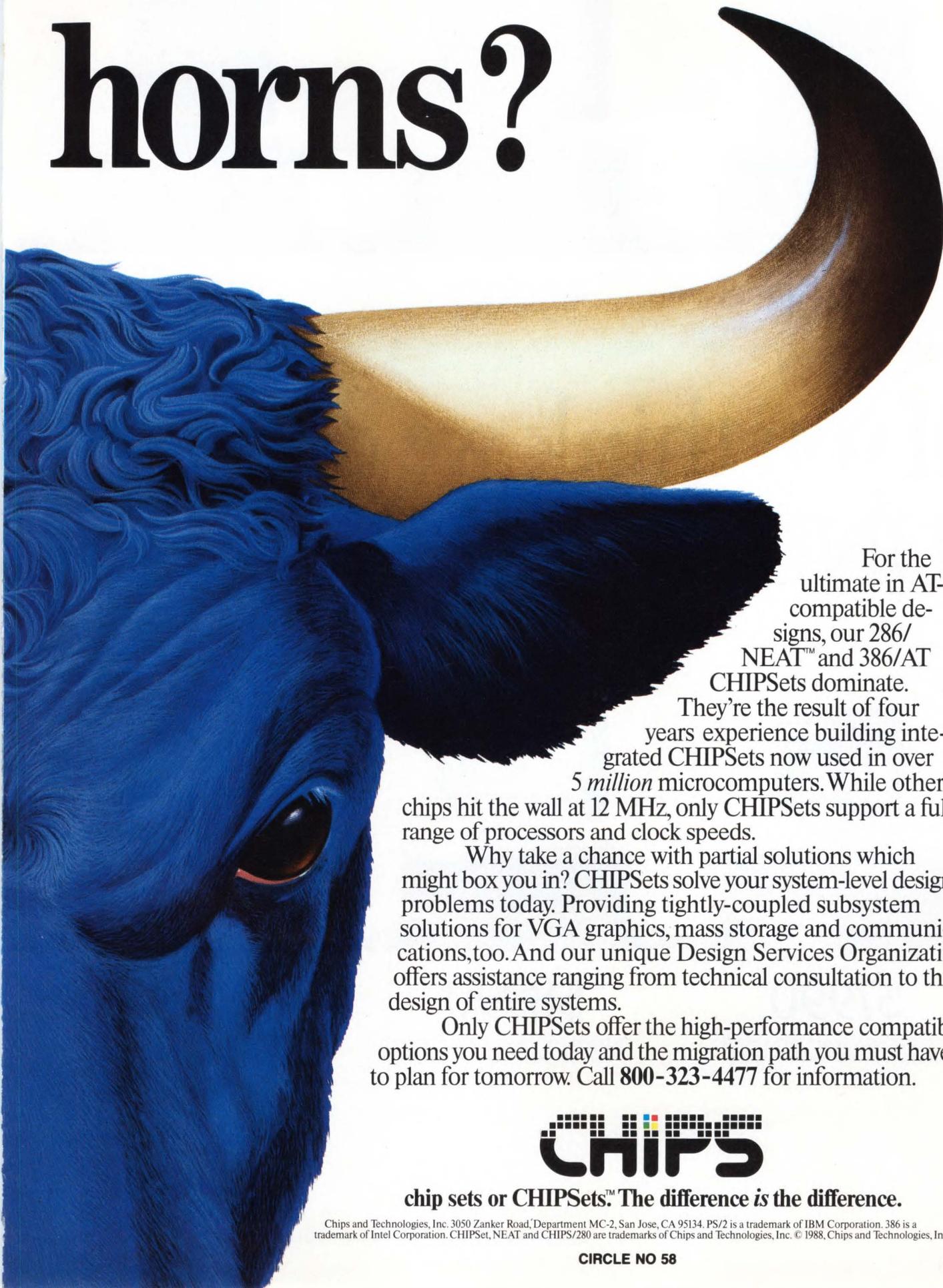
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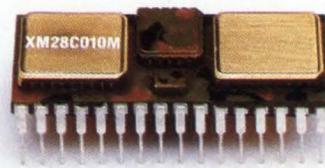
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X2816BM	2048 x 8	16	250, 300	X2004M	512 x 8
X2864AM	8192 x 8	16	250, 300, 350, 450	Serial I/O Part No.	Organ.
X2864BM	8192 x 8	32	120, 150, 180	NOVRAM X2444M	16 x 16
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X28256M	32768 x 8	64	250, 300, 350	E ² PROM X24C16M	2048 x 8
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MAKES IT MEMORABLE

EDITORIAL

That's the way the trade problems crumble



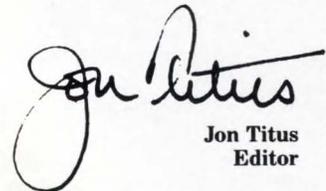
The recent shortage of dynamic-RAM chips has set off a new round of discussions about working with our Asian trading partners. It turns out that there may be a way to help solve some of the semiconductor and trade problems. But before you hear my proposal, you'll need a little background information.

Earlier this year, Federal Express began a new service: It started shipping small packages to Japan at prices lower than the normal shipping costs of Japanese carriers. Because the Japanese have no similar small-package courier service, they decided to stop or slow Federal Express until one of their domestic carriers could offer a competitive service. Instead of levying enough duties and restrictions to shut down Federal Express's new service outright, the Japanese demanded shipping documents for each Federal Express package. The extra paperwork and complex customs processing are making Federal Express shipments uncompetitive with the Japanese shippers, according to *Business Week* (May 30, 1988, pg 116).

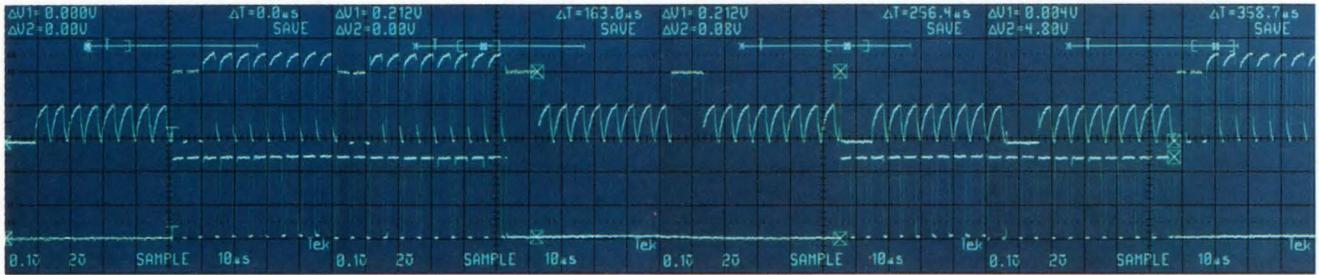
At about the same time, the Japanese taught the Girl Scouts of America a lesson about international trade. US Navy personnel stationed in Japan ordered Girl Scout cookies at \$2 per box. Unfortunately for the sailors, when the cookies arrived in Japan, the unfathomable customs inspectors placed a \$5 duty on each box. After all, cookies are agricultural products which threaten Japanese suppliers' markets. In the end, US Congressional intercession carried the day, and the sailors got their cookies.

Now we're facing a semiconductor crisis that threatens US computer manufacturers—almost all of whom rely on now-scarce DRAM chips from Asia. According to industry watcher Warren Andrews, there may be a conspiracy among foreign DRAM vendors to keep supplies scarce and thus keep prices high. Andrews thinks that the DRAM shortages are part of a concerted plan by Japanese suppliers who ultimately want to control the computer-board and -systems markets, too.

Well, like it or not, the time has come to retaliate against the Japanese by giving them a taste of their own medicine. Just as we depend on DRAMs, Japanese manufacturers depend on many types of US-made semiconductors. But instead of planning a price-and-supply conspiracy, we'll take another approach. Here's the plan: From now on, whenever US companies ship semiconductor products to Japan, they should send them by Federal Express. Let's set a limit of 12 parts per package, though. Also, to show our good will, we'll throw in a box of Girl Scout cookies with each order—I recommend the sticky chocolate-covered Samoas. Perhaps someone in Japan will get the message.


Jon Titus
Editor

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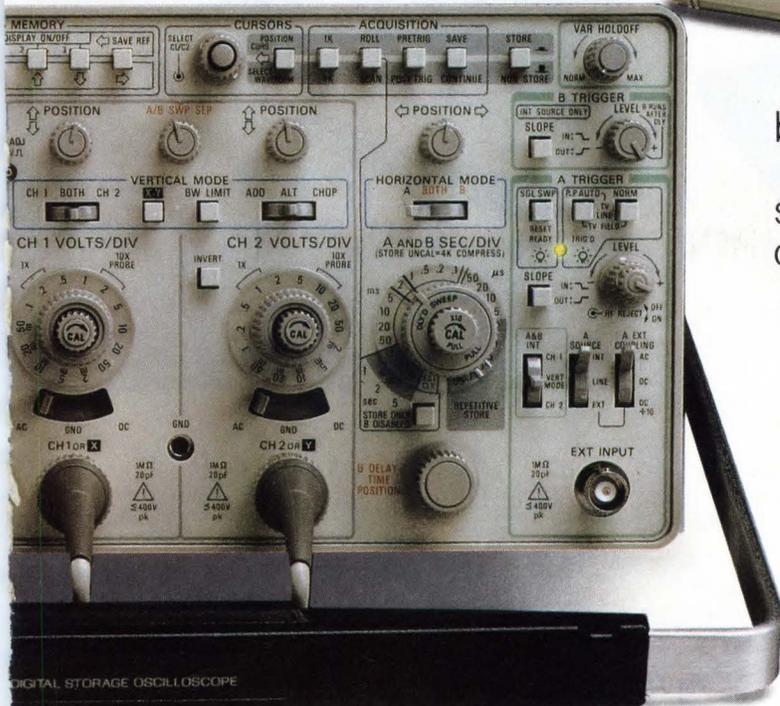
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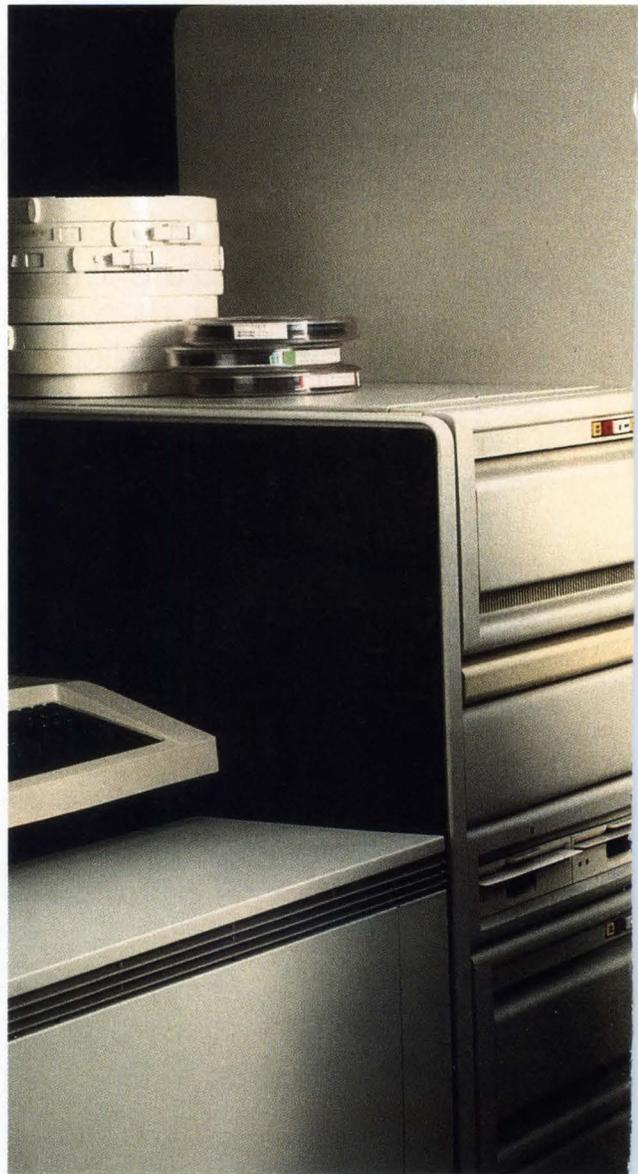
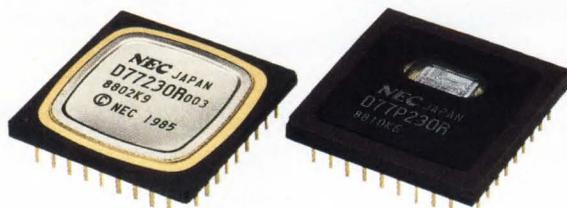
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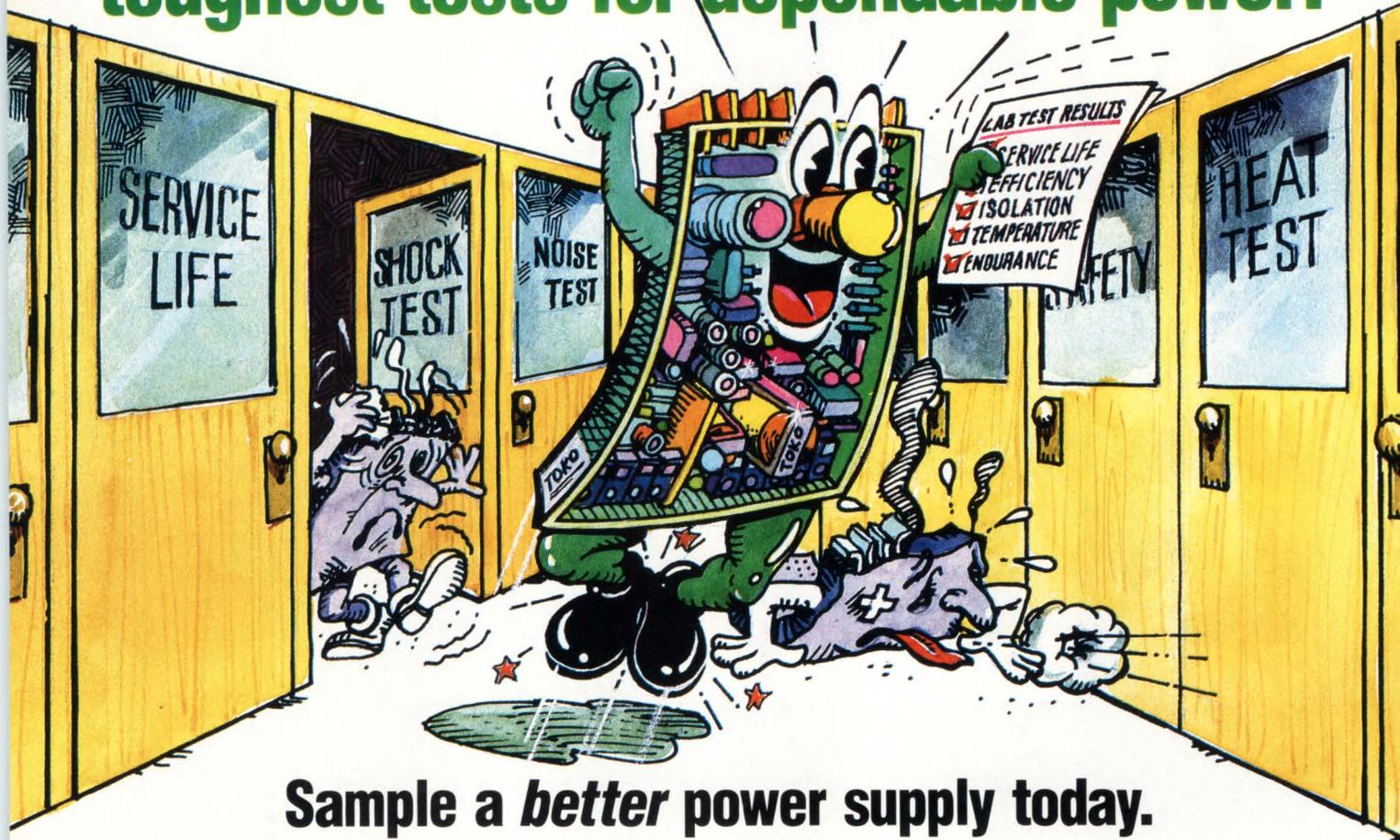
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	90-132	50/75/100W	3	4.4"	7.8"	2.0"
ET	85-132	10/15W	3	2.6"	4.5"	1.3"
EM	170-264	10/15W	3	2.6"	4.5"	1.3"
PS	85-132	10/15/30 50/100W	1	3.8"	3.5"	1.0"
PE	85-132	30/50/100W	1	3.8"	6.3"	1.4"
AS	90-132	75W	1	1.6"	8.0"	4.9"
AR	85-132	150W	1	2.0"	10.3"	6.8"
MK	85-132	150W	1	3.8"	6.7"	2.4"

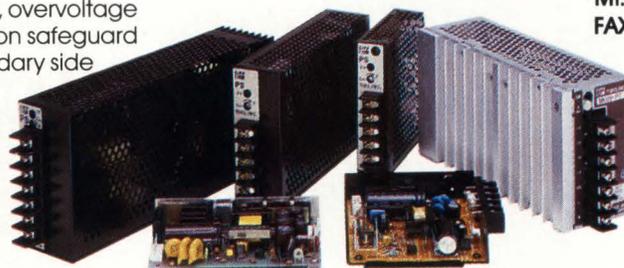
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TECHNOLOGY UPDATE

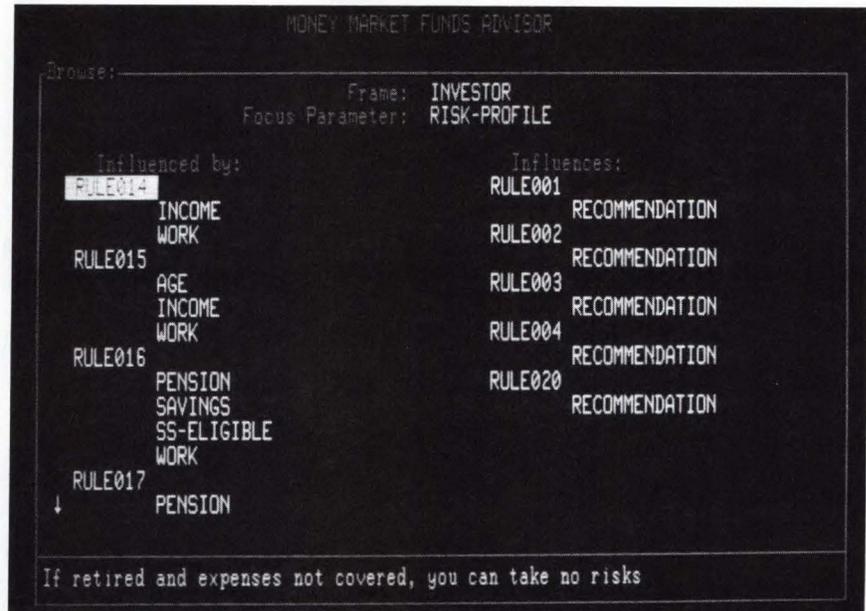
PC-based development products move AI out of the classroom, into the workplace

Chris Terry, *Associate Editor*

Artificial intelligence (AI) was the dreamchild of the 50s—or perhaps it was Aladdin's lamp, which would release a genie of unlimited power and wisdom. In the 70s, it was an expensive lab toy, with which people attempted to make huge computers emulate what they called "natural intelligence," or the structure and method of performing tasks. The scientific results and social implications of AI were—and still are—hotly disputed, and many of the original goals have proved unrealizable, misdirected, or just not commercially useful at present. Nevertheless, the spinoffs from AI research include many new techniques for problem solving and much valuable knowledge about how to define tasks accurately.

You no longer need a supercomputer to run AI-related programs; many such programs will run on modest machines such as the IBM PC/AT and compatibles. Most of the AI products available for PCs are "expert-system shells," tools that let you interrogate a human expert in a given field and build not only his factual knowledge, but also his approach to problem solving, into an "expert system." GoldWorks from Gold Hill Computers is an example. Such a system can help a nonexpert in a certain field to perform a complex task that requires insight into the relative importance of the phenomena observed under varying conditions.

Another AI-based technique that may have important implications for both the hardware and the software of massively parallel systems is the neural network, which is a network of small processors (or their soft-



Most expert systems will show you a list of the existing rules, as well as the dependencies between them. The Texas Instruments Personal Consultant Plus 3.0, for example, lets you create complex expert-system applications for 80286/80386, DOS-based personal computers.

ware equivalent) that purports to model the interconnections and behavior of the neurons in the human brain. A large neural network requires extensive computing power and resources, but at least two simulators that run on PCs and compatibles—Netwerkz from DAIR Computer Systems and Awareness from Neural Systems—can demonstrate the more-obvious properties of neural networks and allow you to familiarize yourself with these properties.

New programming techniques have also emerged from AI studies, as have some new programming languages (and new dialects of established languages) that facilitate them. These techniques can enhance both the performance and the user interface of more traditional applications, such as database managers.

Before examining the details of

expert-system shells, neural networks, and language tools, it may be helpful to consider briefly what AI is and how AI programs differ from traditional programs. "Artificial intelligence" is the general term for an academic field of research that studies the parameters of task performance by designing a system to perform a task, and then seeing how well the system succeeds.

If you wonder how that procedure differs from the design of any other system, consider Elaine Rich's definition: "Artificial intelligence is the study of how to make computers do things at which, at present, people are better" (Ref 1). If you're still confused, ponder the further simplification of the cynic who said: "If we know how we do it, it ain't AI."

One of the dilemmas that AI-systems designers face is that human language is governed by all kinds of implicit assumptions. For example,

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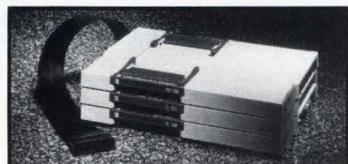
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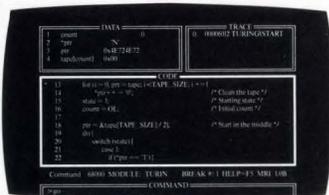


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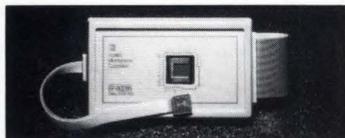
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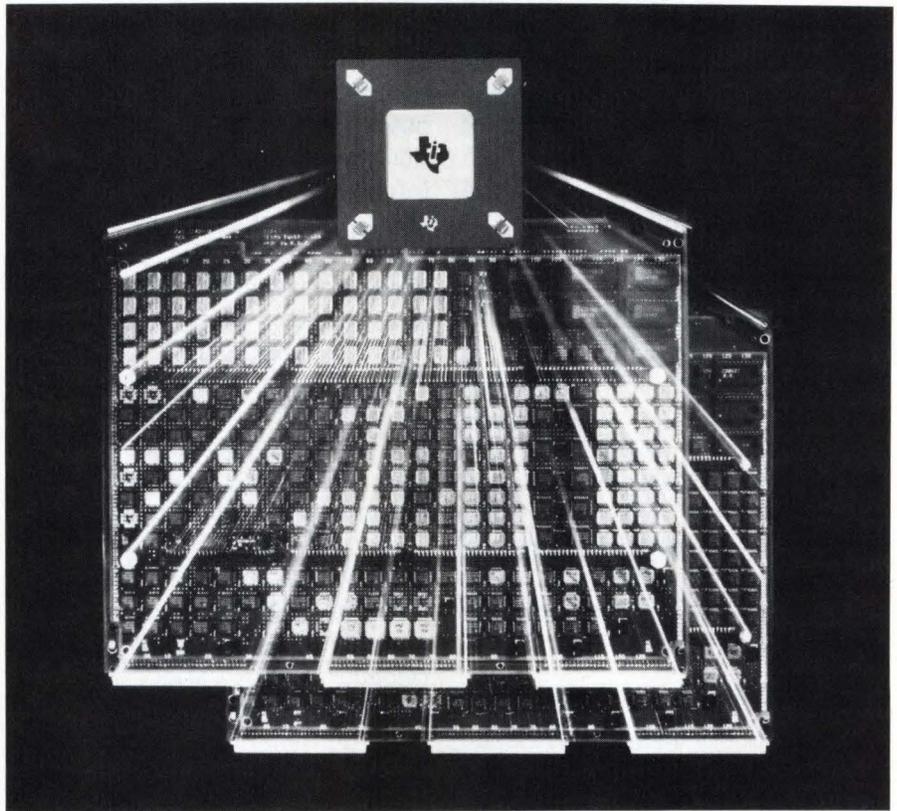
suppose that a computer has control of robotic arms and hands, has definitions of the words "fry," "egg," "pan," "boil," and "stove" in its memory, and has access to those items. We can tell the computer to fry an egg, but we shouldn't be surprised if the computer attempts to perform the task by placing the egg in the pan without breaking the shell. If the computer has to learn that "egg" implies "without the shell" in the context of frying, can we expect it to know that the same word implies "in the shell" in the context of boiling? It is this type of assumption about our environment, not to mention the ambiguity of natural languages, that makes computer simulation of human behavior so difficult to achieve.

You can see, therefore, that AI studies are important for anyone who is designing a system that must take into account the nature of its environment and that must, like a human, attempt to find solutions to problems when the data is incomplete. At a practical level, AI studies have brought new approaches and technological advances to a huge range of disciplines, including natural-language processing, computer vision, speech recognition, robotics, automatic programming and heuristic systems (systems that learn from their experiences).

Expert systems are data-driven

Traditional application programs, such as database managers, are procedure-driven. That is, they process the information contained in the database according to a fixed set of instructions. Knowledge-based programs, such as expert systems, are far more flexible; they dynamically determine the sequence of rules to be employed while the program is running, and they do so on the basis of both the desired result and the data that's available to them.

Another difference between procedural programs and expert systems is that the former use only forward chaining to determine the



Lisp programs run fastest on a machine whose native language is Lisp. The heart of Texas Instruments' Explorer workstation is this Lisp CPU chip.

sequence of rules the program employs. That is, they proceed from a fixed set of input data to a fixed goal by applying the rules in sequence. Expert systems can also employ backward chaining; that is, they can start from a particular goal, break it into several subgoals, and work backward through the rules until the available data fits one or more of the subgoals. If the system does not find an exact match, it can ask for more data; if additional data is not available, the system can indicate the closeness of the match as a percentage, and can also—at any time—explain the rules that it applied in order to reach a particular conclusion or recommendation.

An expert system consists of two major components. One is a *knowledge base* that can store data in a form that allows the representation of both facts (declarative knowledge) and rules of thumb for relating them (procedural knowledge). The other is a *control structure* (also called a *rule interpreter* or an *infer-*

ence engine) that determines the manner in which the knowledge is to be used.

An expert-system shell contains an empty knowledge base and an inference engine, but also contains an editor or some other means of eliciting and storing items of both declarative and procedural knowledge. The vendor usually licenses both a development system that includes all three major components (and often some helpful utility programs) and a run-time system that consists only of the knowledge-base framework and the inference engine. You can distribute the run-time system as part of any expert system that you develop with the package.

Inexpensive expert-system shells

A typical example is the Exsys shell from Exsys Inc. Its development system for IBM PCs and compatibles costs \$395; its run-time system costs \$600 for unlimited distribution. You can license both

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systems for \$900. The shell is written in C, which gives it high execution speed and efficient memory use. If your PC has 640k bytes of RAM, you can develop systems with as many as 5000 rules. The inference engine can use both forward and backward chaining; you can exchange data with most spreadsheets and database programs; and you enter all input in English text, in algebraic notation, or via menu selections. You can get a demonstration disk that has all the features of the full system (including a printed manual, sample expert systems, and a tutorial on how to create expert systems) but allows you to save only 25 rules to disk. The demo disk costs \$15.

Costly expert-system shells

A much more elaborate, flexible, and costly development system is GoldWorks from Gold Hill Computers Inc. This system runs on 80286- or 80386-based machines that have at least 512k bytes of main memory and 5M bytes of extended memory. The system is a frame-based one, which provides flexibility of knowledge representation—in other

words, each data object is not only named, but also contains descriptions of all its parts and their attributes (such as quantity, color, relationships to other parts, etc). The inference engine allows both forward and backward chaining, and provides control mechanisms that handle user-defined rule priorities and certainty factors, as well as rule-inspecting and -debugging facilities. You can exchange data with spreadsheets and database managers. In addition, you get extensive tutorial material, not only on how to create expert systems but also on Lisp programming and AI strategies. The developer's interface includes an Emacs-like editor, a large-memory Lisp interpreter and compiler, and a variety of debugging tools. Prices start at \$7500.

An optional training program called Axle, also from Gold Hill, gives a stage-by-stage demonstration of the development of four different types of expert systems: a manufacturing system, an aerospace system, and two planning systems, one for an industrial application, and the other for oil exploration. These sample systems

include methods for diagnosing equipment malfunctions and help in making decisions about tasks and resources. The program runs on 80286- and 80386-based PCs, and costs \$1995.

Although Texas Instruments (TI) is best known in the AI field for software that runs on the TI Explorer workstation, whose native language is Lisp, TI also provides expert-system shells that run on PCs and compatibles. At the low end of the company's Personal Consultant series is PC Easy, which runs on PCs or PC/XTs and costs \$495. At the high end is PC Plus, which runs on 80286- or 80386-based machines and costs \$2950. Knowledge bases created with PC Easy are upwardly compatible with PC Plus knowledge bases, and both are compatible with the Explorer Symbolic Processing System. TI supplies demonstration disks for PC Easy and Plus.

An interesting newcomer to the ranks of expert-system shells is CxPERT (\$495 from Software Plus). Like other shells, it provides you with a knowledge-representation framework, user-interface mod-

An AI reading list

If you want to know more about artificial intelligence, you'll find the following publications informative. They can also direct you to further, more specialized reading.

1. *AI Expert*, CL Publications Inc, 650 Fifth St, Suite 311, San Francisco, CA 94107. Phone (415) 957-9353. \$27/year (12 issues). Interesting for both the professional and the novice in the AI field.

Rather similar in character to *Computer Language*, it addresses both general problems and the tricks of the trade.

2. *AI Magazine*, American Association for Artificial Intelligence (AAAI), 445 Burgess Dr, Menlo Park, CA 94025. Phone (415) 328-3123. Yearly membership, \$25; 5 issues/year. The professional journal of scientists involved in AI research. A must if you're involved in AI projects.

3. *AI Trends*, DM Data Inc, 6900 E Camelback Rd, Suite 1000, Scottsdale, AZ 85251. Phone (602)

945-9620. In the US, \$295/year (12 issues); elsewhere, \$345/year. Describes trends, important issues, and the administrative and economic vicissitudes of the major players in the AI field.

4. *Artificial Intelligence Letter*, Texas Instruments, Data Systems Group, Box 2909, M/S 2222, Austin, TX 78769. Includes case histories, the viewpoints of eminent AI experts, and a conference calendar.

5. *Understanding Artificial Intelligence*, by Henry C Mishkoff (1985). The Texas Instruments Learning Center, Box 225474, MS-8218, Dallas, TX 75265. \$14.95. A first-class introduction to the AI field, with clear descriptions of the various branches, the issues involved, and some of the products. The book was originally issued in conjunction with the first of the TI-sponsored Satellite Seminars on AI. Highly recommended.

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ules, and an inference engine that allows several layers of backward chaining. According to one reviewer, the forward-chaining feature is somewhat rudimentary, but it's nevertheless very flexible. The unusual feature of this shell, which is written in C, is that it encourages you to use standard C code to perform tasks that the high-level constructs don't support. You create knowledge-base modules in a mixture of C and a knowledge-representation language (KRL) source code; these modules contain the rules, attributes, menu text, and logic that compose the expert system. The KRL compiler processes these modules to produce a C source file and a header file, which you compile with the Microsoft or Lattice compiler. You can then link your object modules to the object libraries supplied with the shell, as well as to other C programs or routines.

Neural networks open new doors

Neural networks have probably existed in rudimentary form for a number of years, but have only recently become practical. They are still immature, but—theoretically—they promise dramatic advances in the technology of pattern recognition. What's important about them is that they're capable of learning, from examples, to recognize not only specific shapes and patterns, but also a gestalt. In other words, they can learn to recognize the clues that allow us, for example, to abstract the concept "dog" from the specifics "Doberman" and "Yorkshire terrier," despite the differences in size, shape, and hair texture. Only three neural-network systems are as yet available for PCs, and they all require the computing power and speed of an 80286-based machine.

At the low end of the scale is Netwurkz (\$79.95) from DAIR Computer Systems. This product is limited in scope and capability, but it serves as a demonstration of the more-obvious properties of neural

networks. It does, however, provide facilities that let you develop simple programs other than those supplied as examples. Another demonstration and learning system is Awareness (\$250) from Neural Systems.

At the high end is the NDS system from Nestor Inc (\$7500 for the PC/AT version). The NDS system emulates the action, as we currently understand it, of the biological neural networks used by the human learning and classification processes. It will learn to recognize images such as industrial objects, alphanumeric characters, and signatures if you present it with examples of those images. The package is menu driven and highly interactive. It is written in C, and it includes extensive diagnostic facilities for fine-tuning its recognition performance. It also provides an interface to Datacube's (Peabody, MA) MaxiVision image-processing hardware for the PC/AT. The combination creates an intelligent vision system that manufacturers can employ in factory automation at a cost of less than \$20,000.

Tsk! Tsk! Such language!

Hardly any programming topic (except one's choice of editor) can so reliably start a heated discussion as one's choice of programming language. Opinions on AI languages just add fuel to the fire. The traditional language for AI programming has for many years been Lisp, because its features make it admirably suited to handling software objects that embody both attributes and procedures specific to those objects. In the last few years, however, other languages have started to edge Lisp out of its formerly pre-eminent position. Even such a dyed-in-the-wool Lisp proponent as Symbolics Inc is starting to rewrite its AI products in the C language, for the sake of portability.

There are several reasons for this shift. First, Lisp is a memory hog; it is liable to create many noncontiguous islands of abandoned data to

which pointers no longer exist. Periodically, the memory must be homogenized into contiguous used and free areas by a time-consuming process called "garbage collection." Second, Lisp runs fastest on machines whose native language is Lisp. Until Texas Instruments produced the Explorer CPU chip, and Symbolics came out with the Ivory CPU chip, the only dedicated Lisp machines were of mainframe size and power, and they had corresponding price tags. Third, Lisp has fragmented into many dialects, which certainly doesn't make for portability. And, last, the syntax is not easy. Experts will assure you that it's possible to write a Lisp program that other people can read and understand easily, but their antagonists will warn you that you might get "Lost In Silly Parentheses."

If you're already a Lisp fan, consider the versions available for the PC, which range from TI's \$95 PC Scheme, through the \$495 Star Sapphire version of Common Lisp (Sapiens Software), to Gold Hill's Golden Common Lisp for 80286-based machines at \$1995. The Star Sapphire package is interesting because it compiles programs to C; to use it, you'll need 640k bytes of RAM, a hard-disk drive, and a C compiler that supports the Huge memory model. For those who want to try out Lisp at minimal expense, however, there's a public-domain, object-oriented dialect called XLisp that you can download from many PC-based bulletin boards for the price of a phone call.

Object-oriented languages

The principal rival of Lisp in the AI field is probably C, partly because of its steadily increasing popularity as an all-purpose language, and partly because AT&T's superset of the language, called C++, is readily available for the PC. This augmented version of C is an object-oriented language. It provides such features as classes, inheritance,

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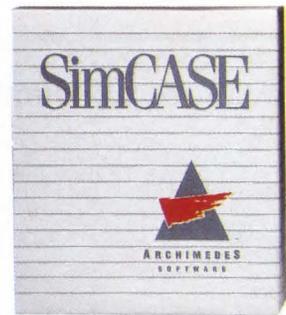
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member functions, constructors and destructors, data hiding, and data abstraction, which are virtually essential for any sophisticated AI programming. In particular, the "classes" feature lets you create modules that contain their own data and data-related operations; you can compile these modules independently, just as you would do in a Modular 2 system. You can save your modules in separate files and reuse them in other C++ programs. C++ usually comes in the form of a translator from C++ to standard C source code, so you'll be able to use your existing C compiler. C++ translators are available from Guidelines Software Inc (\$295) and Oasys. The Oasys version is available for many different machines and their most common C compilers. It costs \$495.

If you just want to experiment with the C++ language, you can do so inexpensively by using Zortech's \$99.95 compiler. Unlike the other packages, which translate C++ code to standard C source code for later compilation and linking,

Zortech's product is a true compiler that generates relocatable object modules for 8088-based machines. Zortech can also supply Bjarne Stroustrup's book *The C++ Programming Language* (\$29.95), which contains the standard specifications of the C++ language. Stroustrup designed the language.

Prolog, the new AI language

Prolog is a nonprocedural programming language. It is conceptually simple and extremely powerful, but so different from procedural languages such as Lisp and C that it's difficult to learn, especially if you're experienced in using a procedural language—you have to develop a totally different way of thinking in order to use it effectively. The language is object-oriented, and it embodies such features as backtracking, which allows the execution of statements to take place not only from top to bottom and left to right (as in procedural languages), but also from right to left and from bottom to top.

The two major implementations of Prolog for IBM PCs and compatible computers are Arity/Prolog and Turbo-Prolog. Arity's package (\$650) includes both a compiler and an interpreter. You can also get the Arity/Expert System and Arity/SQL as options for \$295 each.

Borland's Turbo Prolog 2.0 (\$149.95) also runs on IBM PCs, PS/2s, and compatibles. You must have at least 348k bytes of RAM (640k bytes are recommended) and two floppy-disk drives (a hard-disk drive is recommended). The package allows you to work with multiple internal databases, as well as with an external database system, so you can develop very large databases. It also includes the source code (written entirely in Turbo Prolog) of a Prolog interpreter. There are step-by-step instructions for including the interpreter in your own application programs and for customizing it to suit your needs. The package provides windowing facilities, and is entirely compatible with Turbo C, so that programs written

For more information . . .

For more information on the AI software development tools discussed in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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in either of the languages can call routines (or complete programs) that are written in the other language.

Smalltalk and Modula-2

Two other languages that are well suited to AI-related projects are Smalltalk and Modula-2, though at present these are less widely known and used than Lisp and Prolog. Both are object-oriented languages, and both allow you to construct independently compiled, reusable software modules. Smalltalk comes in two versions for IBM PCs: a full version of the original language (developed at the Xerox PARC research center), which comes from Softsmarts and costs \$995; and a subset that comes from Digitalk Inc and costs \$99. This subset is not a toy—all the basic features are present, and you can use it to develop commercially useful applications.

Many Modula-2 compilers are

available for PCs (Ref 2). Typical compilers are Stony Brook Modula-2 (\$345) and QuickMod (\$95). Together they form an integrated compiler and interpreter package somewhat similar to Turbo Prolog. Both come from Stony Brook Software Inc.

The developers mentioned represent only a small portion of the entire market for AI-related products. More than 50 vendors now offer such products, most of which are expert-system shells and language-development tools. If neural networks live up to their promise, you can expect to see vendors applying them to improve automated manufacturing equipment and to fulfill part of the modern technological wish list—by permitting the development of such items as a voice-activated typewriter and a reliable language translator. Artificial intelligence may yet prove to be the dreamchild of the 50s that will come of age in the 90s.

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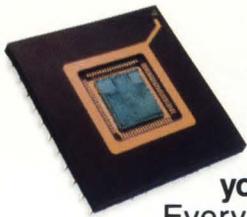
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Processor Clock Speed (MHz)	Typical Instruction Rate (MIPS)*	Power Dissipation (mW)	Interrupt Latency (μs)	Conditional Branch (μs)	16 x 16 Multiply (μs)	ASIC Bus™ Bandwidth (Mbytes/Sec)	Subroutine Call/Return Overhead (μs)
10	15.0	400	0.4	0.10	0.10	20	0.10
8	12.0	320	0.5	0.12	0.12	16	0.12
5	7.5	200	0.8	0.20	0.20	10	0.20
1	1.5	40	4.0	1.00	1.00	2	1.00

*Instruction Rate Measured In Millions Of Instructions Per Second.

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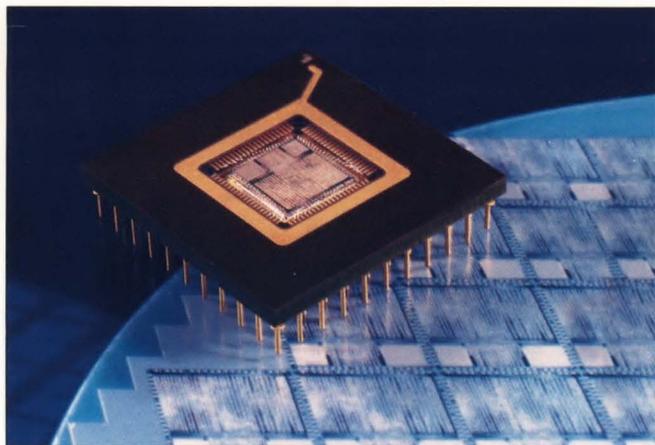


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RTX 2000/2001™ Features

Feature	RTX 2000	RTX 2001
Timer/Counters (on-chip)	3 ea. — 16 bit	3 ea. — 16 bit
Interrupt Controller (on-chip)	NMI and 13 Maskable (Expandable off-chip)	NMI and 13 Maskable (Expandable off-chip)
Memory (on-chip)	256 x 16 Parameter Stack 256 x 21 Return Stack	64 x 16 Parameter Stack 64 x 21 Return Stack
Wait State Controller (on-chip)	Yes	Yes
ASIC Bus™	16 bit	16 bit
16 x 16 Multiply	Single Cycle	20 Cycle
32/16 Divide	21 Cycle	21 Cycle
32/16 Square Root	25 Cycle	25 Cycle
Address Range	1 Mbyte	1 Mbyte
Data Bus	16 bit	16 bit
Byte Operations	Yes	Yes
Package	84 pins	84 pins
883C Compliant	1Q CY89	Not Planned
Semicustom Migration Path	Yes	Yes
Rad-Hard Migration Path	Yes	Not Planned
32 bit Migration Path	Yes	Yes
Development System	Yes	Yes
Forth Compiler	Now	Now
C Compiler	4Q CY88	4Q CY88
Prolog Compiler	1Q CY89	1Q CY89



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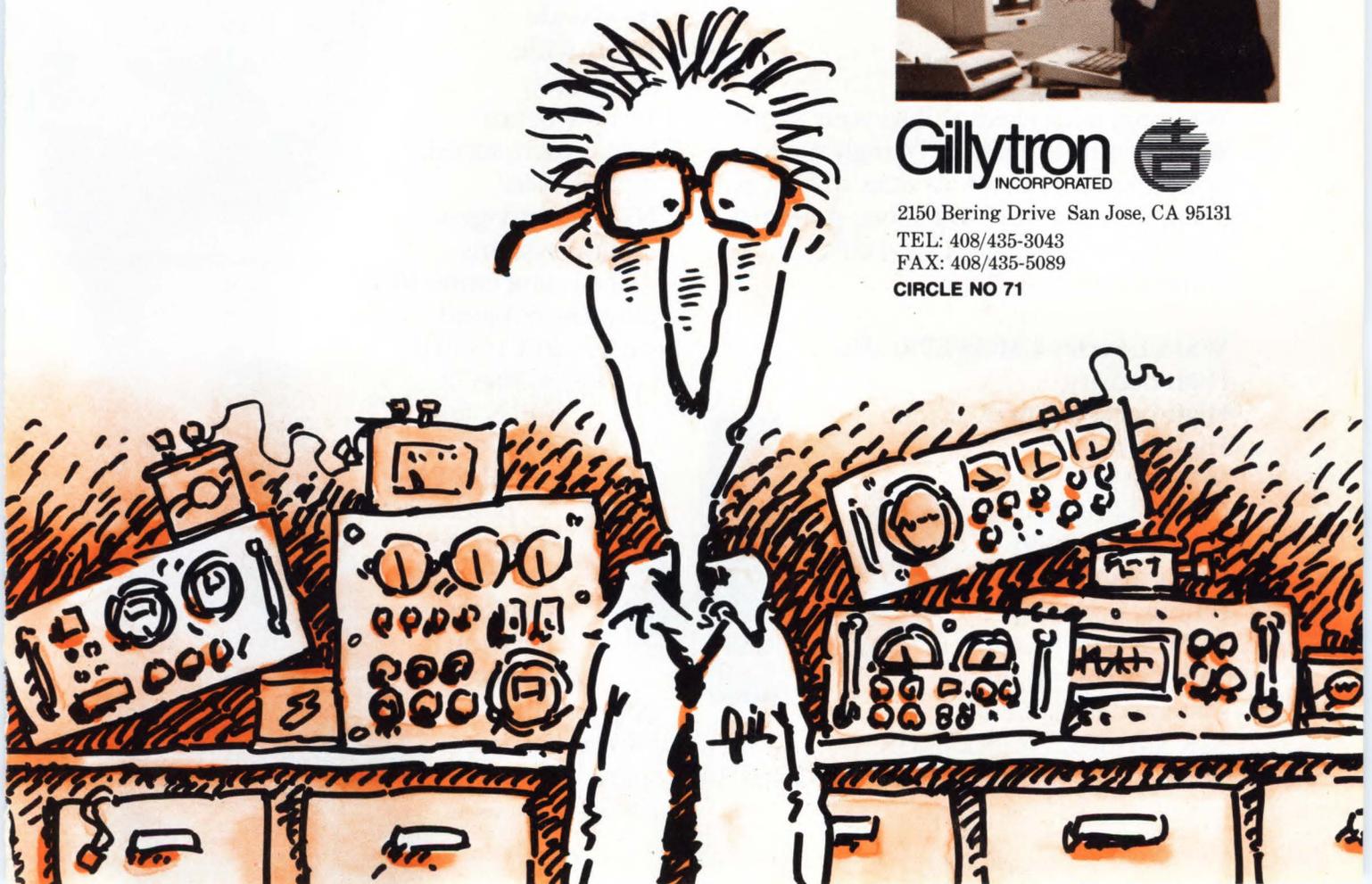
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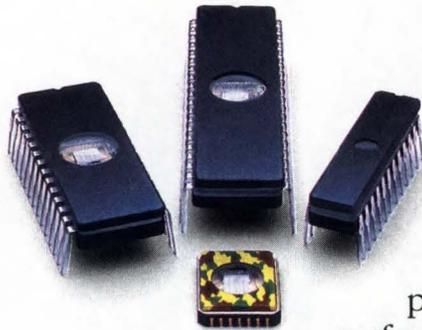
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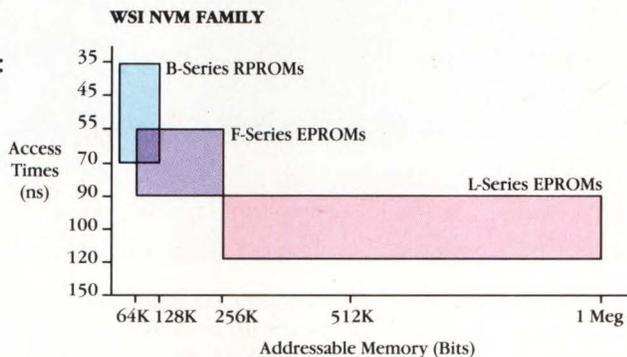
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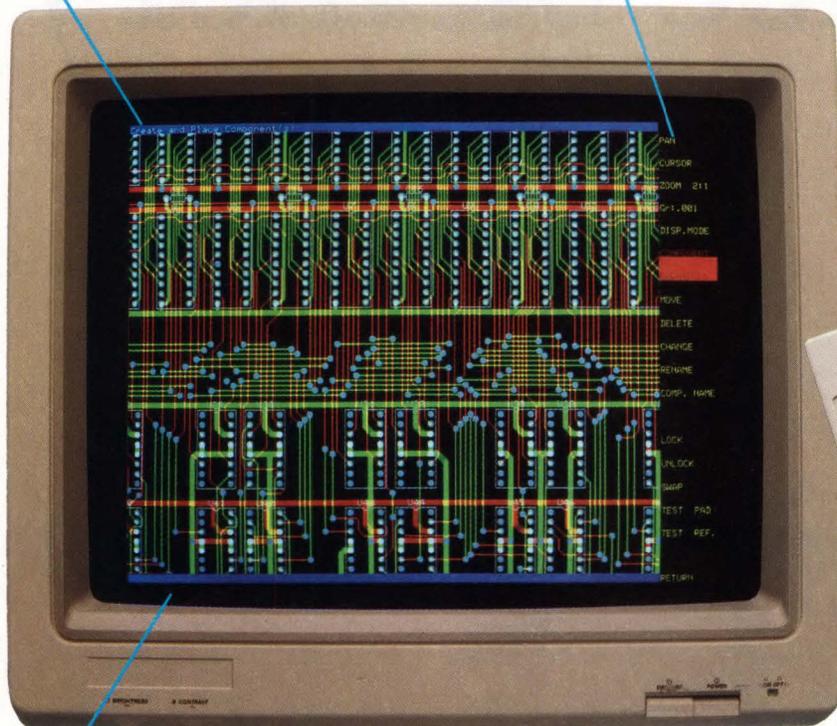
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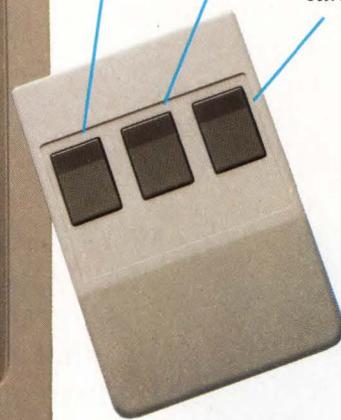
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Dynamic-RAM-controller ICs squeeze maximum performance from DRAMs

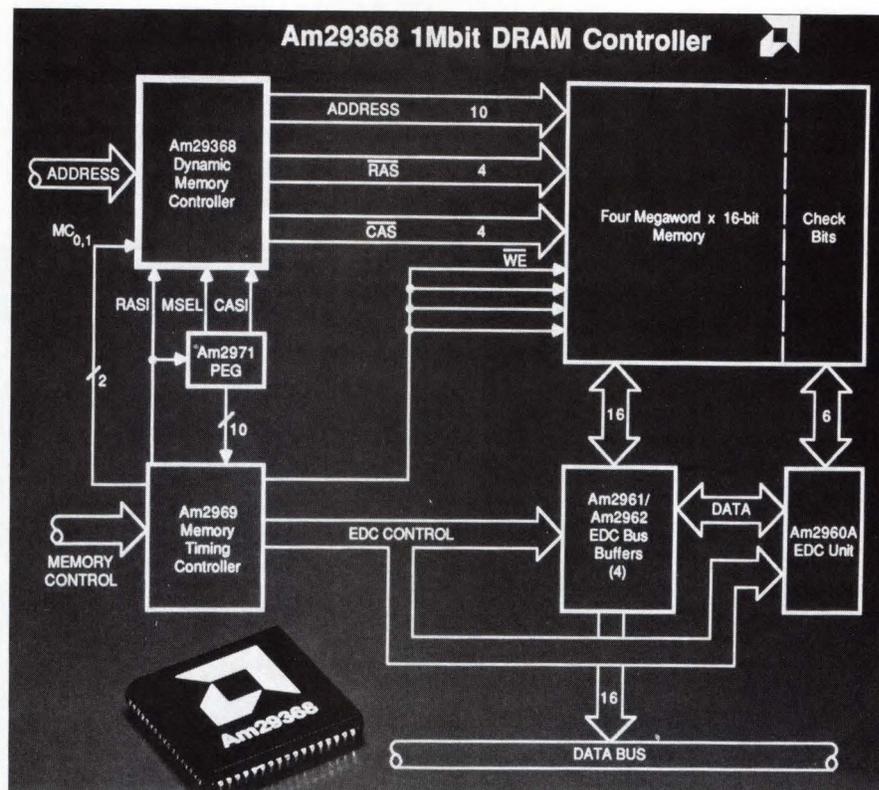
Steven H Leibson,
Regional Editor

Despite this year's acute parts shortage and the subsequent price increase, dynamic RAMs (DRAMs) still cost less than static RAMs (SRAMs) on a bit-by-bit basis, and they still take up less room on your pc board. However, DRAMs employ address-multiplexing and capacitive-storage techniques, which make them fussy about timing: The wrong timing signals can make them lose data, causing you thorny problems when you design DRAM controllers for memory subsystems.

For years, engineers have designed DRAM-controller circuits with general-purpose MSI components and delay lines. The current crop of DRAM-controller ICs, however, solves DRAMs' timing problems much more efficiently in terms of cost, pc-board space, and signal quality. In addition, many of the latest parts can help you take advantage of advanced DRAM features such as burst access. The cost of these controller ICs has dropped over the past few years, so they represent a more attractive alternative than ever to designing your own controller.

Critical timing requirements

When you use DRAMs in a system design, your controller circuitry must satisfy three critical timing requirements: RAS (row address strobe) and CAS (column address strobe) sequencing, refresh, and RAS precharge. DRAMs are also quite sensitive to signal undershoot. If your circuitry does not meet these DRAM timing and signal requirements, your system either will not



DRAM controllers that lack RAS/CAS- or refresh-timing generators—such as AMD's Am29368 DRAM-controller IC—can give you more flexibility to meet unusual DRAM sequencing requirements, but at a cost—they need additional ICs to create the timing signals that generate the sequencing.

work at all—if you're lucky—or will exhibit recurring, intermittent memory lapses. These failures are tough problems to troubleshoot, so you should take extraordinary measures to prevent them when designing a DRAM-based subsystem.

DRAM timing basics

The DRAM multiplexed-addressing sequence boils down to the same four steps for both read and write cycles. First, you present a row address, comprising half of the memory location's address bits, to the DRAMs' address inputs. Then you assert RAS, causing the DRAM to latch the row address. Next, you

present the column address—the second half of the memory address—to the DRAM's address inputs. Finally, you assert CAS, causing the DRAM to latch the column address. The address lines' timing must meet an assortment of setup-and-hold-time specifications with respect to both RAS and CAS.

One way to classify DRAM-controller ICs is by the presence or absence of on-chip RAS/CAS timing. Both types of controller have been available for some time (a selection of both appears in **Table 1**). Controllers with on-chip timing include the Texas Instruments (TI) THCT4502B and SN74ACT4503 and

TECHNOLOGY UPDATE

the National Semiconductor DP8400 controller series. TI's controllers generate the RAS/address/CAS sequencing with synchronous, clocked circuits, and National Semiconductor's devices incorporate precise silicon delay lines. In addition, you can control the timing on the National Semiconductor parts with external circuitry.

Some DRAM controllers contain no timing circuits; they provide RAS, CAS, and multiplexer-control inputs that permit other circuitry to control the timing. One such device

is the Am2968A from Advanced Micro Devices (AMD); it was one of the first DRAM-controller ICs to appear. Its RASI (RAS input), MSEL (multiplex select), and CASI (CAS input) pins accept timing signals from external circuitry.

Because of its early introduction, the Am2968A has become sufficiently popular to gain two alternate-source vendors: Motorola offers the MC74F2968A and Texas Instruments offers the SN74ALS2968 and a similar part, the SN74ALS2967; the latter has low-true RASI and

CASI signals. These controllers have 9-bit, 2-to-1 address multiplexers, so they accommodate DRAMs having capacities as large as 256k bits. AMD and TI now offer the Am29368 and the SN74ALS6302, respectively. These two controllers closely resemble the original Am2968 design, but they have an extra bit in the address multiplexer, so they support 1M-bit DRAMs. If you prefer low-true RASI and CASI signals, you can choose TI's SN74ALS6301 controller, which fills that bill.

TABLE 1 — REPRESENTATIVE DRAM-CONTROLLER ICs

MANUFACTURER	PART NUMBER	LARGEST RAM TYPE SUPPORTED (BITS)	BANKS	ADDRESS LATCHES	RAS/CAS TIMING
ADVANCED MICRO DEVICES	Am2968A	256k	4	YES	EXTERNAL
	Am29368	1M	4	YES	EXTERNAL
	673102	256k	4	YES	INT/EXT
	673103	1M	4	YES	INT/EXT
	673104	1M	4	YES	INT/EXT
AT&T	WE 32103	1M	4	YES	INTERNAL
HITACHI	HD63487 ²	256kx4 STATIC COLUMN	1	NO	INTERNAL
INTEL	8207	256k	4	YES	INTERNAL
	82C08	256k	2	YES	INTERNAL
MOTOROLA	MC74F2968A	256k	4	YES	EXTERNAL
NATIONAL SEMICONDUCTOR	DP8409	256k	4	YES	INT/EXT
	DP8419	256k	4	YES	INT/EXT
	DP8420	256k	4	YES	INTERNAL
	DP8421	1M	4	YES	INTERNAL
	DP8422	4M	4	YES	INTERNAL
	DP8429	1M	4	YES	INT/EXT
NCR	52C40 ²	4M	4	YES	INTERNAL
SIGNETICS	74F764	256k	1	YES	INTERNAL
	74F765	256k	1	NO	INTERNAL
	74F1764	1M	1	YES	INTERNAL
	74F1765	1M	1	NO	INTERNAL
TEXAS INSTRUMENTS	SN74ACT4503	1M	4	YES	INTERNAL
	SN74ALS2967	256k	4	YES	EXTERNAL
	SN74ALS2968	256k	4	YES	EXTERNAL
	SN74ALS6301	1M	4	YES	EXTERNAL
	SN74ALS6302	1M	4	YES	EXTERNAL
	THCT4502B	256k	4	YES	INTERNAL
VLSI TECHNOLOGY	VL4500A	64k	2	YES	INTERNAL
	VL4502	256k	4	YES	INTERNAL
	VL86C110	1M	2	NO	INTERNAL

NOTES:

1. PRICING FOR INTEL AND AT&T PARTS IS FOR 10-MHz VERSIONS
2. SEE BOX, "SPECIALIZED DRAM CONTROLLERS"

TECHNOLOGY UPDATE

One reason that DRAM controllers without on-chip RAS/CAS timing have remained popular is that they allow you to generate unconventional CAS sequencing. For memory-subsystem designs that employ special DRAM features such as page- or nibble-access modes, your controller circuitry must generate multiple CAS cycles for each RAS cycle. The DRAM controller must be able to change address lines while continuing to assert CAS for static-column mode access. Controllers without on-chip timing circuits

give you a good compromise between function and density when you employ DRAM burst-access sequences. Most DRAM controllers with internal timing generators do not support such burst-access sequences, so if you use the controller in such a design, you must circumvent the internal generators.

Special parts for burst access

When used in conjunction with a burst-access DRAM-controller design, TI's SN74ALS6310 and SN74ALS6311 ICs help you take

advantage of DRAMs' static-column or page-mode access features. The parts employ 14-bit address comparators to determine whether the current access cycle has the same DRAM row address as the preceding cycle. This detection function allows external circuitry to postpone the termination of the preceding RAS cycle and the initiation of an additional CAS cycle, if necessary. Each device costs \$7.20 (1000).

You can create timing signals for DRAM controllers by using a counter IC and some decoding logic, a

ON-CHIP REFRESH SUPPORT	PRICE ¹	SPECIAL DEVICE FEATURES
COUNTERS	\$19 (100)	EXTERNAL CAS TIMING SUPPORTS NIBBLE-MODE ACCESS
COUNTERS	\$30 (100)	EXTERNAL CAS TIMING SUPPORTS NIBBLE-MODE ACCESS
COUNTERS	\$19 (100)	TWO CAS OUTPUTS FOR BYTE ENABLES IN 16-BIT SYSTEMS
COUNTERS	\$29 (100)	TWO CAS OUTPUTS FOR BYTE ENABLES IN 16-BIT SYSTEMS
COUNTERS	\$36 (100)	FOUR CAS OUTPUTS FOR BYTE ENABLES IN 32-BIT SYSTEMS
CONTROLLER	\$50 (1000)	DUAL-PORT ARBITER, SUPPORTS OVERLAP OF MEMORY ACCESS AND MMU TRANSLATION
CAS BEFORE RAS	\$25 (5000)	MEMORY-INTERFACE CHIP FOR COMPANY'S HD63484 ADVANCED CRT CONTROLLER
CONTROLLER	\$28.60 (1000)	CONTROLS COMPANION ERROR-CORRECTION CHIP AND PROVIDES MEMORY SCRUBBING
CONTROLLER	\$13.20 (1000)	POWER-DOWN MODE KEEPS DRAMS REFRESHED
COUNTERS	\$17.55 (100)	EXTERNAL CAS TIMING SUPPORTS NIBBLE-MODE ACCESS
CONTROLLER	\$6 (1000)	INTERNAL OR EXTERNAL REFRESH CONTROL, REQUIRES EXTERNAL REFRESH CLOCK
CONTROLLER	\$11 (1000)	INTERNAL OR EXTERNAL REFRESH CONTROL, REQUIRES EXTERNAL REFRESH CLOCK
CONTROLLER	\$12 (1000)	WAIT-STATE GENERATOR; MEMORY INTERLEAVING; SUPPORTS NIBBLE, PAGE, AND STATIC-COLUMN ACCESS
CONTROLLER	\$15 (1000)	WAIT-STATE GENERATOR; MEMORY INTERLEAVING; SUPPORTS NIBBLE, PAGE, AND STATIC-COLUMN ACCESS
CONTROLLER	\$20 (1000)	DUAL-PORT; WAIT-STATE GENERATOR; MEMORY INTERLEAVING; SUPPORTS NIBBLE, PAGE, AND STATIC-COLUMN ACCESS
CONTROLLER	\$15 (1000)	INTERNAL OR EXTERNAL REFRESH CONTROL, REQUIRES EXTERNAL REFRESH CLOCK
CONTROLLER	\$23.73 (1000)	DUAL-PORT I/O BUFFER CONTROLLER; ADDRESS AND LENGTH COUNTERS ON BOTH PORTS
CONTROLLER	\$9 (1000)	DUAL-PORTED; SUPPORTS EXTERNAL MULTIPLEXING FOR DRAMS LARGER THAN 256k
CONTROLLER	\$9 (1000)	DUAL-PORTED; SUPPORTS EXTERNAL MULTIPLEXING FOR DRAMS LARGER THAN 256k
CONTROLLER	\$11 (1000)	DUAL-PORTED; SUPPORTS EXTERNAL MULTIPLEXING FOR DRAMS LARGER THAN 1M
CONTROLLER	\$11 (1000)	DUAL-PORTED; SUPPORTS EXTERNAL MULTIPLEXING FOR DRAMS LARGER THAN 1M
CONTROLLER	\$15.60 (1000)	INTERNAL OR EXTERNAL REFRESH INITIATION
COUNTERS	\$11.40 (1000)	EXTERNAL CAS TIMING SUPPORTS NIBBLE-MODE ACCESS
COUNTERS	\$11.40 (1000)	EXTERNAL CAS TIMING SUPPORTS NIBBLE-MODE ACCESS
COUNTERS	\$21.60 (1000)	EXTERNAL CAS TIMING SUPPORTS NIBBLE-MODE ACCESS
COUNTERS	\$21.60 (1000)	EXTERNAL CAS TIMING SUPPORTS NIBBLE-MODE ACCESS
CONTROLLER	\$8.40 (1000)	ON-CHIP ARBITRATION BETWEEN READ/WRITE ACCESS AND REFRESH
CONTROLLER	\$4.95 (10,000)	INTERNAL OR EXTERNAL REFRESH INITIATION
CONTROLLER	\$7.84 (10,000)	ON-CHIP ARBITRATION BETWEEN READ/WRITE ACCESS AND REFRESH
CONTROLLER	\$14.12 (10,000)	ON-CHIP MMU, 3-CHANNEL DMA CONTROLLER, PAGE-MODE ACCESS LOGIC

TECHNOLOGY UPDATE

delay line, or a timing-generator PLD. Counters cost very little, but the combination of a counter and decoding circuits may not be able to create the precise timing resolution you seek. Delay lines provide very precise timing signals with a resolution of a few nanoseconds, and they operate asynchronously, which is advantageous for many designs. Delay lines are often expensive, however.

PLDs give you a lot of flexibility to create complex timing sequences. An example of such a PLD is AMD's \$14.75 (100) Am2971A programmable event generator (PEG), an improved version of the company's Am2971, which runs at 100 MHz and can switch any of its 12 outputs at 10-nsec intervals. (The original Am2971 runs at 70 MHz and can only switch output states every other clock cycle.) The Am2971A has an on-chip phase-locked loop, so it can run at a frequency that's a multiple of your system's clock frequency. AMD offers a \$200 adapter and software kit, AmPegasus, that allows you to program the Am2971 and Am2971A on a Data I/O (Redmond, WA) Model 29 programmer.

Don't forget the refresh

Once you have a memory subsystem's RAS/CAS timing worked out, you must accommodate the DRAMs' need for refresh cycles. Because DRAMs store data as charge on

capacitors, each DRAM memory cell must be refreshed periodically. The traditional refresh technique involves a RAS-only cycle, although some DRAMs implement additional schemes. Every RAS address must be exercised within a refresh-time interval specified by the DRAM manufacturer. Failure to refresh the DRAMs allows the stored charge to bleed off the capacitors and produces memory lapses.

Most DRAM controllers incorporate some sort of refresh-support circuitry, because the function is crucial to proper DRAM operation. Simpler DRAM controllers have a counter that maintains the value of the next row address to be refreshed. You must add a refresh timer to help these parts generate refresh cycles. Here again, you can use a counter IC or a PLD to generate the necessary timing. Or you can use a device designed specifically for that purpose, such as TI's SN74ALS6300 refresh timer, which costs \$7.20 (1000).

More advanced DRAM controllers incorporate complete refresh-control circuitry that generates refresh cycles at appropriate intervals and arbitrates among memory-access requests from other system components (the μ P, the DMA controller, etc) and the on-chip refresh timer. On-chip arbitration lets you avoid adding extra circuitry to the memory subsystem's critical timing

path and can reduce the time needed to arbitrate between access and refresh cycles.

For example, National Semiconductor's DP8422, which incorporates both a refresh controller and a refresh arbiter, has an address-strobe-to-CAS delay of 79 nsec. That delay represents the device's critical timing path. The company's DP8429 controller, which does not incorporate a refresh arbiter, has a critical-path RASIN-to-CAS delay of 70 nsec.

Although the DP8429 initially appears to be faster than the DP8422, it's actually not. To make the DP8429 perform memory accesses as quickly as the DP8422, you must make sure that the refresh-arbitration circuitry you place between the DP8429 and your μ P adds no more than 9 nsec of delay to that critical path. Some lower-performance-system designs use the host μ P or a DMA controller to refresh the DRAMs, so they don't need circuitry to arbitrate between access and refresh cycles and they don't require a DRAM controller with a refresh arbiter.

A rest stop for tired DRAMs

Once you've satisfied both the RAS/CAS and the refresh timing, you may also need to ensure that the DRAMs' RAS-precharge requirements are met. The RAS-precharge period allows the DRAMs to rest

Special DRAM controllers suit niche applications

Although most DRAM controllers fall into the general-purpose category, a few companies now offer specialized devices for niche applications. These controllers allow DRAMs to work in designs that previously employed static RAMs (SRAMs). For example, Hitachi's HD63487 Memory Interface and Video Attribute Controller (MIVAC) joins the company's HD63484 advanced CRT controller to as many as four 256k \times 4-bit static-column DRAMs. Thus, five ICs can replace as much as 0.5M bytes of SRAM.

NCR's 52C40 CMOS Memory Array Controller

(CMAC) targets I/O applications that require high-speed, dual-ported buffer memories. The CMAC addresses as many as 16M words of DRAM and supports data-transfer rates to 3M words/sec. Each of the device's two ports incorporates an address register and a transfer-length counter so that address generation can occur entirely on the chip during transfers, without intervention by the host μ P. Because the buffer-memory data path does not flow through the CMAC, you can implement any word width your application requires.

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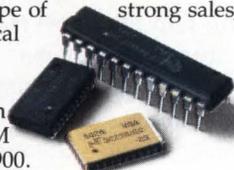
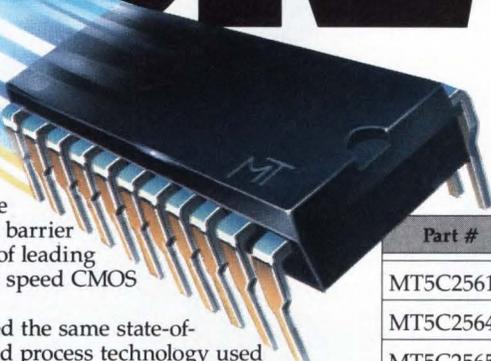
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MT5C2568	32K X 8	25ns	PDIP, CDIP, SOJ, LCC
MT5C6401	64K X 1	15ns	PDIP, CDIP, SOJ
MT5C6404	16K X 4	15ns	PDIP, CDIP, SOJ
MT5C6405	16K X 4 \overline{OE}	15ns	PDIP, CDIP, SOJ
MT5C6406/7	16K X 4 s.I/O	15ns	PDIP, CDIP, SOJ
MT5C6408	8K X 8	15ns	PDIP, CDIP, SOJ, LCC
MT5C1601	16K X 1	15ns	PDIP, CDIP, SOJ
MT5C1604	4K X 4	15ns	PDIP, CDIP, SOJ
MT5C1605	4K X 4 \overline{OE}	15ns	PDIP, CDIP, SOJ
MT5C1606/7	4K X 4 s.I/O	15ns	PDIP, CDIP, SOJ
MT5C1608	2K X 8	15ns	PDIP, CDIP, SOJ

*Slower speeds also available.

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between access cycles. During RAS precharge, a DRAM recovers from a previous cycle by charging internal nodes to appropriate reference-voltage levels, in preparation for the next cycle. DRAMs require RAS-precharge periods between successive access cycles, following an access and just before a refresh cycle, and just before an access cycle that immediately follows a refresh cycle.

If you fail to comply with a DRAM's RAS-precharge requirements, you invite memory failures. Many μ Ps normally allow ample time between access cycles for RAS precharge, but adding refresh cycles and DMA accesses to the cycle mix can complicate system timings and create RAS-precharge period violations. Multiprocessor-based designs can also encounter RAS-precharge problems.

A DRAM controller that incorporates a RAS-precharge timer and a refresh controller helps you avoid RAS-precharge problems. National Semiconductor's DP8420, DP8421, and DP8422, for example, contain a programmable timer that enforces a delay of 1 to 3 clock cycles between accesses. However, you can add circuitry to less-complex controllers to serve the same purpose. In simpler systems that lack DMA controllers and do not employ multiple processors, you may find that you don't need RAS-precharge timing circuitry, because the system's design inherently precludes such problems.

Two ports may be better than one

Shared-memory, multiprocessor systems place additional burdens on the memory-subsystem designer beyond the need to avoid RAS-precharge violations. Besides the refresh-cycle arbitration circuitry, you need circuitry to arbitrate among multiple access requests. For synchronous systems, arbitration generally doesn't present too much of a problem, but asynchronous arbitration logic introduces one of the worst problems a logic designer can face: metastability.



The data sheets, application notes, and devices packaged in the \$149 Memory Management Design Kit from Texas Instruments constitute a complete memory-subsystem design package. The kit also includes floppy disks containing graphic-symbol libraries from Logic Automation (Beaverton, OR) and FutureNet (Chatsworth, CA); the libraries support the automated design of memory subsystems that use parts from the kit.

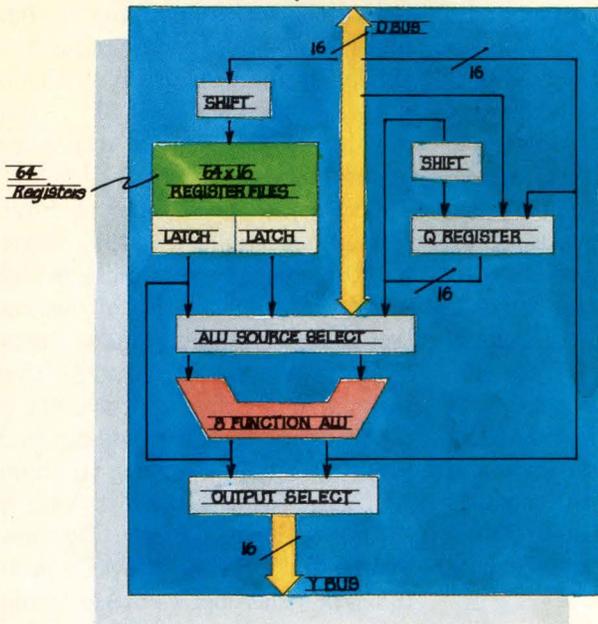
When an arbitration flip-flop enters a metastable state because of setup-and-hold violations, its outputs assume an indeterminate value. In practice, that means that either no requesting processor will be granted access to the memory subsystem, or more than one processor will be granted simultaneous access. Either case generally results in a catastrophic system crash. Asynchronous, multiport arbiters constructed from MSI components

are riddled with metastability problems.

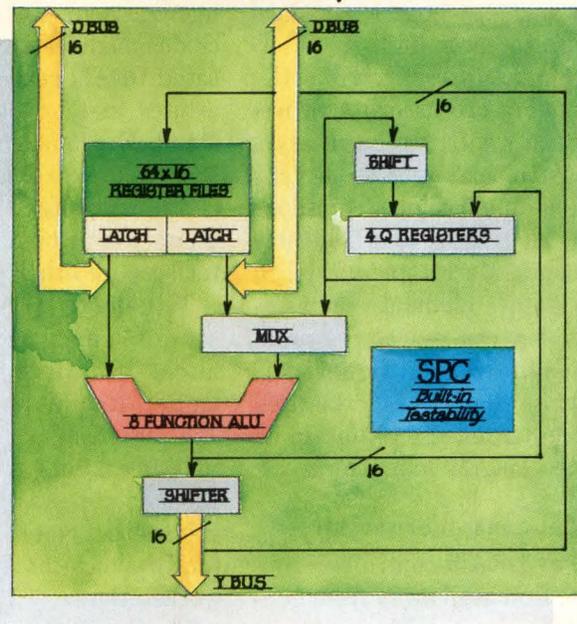
Some DRAM-controller vendors offer dual-ported parts and attack the metastability problem in a variety of ways. National Semiconductor's DP8422 contains synchronous dual-port arbitration circuitry. Your design must meet the part's setup-and-hold requirements. For systems in which the various requesters all run on synchronized clocks, this approach is the simplest solution.

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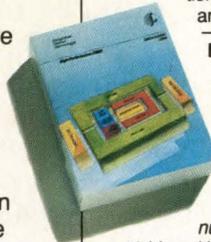
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However, not all multiprocessor systems have the luxury of synchronous operation. For example, a system that includes both a standard μ P and a processor built from bit-slice components rarely runs the two dissimilar processors synchronously. Such systems require asynchronous arbiters built from very fast, metastable-hardened flip-flops that have small setup-and-hold-time requirements. Metastable-hardened flip-flops do not eliminate metastability but they can reduce the problem to insignificance. Signetics is one company that has incorporated metastable-hardened flip-flops in its dual-ported DRAM controllers.

The DRAM-controller toolkit

Multiport DRAM controllers represent the first step away from general-purpose parts. If you think your design might benefit from an even more tailored device, consider using TI's DRAM-controller ASIC

toolkit, which lets you employ the company's 1- μ m ASIC process to build custom controllers with as many as four ports. The toolkit includes modules for a fairly sophisticated DRAM controller, for a 4-port arbiter, and for several interfaces to standard μ Ps such as the Motorola 68020 and 68030 and Intel's 80186, 80286, and 80386. The company can assist you in building processor interfaces for other μ Ps as well.

TI defines an ASIC toolkit as a set of supermacros (functional blocks or modules). Its DRAM-controller toolkit works with its TSC500 standard-cell library. The toolkit costs between \$10,000 and \$20,000, depending on the modules you license, and it runs on the Mentor Graphics family of engineering workstations.

The toolkit's DRAM controller contains several programmable or selectable functions, including RAS/CAS timing, latch-and-go circuitry

that allows the host μ P to initiate a write to memory and then immediately proceed to the next bus cycle before the write operation is complete, a row-detection comparator similar to that provided by the company's SN74ALS6310 and SN74ALS6311, and a wait-state generator.

Because of the number of different options available to the controller, the company recommends that you make at least some of the controller's programming signals accessible to external circuitry, either through input pins or via a set of control registers. By adding such programmability, you can create an ASIC that you can incorporate in several different designs. This programmability also allows you to tune the controller's DRAM timing sequences once the ASIC is installed on a pc board. The ability to perform such fine-tuning can be critical when you need to squeeze every

Careful layout optimizes memory performance

The main enemy of precise DRAM timing control is capacitance contained in the pc-board traces and in DRAM address-line inputs. Large capacitive loads slow DRAM-controller performance, a factor you must take into account when calculating the overall performance your memory subsystem will deliver. The amount of capacitance your memory subsystem presents to the controller depends on the number and type of DRAMs you use and on the pc-board layout.

Further, if you add external buffers to help the DRAM controller drive high capacitances, you'll have to account for the buffer delays in your timing calculations. If the controller you select does not have a sufficient number of RAS outputs to drive the DRAM banks your application requires, you'll have to add external multiplexing circuitry. You may also need to add external multiplexers to the DRAM controller's CAS outputs for 16-bit-word, 32-bit-word, and wider memory subsystems that must also support byte-wide transfers. Most DRAM controllers lack multiple CAS drivers. Some other devices that do have more than one CAS output can't use these CAS drivers to perform byte-mode accesses. Multiplexers introduce

additional delay.

Because it's very tough to accurately predict and model these buffer delays, multiplexer delays, and pc-board capacitances before fabricating a pc board and building a prototype memory subsystem, you should design flexibility into the address-sequence timing for a DRAM array. No amount of CAE modeling is going to allow you to build an optimized circuit from the loose characterizations of MSI components and modeled pc-board-trace characteristics. If you use a DRAM controller with internal timing, you'll want to make sure the part allows you to tweak sequence timing. If you use external circuitry for sequencing control, be sure to build some timing leeway into that circuitry.

Line reflections also hamper your ability to accurately model the performance of a memory subsystem. The long traces generally used to wire large DRAM arrays are transmission lines. You must either terminate these lines to prevent reflections or take reflections into account.

If your design employs proper terminations and output buffers capable of driving the line's characteristic impedance, you'll observe incident-wave

TECHNOLOGY UPDATE

unnecessary nanosecond out of the memory's access time.

One module this DRAM controller toolkit does not include is a set of DRAM output drivers. All of the DRAM controllers listed in **Table 1** can drive the high-capacitance loads of large DRAM arrays, but TI's 1- μm process can't build such husky output circuits. If you use this toolkit to design an ASIC DRAM controller, you should plan to add external buffers to your final circuit. Buffers add additional delay to the DRAM control-signal timing, so access to the controller's programmable timing features will be even more important.

The toolkit's four arbiter ports employ double-latch synchronizers to handle asynchronous access requests. The latches in the synchronizer operate from opposite edges of the controller's 50-MHz clock. TI claims it has thoroughly characterized the metastable characteristics

of flip-flops built with its 1- μm process and verified that flip-flops entering a metastable state at one edge of the clock will recover in less than 10 nsec—before the next clock edge. Thus, the second synchronizer latch prevents any metastability that might occur in the first latch from confusing the arbiter. This synchronization technique adds a clock delay of between 0.5 and 1 (less than 20 nsec) to a memory subsystem's access time.

Controllers tailored to a μP

You may not need to resort to an ASIC in order to obtain a specialized DRAM controller. VLSI Technology and AT&T manufacture controllers specifically adapted to μPs from those companies. Both companies' parts illustrate ways in which you can closely integrate DRAM-controller functions in a system.

AT&T's WE 32103 DRAM controller is a companion part for the

company's WE 32100 32-bit μP . Because the controller is intimately mated to the processor, it can boost the memory subsystem's performance beyond the level you might achieve with a general-purpose part. For example, the controller initiates memory cycles early in the processor's bus cycle by emitting an appropriate row address and asserting RAS, but it delays CAS until its chip-select input is asserted. In the event that the current bus cycle is not directed at the DRAM array, the controller terminates the memory cycle without asserting CAS, transforming the operation into an extra refresh cycle.

Likewise, by using low-order, untranslated address bits for the row address, the controller can initiate a memory cycle before the processor's memory-management unit (MMU) translates a logical address to a physical address. This feature allows the controller to overlap MMU

switching in your circuit—in other words, the voltage at the DRAM's input will reach proper logic levels when the incident wave reaches that pin.

However, if your signal lines are unterminated and the output buffers in your design can't drive the line's characteristic impedance, or if you employ a series line termination (limiting the output buffer's drive current), you'll observe reflected-wave switching: The voltage at the DRAM's input will move halfway towards the buffer's output voltage when the incident wave passes it and will match the driver's output voltage after the wave is reflected at the far (unterminated) end of the line. Thus, reflected-wave switching takes somewhat longer than incident-wave switching because signals must propagate over longer paths before switching occurs.

Signetics' DRAM controllers give you a choice between incident-wave switching and reflected switching. The company's 74F764, 74F765, 74F1764, and 74F1765 controllers all incorporate unterminated output drivers, which provide incident-wave switching at the expense of allowing undershoot. Significant voltage undershoot can

wreck DRAM performance, but you can add line terminations to reduce this problem. The company also offers these same four devices with internal terminations at the same price as the unterminated parts. These parts (designated by a -1 suffix on the part number) provide reflected-wave switching and reduce undershoot. Signetics claims that arrays driven by its reflected-wave parts generally need no further termination.

You must also be very careful to provide good grounding and power-supply paths to the DRAM controller, because large DRAM arrays exhibit highly capacitive loads. At times—such as during a refresh cycle—the DRAM controller may try to change the logic levels on all of the address lines in the entire memory array simultaneously. During such events, the current flowing through the DRAM controller's power and ground pins will peak as charge stored in those address lines is dumped. If you don't provide low-impedance paths and adequate bypass capacitance to the ground and power pins, the logic levels inside the chip will shift as the ground rises and V_{CC} droops, causing the controller to behave unpredictably.

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and memory-subsystem operation, further improving system performance. The DRAM controller can perform burst-access cycles, which also enhance system performance, on page- and nibble-mode DRAMs for WE 32100 double- and quadruple-word data transfers.

Similarly, VLSI Technology's VL86C110's memory controller is closely coupled to the company's VL86C010 32-bit RISC (reduced instruction set computer) μ P. Acorn Computers Ltd (Cambridge, UK) developed the controller as part of a chip set for a series of low-cost, 32-bit workstations, but VLSI Technology markets the part to other companies as well.

The VL86C110 incorporates several functions not generally found in general-purpose DRAM controllers. For example, the device contains a 3-channel DMA controller, which was originally included in the IC's design to support video, sound, and cursor operations in Acorn's work-

stations. The DRAM controller translates the RISC μ P's ability to signal the occurrence of sequential memory accesses into multiple-CAS access cycles for page-mode DRAMs. The controller also incorporates an MMU that's tailored to the Acorn workstation's memory map and ROM interface circuitry; the MMU accommodates ROMs with access speeds as slow as 450 nsec. Consequently, the VL86C010 contains a clock generator that drives the RISC μ P and allows the controller to stretch the clocks during accesses to slow ROMs.

The diversity and price range of the DRAM controllers listed in **Table 1** demonstrate that no single component can possibly meet the needs of every application. Fortunately, this diversity works to your advantage. If you carefully list your application's needs and prioritize the features you'd like, you'll undoubtedly find a controller that meets your requirements. **EDN**

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For more information . . .

For more information on the DRAM-controller ICs mentioned in this article, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

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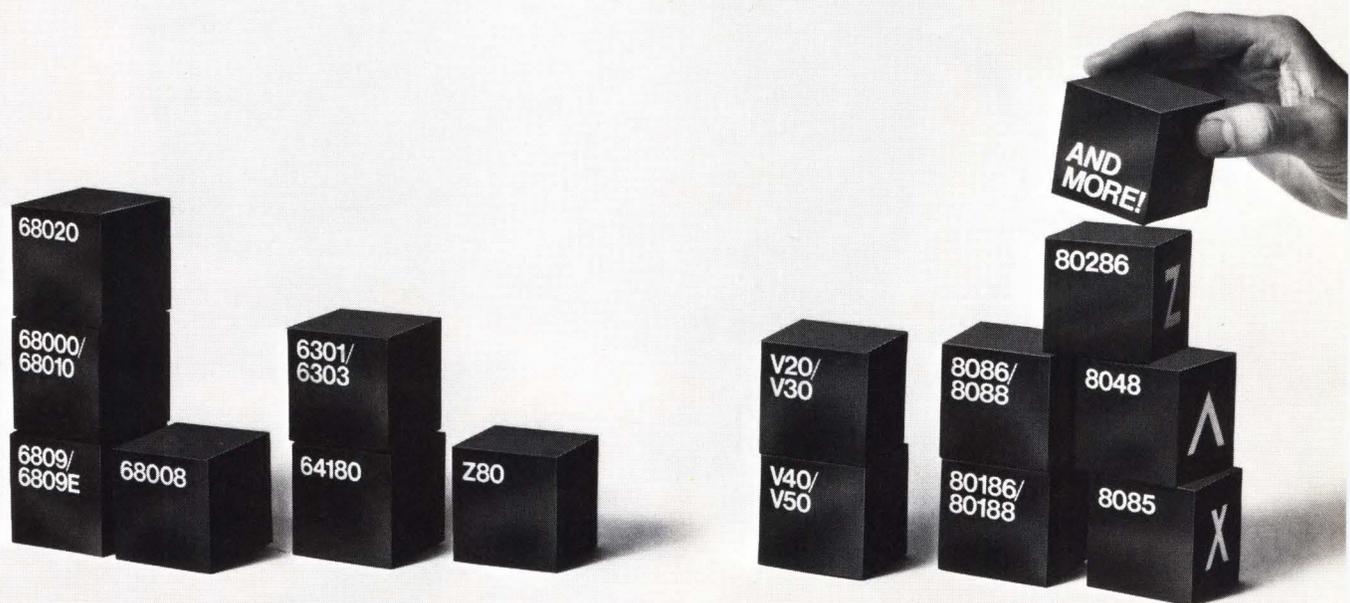
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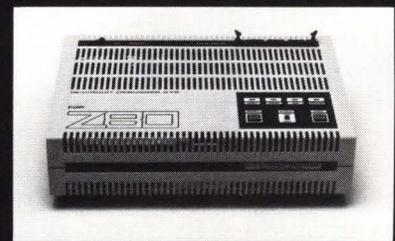
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The software package includes a C-language cross-compiler for the Unix host, communications software for the Unix host and OS-9 target, and a C compiler and a debug package for the OS-9 target. The C cross-compiler outputs executable OS-9 memory modules.

After downloading the modules via the network, you can debug the code at the source or symbolic level with the OS-9-based debugger.

In addition, the implementation of the TCP/IP allows the user to access the entire OS-9 operating system from the Unix host. The software supports remote log-in with the Telnet TCP/IP terminal-emulation application; it also supports file transfers with the TCP/IP file-transfer-program application, thus allowing you to perform debug operations from the Unix host.

After debug, you can deploy the OS-9-based target as a stand-alone system, or you can employ the target as a real-time front end to a Unix-based supervisor system. The downloaded code can access all of

the shareable system modules in OS-9 such as a library of I/O and mathematical routines. In diskless applications, the entire OS-9 operating system, and the C compiler and debugger can be stored in ROM.

The company presently offers the Unibridge package for Sun workstations, Hewlett-Packard Series 300 workstations, and DEC VAX systems. Unibridge for the VAX works with the VMS operating system as well as with DEC's version of Unix. The package costs \$6500.

—Maury Wright

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as it is when programming devices of a single type.

Clearly, the designers of the Gangpro-SP had production applications in mind; the unit is a stand-alone programmer with 512k bits of program RAM expandable to 4M bits—enough to hold eight JEDEC files. You can operate the programmer with a small handheld keypad included in the base price (or you can connect an ASCII terminal to

programming algorithms stored in EEPROMs inside the unit; the vendor distributes library updates on PC-formatted disks.

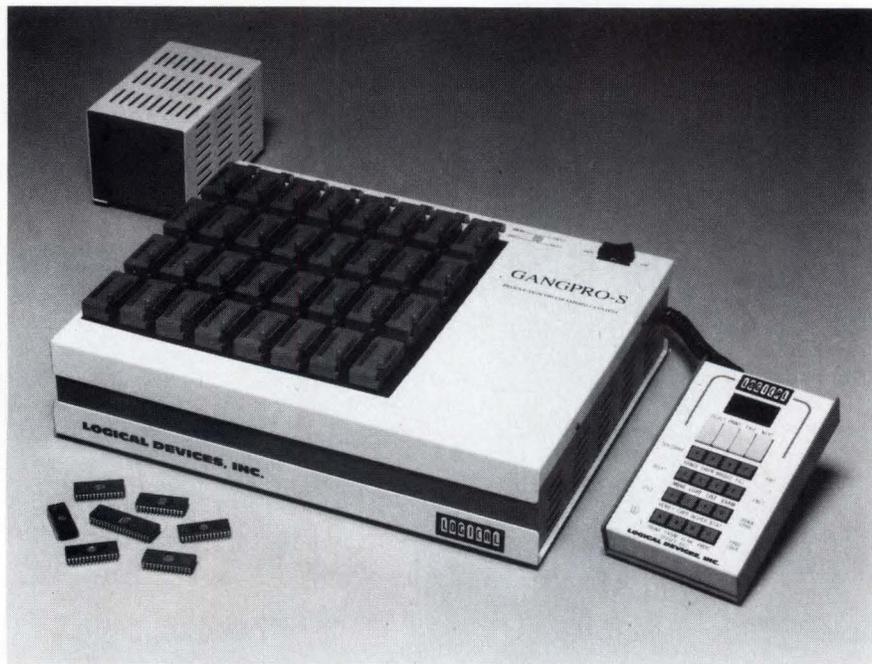
You can upgrade the unit to gang-program EPROMs and some single-chip microprocessors, as well as PLDs. (The configuration that handles 20- and 24-pin DIP PLDs can program eight EPROMs at once; a version that handles *only* EPROMs can program 32 devices simultaneously.) The EPROM/ μ P programming capability gives the instrument broad enough device coverage to make it the only production programmer in many companies. Another feature that should make the programmer popular in production is its internal clock/calendar. It can store the times at which you modify the RAM contents; a label-printing program running on a PC linked to the programmer's serial port can then print out labels that you can place on newly programmed ICs to indicate the exact version of the data they embody.

The Gangpro-SP8 (with eight 20- and 24-pin PLD programming stations) sells for \$7995. The EPROM- μ P upgrade costs \$600/station.

—Dan Strassberg

Logical Devices Inc, 1201 NW 65th Pl, Fort Lauderdale, FL 33309. Phone (800) 331-7766; in FL, (305) 974-0975. TLX 383142.

Circle No 703



This stand-alone programmer can program 32 EPROMs. When configured to program 20- and 24-pin PLDs (and optionally, EPROMs and μ P), it has eight programming stations.

figurations that handle plastic leaded-chip carriers and pin-grid packages with as many as 68 pins. It can do PLD set programming as well—that is, write *different* data into each of the ICs plugged into it. In fact, the instrument can actually program device sets composed of several types of ICs, though when operating in this mode it isn't as fast

the RS-232C port). You can make the RAM nonvolatile by installing a battery backup option. The keypad-controlled configuration should appeal to departments that can't justify dedicating a PC or terminal to a programmer and have trouble allocating shared resources. The only time you need to connect a PC is when you update the library of pro-

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Part Number	Function	t _{pd}	f _{max}	Power	Package
CXB1100Q	Quad 3-in OR/NOR	390 ps	1.5 GHz	530 mW	24 FLAT
CXB1101Q	Quad 3-in AND/NAND	470 ps	1.5 GHz	700 mW	24 FLAT
CXB1102Q	Quad 2-in EXOR/NOR	490 ps	1.5 GHz	680 mW	24 FLAT
CXB1103Q	Quint Line Receiver	410 ps	1.5 GHz	650 mW	24 FLAT
CXB1104Q	Dual D Flip Flop	620 ps	3.2 GHz	520 mW	24 FLAT
CXB1105Q	Triple Fan-out Buffer	590 ps	1.5 GHz	720 mW	24 FLAT
CXB1106Q	4-Stage Ripple Counter		3.4 GHz	720 mW	24 FLAT
CXB1107Q	Decision Circuit		3.2 GHz	430 mW	24 FLAT
CXB1108Q	Laser Driver		2.0 GHz	740 mW	16 FLAT
CXB1109Q	Quad D-FF with Master Reset	620 ps	3.4 GHz	790 mW	24 FLAT
CXB1110Q	16 to 1 Multiplexer	610 ps	1.5 GHz	680 mW	24 FLAT
CXB1111Q	Look Ahead Carry Block	580 ps	1.5 GHz	610 mW	24 FLAT
CXB1112Q	Phase Frequency Detector	720 ps	0.8 GHz	500 mW	24 FLAT
CXB1113Q	4 to 1 Multiplexer		2.0 GHz	950 mW	24 FLAT
CXB1114Q	1 to 4 Demultiplexer		2.5 GHz	1100 mW	24 FLAT
CXB1130Q	9, 8, 4-bit Multiplexer		1.6 GHz	730 mW	32 FLAT
CXB1131Q	9, 8, 4-bit Demultiplexer		1.6 GHz	1000 mW	32 FLAT
CXB1132Q	9, 8, 4-bit Universal Shift Register		1.3 GHz	910 mW	32 FLAT
CXB1133Q	22, 15, 7-Stage Scrambler		1.6 GHz	600 mW	24 FLAT
CXB1134Q	22, 15, 7-Stage Descrambler		1.6 GHz	610 mW	24 FLAT
CXB1135Q	8-16 bit Comparator		1.3 GHz	630 mW	32 FLAT
CXB1136Q	8-bit Universal Counter		1.2 GHz	730 mW	32 FLAT
CXB1137Q	8-bit Shift Matrix	1250 ps		700 mW	24 FLAT
CXB1138Q	4-bit Arithmetic Logic Unit	1460 ps		680 mW	24 FLAT

packs. The list you see here is only partial. So if you don't see what you need, please inquire with your specific requirements.

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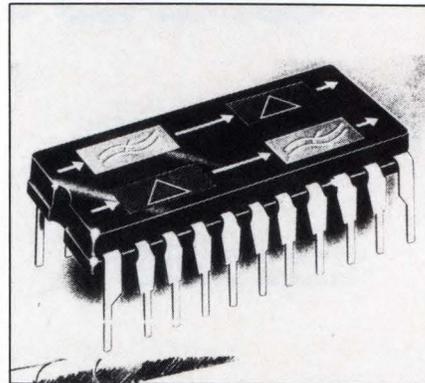
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Delta codec meets requirements for military communications

Meeting the requirements of the NATO Eurocom D1-IA8 specification, the FX619 full-duplex, single-chip CVSD (continuously variable slope delta) codec is suitable for use in a variety of military communications systems including delta multiplexers, switches, and telephones. Because it includes both encoder and decoder sections, as well as the audio filters that are required on the encoder input and decoder output, the device can significantly reduce component count, particularly on multichannel line cards. All you need to add are input and output buffers to convert the unbalanced input and output of the FX619 to

the balanced 600 Ω input and output required by the Eurocom spec. Fabricated in CMOS, the device operates from a single 5V supply and draws a typical supply current of 4.5 mA in its active mode, and 500 μ A in its standby mode.

You can program the delta codec's sampling rate to 16k, 32k, or 64k bps, with all timing for the device's switched-capacitor filters and CVSD modulator and demodulator derived from an on-chip oscillator that accepts a 1.024-MHz crystal. Or, you can clock the device from an external clock source to achieve sampling rates within the range of 8k to 64k bps. The device provides



Incorporating input and output filters, as well as a full-duplex delta codec, the FX619 can reduce parts counts in military communications equipment.

clock outputs that allow you to synchronize external circuitry to the codec.

For multiplexer applications, an enable input allows you to enable or disable the encoder section of the device. Other features include an encoder forced-idle mode that generates a 10101010-output bit stream, and a decoder forced-idle mode that produces an output bias of half the supply voltage. You can also program the device to perform either a 3- or 4-bit companding algorithm.

The FX619 is available in a 22-pin ceramic DIP or a 28-lead ceramic surface-mount package. It has an operating temperature range of -40 to $+85^{\circ}\text{C}$ and is processed to MIL-STD-883C requirements. It sells for £20 (1000).— **Peter Harold**

Consumer Microcircuits Ltd, 1 Wheaton Road, Witham, Essex CM8 3TD, UK. Phone (0376) 513833. TLX 99382.

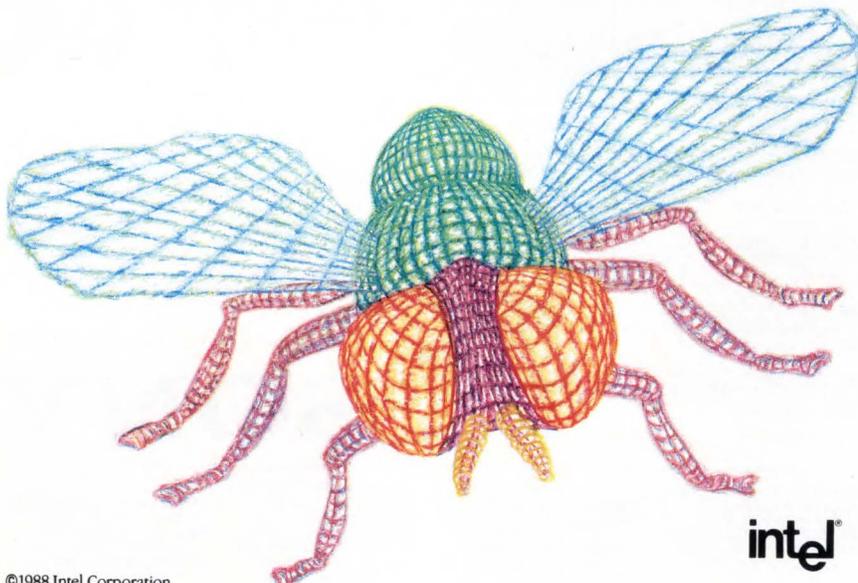
Circle No 701

Mx-Com Inc, 4800 Bethania Station Rd, Winston-Salem, NC 27105. Phone (919) 744-5050.

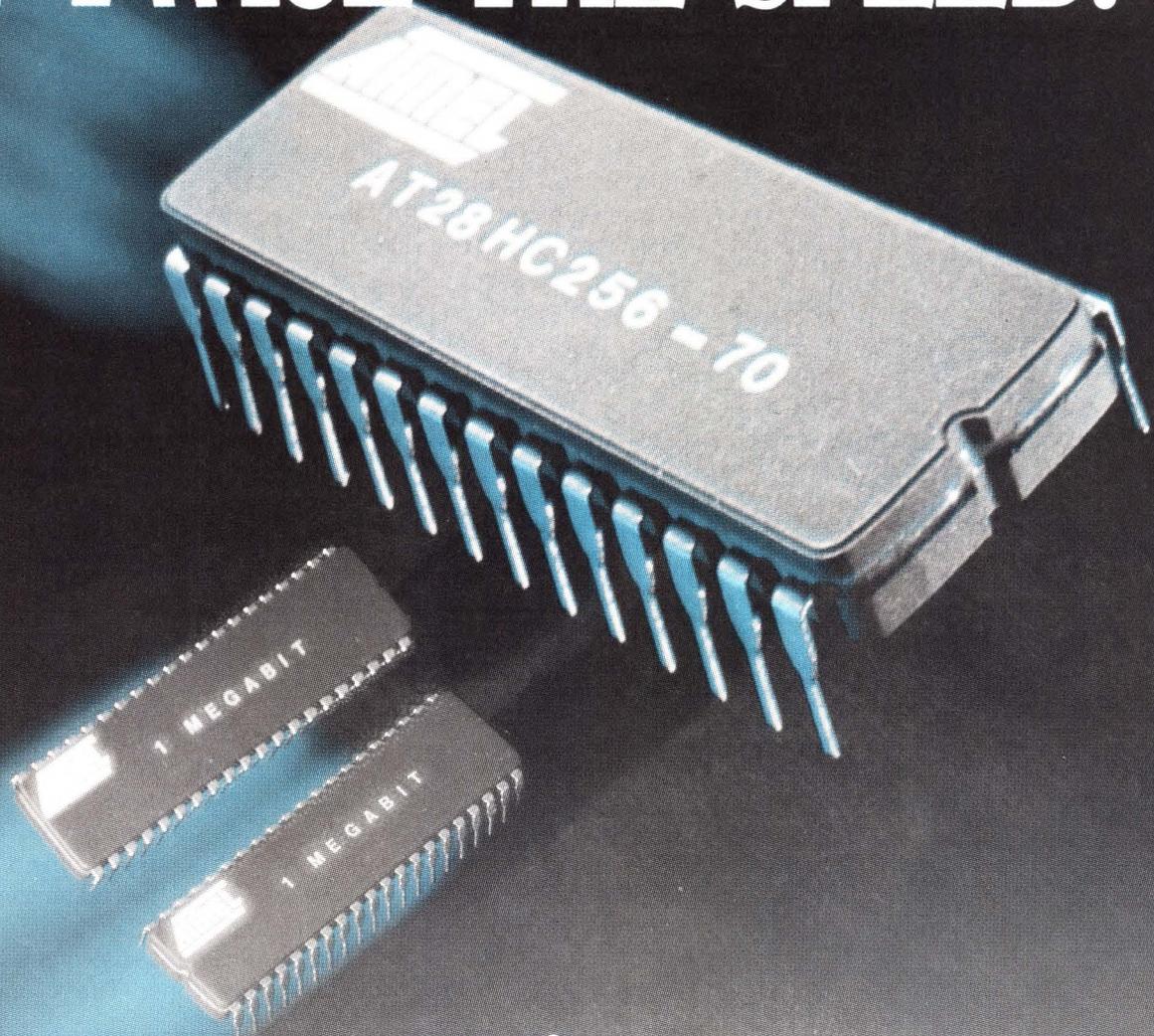
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256K CMOS E²PROM Family

Density	Part Number	Organization	Speed (ns)							Package P D L J F	Mil 883C
			70	90	120	150	200	250	300		
256K	AT28C256	32K x 8
256K	AT28HC256	32K x 8

P-Plastic; D-Ceramic Dip; L-Leadless Ceramic; J-Plastic j-leaded; F-Flat Pack

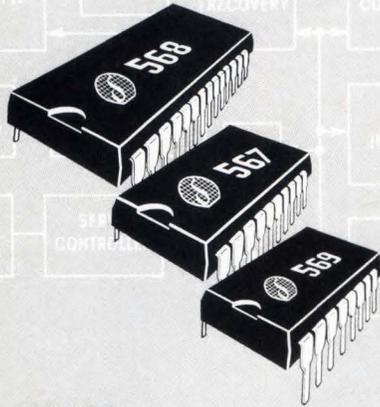


CIRCLE NO 80

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- Quadrature servo pattern
- Linear velocity control loop
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SSI 569 SERVO MOTOR DRIVER

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- Compatible with complementary power FETS
- Bridge output driver configuration
- Automatic head retract and spindle motor brake command in the event of power supply failure

Now, with Silicon Systems new Servo Chip Set, HDD designers have the means to provide fast, precise, head positioning in their high performance hard disk drives.

The new chip set provides superior performance and features lower power dissipation, reduced board space, and lower cost than alternative design approaches. With its high level of integration, the set includes all the functional building blocks needed in the servo channel, and it is easily controlled via the microprocessor interface.

For more information, contact:
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INNOVATORS IN INTEGRATION

CIRCLE NO 84

DSO 400M - sample /sec stores 50k-word records

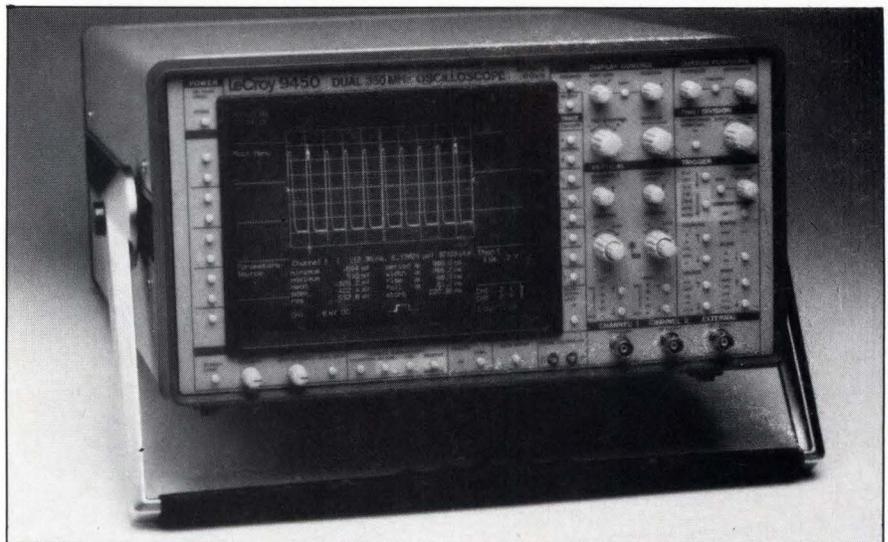
A DSO (digital-storage oscilloscope) whose maximum sampling rate is the same as the LeCroy 9450's—400M samples/sec—but whose maximum record length is a fairly standard 1k words can sample at its maximum rate only at sweep speeds faster than 250 nsec/div. The 9450 is different. Using flash ADCs, it can sample two channels simultaneously to 8-bit precision at 400M samples/sec, and it can do so with its sweep speed set from 1 nsec to >10 μ sec/div. It owes this unusual ability to acquisition memories that, with 50k words of battery-backed RAM for each of the scope's two channels, are approximately 50 times as deep as those of most competitive scopes. Each memory can store a single waveform record, or you can partition it to store as many as 200 records.

The 9450 is neither the least nor the most expensive high-performance DSO on the market today, but the array of features it offers in

addition to its unusual memory depth clearly make it worth a careful look by anyone considering the purchase of a DSO with fast real-time-sampling capability. People who take a close look are bound to be impressed by the clarity of the 4096 \times 4096-pixel display on the 5 \times 7-in., amber-phosphor CRT and the scope's ability to expand a portion of a waveform for close inspection—as much as 1000 times horizontally or 10 times vertically.

A noteworthy feature of the display is the way it portrays waveforms. To avoid an effect known as "perceptual aliasing" the scope draws straight lines between sampled data points. But to avoid confusing you about where the data was actually sampled, it highlights the sampling points.

Like many DSO manufacturers, LeCroy has taken considerable care to provide its scopes with a human interface that mimics those of analog scopes. The 9450, of course, aug-



A 5 \times 7-in. amber-phosphor CRT and controls that look and feel familiar to analog-scope users hide a number of unusual features of this 400M-sample/sec DSO. For example, two 50k-word display memories allow you to use the maximum sampling rate with relatively long-duration sweeps.

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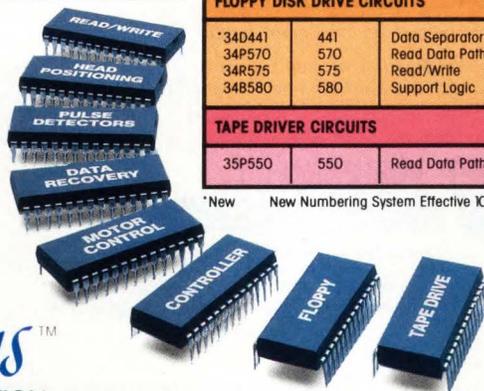
The adjacent chart illustrates that Silicon Systems can also provide more than a score of circuits for pulse detection, data recovery, head positioning, spindle motor control, and controller electronics. And the list continues to grow.

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MICROPERIPHERAL IC SELECTION CHART

SSI Device Numbers		Head Type	# of Channels	Max Input Noise nV/√Hz	Max Input Capacitance (pF)	Read Gain (Typ)	Write Current Range (mA)	Power Supplies	Read/Write Data Port(s)
New	Old								
HDD READ/WRITE AMPLIFIERS									
32R1048	104	Ferrite	4	2.4	23	35	15 to 45	+6V, -4V	Differential, Bi-directional
32R104BLN	104L	Ferrite	4	1.7	23	35	15 to 45	+6V, -4V	Differential, Bi-directional
32R114	114	Thin Film	4	1.1	65	123	55 to 110	±5V	Differential/Differential
32R115	115	Ferrite	2, 4, 5	1.8	20	40	30 to 50	±5V	Differential, Bi-directional
32R117	117	Ferrite	2, 4, 6	2.1	23	100	10 to 50	+5V, +12V	Differential/TTL
32R117A	117A	Ferrite	2, 4, 6	1.7	20	100	10 to 50	+5V, +12V	Differential/TTL
32R188	188	Ferrite	4	2.4	18	43	35 to 70	+6V, -5V	Differential, Bi-directional
32R501	501	Ferrite	4, 6, 8	1.5	23	100	10 to 50	+5V, +12V	Differential/TTL
*32R510A	510A	Ferrite	2, 4, 6	1.5	20	100	10 to 40	+5V, +12V	Differential/TTL
*32R511	511	Ferrite	4, 6, 8	1.5	20	100	10 to 40	+5V, +12V	Differential/TTL
*32R512	512	Thin Film	8	0.9	32	150	10 to 40	+5V, +12V	Differential/TTL
*32R514	514	Ferrite	2, 4, 6	1.5	20	150	10 to 40	+5V, +12V	Differential/TTL
32R520	520	Thin Film	4	0.9	65	123	30 to 75	±5V	Differential/Differential
32R521	521	Thin Film	6	0.9	65	100	20 to 70	+5V, +12V	Differential/TTL
*32R522	522	Thin Film	4, 6	1.0	32	100	6 to 35	+5V, +12V	Differential/TTL
HDD PULSE DETECTION									
32P540	540	Read Data Processor			Time Domain Filter				
32P541	541	Read Data Processor			AGC, Amplitude & Time Pulse Qualification, RLL Compatible				
HDD DATA RECOVERY									
32D531	531	Data Synchronizer			Data Synchronizer/Write Precompensation				
*32D532	532	Data Separator			Data Synchronizer/2, 7 RLL ENDEC				
*32D533	533	Data Synchronizer			Data Synchronizer/Write Precompensation				
*32D534	534	Data Separator			Data Synchronizer/MFM ENDEC/Write Precompensation				
*32D535	535	Data Separator			Data Synchronizer/2, 7 RLL ENDEC/Write Precompensation				
HDD HEAD POSITIONING									
32H101A	101A	Preamplifier-Ferrite Head			AV = 93, BW = 10MHz, e _n = 7.0nV/√Hz				
32H116	116	Preamplifier-Thin Film Head			AV = 250, BW = 20MHz, e _n = 0.94nV/√Hz				
*32H567	567	Servo Demodulator			Di-bit Quadrature Servo Pattern; PLL Synchronization				
*32H568	568	Servo Controller			Track & Seek Mode Operation; Microprocessor Interface				
*32H569	569	Servo Motor Driver			Head Parking, Spindle Motor Braking				
HDD SPINDLE MOTOR CONTROL									
32M590	590	2-Phase Motor Speed Control			±0.035% Speed Accuracy; Unipolar Operation				
32M591	591	3-Phase Motor Speed Control			±0.05% Speed Accuracy; Unipolar Operation				
*32M593	593	3-Phase Motor Speed Control			±0.037% Speed Accuracy; Bipolar Operation				
HDD CONTROLLER/INTERFACE									
*32B450A	450A	SCSI Controller			Async transfer to 2MBPS; Initiate/Target Modes; Internal Drivers; CMOS				
*32C452	452	Storage Controller			20Mbits/sec; CMOS; Programmable; AIC-010 Compatible				
*32C453	453	Buffer Controller			Non-mux addressing to 16K; CMOS; AIC-300 Compatible				
32B545	545	Support Logic			Includes ST506 Bus Drivers/Receivers				
FLOPPY DISK DRIVE CIRCUITS									
*34D441	441	Data Separator			High Performance Analog Data Separator, NEC 765 Compatible				
34P570	570	Read Data Path			2 Channel Read/Write With Read Data Path				
34R575	575	Read/Write			2, 4 Channel Read/Write Circuit				
34B580	580	Support Logic			Port Expander, Includes SA400 Interface Drivers/Receivers				
TAPE DRIVER CIRCUITS									
35P550	550	Read Data Path			4 Channel Read/Write With Read Data Path				

*New New Numbering System Effective 10/1/87

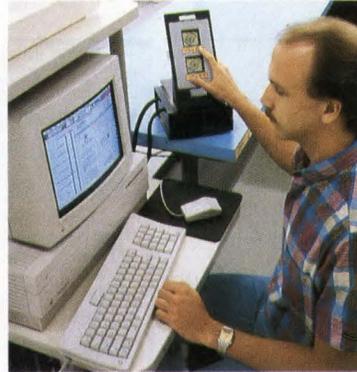
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EDUCATION

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"LabVIEW is the best single software entity that has been written to date for any computer for any purpose." Dr. John O'Dell, professor of Mechanical Engineering, uses LabVIEW in his course on computer-controlled systems.



AUTOMATED TESTING

Sundstrand-Sauer

"With LabVIEW, I have reduced testing time for our control panels from 15 minutes to less than 1 minute." Jay Herman is in charge of testing Sundstrand control panels used on concrete paving machines. A GPIB-controlled power supply tests the power requirements for these machines. Analog and digital lines on the control panel are tested with the NB-MIO-16 board.

MEDICINE

Sahlgren University Hospital-Sweden

"Without any earlier experience with programming, we were writing our own applications after the LabVIEW 3-day training course." Dr. Anders Ullman uses LabVIEW in clinical pharmacology. Muscle contractions evoked by nerve stimulation or by different drugs are measured via isometric force transducers with a plug-in analog input board. Each channel is monitored on a LabVIEW strip chart.



PHYSICS

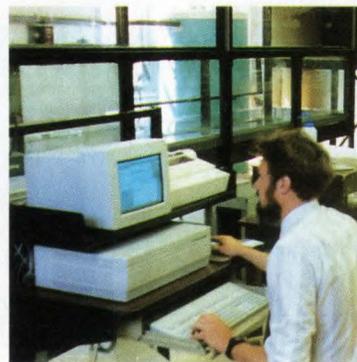
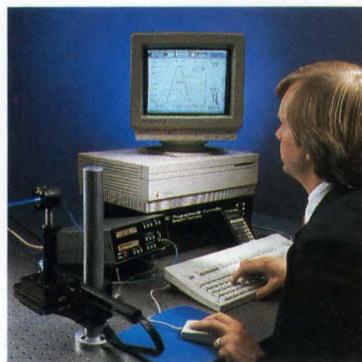
The University of Texas
at Austin

"We initially set up our system on a MicroVAX. It took 6 months. With LabVIEW and a Macintosh II, we got it working in a couple of weeks." Azucena Overman, graduate student in the Physics Department, researches the chemical properties of surfaces. In her research, LabVIEW controls GPIB instruments and graphs the data collected.

OPTICS

Newport Corporation

"LabVIEW is the software system we needed to complement our instruments." Scott Jordan includes LabVIEW with a Newport Optical Power Meter and a Newport Programmable Controller in a laser control system marketed by Newport Corporation.



CIVIL ENGINEERING

Stanford University

"LabVIEW is the most flexible data acquisition software I've ever seen—it's also a bit of fun." Dr. Steven Monismith of the Civil Engineering Department uses an experimental pond to research double diffusive systems. LabVIEW and an NB-MIO-16 board measure signals from temperature and conductivity probes in the pond, and control a motor that varies the depth of the probes.

SEMICONDUCTOR RESEARCH

Raytheon Company

"LabVIEW is the system of choice for data acquisition." John Day uses LabVIEW and GPIB instruments to measure physical properties of GaAs semiconductors. LabVIEW generates graphs of capacitance versus frequency and capacitance versus voltage.

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SIMULATION

Engineering Measurements Company

"LabVIEW saved me several months of development." John Wacers simulates digital signal processing algorithms with LabVIEW. The algorithms are burned into EPROMs on intelligent flow meters manufactured by Engineering Measurements Company.

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UPDATE

ments that interface with on-screen menus and "soft" keys adjacent to its screen. In addition, automated measurement modes abound. For example, the scope can automatically set its sensitivity, sweep speed, and sweep delay to provide a clear picture of a low-repetition-rate pulse. Then, without your having to take additional action, it can provide a numeric display of as many as ten parameters of the pulse train—for example, repetition rate, 10-to-90% rise time, and RMS voltage.

LeCroy boasts about the 9450's flexible triggering: Not only can it delay starting a sweep for a selectable interval following a trigger condition, but it can also delay the sweep until it has recognized a selected number of trigger events—the number can be as large as a billion. A glitch-capture feature lets you trigger on pulses either narrower or wider than a selected duration, and the duration can be as small as 2.5 nsec. Several pattern-triggering modes let you set the scope to trigger only after specified data patterns appear at the two signal inputs, the trigger input, or some combination of the three.

In addition to real-time sampling of periodic or nonperiodic waveforms, the 9450 can also perform random equivalent-time sampling of periodic signals. It can do so at an effective rate of 10G samples/sec. When performing equivalent-time sampling, the scope's frequency response is governed by the 350-MHz bandwidth of its input channels, not by the sampling rate.

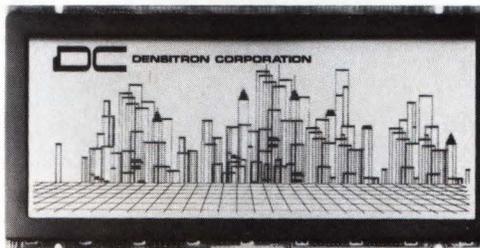
The 9450 includes RS-232C and IEEE-488 ports. You can power it from 110 or 220V ac from 48 to 440 Hz. It weighs 33 lbs and has a list price of \$18,900. Delivery is four to eight weeks ARO.

—Dan Strassberg

LeCroy, 700 Chestnut Ridge Rd., Chestnut Ridge, NY 10977. Phone (914) 425-2000. TWX 710-577-2832.

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PRODUCT UPDATE

Disk drive offers 25M bytes of removable storage

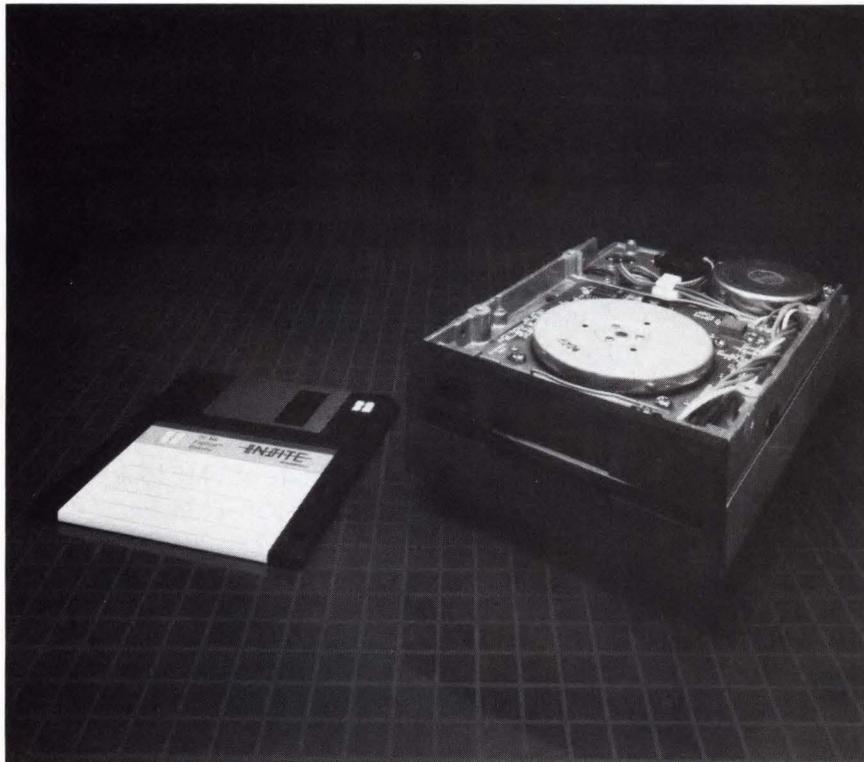
The Model I325 Floptical disk drive is a removable-disk storage system in a 3½-in. format. It provides 25M bytes of unformatted disk capacity and 20.8M bytes of formatted memory. Combining magnetic recording and the high track densities of an optical servomechanism, the drive delivers the best features of both technologies.

Providing portability, data security, and unlimited storage capacity, the drive combines the benefits of a removable, flexible medium with the low cost of a 20M-byte drive. Servo techniques developed for compact disks let the drive employ floppy-disk-drive elements such as spindle- and stepper-actuator motors, disk-loading mecha-

nisms, and spindle clamps. This design translates to cost savings in production.

The drive accepts a double-sided, high-density diskette. The manufacturer optically inscribes 1250 concentric grooves that are spaced approximately 20 µm apart. This arrangement provides a track density of 1250 tpi. Track densities of conventional magnetic floppy-disk drives range from 48 to 135 tpi; pure optical disk drives have densities over 15,000 tpi.

Because the tracks are invulnerable to erasure, the encoded optical tracks on the floppy's medium provide the servo for the drive. In addition, you don't need a defect-free servo pattern as you do in a



Combining magnetic recording with optical servo tracking, the Model I325 Floptical disk drive provides a low-cost, 20M-byte storage system with removable flexible medium.



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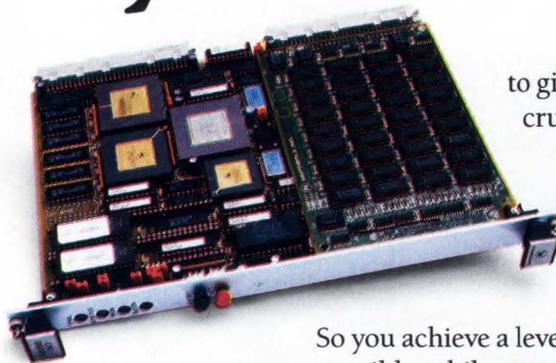
CIRCLE NO 265

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UPDATE

magnetically encoded servo. The drive records data on the magnetic medium between the servo tracks. A magnetic head reads and writes data at a recording density of 23.3k bpi.

Closed-loop optical servos enable the head to follow any data-track eccentricities caused by the drive or the medium. The servo uses LEDs similar to those in compact disks. To provide a position-error signal, the servo tracks the LED's reflected light through a low-cost optical lens onto a quad-element photodetector. The average seek time for the drive is 65 msec.

Before production, the company modifies a standard 3½-in. removable disk so that medium manufacturers don't have to alter their manufacturing processes. Using a proprietary servo formatter, the vendor licenses manufacturers to supply the diskettes.

The drive comes with an embedded disk controller and a common-command-set SCSI. The controller includes provisions for data formatting, error checking and correction, and defect mapping. For an IBM PC, PC/XT, PC/AT, or compatible computer without a SCSI host adapter, the company provides an optional host adapter. The drive is compatible with Apple's SCSI.

The company currently offers the units in evaluation-unit quantities. Volume production will begin in the fourth quarter of 1988. The disk drives will cost less than \$250 (OEM qty).—**John Gallant**

Insite Peripherals, 2363 Calle del Mundo, Santa Clara, CA 95054. Phone (408) 727-8484. FAX 408-727-7917.

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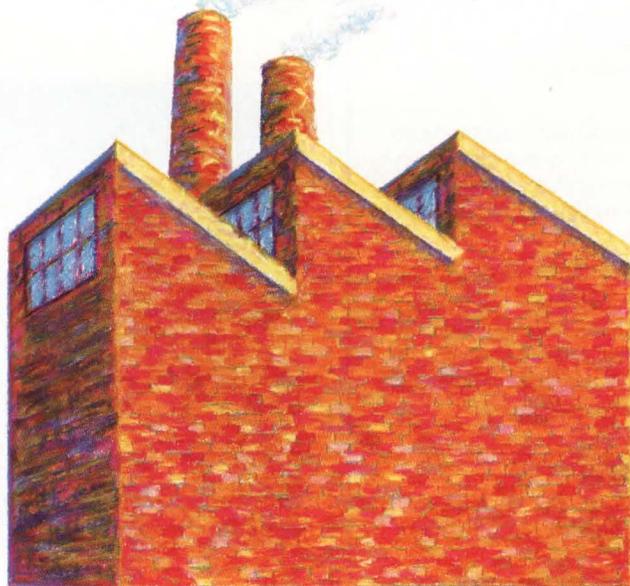
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PRODUCT UPDATE

Low-cost PC clone serves as real-time system

Configured as a real-time software-development workstation, the System 120 costs \$9250. The development system runs the vendor's compilers, assemblers, debuggers, monitor ROMs, editors, and real-time operating systems. In addition, the workstation can control proprietary in-circuit emulators and logic and software-performance analyzers. All the code that you develop will run on the company's Multi-bus systems and the workstation.

The workstation employs a 16-MHz 80386 μ P and the IBM PC/AT backplane of the vendor's System 301 PC/AT clone. It comes with a 2M-byte RAM, a 360k-byte floppy-disk drive, and a 40M-byte hard-disk drive. You can expand the RAM to 16M bytes and the hard disk to 80M bytes. In addition to the company's iSDM monitor ROM, the workstation comes with a clone BIOS ROM. The workstation can communicate over the DOS Open-Net LAN. The maker claims that the workstation can use most IBM PC/AT cards in its eight expansion slots.

The workstation's software package comprises both a configurable and a preconfigured iRMX II.3 operating system, PL/M, a 386 assembler, the AEDIT screen editor, and the Soft-Scope II source-level debugger. You can target real-time development for the host workstation or for other systems that use iRMX. Other languages such as Fortran, Pascal, and C are available.

The iRMX II operating system used in the System 120 provides programming facilities for interrupt management with custom exception handlers; support for multiple real-time tasks; preemptive, priority-based scheduling with round-robin (time-slice) scheduling within a priority level; and intertask communication through mailboxes and semaphores. Diskless OEM versions are available for \$3800 (50).

—Charles H Small

Intel Corp, Literature Dept
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Circle No 704



The System 120 is an IBM PC/AT clone that comes with a complete line of real-time software-development tools.

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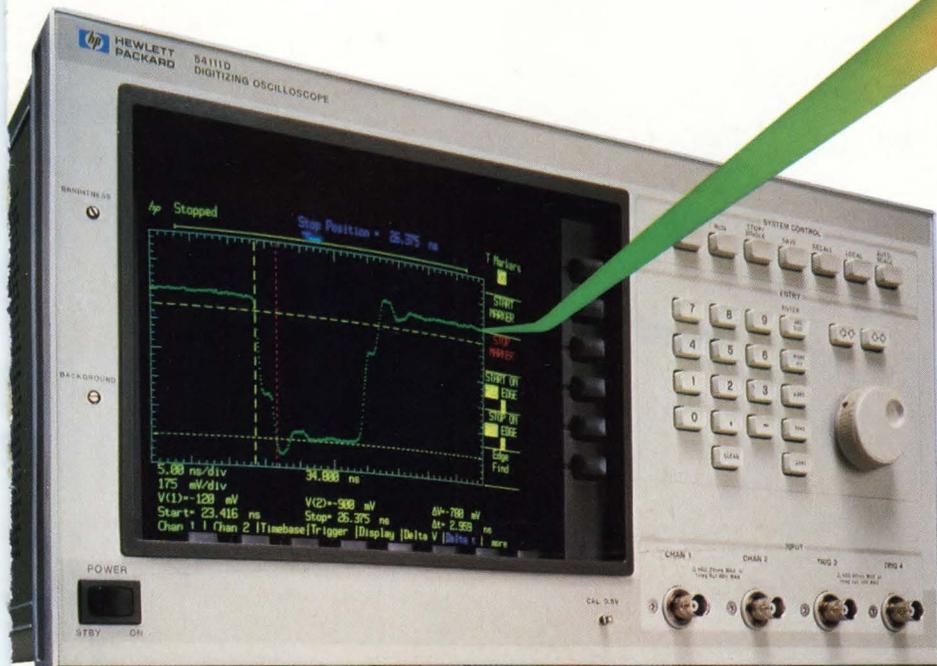
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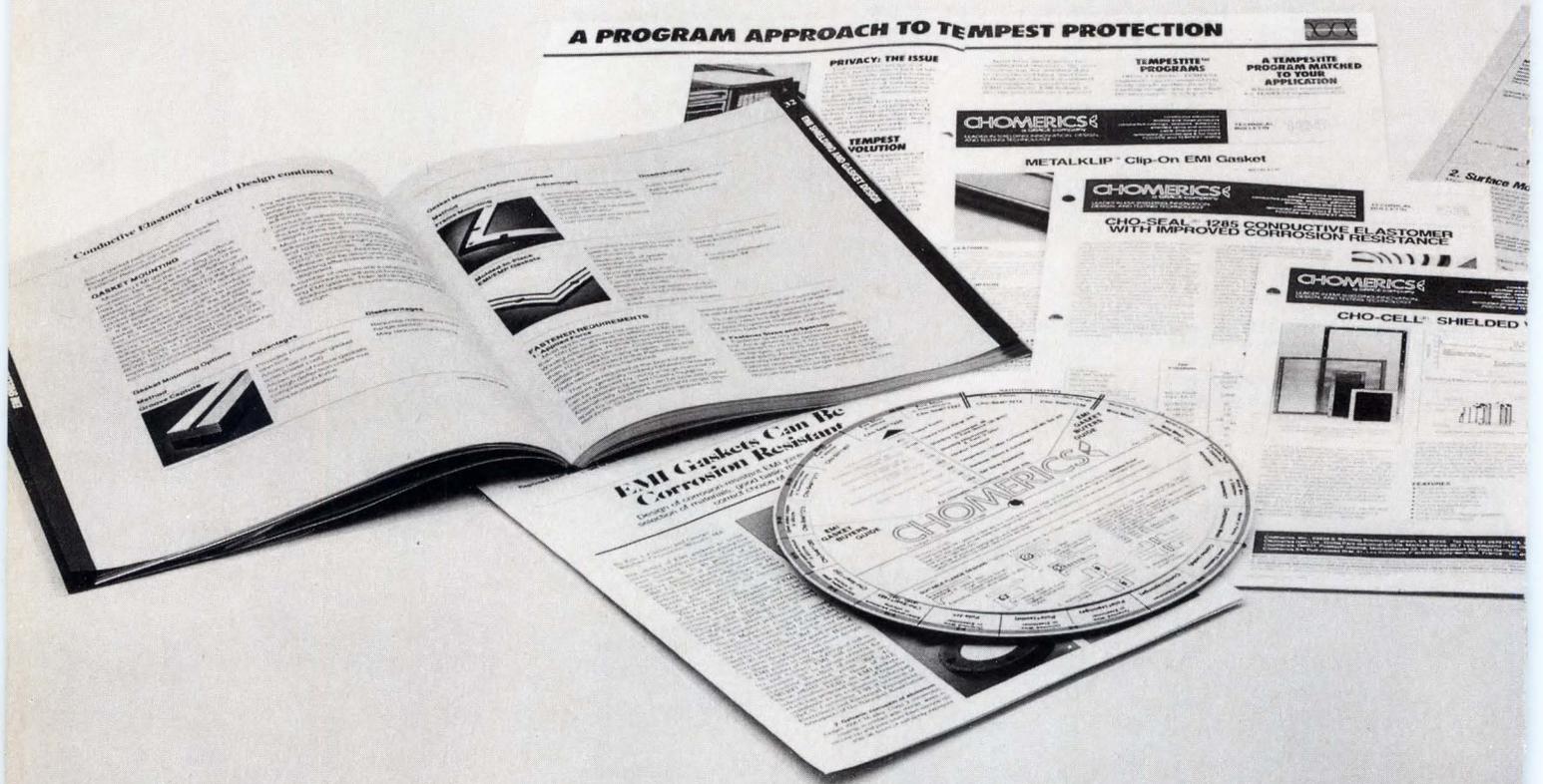
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*See our Application Note on 2 gigasample/s performance.



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- **Incorporating EMI shielding in your design**
CIRCLE NO. 39
- **Applications and material selection**
CIRCLE NO. 40
- **FCC/VDE compliance for commercial equipment**
CIRCLE NO. 41
- **MIL-SPEC compliance for military systems**
CIRCLE NO. 42
- **TEMPEST applications**
CIRCLE NO. 43
- **EMI testing**
CIRCLE NO. 44



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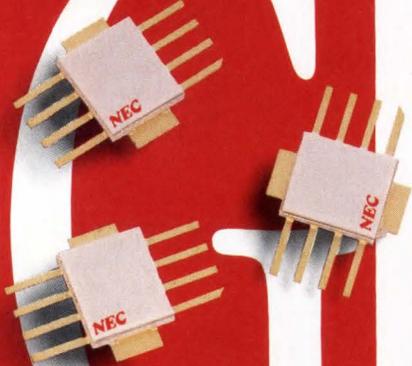
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CIRCLE NO 91

10 GHz



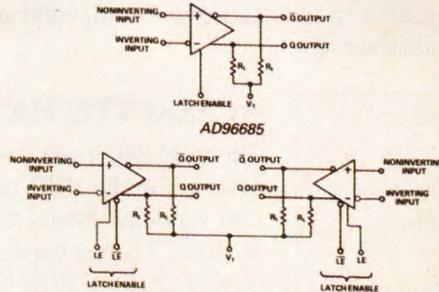
AD96685/AD96687

FEATURES

- 2.5ns Propagation Delay
- Consistent 50ps Propagation Delay Dispersion
- 0.5ns Latch Setup Time
- Stable Transition Zones
- Low Power Dissipation

APPLICATIONS

- High Speed Triggers
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- Threshold Detectors



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AD96687

Functional Block Diagrams

PRODUCT DESCRIPTION

The AD96685 (single) and AD96687 (dual) are ultrafast voltage comparators with short, consistent propagation delays and setup times. Both devices feature an incredible 50ps propagation delay dispersion for any overdrive from 100mV to 1V.

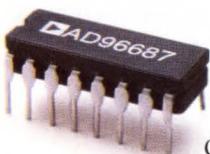
Propagation delays for both units are 2.5ns, and both have stable transition zones. They are manufactured with a high performance bipolar process and have differential inputs and complementary outputs fully compatible with ECL logic levels. Their 30mA output currents are capable of driving 50Ω terminated transmission lines; a latch enable input allows operation in either a sample mode or a track mode.

There are six models of the single AD96685 comparator; three operate over an industrial temperature range of -25°C to +85°C, and the other three are for extended temperatures of -55°C to +125°C. Two of the four models of the dual AD96687 unit operate over industrial temperatures, and the other two are for extended temperatures.

PRODUCT HIGHLIGHTS

1. Propagation delay dispersion of 50ps is the lowest available. Because of this extremely low dispersion, the AD96685 and AD96687 comparators can be used to make very fast, accurate and repeatable measurements despite wide variations in input overdrive; this improves performance for systems using these units.
2. The ultrafast latches allow the comparators to operate in a high speed sample (track)-and-hold mode. When the latch is used properly, input pulses of extremely short duration can be accurately detected and held for additional processing.
3. Since the latch operates on the input state of the comparator, the output state is dependent on the input at the time of the LATCH ENABLE command. This contrasts with strobed comparators, which operate on the output regardless of the input conditions at the time of the strobe.
4. Due to the elegant design of the AD96685 and AD96687 comparators, oscillation-free performance extends over a wide variation of input slew rates and overdrive conditions. This characteristic is not available in many other pin-compatible devices; they often have severe restrictions on how they can be used.

COMPARED TO WHAT'S ON THIS PAGE, NO OTHER COMPARATORS ARE EASIER TO USE.



If the output from your present comparator makes it difficult to use, take a look at the incomparable AD96685 and AD96687. They're the only comparators whose propagation delays remain constant to within 50 picoseconds for any overdrive from 100mV to 1V, so you always get consistent output.

The AD96685 and AD96687 also give you consistent speed, since they switch in 2.5ns, with a setup time of 0.5ns. And they have remarkably stable transition zones, which minimize oscillation.

But speed isn't achieved at the expense of power. The single AD96685 dissipates a mere 118mW, and the

dual AD96687 needs just 237mW.

In addition, the AD96685 and AD96687 each have an offset voltage of 1mV typical for a consistent starting point, and an input voltage range of -2.5V to +5V.

Now despite all these advantages, you won't have to change your board design for the AD96685 and AD96687. They're ECL-compatible and drop-in replacements for standard devices.

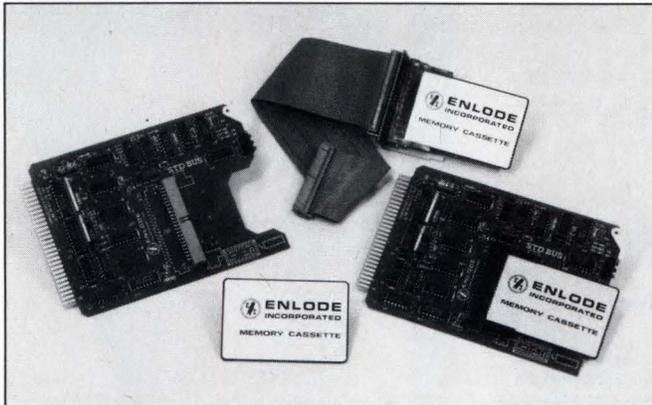
If you'd like a further comparison of the AD96685 and AD96687, call your nearest Analog Devices sales office, or our applications engineers at (919) 668-9511.



Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106; Headquarters: (617) 329-4700; California: (714) 641-9391, (619) 268-4621, (408) 559-2037; Colorado: (719) 590-9952; Maryland: (301) 992-1994; Ohio: (614) 764-8795; Pennsylvania: (215) 643-7790; Texas: (214) 231-5094; Washington: (206) 251-9550; Austria: (222) 885504; Belgium: (3) 237 1672; Denmark: (2) 845800; France: (1) 4687-34-11; Holland: (1620) 81500; Israel: (052) 911415; Italy: (2) 6883831, (2) 6883832, (2) 6883833; Japan: (3) 263-6826; Sweden: (8) 282740; Switzerland: (22) 31 57 60; United Kingdom: (932) 232222; West Germany: (89) 570050

READERS' CHOICE

Of all the new products covered in EDN's May 26, 1988, issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, refer to the indicated pages in our May 26, 1988, issue, or use EDN's Express Request service.



◀ CASSETTE MEMORY

The 234/334C cassette memory system for the STD bus comes in two versions: Model 234-1 comes with a TTL bus card, and Model 334C-1 is the CMOS bus version. (pg 220).

Enlode Inc.
Circle No 603

68HC11 EMULATOR

The 68HC11 emulator aids microcode development. It draws power from the 52-pin PLCC socket on your board via one cable (pg 260).

Xytek Industries Inc.
Circle No 602

CAD PACKAGE

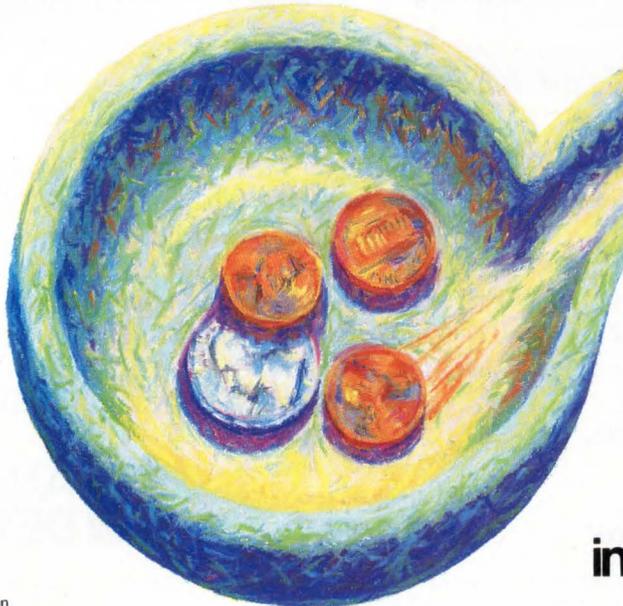
The Resicalc CAD package lets you design through-hole, surface-mount, or leadless-carrier resistor networks on an IBM PC or compatible system (pg 94).

Ericsson Business Area Components.

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Circle No 607

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RISC CHIP SET

The 88000 chip set takes advantage of the silicon-saving RISC architecture to integrate all the major CPU-board functional blocks (pg 103).

Motorola Microprocessor Products Group.
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ACCELEROMETER

The SXL Series accelerometers employ a 0.16×0.16-in. sensor chip and have 200g measurement capability (pg 240).

Sensym Inc.
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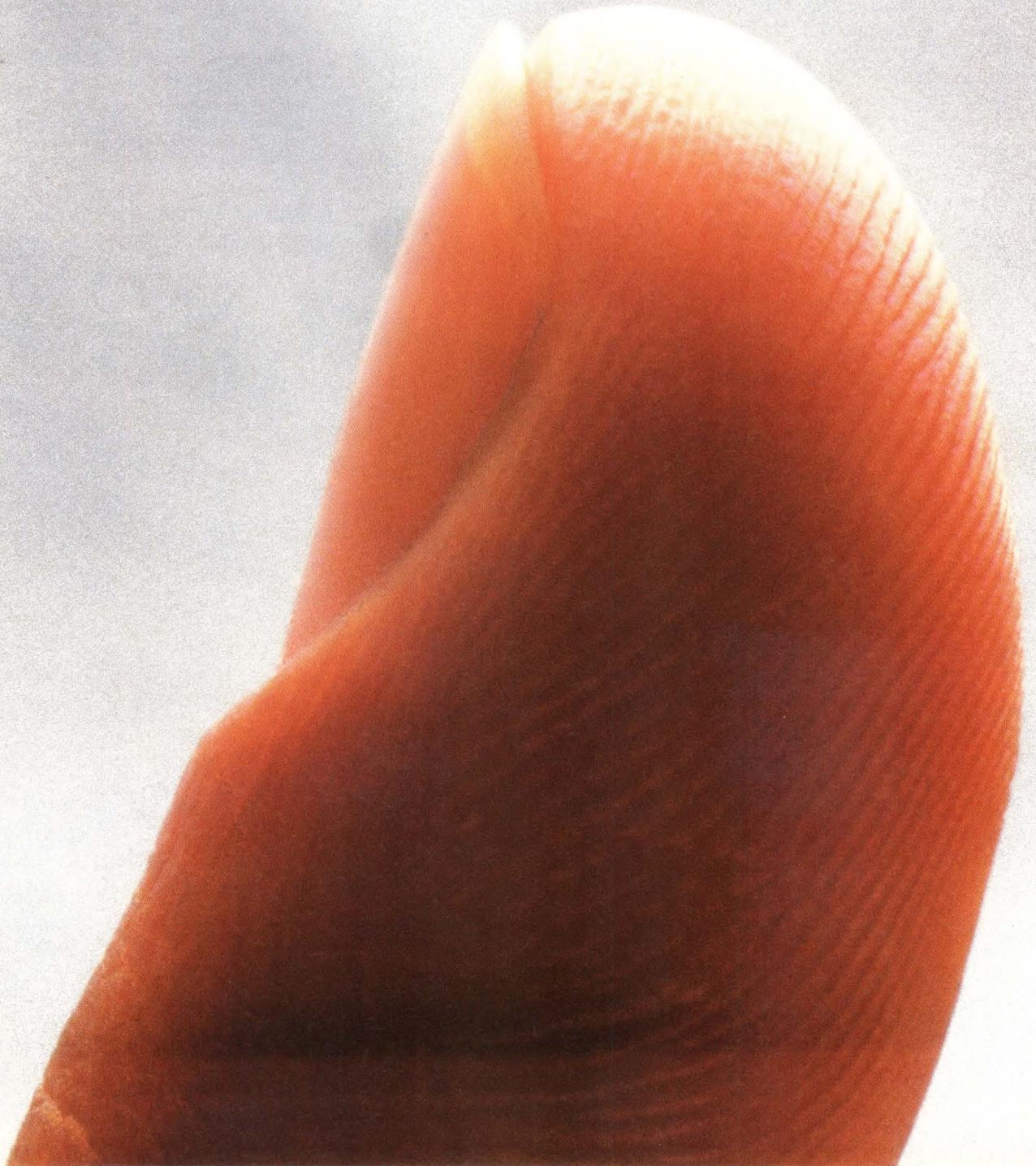
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How to please significant portion



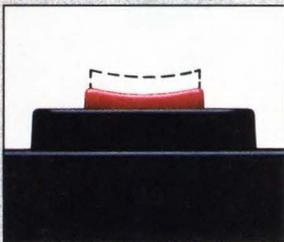
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Pushbutton-operated devices are much more marketable when the buttons respond in satisfying ways to the user's touch.

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Actuator travel of 0.050" is more than twice that of conventional low-profile keypads.

ductive rubber pad, tested to ten million operations, that rewards the finger with a satisfying snap back when a button is actuated.

The result is a control panel that adds to a user's comfort and confidence, for about the same price as those that generate feelings of vagueness and uncertainty.

But that's not the only bright feature of these new controls.

You can also get them in full-face, LED lighted versions that show up unmistakably, even in broad daylight.

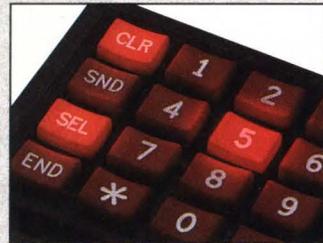
And each button can be made to light independently of its on/off status,

enabling the panel to guide a user through a sequence of operating steps.

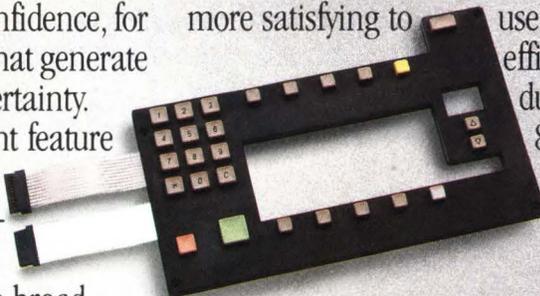
These new panels are available off-the-shelf in several standard arrays, or in custom packages with microprocessors, visual displays, special enclosures, or attachment cable included.

Making controls more responsive is just one of the many ways we can help you build competitive advantages into your products.

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Selective button lighting helps guide a user through a sequence of operating steps.



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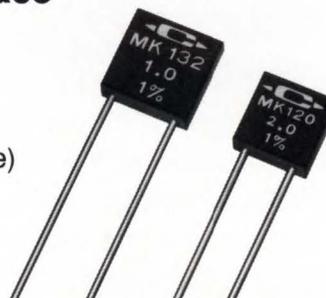


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Radial Lead Design Takes Less Board Space

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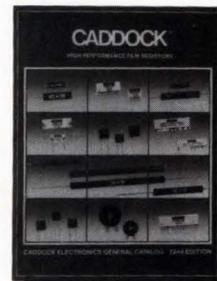
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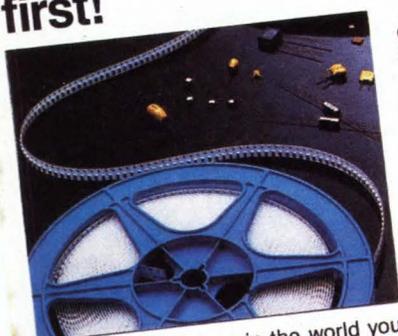
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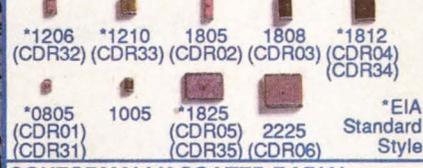
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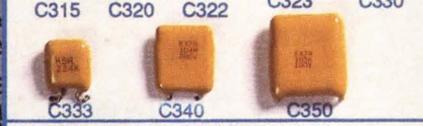
CERAMIC

CHIPS(Surface Mounted Device) 1pF-2.2 μ F



*1206 (CDR32) *1210 (CDR33) 1805 (CDR02) 1808 (CDR03) *1812 (CDR04) (CDR34)
 *0805 (CDR01) (CDR31) 1005 (CDR35) *1825 (CDR05) 2225 (CDR06) *EIA Standard Style

CONFORMALLY COATED RADIAL



Golden Max 1pF-6.8 μ F
 C315 C320 C322 C323 C330
 C333 C340 C350

CONFORMALLY COATED AXIAL

Aximax 10pF-1 μ F



C410 C412 C420 C430 C440
 C052 (CK05) C062 (CK06) C056 (CKR05) C066 (CKR06)

MOLDED RADIAL

1pF-3.3 μ F



C114 (CK11) C124 (CK12) C192 (CK14) C202 (CKR15) C222 (CK16) (CKR16)

FILM

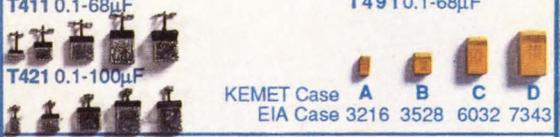
Metallized Polycarbonate



Flat Kap. 0.01-1 μ F
 F110, F120, F130 (4 Case Sizes Available)
 F141, F241 (CRH01-5), F242 (CRH06-0), F245 (CHR01A, D, G, K, N), F246 (CHR01B, E, H, L, P), F247 (CHR01C, F, J, M, R), F248 (CHR10)

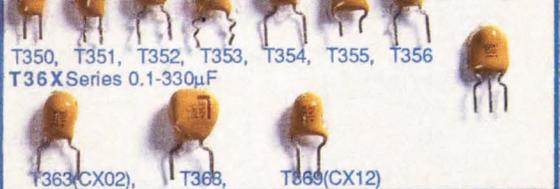
TANTALUM

CHIPS(Surface Mounted Device)



T411 0.1-68 μ F T491 0.1-68 μ F
 T421 0.1-100 μ F
 KEMET Case A B C D
 EIA Case 3216 3528 6032 7343

CONFORMALLY COATED RADIAL



T350 Series Ultradip 0.1-680 μ F T396/T398 Ultradip III 0.1-300 μ F
 T350, T351, T352, T353, T354, T355, T356
 T36X Series 0.1-330 μ F
 T363(CX02), T366, T669(CX12)

MOLDED AXIAL



0.1-330 μ F
 T322/T323 (CX01/CX05)

HERMETICALLY SEALED



0.0047-1200 μ F
 T120, T222 (CSR04) & T220 Series
 T110, T140, T210, T212 (CSR13), T216 (CSS13) T240, T242 (CSR23), T252 (CSR33) T256, T262 (CSR21) Series

MOLDED AXIAL/RADIAL



Flat Kap. .001-1 μ F
 F310 (CFR04R), F311 (CFR04A), F320, F321, F330, & F331
 (8 Case Sizes Available)

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 — Ron*

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LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
TRANSFORMERS								
Toroidal	0	13	56	25	0	6	10.6	10.6
Pot-Core	0	11	55	28	0	6	10.9	12.5
Laminate (power)	0	32	37	26	0	5	9.3	11.7
CONNECTORS								
Military panel	0	0	27	55	9	9	16.0	11.5
Flat/Cable	9	47	35	9	0	0	5.1	5.7
Multi-pin circular	0	28	38	28	6	0	9.6	9.2
PC (2-piece)	7	20	46	27	0	0	8.4	6.7
RF/Coaxial	6	22	39	33	0	0	8.8	7.8
Socket	11	37	33	19	0	0	6.4	6.6
Terminal blocks	8	57	23	12	0	0	4.9	4.0
Edge card	5	26	58	11	0	0	6.9	6.0
D-Subminiature	12	24	48	12	4	0	7.2	6.0
Rack & panel	0	17	66	17	0	0	8.3	9.0
Power	0	22	57	21	0	0	8.3	7.6
PRINTED CIRCUIT BOARDS								
Single sided	5	49	41	5	0	0	5.0	5.8
Double sided	0	38	56	6	0	0	6.2	6.7
Multi-layer	0	8	64	28	0	0	9.7	10.6
Prototype	0	83	10	7	0	0	3.5	3.7
RESISTORS								
Carbon film	30	24	22	24	0	0	6.0	4.3
Carbon composition	24	28	16	32	0	0	6.9	3.5
Metal film	23	25	26	26	0	0	6.7	4.6
Metal oxide	16	32	26	26	0	0	6.8	5.4
Wirewound	9	28	36	27	0	0	7.7	6.3
Potentiometers	0	44	33	23	0	0	7.2	6.1
Networks	8	42	25	25	0	0	6.8	7.0
FUSES								
Switches	44	28	20	8	0	0	3.4	3.2
SWITCHES								
Pushbutton	12	42	31	15	0	0	5.7	5.9
Rotary	0	45	38	17	0	0	6.6	5.8
Rocker	5	42	32	21	0	0	6.7	6.9
Thumbwheel	0	47	29	24	0	0	7.1	8.2
Snap action	5	42	32	21	0	0	6.7	5.9
Momentary	12	41	35	12	0	0	5.5	6.5
Dual-in-line	13	31	37	19	0	0	6.6	7.7
WIRE AND CABLE								
Coaxial	26	59	11	4	0	0	2.7	5.2
Flat ribbon	24	56	16	4	0	0	3.0	4.4
Multiconductor	17	54	25	4	0	0	3.7	5.4
Hookup	33	48	15	4	0	0	2.8	3.3
Wirewrap	30	45	15	10	0	0	3.7	4.8
Power cords	15	52	22	11	0	0	4.5	5.1
POWER SUPPLIES								
Switcher	0	20	60	20	0	0	8.4	8.6
Linear	8	25	50	17	0	0	7.2	8.0
CIRCUIT BREAKERS								
Heat sinks	10	25	45	15	5	0	7.8	8.8
BATTERIES								
Lithium coin cells	6	52	24	12	6	0	6.4	6.5
9V alkaline	20	47	20	13	0	0	4.6	2.9
Real-time clock back-up	8	25	50	17	0	0	7.2	5.7
RELAYS								
General purpose	14	41	28	17	0	0	5.7	5.6
PC board	8	46	21	25	0	0	6.6	5.5

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Last month's average (weeks)	Average (weeks)
DISCRETE SEMICONDUCTORS								
Dry reed	14	21	29	36	0	0	8.5	6.3
Mercury	10	10	30	50	0	0	10.6	11.2
Solid state	5	33	33	29	0	0	7.9	9.2
DISCRETE SEMICONDUCTORS								
Diode	22	29	19	19	11	0	8.0	6.2
Zener	20	33	7	33	7	0	8.3	7.6
Thyristor	10	29	29	32	0	0	8.0	6.6
Small signal transistor	24	23	19	24	10	0	8.4	4.9
MOSFET	10	25	35	30	0	0	8.1	7.9
Power, bipolar	19	25	35	25	6	0	8.0	7.8
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	0	19	43	38	0	0	9.9	10.1
CMOS	10	28	28	31	3	0	8.5	8.0
TTL	14	20	33	33	0	0	8.3	5.6
LS	23	31	23	23	0	0	6.1	6.5
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	8	26	33	33	0	0	8.4	9.1
OP amplifier	22	26	26	26	0	0	6.7	7.6
Voltage regulator	18	32	23	27	0	0	6.8	6.3
MEMORY CIRCUITS								
DRAM 16K	0	7	20	40	0	33	18.3	14.6
DRAM 64K	0	12	22	44	0	22	15.8	14.6
DRAM 256K	0	11	6	39	11	33	20.0	19.5
DRAM 1M-bit	0	13	7	27	20	33	20.5	22.6
SRAM 4K x 4	0	7	27	33	13	20	17.1	15.3
SRAM 8K x 8	0	6	17	32	17	28	19.6	16.6
SRAM 2K x 8	0	6	24	28	24	18	18.3	17.8
ROM/PROM	0	14	29	43	7	7	13.4	13.2
EPROM 64K	0	16	36	26	11	11	13.6	11.4
EPROM 256K	0	19	19	42	10	10	14.3	13.9
EPROM 1M-bit	0	17	17	41	17	8	15.1	15.8
EEPROM 16K	0	15	38	38	0	9	12.2	14.7
EEPROM 64K	0	15	31	46	0	8	12.6	14.1
DISPLAYS								
Panel meters	0	27	53	20	0	0	7.9	7.3
Fluorescent	0	10	45	45	0	0	11.0	10.4
Incandescent	9	28	36	27	0	0	7.7	6.3
LED	26	13	48	13	0	0	6.1	7.1
Liquid crystal	7	7	50	36	0	0	9.9	12.2
MICROPROCESSOR ICs								
8-bit	0	28	28	44	0	0	9.8	8.9
16-bit	0	27	27	46	0	0	10.0	9.2
32-bit	7	13	40	40	0	0	9.8	12.0
FUNCTION PACKAGES								
Amplifier	9	19	45	27	0	0	8.3	8.9
Converter, analog to digital	7	29	29	35	0	0	8.5	9.4
Converter, digital to analog	9	19	36	36	0	0	9.0	9.6
LINE FILTERS								
Capacitors	9	28	27	36	0	0	8.4	7.9
CAPACITORS								
Ceramic monolithic	13	40	27	20	0	0	6.1	7.0
Ceramic disc	18	32	29	21	0	0	6.3	6.1
Film	19	33	26	22	0	0	6.2	6.4
Aluminum electrolytic	10	29	29	29	3	0	8.3	7.7
Tantalum	16	28	34	19	3	0	7.1	8.0
INDUCTORS								
	0	25	56	19	0	0	8.0	8.5

Source: Electronics Purchasing Magazine's survey of buyers.

EDN August 18, 1988

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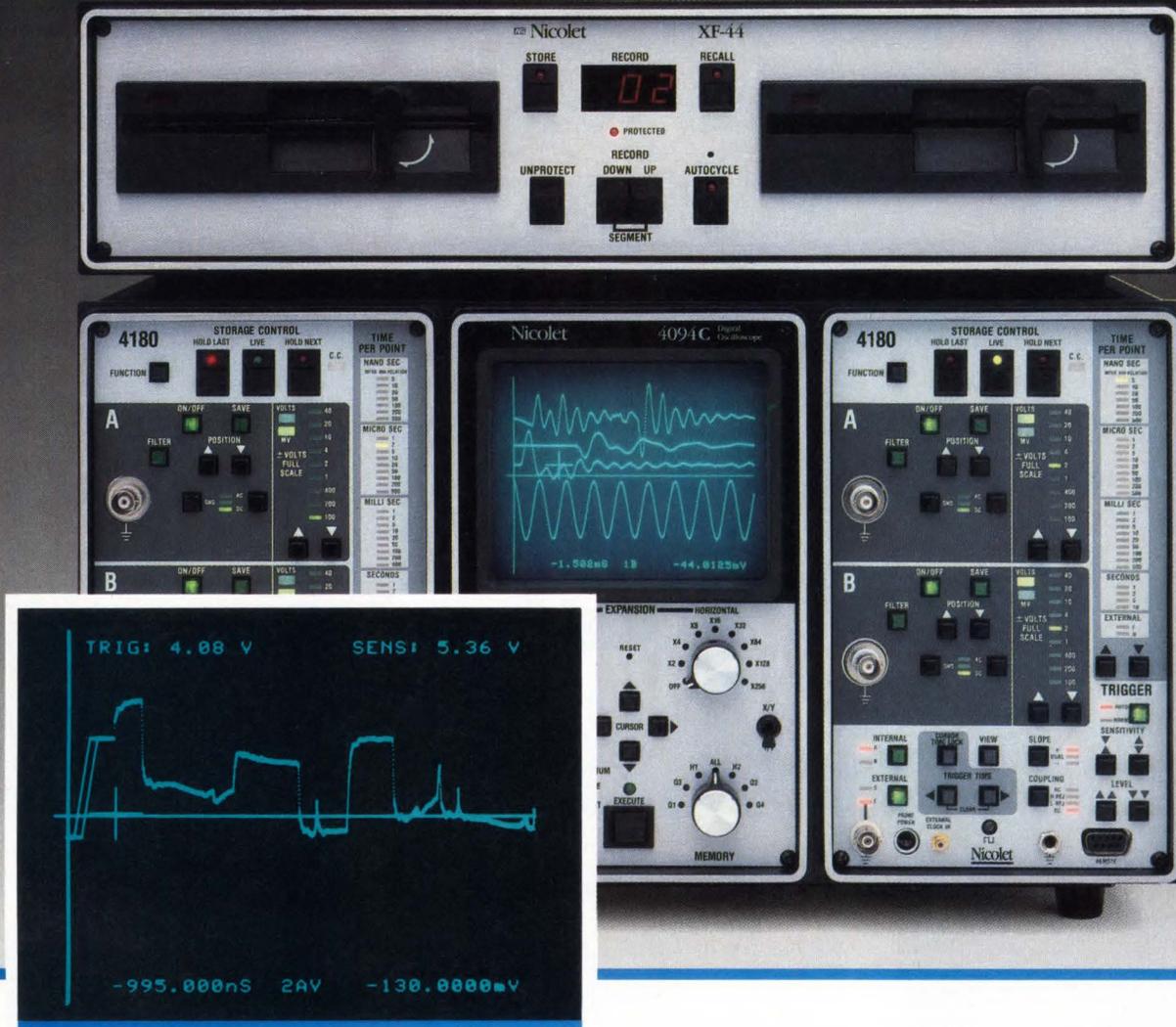
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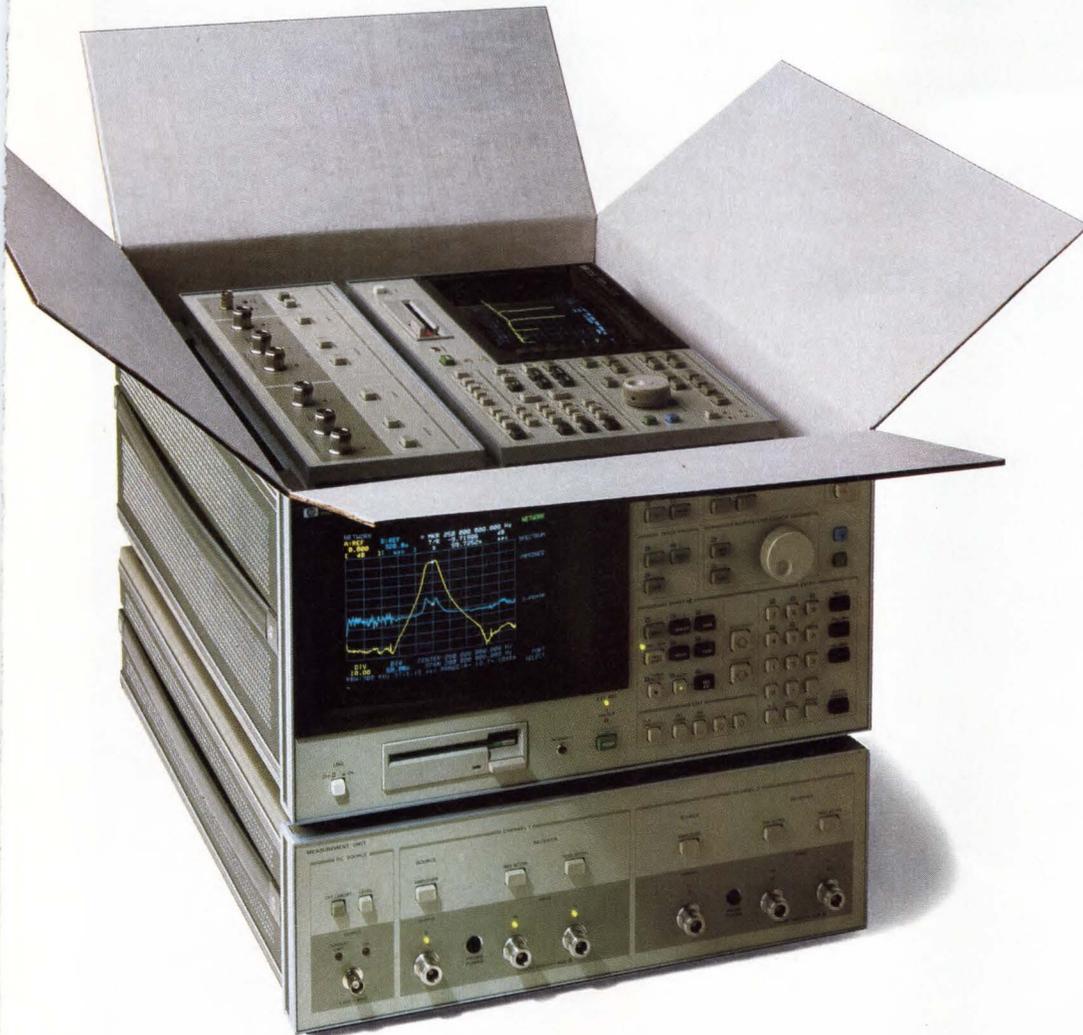
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The technology and manufacturing processes for flat-panel displays are changing fast—particularly for large-area displays with expanded information content. In choosing a model, however, you need to consider other aspects, too, from brightness and contrast to viewing angles. And don't forget the price—it can decide the issue.



Light weight and compact design are the hallmarks of flat-panel displays. Now manufacturers are also improving their manufacturing materials and processes to raise performance levels and lower costs as well. (Photo courtesy Planar Systems)

Flat-panel displays

Dave Pryce, *Associate Editor*

Flat-panel displays are changing the way we view information, not only in wrist watches and calculators but in bigger applications like portable computers and terminals that require complex graphics. Manufacturers have continued to refine some of the smaller and simpler products that have been around for years, but it's within the realm of displays with large areas and expanded information content that you can see significant trends and sometimes dramatic progress. In these areas, manufacturers are working to make flat-panel displays that are suitable for more and more complex applications, while improving performance levels of those displays and lowering their cost.

The LCD (liquid-crystal display) is well known for its nearly universal use in digital watches and pocket calculators. Perhaps less well known is the use of LCDs and VFDs (vacuum-fluorescent displays) in such applications as automotive dashboards. Many of today's cars—to the dismay of the purist—use LCDs and VFDs to replace traditional analog speedometers, tachometers, and gauges for oil pressure, water temperature, and gasoline. VFDs, along with LCDs and PDPs (plasma display panels), are also frequently used as readouts

in gasoline-station pumps and industrial control equipment. And the LCDs, PDPs, and ELDs (electroluminescent displays) that are available in expanded information content versions are very practical for use in portable computers and in applications that require complicated graphics.

The LCD has probably saved the individual consumer hundreds of dollars in battery replacement costs—its predecessor, the LED (light-emitting diode), burned out batteries at a furious rate. LCDs have more modest power requirements; a digital watch with an LCD typically operates for two years or more on its original battery. Their low power requirements make them particularly suitable for portable computers.

Active-matrix enhances large-area LCDs

One recent development that has contributed to the growing popularity of LCDs is the active matrix. Alphasil Inc, for example, makes custom and semi-custom active-matrix LCDs that contain amorphous-silicon, thin-film transistors (TFTs) that switch individual pixels (dots) on and off; external row- and column-drivers are still required. All of Alphasil's active-matrix flat-panel displays (AMFPDs) offer at least a 10:1 contrast ratio.

AMFPDs are available as reflective, transmissive, or

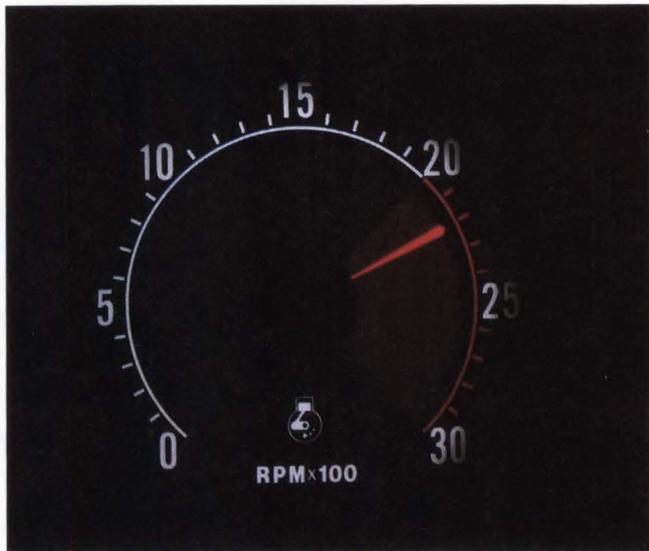
LCDs have probably saved the individual consumer hundreds of dollars in replacement battery costs.

transflective displays. Like most other LCDs, the reflective AMFPDs contain no backlighting. Because reflective units depend on ambient light alone to illuminate the screen, they perform best when that light is high. The transmissive displays are backlit continuously when in use and are thus suited for indoor applications where the ambient light is low. Transflective displays can operate either way; they're most appropriate where displays must operate in a wide range of indoor and outdoor lighting conditions. For backlighting, both the transmissive and transflective screens use a low-power, high-efficiency neon fluorescent tube. Alphasil also offers thin-film electroluminescent (EL) backlighting for situations where the lower surface brightness that the backlighting creates under ambient light is not a problem.

Alphasil's products include AMFPDs with matrices of 640×200 (CGA), 640×350 (EGA), 640×400, 640×480 (VGA), and 640×640 pixels. The 640×350-pixel unit has an active display area of 3.5×5 in. and contains 224,000 pixels with a built-in 2:1 redundancy. According to Alphasil, all of the displays feature a viewing angle of 160° for any pixel, a minimum contrast ratio of 10:1, and power consumption of less than 3W with backlighting. All models have a refresh rate of 60 Hz and include digital and RGB interfaces. These large-area displays, which are available in sizes through 5×5 in., are fairly expensive, and find primary use in military and avionics applications. Prices depend on the particular display; they range from about \$1000 to \$2000 in small quantities.

Panasonic Industrial makes dot-matrix LCD modules that fit the large-area category without using the active-matrix technology. The EDM-DG648A01D (8-in. diagonal) and the EDM-DG64AA41D (9.5-in. diagonal) are both birefringent displays (see **box**, "A glossary of display terms," pg 144). The 8-in. display has a 640×200-pixel format with an effective viewing area of 6.46×4.886 in. The 9.5-in. display has a 640×400-pixel format with a viewing area of approximately 8.078×5.04 in. These LCD modules can display a sufficient amount of alphanumeric and graphics to replace CRTs in most configurations. The dot size is 0.00827×0.022 in. (0.21×0.56 mm) for the 8-in. display, and 0.011×0.011 in. (0.28×0.28 mm) for the 9.5-in. display. Both modules operate from 5 and 24V dc supplies. For applications in low-light work areas, an optional EL backlight is available. The displays cost from \$200 to \$250 each.

Industrial users are also finding LCDs functional.



This automotive tachometer display is typical of the applications for Taliq Corporation's liquid-crystal film. By combining light-controlling liquid-crystal thin films with graphic overlays and color reflectors, the company can produce complete front-panel assemblies.

Seiko Instruments, for example, makes LCD modules that are used in various industrial displays. Its alphanumeric models range in capacity from 1×16 to 4×40 characters. Featuring blue characters on a white background, these modules have high contrast and a wide viewing angle.

Sharp Electronics Corp makes several large-area LCDs. Their dot-matrix monochrome types include formats of 640×400, 640×480, and 720×400 dots. The viewing areas of these displays are 8.589×5.476 in., 9.338×7.09 in., and 10.24×5.79 in, respectively. All are double-supertwist types that offer high contrast. The 640×480-dot display is particularly well suited for use with the IBM VGA graphics standard. Sharp recently introduced a small-area (3-in. diagonal) color display with a 384×240-dot format that uses active-matrix TFT technology.

LC film can be colorful

Although most manufacturers are still developing color technology for large-area displays with expanded information content, Taliq Corporation is already providing some solutions to the need for color in limited information content applications. Based on a technology it calls nematic curvilinear-aligned phase, Taliq makes plastic liquid-crystal film that's used in its custom Varilite color displays. By combining layers of light-controlling liquid-crystal thin film with graphic

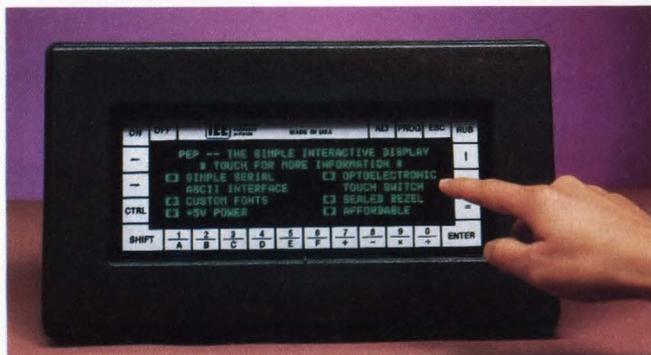
overlays, color reflectors, and membrane switches, Taliq manufactures fully integrated front-panel assemblies that are useful in automotive, industrial, medical, office-automation, and home-appliance applications.

Taliq sells sheets of liquid-crystal film as well as complete custom displays. A sheet of 12 numeric (7-segment), or alphanumeric (16-segment) characters costs \$19.50 for 1-in.-high characters and \$27.30 for 2-in.-high characters. You can order the film in red, green, blue, yellow, or orange. The film has die-cut adhesive on both sides. A typical prototype order for a custom display costs \$3000 to \$5000 and includes all engineering and art-work charges, and 5 to 10 samples. Pricing for large quantities depends heavily on the actual display; a typical automotive tachometer display, for example, might cost \$6 at the 25,000-piece level.

The bright blue-green color of a VF display is eye pleasing and it's undoubtedly a major factor in VFDs' popularity. Although usually limited to small-area displays with limited information content, VFDs are widely used in automobiles, medical equipment, industrial controllers, and point-of-sale terminals. At least one company offers a VF display that combines expanded information content with a display area large enough to make it suitable for both text and graphics.

VF display features touchscreen

Industrial Electronic Engineers (IEE) makes a variety of VFD modules (they also make EL and plasma displays). The IEE model 4283-01, for example, is one of a family of display modules that uses VF technology to good advantage. The module integrates a 6-line by 40-character VF display with an infrared touchscreen. Each of the display's 240 characters is formed by a 5×7-dot matrix that is 0.197-in. high. The module has

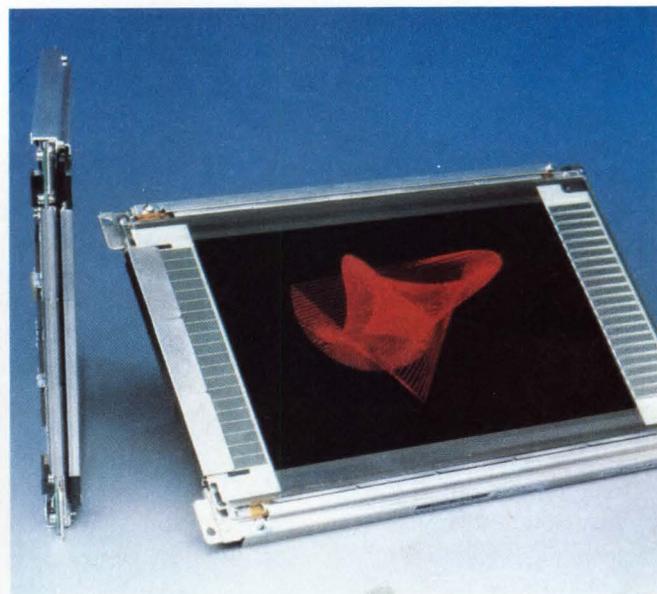


This interactive touch-entry display module from IEE integrates a 6-line by 40-character VF display with an infrared touchscreen.

three software-controlled brightness levels ranging as high as 185 fL. In addition, a wide spectrum of colored filters is available for particular applications. These display characteristics, combined with the touchscreen, make the 4283-01 suitable for a variety of menu-driven applications.

Unlike resistive-membrane and capacitive touchscreens, the infrared type used in the 4283-01 uses no overlays that could obscure the display in any way. The module provides for 969 active switch locations and is immune from false triggering by ambient light—even direct sunlight. You can use this display module to store and retrieve as many as 127 user-programmable messages by means of its 8k bytes of CMOS RAM. A battery-backup circuit retains the messages in the event of power failure. The module operates from a single 5V supply; an onboard μ P controls all display and touchscreen operations, a diagnostic test program, and the serial data interface with the host computer. Prices for the 4283-01 start at \$800 (100).

Futaba Corporation is also pushing the application boundaries for VF displays into previously uncharted areas. The Futaba GP1019A03A uses a high-resolution display technology that allows a pixel pitch of 0.0074×0.01 in. (0.1875×0.225 mm). This VFD module has a pixel count of 640×400 in a display area of 4.72×3.54 in. Its luminous display is a distinctive green



Featuring a distinctive orange color, this plasma panel from Fujitsu provides a high-resolution 640×400-dot display and a 10-in. (diagonal) viewing area.

The VF display's bright, green-colored display is easily visible.

color, whose wavelength is about 500 nm (you can modify this color by the use of filters). The luminance of the display is moderately high—40 fL (140 cd/m²). It operates from supply voltages of 5 and 135V dc. You connect the display module to the host system via the horizontal sync, vertical sync, and data (RGB) signals. By combining any two of the R, G and B inputs, you can produce a halftone display. Using a liquid-crystal color shutter (Sony-Tektronix 7-in. LCCS) provides a display in three colors, which tend to be combinations of orange and green. The GP1019A03A VFD module costs \$795 in lots of 100 pieces.

Although large-area plasma displays bear little physical resemblance to the Burrough's Nixie tube, the basic operating principle is the same. The Nixie tube, popular in the early sixties, contained a series of electrodes

in the shape of numerals (0 to 9) and a neon gas mixture. Later in that decade, Beckman and Sperry introduced segmented displays that included multiple digits and alphanumeric capabilities in a single glass envelope. The same visible glow (typically orange-red) emanates from today's plasma displays (PDPs). In all cases, the glow results from the ionization of a neon gas. The gas discharge, or ionization, occurs when electrodes within the gas are subjected to a minimum threshold voltage.

PDPs come in a wide variety of shapes and sizes, ranging from small alphanumeric and bar-graph displays to large-area displays suitable for text and graphics in computer and video terminal applications. Companies such as Cherry Electrical Products, Dale Electronics, Dixy Corporation (Fuji Electronics),

A guide to flat-panel displays

Flat-panel displays have a long way to go before they supplant cathode-ray tubes. CRTs, which are one of the last strongholds of vacuum-tube technology, still account for nearly 70% of the estimated \$9 billion electronic display market. They are inexpensive when compared with other technologies, and they have the best resolution and color capability. What's more, they're widely available. The CRT screen is also equal, or superior, to other displays in terms of brightness, contrast, and general visibility. Their main disadvantages are bulkiness, weight, and high power requirements—factors that are of particular importance for battery-operated and portable equipment. What follows is a list briefly explaining the different flat-panel technologies that may someday replace CRTs in most applications.

ELD (electroluminescent display)—ELDs depend on the

properties of substances such as Zn doped with Mn to luminesce when subjected to a high voltage. The higher the voltage, the brighter the luminance. This effect also can generate gray-scale images. A dot-matrix ELD panel consists of column electrodes behind a layer of luminescent material, with transparent row electrodes in front of the material. ELDs offer high resolution and exhibit a yellow-on-black display of high contrast that is pleasing to the eye. This type of flat panel is useful for applications that require both large-area displays and expanded information content, such as portable computers.

There are two basic types of ELDs: ac thin-film (ACTFEL) and dc thick-film (DCTFEL). Although both types can produce the same levels of light intensity, contrast, and resolution, manufacturers of each type claim certain cost or performance advantages. In the past, both

types have shown signs of wearing out earlier than CRT counterparts, whose half-life is typically 10,000 hours. New materials and processing techniques, and the use of electronic circuitry, however, have largely eliminated these premature effects of extended use. ACTFEL displays, for example, used to show latent images on the screen as they got older, but symmetric driving circuits have overcome this problem.

LCD (liquid-crystal display)—In a twisted-nematic LCD display (TNLCD), a liquid-crystal mixture is sandwiched between two glass plates that are coated with a polarizer and lined with transparent electrodes. The application of an electric field shifts the nematic molecules so that they line up with the field, and so changes the molecules' optical characteristics. The refractive index of these molecules depends on their orientation relative to the direction of the incident

Fujitsu Components, Interstate Electronics Corp (IEC), Industrial Electronic Engineers (IEE), and NEC Electronics, all make plasma displays. AC-memory, ac-refresh, and dc-refresh are the three principal plasma-display technologies in use at this time (see box, "A guide to flat-panel displays").

Dale Electronics, for example, makes bar-graph plasma displays that use multiple segments to create a 10-in.-high single-bar model (PBG-C7005), and a 7.78-in.-high dual-bar model (PBG-C7008) that sell for \$55 and \$48, respectively (100). They also make a full-field, dot-matrix graphic display (APD-192G088-1) that has 192 columns and 88 rows. This display includes all drive electronics and a μ P-based controller. Designed for use in computer terminals and other systems requiring a self-contained readout, the display is programmable to

Text continued on pg 146



An IBM PC portable demonstrates the use of Alphasil's active-matrix LCD. The portable system provides a way for OEMs to demonstrate their own applications before investing in a custom or semicustom display.

light. In a standard LCD panel, the application of an appropriate (low) voltage aligns the crystals so that they either transmit or block the polarized light. A dichroic dye included in the crystal material colors the light that passes through it.

LCDs are quite inexpensive, consume very little power, and are thin, durable, and lightweight. Their major disadvantages are poor contrast, low brightness, and a reduction in performance as display size increases. The newer active-matrix types overcome some of these disadvantages but, because each pixel requires a separate drive transistor, the display and the drive circuitry are more complicated—and expensive—than conventional types. Backlighting of LCDs is becoming common for applications where the ambient light level is low.

PDP (plasma display panel)—All plasma displays contain a gas, usually neon, that glows

when subjected to a high voltage. In a dot-matrix display, this voltage is applied between two sets of electrodes; one set runs vertically, the other runs horizontally; the gas is in between the two. Plasma displays exhibit a characteristic orange or red-orange color.

There are three basic plasma technologies: dc-refresh, ac-refresh, and ac-memory. The basic difference between the refresh types and ac-memory plasma displays is that the memory display includes dielectric layers: AC-memory displays have dielectric layers that separate the gas from the activating electrodes. The dielectric in an ac-memory display restricts the electrodes to capacitive coupling with the gas, a condition that allows the gas to stay lit until another signal turns it off. This action serves to create a kind of pixel memory, which eliminates the need for screen refresh in ac-memory plasma displays. Both

the ac- and dc-refresh types require refreshing at least once every 1/60 of a second to prevent flickering.

VFD (vacuum-fluorescent display)—VF displays are well suited for applications that need only limited information content, such as dashboard displays in cars. For displays of less than about 200 characters, this type offers the best cost/character ratio. VFDs have a pleasant blue-green color that is usually brighter than either PDPs or ELDs. VFDs use essentially the same operating principle as a triode vacuum tube: The phosphor-coated anode segments radiate light when struck by electrons emitted by the filament cathode, and a metal-mesh grid controls the flow of electrons from the cathode to the anode. Phosphor alignment problems for high-end applications tend to reduce production yields.

A glossary of display terms

Acuity—The uniformity of light emission across a pixel and its degree of edge definition. Assuming the contrast ratio is high enough for easy distinction of off- and on-pixels, the uniformity of emission of the on-pixels, together with the size and shape of the pixels themselves, dictates the sharpness of the images.

Aspect ratio—The ratio of the display's width to its height. The aspect ratio of the typical TV screen or IBM monitor is 4:3. Flat-panel displays come in a variety of aspect ratios, depending on the particular application.

Birefringence—Double refraction. The splitting of a light beam into two light waves when the beam enters a crystal. The resultant two light waves vibrate in directions that are perpendicular to each other.

Brightness—The light-intensity, or luminosity, of the display. Brightness is measured in foot lamberts (fL), or in candelas per meter squared (cd/m^2). Note: $1 \text{ cd}/\text{m}^2 = 0.292 \text{ fL}$.

CGA—Color-graphics adapter. An electronic display standard that specifies a resolution of 640×200 pixels in the 2-color mode, and 320×200 pixels in the 4-color mode (from a palette of 16 colors). The horizontal scanning frequency is specified as 15.75 kHz.

Contrast Ratio—The ratio of on-pixel brightness compared to the off-pixel brightness. It represents the difference in light intensity between the foreground

and background of a display. Black and white provide the ideal contrast. Depending on the type of display, contrast ratios for flat-panel displays vary from a value of less than 3:1 for some LCD types, to values of 20:1 or more for some ELD types. The perceived contrast depends on the ambient light, but a contrast of about 7:1 is generally considered as an acceptable ratio. Above a ratio of about 15:1, the human eye perceives little difference in contrast.

Controller—A pc board that goes behind the display (or in the computer bus). The controller lets the computer communicate with the display. For a CRT raster-scan display, the controller provides the signals needed for horizontal sync, vertical sync, and serial data. Flat-panel displays usually require an additional signal—the dot-clock signal—to control the transfer speed of the pixel information.

CRT—Cathode-ray tube—An electron tube used in TV receivers, oscilloscopes, radar equipment, and computer equipment to display data. Usually rectangular with a 4:3 aspect ratio, CRTs' diagonal measurement ranges generally from about 5 to 28 in. The diagonal of CRT monitors for computers or video terminals are typically between 12 and 14 in.

Display size—The illuminated area of the display that is available for viewing data. Manufacturers of CRTs usually measure them according to their *diagonal*

sizes. For flat-panel displays, manufacturers usually specify the height and width.

Dithering—A computer-graphics technique used to provide shading by turning points on a pixel on and off. In monochrome plasma displays, for example, each pixel can consist of a cluster of four points (sub-pixels), each of which can be on or off. By turning these sub-pixels on in various combinations, the plasma display can show four levels of brightness, or gray-scale shading.

Dot—See **Pixel**.

Dot-clock signal—The signal that controls the pixel rate for the display system. Digital technologies, such as flat-panel displays, require this signal to tell the host system how fast to read the individual pixel information from the system to the panel. This signal is not required for CRT analog displays.

Duty cycle—Response time. The amount of time it takes for an electronic display to refresh every pixel on the screen. The maximum acceptable time is about 16.6 msec, which corresponds to a minimum refresh rate of 60 Hz. At refresh rates slower than about 60 Hz, the human eye begins to detect a flicker in the display.

EGA—Enhanced-graphics adapter. An electronic display standard that specifies a resolution of 640×350 pixels with 16-color capability (from a palette of 64 colors). Included in this standard are 80- and 40-column

text modes, and CGA emulation.

ELD—Electroluminescent display.

Fill factor—The percentage of the total area of the display that is illuminated at any given time, compared with the surrounding nonilluminated area. Displays with a low fill factor (20%) tend to look like a collection of dots. Displays with fill factors of 50% or more exhibit greater apparent brightness and are generally more readable and aesthetically pleasing.

Flat-panel display—An electronic display with a package thickness that is a fraction of the display's height or length. Flat-panel displays include ELD, LCD, LED, PDP, and VFD types (see **box**, "A guide to flat-panel displays," pg 142). Package thickness, which is typically 0.75 to 1.5 in., varies approximately from 0.5 in. to 2.5 in. The pc board containing the electronics sometimes accounts for a significant portion of the total thickness.

LCD—Liquid-crystal display.

LED—Light-emitting diode. A display that uses diodes made of gallium arsenide or gallium arsenide phosphide to emit light when current is supplied.

Nematic—Threadlike—the typical shape of a liquid-crystal molecule.

PDP—Plasma display panel.

Pixel—A picture element. The smallest unit of a video display. In CRT applications, the pixel's color and intensity is coded into an electrical signal for transmis-

sion from the system to the display. For flat-panel displays, "pixels" and "dots" are interchangeable.

Plasma—An ionized gas containing an approximately equal number of positive and negative charges. The gas emits light when subjected to a sufficiently high voltage.

Resolution—A somewhat nebulous term that manufacturers of flat-panel displays define in different ways. A number of factors determine the real or visually apparent resolution. These factors include the pixel (dot) size and pitch, the number of lines per inch, and the total number of pixels. Although the type of display (ELD, LCD, PDP) can have a significant effect on the apparent resolution because of differences in contrast and brightness, the best quantitative measurement is probably the total pixel count in a given area.

Sparkling—A computer-graphics technique that turns off a pixel every other time the screen is refreshed. Unlike CRTs, which typically use high-persistence phosphors, flat-panel displays turn off when the power to a pixel is removed. Sparkling can provide a 2-value gray scale that is satisfactory for a monochrome display or the 2-color 640×200-pixel CGA mode. For the 4-color 320×200-pixel CGA mode, flat-panel displays sometimes use dithering to provide a 4-value gray scale.

Super-twist LCD—A liquid-

crystal display that rotates the plane of polarization in the range of 180 to 270° in contrast with a conventional twisted-nematic LCD, which imposes only a 90° twist on the plane of polarized light passing through the display. In addition, an alignment layer in the display provides a pre-tilt of from 10 to 30°. The pre-tilt and increased twist give super-twist LCDs contrast ratios of about 10:1 and viewing angles as high as 60°.

Twisted-nematic LCD—Also, TN-LCD. A display in which the liquid-crystal material imposes a 90° rotation (twist) on the plane of polarized light passing through the display. Conventional TN-LCDs have contrast ratios of less than 3:1 when viewed head on, and exhibit viewing angles of less than 40°.

VGA—Video-graphics array. An electronic display standard that specifies a resolution of 640×480 pixels with 16-color capability, and 320×200-pixel resolution with 256-color capability (from a palette of 256k colors) The array's functions are available on an add-in board as an adapter.

Viewing angle—The range of angles at which you can read a display, measured in angular degrees of distance from the perpendicular. A viewing angle of 120°, for example, lets you read the display at any angle from 0 to 60° from a plane that is perpendicular to the surface of the display. A conical viewing angle lets you read from above, below, or either side of the display.

The ubiquitous orange-colored plasma display is used in a wide range of applications from gas-station pumps to personal computers.

operate in a serial or parallel mode, and contains all the necessary refresh memory, character generation, and control logic. A 4k×8-bit EPROM generates 256 characters consisting of 128 ASCII characters and 128 block graphics characters. The viewing area of the \$699 (100) display is 7.66-in. wide by 3.5-in. high.

Plasma display uses PWM

Dixy Corporation makes a plasma graphics display (D0640AX) that has a light intensity of 35 fL, which is about 20% brighter than its earlier models. The viewing area of the display is 10.086×6.30 in., the viewing angle is 115°, and the resolution is 640×400 pixels. Using pulse-width modulation, the D0640AX provides 16 gray-scale levels. The scan frequencies for this orange neon display are 21.0526 MHz (dot clock), 24.8262 kHz (horizontal sync), and 56.4334 Hz (vertical sync). You can adjust the display for dot-clock phase, horizontal location, vertical location, brightness, and signal polarity. Samples cost \$1950 each.

Although most suppliers of plasma displays that use ac-memory technology sell exclusively to the military, Fujitsu Components also sells its products commercially. According to Fujitsu, ac-memory displays offer three major advantages compared to other plasma-display technologies: Continuous pixel illumination provides a high resolution. A steady brightness eliminates the flickering that screen refreshing can sometimes cause. And the displays have a higher reliability rate (the company specifies an MTBF rate of 50,000 hours).

Fujitsu's FPF-8050-HFUG module features a

640×400-dot viewing area of 8.3×5.2 in. (10-in. diagonal). The display's 0.008-in. (0.2-mm) pixels are arranged in a 0.013×0.013-in. (0.33×0.33 mm) dot pitch. The assembled display, including drive circuitry mounted to the back of the panel, is just over 1-in. thick. The use of 64-bit LSI drivers reduces power consumption to 35W at 100% illumination. This orange-on-black display has a character brightness of 44 fL, a contrast ratio of 20:1, and a viewing angle of 120°. Designed for use in such applications as medical instrumentation and transportable computers, the FPF-8050-HFUG costs \$945 (the cost decreases to between \$400 to \$500 if you buy 5000 units in a year).

Although electroluminescent displays are not yet a major factor in the total market for flat-panel displays, electroluminescent displays (ELDs) are gaining popularity. For one thing, the characteristically bright, high-contrast, yellow-on-black display is probably more pleasing to the eye than any other type of flat-panel display. What's more, as manufacturers of large-area ELDs succeed in reducing manufacturers costs and power consumption, you can expect to see more of these attractive displays in such applications as computer terminals and transportable computers.

The Seal-Touch Terminal from Digital Electronics Corp is a \$3950 ELD that's suitable for the shop floor. Its 9-in. (diagonal) panel features an infrared touch-screen in a completely sealed cast aluminum case. The package is lightweight and compact—it measures 10.5×11.5×3-in.—so you can mount it on a bench, a wall, or other equipment. The Seal-Touch unit emulates VT-52, VT-100, and VT-220 terminals. It has an 80×25-character format, line graphics, downloadable fonts, pop-up touch menus, and onscreen touch keypads. An auxiliary port lets you use the unit with an attachable keyboard. The terminal supports RS-232C, RS-422, or RS-485 interfaces.

ELDs overcome their drawbacks

Despite the fact that EL displays are aesthetically appealing, they have not yet been widely accepted because, relatively speaking, they have cost a lot and they haven't lasted very long. But these barriers to their success are disappearing as manufacturing implements new processing techniques and materials as well as new driving schemes.

Stand-alone ELDs are available from several companies. Finlux Inc (Lohja Corp), Planar Systems, and Sharp Electronics make ac thin-film (ACTFEL) displays; Cherry Electrical Products makes dc thick-film



Dot-matrix plasma displays are useful for charting graphic data. This 192-column by 88-row panel from Dale Electronics is used in computer terminals and other systems that require self-contained readouts.

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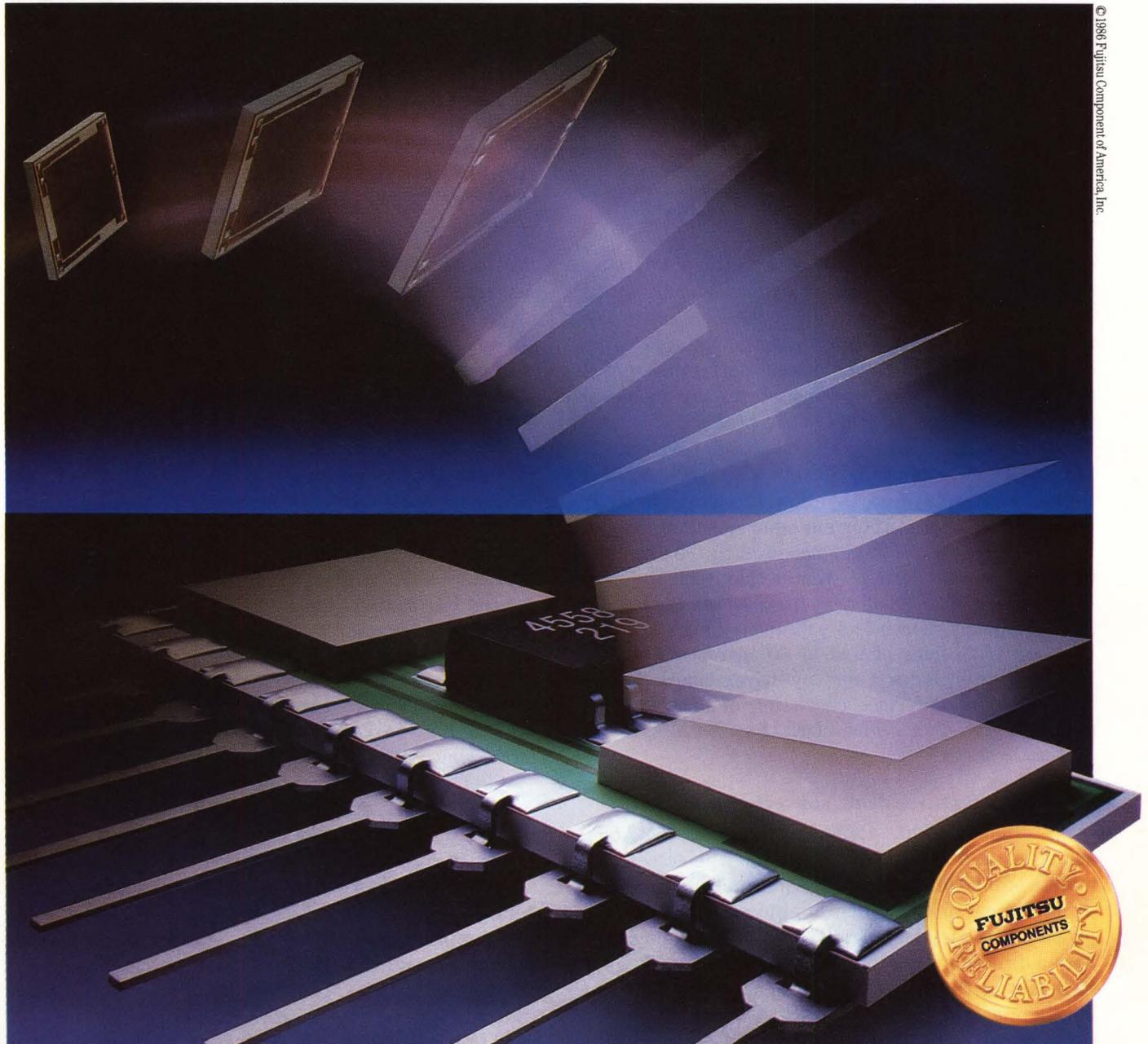
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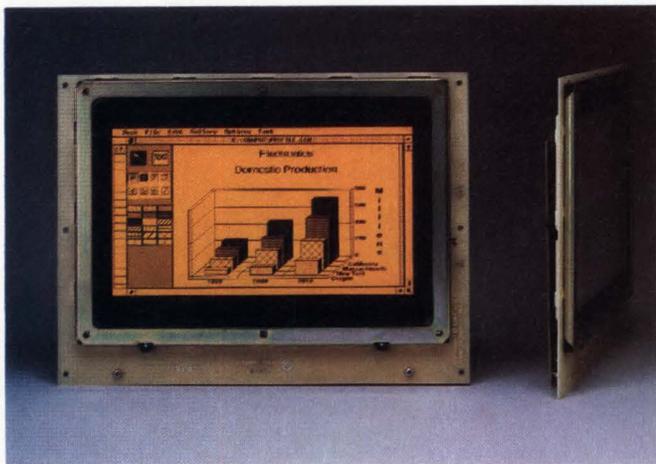
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This EGA-compatible EL display, the EL8358HR, is suitable for MS-DOS-based text and graphics applications. The Planar Systems display has a resolution of 640×400 pixels and a viewing area of 5×8 in. The high-contrast module has a 30-fL pixel brightness.

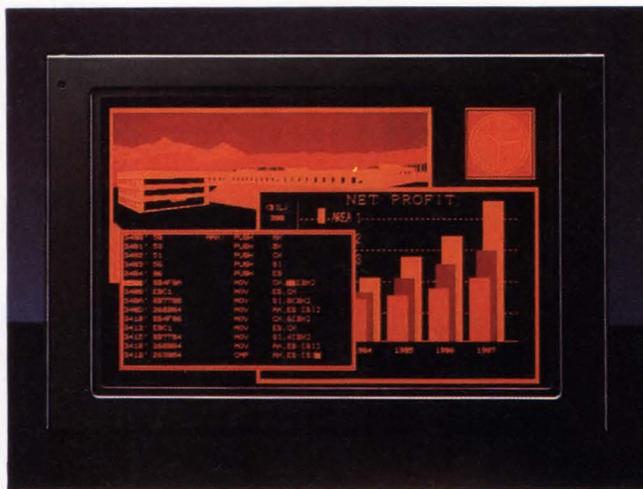
(DCTFEL) modules. Finlux Inc, for example, now uses a thin-film deposition process, which it calls atomic-layer epitaxy. The process gives the ZnS active layer more uniformity. According to the company, this process not only enhances the overall performance of the display, but also improves manufacturing yields and lengthens the operating life of the product.

Finlux makes ELDs with pixel counts from 320×256 to 640×400 at prices from \$590 to \$730 (100). All of the company's displays have yellow foregrounds with a 520-nm wavelength. Their emission spectrum is 60-nm wide. A typical pixel luminance is 26 fL (90 cd/m²); the displays' contrast ratio is greater than 10:1.

Finlux's MD640.400 display has a screen resolution of 640×400 pixels, which lets you display high-resolution graphics of 25 lines of text at 80 characters per line. This display includes a display-driver board that features a digital interface consisting of four TTL-level signals: video data, video clock, horizontal sync, and vertical sync.

EL display features dc/dc converter

The MD640.400 has a viewing area of 4.806×7.68 in. and scans at a refresh rate of 60 Hz. The screen has a matrix of 0.009-in. (0.22-mm) square pixels on a 0.012-in. (0.3-mm) pitch, which is equivalent to about 83 pixels/in. Its viewing angle is 140°. The display comes with a dc/dc converter that you can either use remotely or mount at the rear of the assembly. The converter, which operates on dc inputs of 5V and 12 to 15V, consumes about 16W of power. Finlux is actively work-



Featuring a light intensity of 35 fL and a resolution of 640×400 pixels, this Dixy plasma display panel has a viewing area of 256×160 mm.

ing on the development of large-area EL multicolor displays, but production of these types is several years away. Gray-scale displays will be available in several sizes next year.

Planar Systems, a major supplier of ACTFEL displays, has several models of various sizes and pixel counts in its product line. Most notable is its EL8358HR, a display with a high-resolution (640×400-pixel) viewing area of about 5×8 in. It's EGA compatible and suitable for use with MS-DOS-based text and graphics. The EL8358HR is priced at \$675 (100), including the power supply.

Planar has recently upgraded all of its ELDs, including the EL8358HR. Pixel brightness for that model is now 30 fL (compared to the previous 20 fL), and maximum peak power consumption is down from 25W to between 14 and 16W (the typical average is 10W). Like Finlux, Planar uses square pixels that are 0.0087 in. (0.22 mm) on each side and have a 0.012-in. (0.3 mm) pitch, which gives the display a density of 83 pixels/in.

When you use the circular-polarizing filter that comes standard with the EL8358HR, you get a contrast ratio of 60:1. The filter doesn't enhance the contrast; rather it reduces any glare or reflection that might affect your view of the panel. As is customary, Planar defines contrast as the ratio of light intensity between the on-pixel and the off-pixel (see box, "A glossary of display terms"). The contrast ratio for the EL8358HR 30 to 0.2 fL, or 150:1 (the filter reduces this ratio to 60:1). One might argue that a contrast ratio of 60:1 is superfluous, but Planar points out that in

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EL displays are gaining in popularity; their high-contrast, yellow-on-black color is aesthetically pleasing.

situations where the display is viewed briefly from a distance, this high ratio is advantageous. The company does agree, however, that for constant close-up viewing of equipment like computer screens, you might want to lower this ratio by reducing the brightness of the display.

Planar has developed an RGB color display for use in military applications and is working on reducing the costs of the materials and manufacturing process so that the display will be commercially viable. It expects to be able to produce economical commercial displays in about two years.

It's important to get the right RGB balance

One technical problem with RGB displays involves obtaining both chromaticity and intensity values that strike the right balance of red, green, and blue. This balance is important in order to accommodate the varying sensitivity of the human eye to different wavelengths of color. The display's luminescent material is the key to the light intensity of these colors, and chemistry plays a dominant role in achieving the proper balance. Monochrome EL displays typically use Mn-

doped ZnS to produce their characteristic yellow color, but the color blue, for example, requires Ce-doped SrS. To obtain the red and green colors for an RGB display, manufacturers use the same ZnS used for a monochrome display, but the doping agents are more exotic chemicals than Mn. Another problem in the making of RGB displays is that you need more pixels for any given area. For example, a 640×480-pixel monochrome display translates into a 1920×480-pixel RGB display.

Cherry Electrical Products has been a leading maker of gas-plasma displays for the past 15 years. Now it's starting to be prominent in ELD arena. Cherry uses a dc thick-film approach that it claims offers advantages over the more common ac thin-film types such as simple and rugged construction, the absence of potential thin-film dielectric breakdown, and higher manufacturing yields. Moreover, the Cherry EL displays are very thin; including the electronics board, they measure less than 0.6-in. thick.

Cherry offers two 640×200-pixel EL displays with a viewing angle of 160°. The EL1C-A000 has an active viewing area of 8.96×3.9 in. The EL1C-B000 has an active viewing area of 7.68×4.8 in. The pixel size and pitch (aspect ratio) differ with the model number. The pixels in the A000 display measure 0.010×0.017 in. and have a pitch of 0.014 in. (horizontal) by 0.020 in.



With its characteristic yellow-on-black color, EL displays provide high contrast. This electroluminescent flat-panel display from Digital Electronics Corp has an infrared touchscreen and is completely sealed in a cast aluminum case for use in harsh environments.

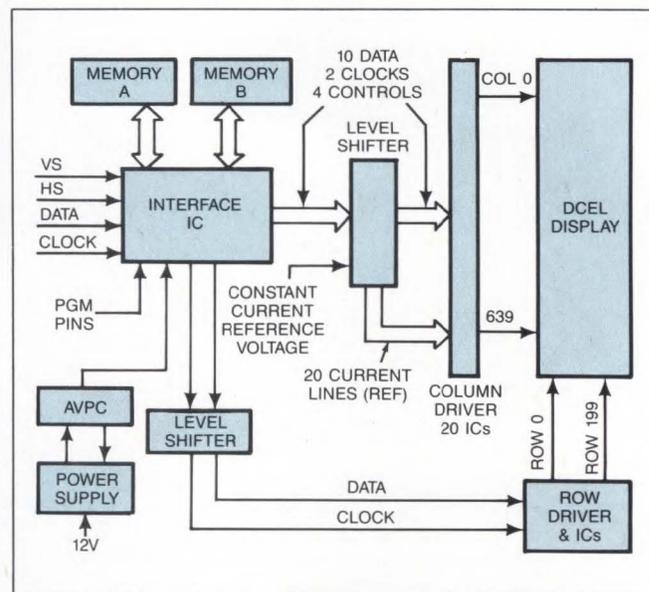


Fig 1—DCTFEL displays require specialized drive circuitry. This circuit works with Cherry's electroluminescent models and provides data and timing signals for the row drivers and constant-current column drivers. Video data with a frame rate of 60 Hz is translated into a 240-Hz frame rate for the column drivers.



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	Input Voltages	Matrix Configuration	Display Area	Size	Weight
MD640.200-20	+5V/ +12V	640x200 pixels	4.8 x 7.68 in. (122 x 195mm)	6.24 in. (158.5mm)H 9 in. (228.5mm)W 1.38 in. (35.0mm)D	16.8 oz. (470g)
MD512.256-39S**	+5V/ +12V 37S +5V/ +15V 38S +5V/ +24V	512 x 256 pixels	3.85 x 7.69 in. (95.2 x 97.7mm)	5.67 in. (140mm)H 10.2 in. (260mm)W 1.38 in. (35.0mm)D	23 oz. (650g)
MD640.400-52	+5V/ +12V	640 x 400 pixels	4.8 x 7.68 in. (122 x 195mm)	6.24 in. (158mm)H 9 in. (228.5mm)W 1.38 in. (35.0mm)D	20 oz. (560g)
MD640.350-60	+5V/ +12V	640 x 350 pixels	4.8 x 7.05 in. (122 x 179mm)	6.24 in. (158mm)H 9 in. (228.5mm)W 1.38 in. (35.0mm)D	20 oz. (560g)
MD320.256-71	+5V/ +15V	320 x 256 pixels	3.0 x 3.78 in. (76.7 x 96 mm)	4.33 in. (110mm)H 5.12 in. (130mm)W 1.38 in. (35.0mm)D	15 oz. (420g)

*Process developed by Lohja Corporation, Finland

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Plasma displays are often combined with infrared touchscreen panels for use in industrial control applications.

(vertical); its aspect ratio is 1.4:1. In the B000 display, the pixels measure 0.008×0.0202 in. and have a pitch of 0.012-in. horizontal by 0.024-in. vertical; its aspect ratio is 2:1. Pixel luminance is nominally between 20 and 25 fL, and Cherry specifies less than 30% degradation in brightness over 10,000 hours. Both models sell for \$565 (100) (\$250 in OEM quantities).

AC thin-film vs dc thick-film displays

Although there are numerous small differences between ac thin-film (ACTFEL) and dc thick-film (DCTFEL) displays, the major difference involves the operation of the two types of displays. An ac thin-film display is capacitive in nature and its brightness is limited by drive voltage and by pulse-repetition frequency. A dc thick-film display is resistive in nature and its brightness is proportional to its constant drive current. Cherry spent several years developing its dc thick-film displays, and their successful operation owes nearly as much to their electronics drive circuitry as it does to their basic construction.

The Cherry drive circuitry (Fig 1) uses some custom and standard ICs from Siliconix and Texas Instruments. The interface IC provides data and timing signals for the constant-current column drivers, row drivers, and control signals. The frame rate for incoming video data is 60 Hz; for data output to the column

drivers, it's 240 Hz. The higher frame rate for the column drivers provides a brighter display with less power consumption, thus lengthening the life of the EL display.

Four TTL signals—vertical sync, horizontal sync, data, and clock—control the circuit operation. The level-shifter IC converts the 5V CMOS-logic outputs of the interface IC to 12V signal levels needed for the column drivers. It also converts a 0 to 12V analog reference to a constant current capable of driving 20 column drivers. The column-driver IC provides a controlled capacitive charging current, and an illuminating current with a programmable range from 100 μ A to 1 mA. The row-driver IC sinks a minimum of 200 mA when on. The power supply operates from a single 12V input. An automatic voltage- and pulse-control circuit adjusts the output of the power supply to provide a preset luminance level throughout the life of the panel. Cherry has two excellent papers on the development and construction of its EL displays and the electronic drive circuitry (Refs 1 and 2).

Flat-panel displays employ several different technologies and are available in a range of sizes and shapes. From simple bar graphs to displays large enough for use in computers, you have a wide choice when looking for a display to suit a particular application. LCDs, VFDs, and PDPs will likely continue to dominate

Manufacturers of flat-panel displays

For more information on flat-panel displays, contact the following manufacturers directly, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service.

Alphasil Inc
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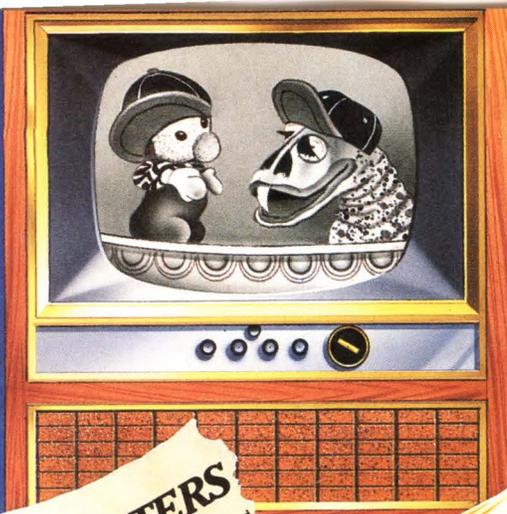
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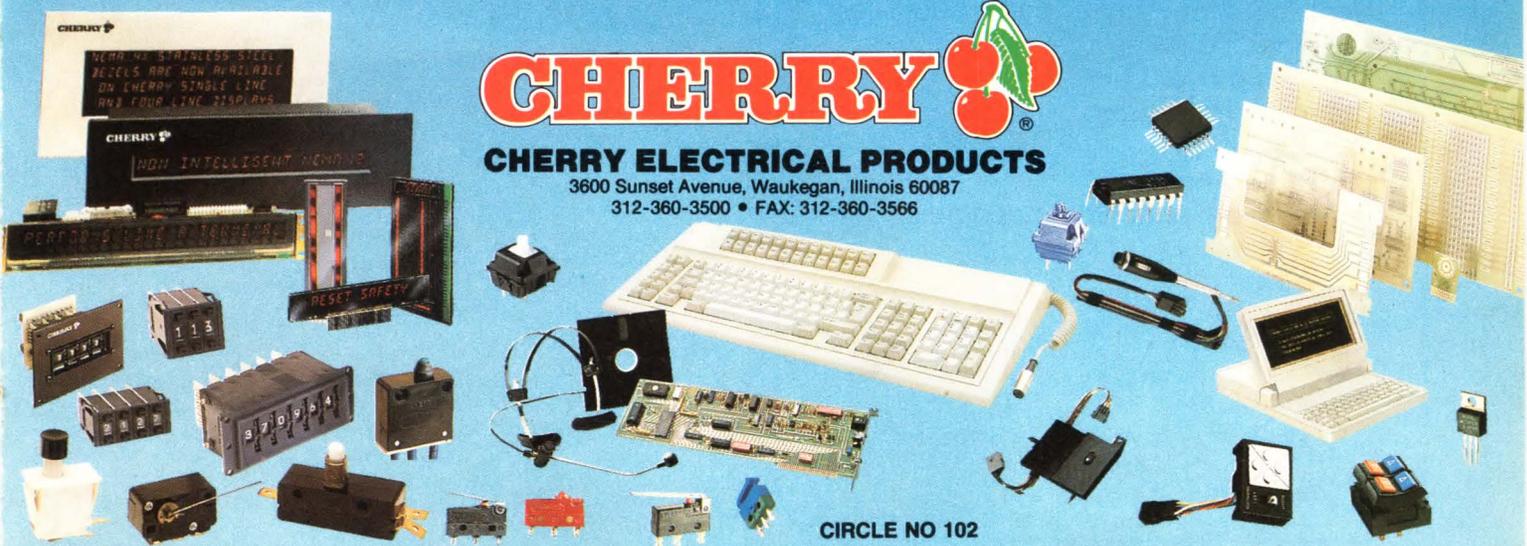
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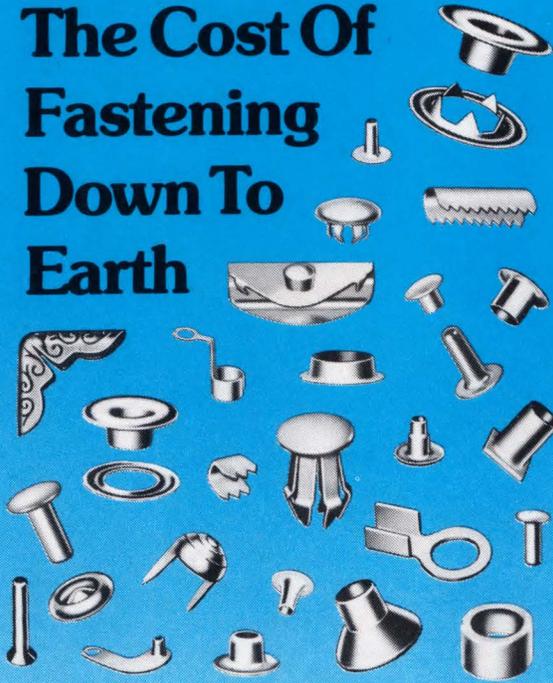
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limited information content applications, while PDPs, ELDs, and active-matrix LCDs strive to satisfy the demands for large-area displays capable of providing expanded information content. As ELDs and active-matrix LCDs come down in price, you can expect to see more of them in more and more demanding applications. These types of displays will also be available in color, probably within the next three years. **EDN**

References

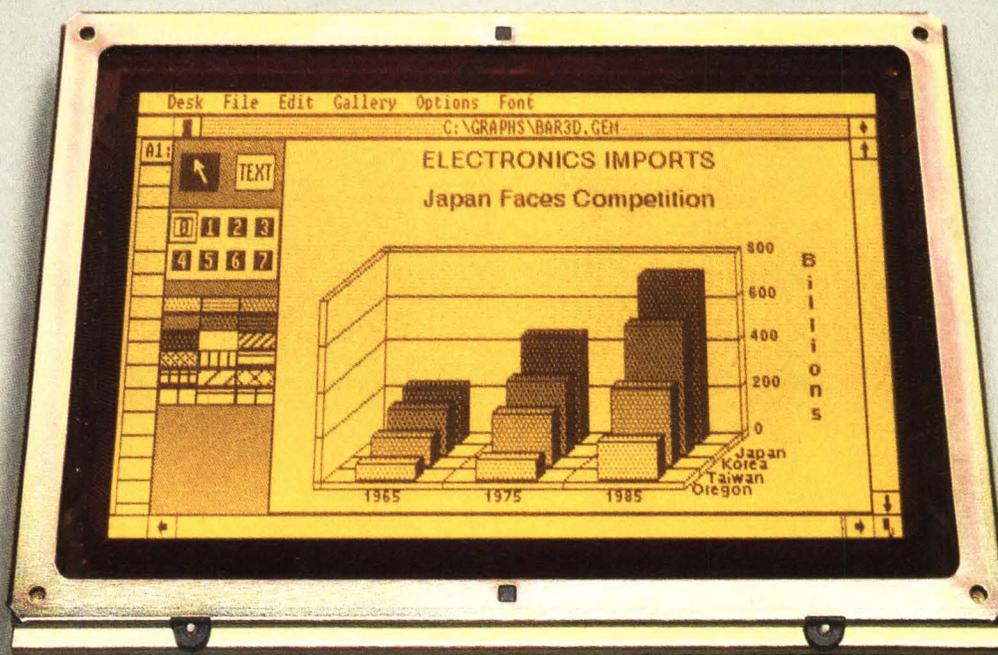
1. Channing, D and L Chiang, "Drive System for a 640x200 dc EL display," Cherry Display Products, Waukegan IL.
2. Glaser, David, and George A Kupsky, "DC electroluminescent 640x200 display panel," Cherry Display Products Corp, El Paso, TX.

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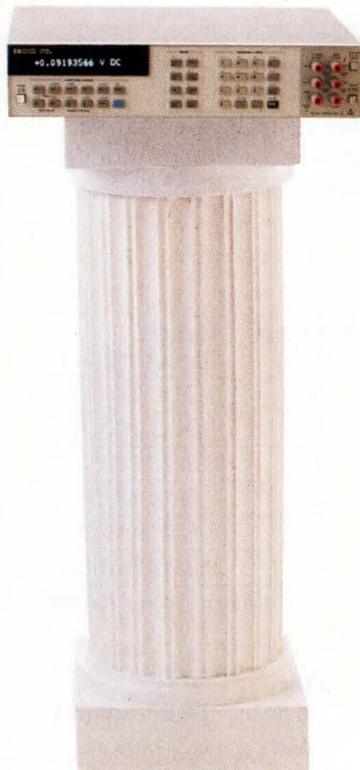
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GP1006B	GP1006B04	256X64	200	9.84X3.35X1.77
GP1009B	GP1009B03	240X64	200	6.2X2.76X1.57
GP1010B	GP1010B01	176X16	200	7.32X2.16X1.70
GP1002C	GP1002C02	320X240	100*	7.10X6.30X1.60
GP1004B	GP1004B03	640X400	30	9.65X7.28X1.85

*Different Versions Available

DOT MATRIX DISPLAYS/MODULES

Futaba Display	Futaba Module	Char. X Row	Dot Format	Char. Ht. (in.)	Module Dimensions (in.)
20SD01Z	M20SD01	20X1	5X7	0.200	6.3X1.97X.75
20SD42Z	M20SD42	20X1	5X12	0.344	7.1X2.16X.88
40SD02Z	M40SD02	40X1	5X7	0.200	9.45X2.16X.88
40SD42Z	M40SD42	40X1	5X12	0.344	9.45X2.16X.88
202SD03Z	M202SD03	20X2	5X7	0.200	6.7X2.56X.90
402SD04Z	M402SD04	40X2	5X7	0.200	10.43X2.56X.90

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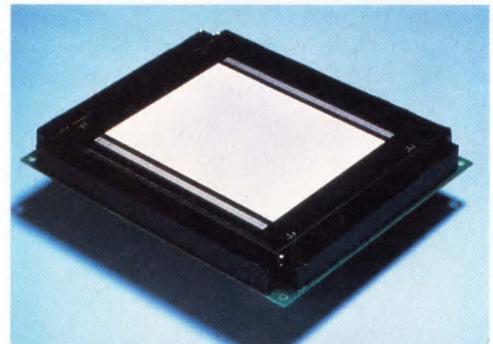
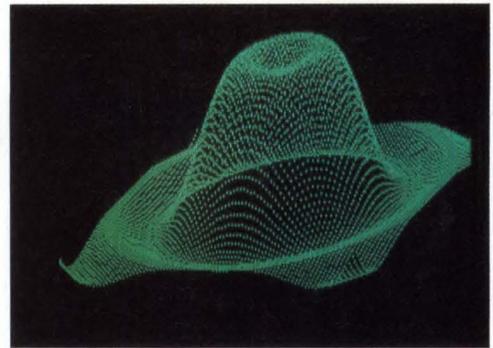
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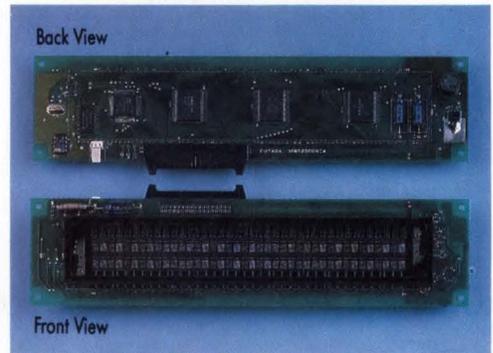
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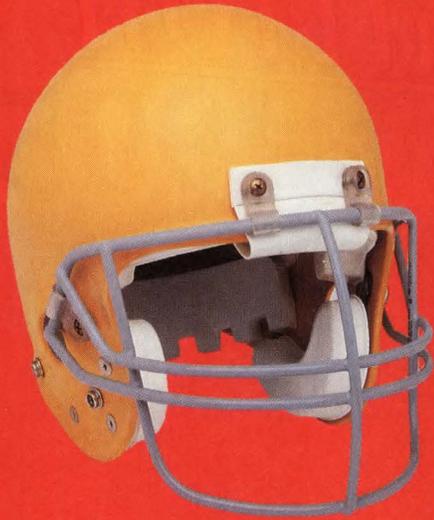
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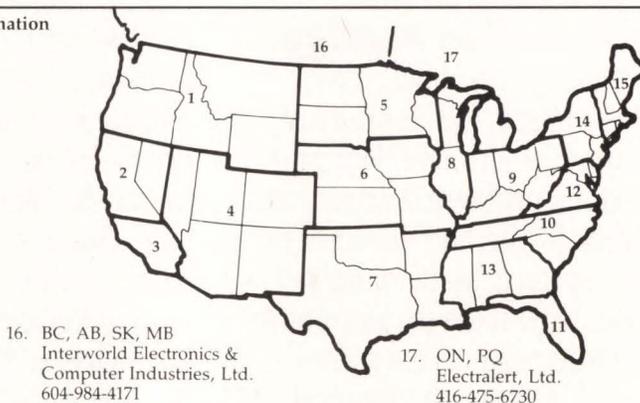


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Kevin Walsh, *Electrical Engineering Software* and Gary Lum, PhD, *Lockheed Missiles and Space Co*

To ensure the reliable operation of spaceborne electronic systems, you must consider radiation effects such as single-event upset (SEU), a condition that can bring on system failure. Circuit-simulation software can help you predict the effects of SEU on your spaceborne circuits and systems. Such software lets you model the effects of SEU on your system and identify critical circuit nodes—nodes susceptible to state changes that can cause system failure.

By combining the computer simulation with dosimetric data obtained in the lab, you can then construct a survivability profile for your system. The survivability profile defines the radiation levels your system will tolerate. With that information, you can make corrections at the design stage to harden your circuits against

the effects of an SEU occurrence. (Note, however, that SEU is not the only radiation effect that you need to be concerned about. Van Allen-belt radiation, for example, can cause long-term degradation in system performance even when it doesn't cause SEU.)

Upsets result when particles hit silicon

Single-event upset occurs when a high-energy ionizing particle irradiates a circuit or passes through an IC. In spaceborne systems, SEU can result from radiation that occurs naturally in space—cosmic radiation or Van Allen-belt radiation—or it can result from manmade sources such as nuclear explosions. The most common effects of SEU are logic-bit flips in high-density circuits, including MSI, LSI, and VLSI circuits. As **Fig 1a** shows, these state changes result when charged particles deposit charge in a semiconductor device's sensitive junction region. Protons are a special case—they create nuclear reactions, each of which generates a number of secondary reactions, including nuclear recoils, that deposit charge (**Fig 1b**). Most SEU errors are correctable or “soft” errors; usually, when a cell suffers SEU it demonstrates no degradation or change of hardware characteristics.

However, recent data indicates that SEU can cause device latchup in power MOSFETs. In such cases, SEU can cause permanent damage. If you're designing circuits for use in environments where SEUs are likely to happen, you need to understand the effects of ionizing particles on semiconductor devices so that you can protect your systems.

By analyzing models of key portions of circuits, simulation can tell you how the circuits will react when charged particles hit semiconductor surfaces.

Examining an electronic system for susceptibility to environmental radiation can be time-consuming, especially if the system consists of multiple ICs. If you know what circuits and subsystems are most likely to be affected by radiation, you can reduce the time you spend in simulating the circuit. For example, unless you take special precautions, the probability is high that SEU will alter data stored in memory elements—these elements react dramatically to SEU, and most systems contain a lot of them. It doesn't matter how data gets into a memory cell; the system can't distinguish correct information from information altered by radiation. Moreover, SEU-induced state changes can cause significant system damage. So IC memories are logical candidates for detailed simulation.

Another circuit area to explore is the registers in microprocessors. Registers often contain pointer information that, if altered, can cause the retrieval or processing of spurious data. Systems with sequential

logic also suffer from potentially damaging state changes. A state change in one node can affect the proper sequencing of the signals through the logic. SEU can affect synchronous logic, but it corrupts the data only when it occurs on the clocking phase. SEU also affects analog circuits, but not as dramatically, because analog circuits typically aren't state oriented. Nevertheless, understanding the impact of SEU on analog circuits and hardening your circuits against it can make your systems more reliable.

Upset in a static RAM—a case in point

Fig 2 is a schematic of a cell in a nonvolatile RAM, a RAM that normally retains data as long as you don't remove power from it. This cell is typical of the multiple cells that make up the RAM. As a memory cell, it's particularly susceptible to SEU-induced state changes. The accumulation of charge on the nodes that make up the cell controls the cell's state. Although the simula-

Simulator makes radiation hardening easy

When you perform circuit simulation, you must be able to describe how particles interact with semiconductor material and to analyze the electrical result. The Precise ASD software package from Electrical Engineering Software provides an easy way for design engineers to describe these behaviors and simulate them. The software runs on a variety of systems, from workstations to supercomputers. The simulator's functions are mathematical expressions that can depend on time, frequency, temperature, or any variable you choose. Because the simulation program evaluates them as the simulation progresses, these functions serve to model a variety of effects, from time-dependent switches to photocurrents generated in silicon material by nuclear explosions.

You can use the package, for

example, to describe what would happen if you were to connect a photocurrent generator to key silicon junctions of an IC. The derivation of the photocurrent translates into a mathematical expression that you then transfer to the Precise simulator. The photocurrent definition is:

$$I_{PP} = \gamma \cdot q \cdot g \cdot A \cdot L \cdot (\text{erf}(t/\tau) - u((t - PW)/\tau)) + \gamma \cdot q \cdot g \cdot A \cdot W \cdot (u(t) - u(t - PW)),$$

where I_{PP} =photocurrent in amperes, γ =dose rate in rads, $q=1.6 \times 10^{-19}$ coulombs, $g=4.2 \times 10^{13}$ carriers/(rad-cm³), A =area of junction in cm², L =diffusion depth in cm, τ =minority current lifetime in sec, PW =photocurrent pulse width (duration) in sec, W =depletion depth in cm, $u(x)$ =a unit step function of x , and $\text{erf}(x)$ =dimensionless error

function. The function $\text{erf}(x)$ equals

$$1 - (1 + a_1x + a_2x^2 + a_3x^3 + a_4x^4)^{-4} + E(x),$$

where $a_1 \dots a_4$ are coefficients and $E(x) \leq 5\epsilon^{-4}$.

You can use Precise to evaluate the photocurrent equation by creating a function file with the system editor and defining the expression. This expression uses a unit step-function definition, $u(t - PW)$. To simulate what would happen when you stimulate a circuit with the function, you place dependent current sources that reproduce the function at the circuit's critical pn junctions. Simulating with this photocurrent definition can give you an indication of how the circuit would respond to the photocurrents that would be generated by a thermonuclear explo-

tion covers a single cell, controlled sources simulate the presence of other cells. You can adjust these controlled sources to model different RAM sizes. To model the remaining cells, you multiply the source outputs by an appropriate constant.

To predict the effect of a particle's entering a circuit, you require a model for the current that's created as the particle moves through the material. As the particle passes through the depletion layer and into the substrate, it produces a track of mobile holes and electrons. These charges form along the track of the particle. The charges distort the charge distribution in the semiconductor material and cause funnel-shaped equipotential surfaces to extend into the substrate. The gradient of these equipotentials propels electrons (which are produced as the particle passes through the material) back up through the funnel, as **Fig 1a** shows.

Sufficient charge buildup will cause a change in the cell's state. If the particle passes close to the node, the

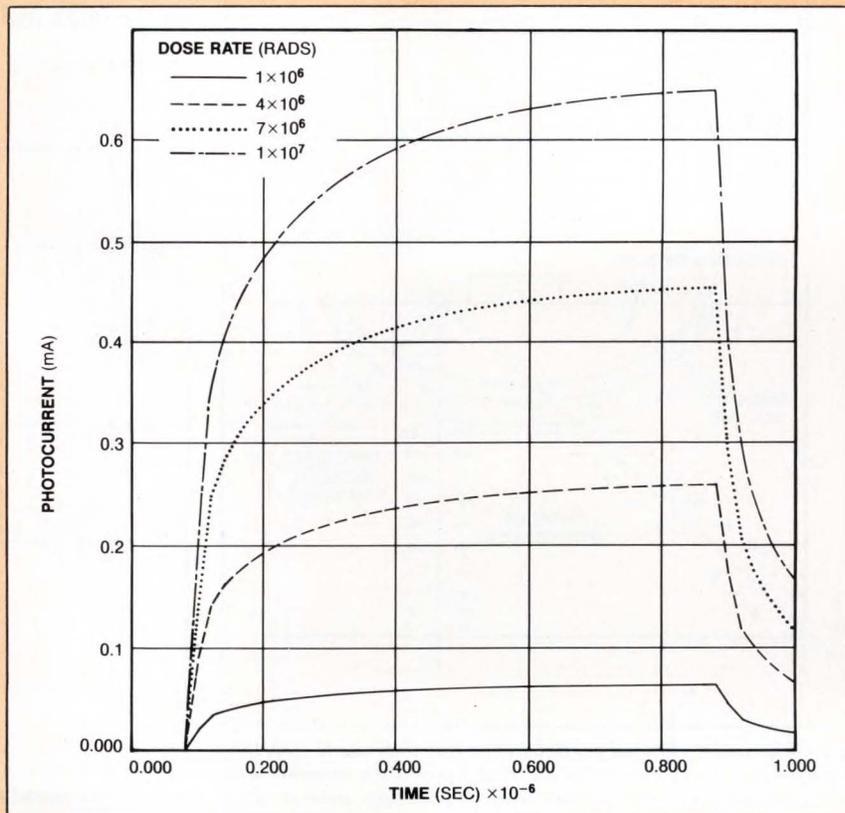
charge accumulates in picoseconds. If the particle passes further from the node, the charge-collection time is on the order of nanoseconds or microseconds. The current created by the particle depends on the semiconductor material, the charge collection, and the angle at which the particle hits.

By performing simulation, you can predict what particles and particle energies will cause the memory cell to change state. First, you must analyze the circuit with a transient simulation while using dependent-current-source modeling to model the particle's motion through the material. Next, you change the current to reflect the incident particles' differing amounts of energy and the range of angles at which they hit the semiconductor. After trying different system-hardening techniques, you can compare the circuit's response to the same upset. By simulating the circuit's response to upsets, you can test alternatives quickly, accurately, and inexpensively. If your circuit-simulation program

sion (**Fig A**).

The simulator lets you analyze the transient response while varying other parameters. This mixed-domain, or 2-dimensional, analysis gives you a family of responses based on the setting of the parameter. You can add a third dimension with the SET command. In this case you might use SET to establish a third analysis dimension in which pulse width (PW) is a parameter.

Fig A—A simulated photocurrent source shows a current buildup that reaches its final value in under a microsecond.



The most common effects of single-event upset are logic-bit flips in high-density circuits, including MSI, LSI, and VLSI circuits.

permits you to use a flexible definition of current, it can provide a picture of the survivability of the circuit state as particles with different energy hit the cell at varying angles of incidence.

Equations describe the SEU function

The simulator models the effect of a particle passing through a RAM by placing a current source on the RAM circuit, as Fig 2 illustrates. The current source is in parallel with the transistor on which the particle can have the most effect, given the circuit configuration. In this case, the most susceptible transistor is Q_4 —because

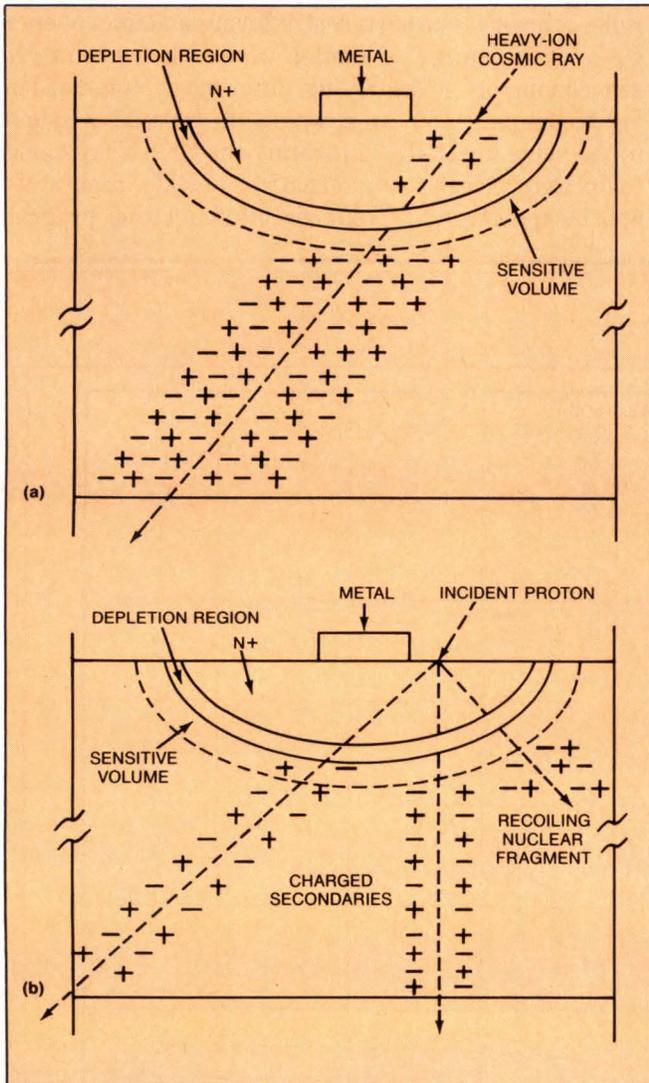


Fig 1—When most charged particles enter a semiconductor die, they deposit charge in regions of the die, and hence often interfere with device function (a). Protons create nuclear reactions, each of which generates secondary reactions that deposit charge (b).

OUT_2 is high. Over time, current builds up at the OUT_1 node. This current changes the basic state of the node. The analytical approximation of the current is:

$$I(t) = I_0 \sec\theta (\epsilon^{t/\alpha} - \epsilon^{t/\beta})$$

where I_0 is approximately the maximum current; θ is the angle of incidence of the particle to the IC; α is a collection time constant of the junction; and β is the time constant for initially establishing the ion track. Typical values for α and β are 150 psec and 40 psec, respectively. The maximum current, I_0 , is proportional to the energy of the particle and the doping profile of the semiconductor material. I_0 varies according to the particle type—heavy ions, alpha particles, or protons. The total current increases as the angle of incidence varies from grazing to near normal.

If you formulate the basic equation as a time-dependent function, you can analyze it with a simulator such as Precise (see box, "Simulator makes radiation hardening easy"). Precise lets you define and name the function in an independent file so you can easily reference it in different circuit locations. You place the current-source element, which references the function, on the latch node of the RAM cell (Fig 2).

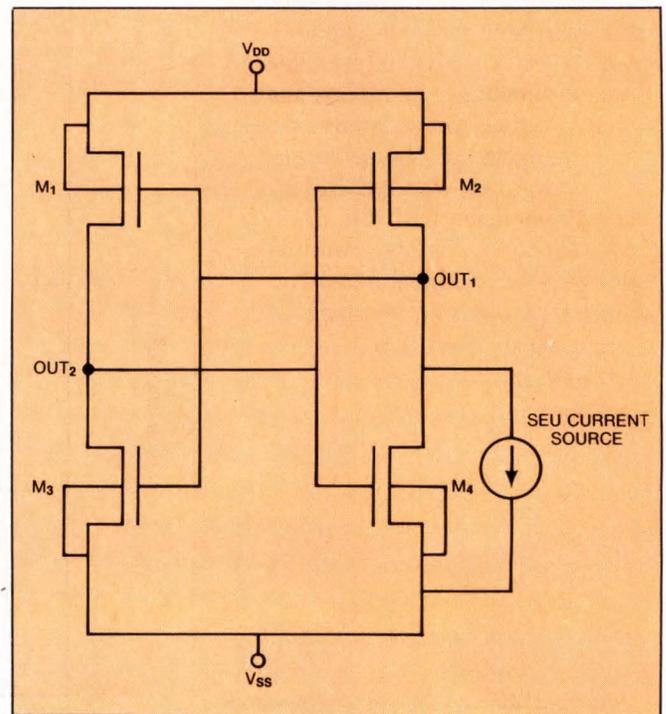


Fig 2—You model the effect of radiation on this static-RAM cell by placing a current source in parallel with one transistor.

In Precise notation, the function called "SEU" is defined thus:

```
FUNCTION SEU(I0,ANGLE)
I0*1/COS(ANGLE)*[EXPN(TIME/150PS)-EXPN(TIME/40PS)].
```

The current source, which represents the SEU function, is defined as:

```
ISEU Node1 Node2 SEU(I0,ANGLE),
```

where ISEU is the current-source definition, Node1 and Node2 define the connection of the source to the circuit, and SEU is a call to the current function that defines the particle's penetration of the semiconductor material vs current and time. You define the function by using a simple mathematical syntax available in the Precise simulator. This special language syntax lets you define behaviors quickly and easily. In this case, the function definition takes advantage of the language syntax that allows TIME to appear as a variable in the function. In addition, the SEU function has two arguments: I_0 passes into the function and takes values based on the particle of interest and the doping profile;

ANGLE is the value that determines how the particle strikes the semiconductor material.

Fig 3 shows the actual current generated from the SEU function by a particle (whose energy is represented by an I_0 of 0.5 mA) that strikes the IC die at incidence angles ranging from 0.1 to 1.3 radians (approximately 6 to 70°).

Ready . . . set . . . simulate!

You now simulate the RAM cell to see its response to the application of a selected particle energy at different angles. Precise's mixed-domain capability allows you to vary two different domains in the same simulation. In this case, you vary time and particle angle. The SEU function changes the amount of current delivered to the node during the transient analysis. While holding I_0 constant at 0.5 mA, you vary ANGLE from 0.1 radians to 1.1 radians. Fig 4 shows the result as a family of curves that represents the cell reaction to the particle current's striking at different angles. The grazing angle of 0.1 radians does not cause the cell to change state. However when the angle reaches 1.1 radians, the current is sufficient to change the state of the cell. The penetration of a charged particle and its subsequent

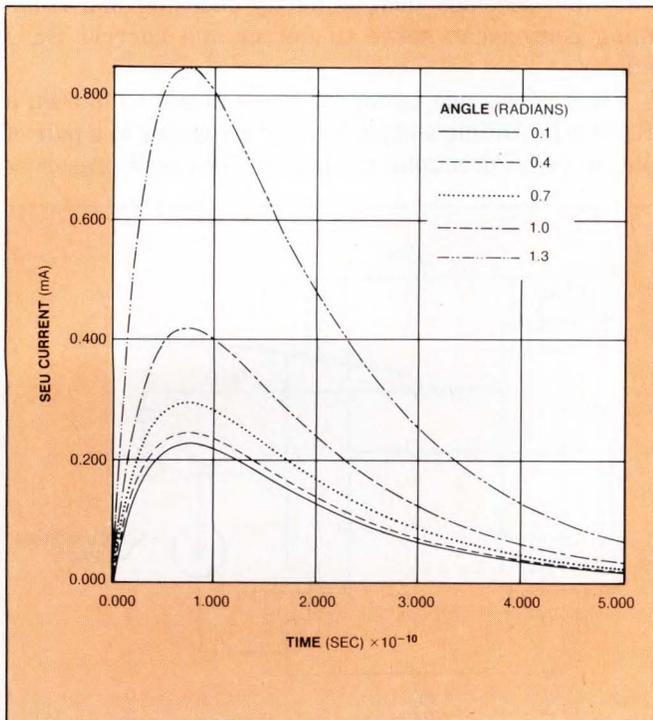


Fig 3—When particles of a given energy level strike a silicon die at angles of 0.7 radians or less, the peak current barely exceeds 0.2 mA. At larger angles, the current increases rapidly, though.

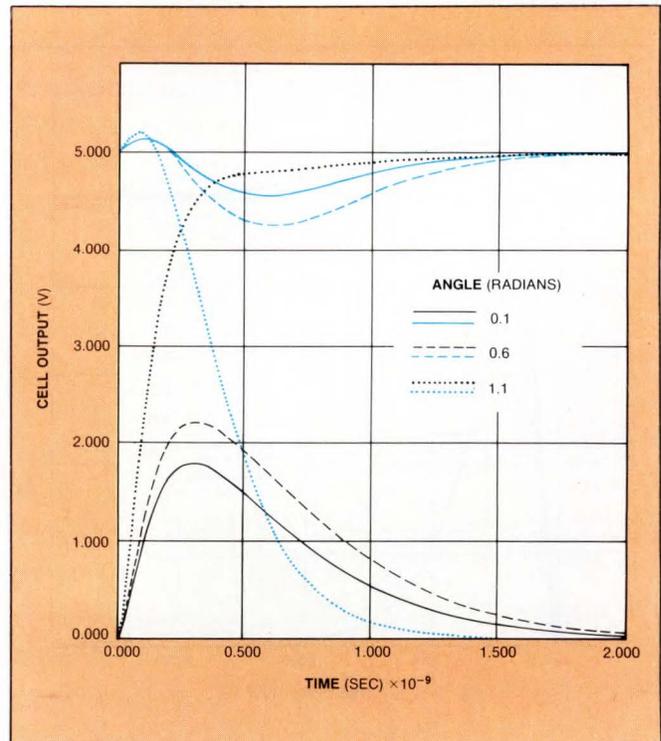


Fig 4—A particle striking the static-RAM cell at an angle of 1.1 radians or more will change the cell's state from 0 to 1 or from 1 to 0.

Unless you take special care, SEU will probably alter data stored in memory elements—and most systems have a lot of memory elements.

reaction with the semiconductor material at this current and angle is an SEU that causes a state change in the RAM cell.

For further analysis, you next set the particle angle at the nominal value of 0.7 radians. To see how sensitive the cell is to particles of different energy, you now simulate a variation in particle energy. You use particle energies that result in currents ranging from 0.1 to 1.1 mA. The resulting graph (Fig 5) shows how level shift varies with particle energy for this range of currents.

Hardening isn't necessarily hard to do

The modifications necessary to minimize the effects of SEU on your assemblies fall into three design categories: process, chip, and system. Your choice of a hardening approach will depend on your design objectives and the cost of the approach. Techniques for hardening circuits, for example, usually increase circuit costs by increasing die size or adding circuit elements for decoupling. Further, because it introduces large RC time constants, decoupling can also reduce circuit speed. You must judge each hardening technique on its effectiveness, its cost, and its effect on the system's performance.

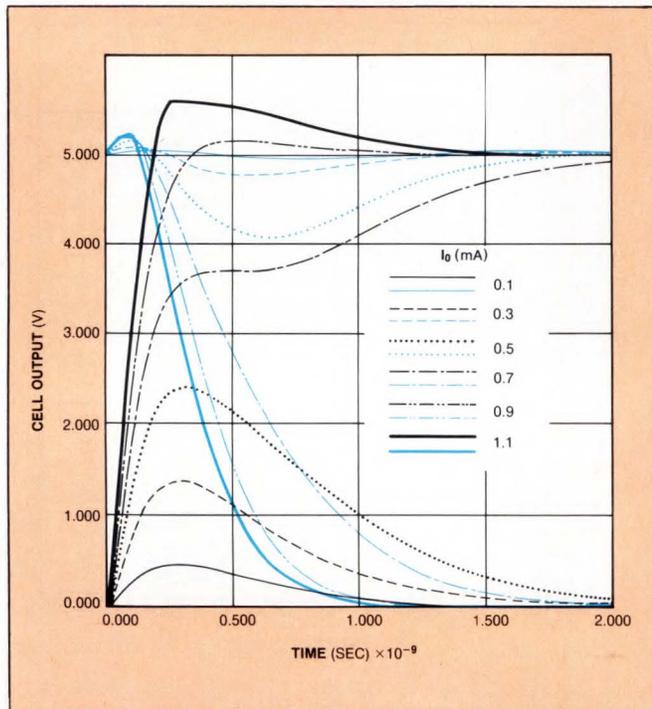


Fig 5—As incident-particle energy increases, the cell's output shifts but returns rapidly to its original level. Particles whose energy exceeds a threshold level cause the cell's state to flip.

Certain semiconductor-fabrication processes minimize SEU by using epitaxial silicon structures to truncate the charge-funneling effect. SOS (silicon-on-sapphire) or SOI (silicon-on-insulator) devices can serve this purpose. These devices can be very thin, having shallow junctions, in order to minimize the interaction time of the particles with the junctions. Retrograde junctions or buried, heavily doped layers can also help to preserve the state of the cell.

In chip design, varying the geometry to increase device widths can help preserve the cell state. By both varying the device geometry and increasing the supply voltage, you can achieve a fairly high level of hardness with relative ease. The use of decoupling resistors and capacitors or diodes can preserve the state of a latch. Adding local circuit redundancy by including additional components can strengthen nodes' resistance to state changes. You should examine the critical paths of sequential circuits for susceptible nodes. If several flip-flops are connected in series, path isolation or decoupling can prevent the propagation of an error that occurs when the state of the first flip-flop changes. Finally, from a systems point of view, using error-detection schemes such as parity checking and Hamming coding can serve to detect and correct SEU effects.

Fig 6 shows one technique you can use to harden a RAM cell. Adding a capacitor and a resistor to a pair of output nodes decouples the nodes. The result preserves

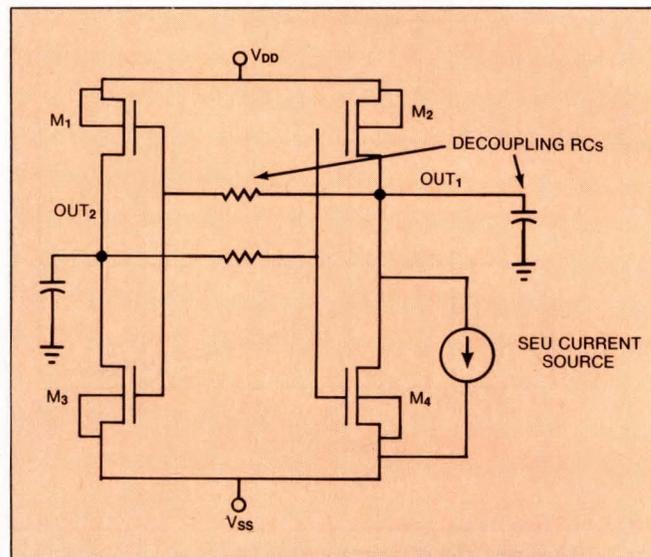


Fig 6—Adding a pair of RC networks to the static-RAM cell yields a hardened design without requiring you to change the device geometries or the fabrication process.



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With simulation, you can predict what particles and particle energies will cause a memory cell to change state.

the charge on the node during an upset, making the circuit less likely to switch states.

To study the impact of the added components, you can run another transient simulation. From Fig 7 you can see that the particle energy that caused a change in the cell state no longer has an effect; however, the additional components increase the circuit's complexity. You can also change the device geometries to prevent an upset from causing a shift in state. Because it doesn't increase circuit complexity, changing geometry can be more cost effective than adding components. You can easily test this hardening alternative by changing the device dimensions and resimulating. To study the cell reaction to the SEU function, you set up the device dimensions as Precise variables and conduct the simulation with varying device widths and lengths.

Simulation helps raise reliability

Analyzing SEU by using simulation is an effective means of identifying potential circuit problems before they occur in production systems: In effect, simulation lets you harden a system before building it. Further, simulation is a cost-effective alternative to dosimetric prototyping for SEU analysis. Finally, circuit simulation is a fast and accurate method of studying different hardening techniques for overall effectiveness. Al-

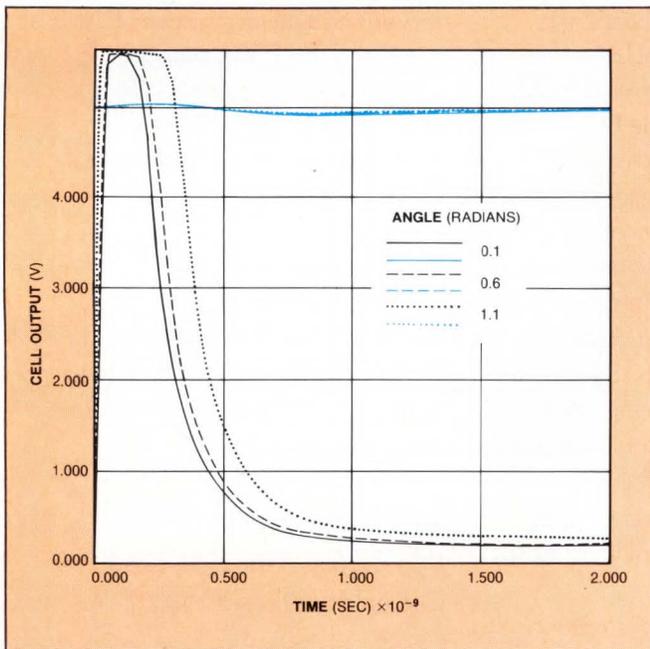


Fig 7—When you add components to the design and run another transient simulation, you find that particles that caused the original cell to change states no longer affect the cell's output.

though the example presented here addresses only SEU, simulation is just as useful for analyzing other environmental effects on circuits—for example, temperature and mechanical stress—as well as the effects of parameter variation in manufactured components.

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Authors' biographies

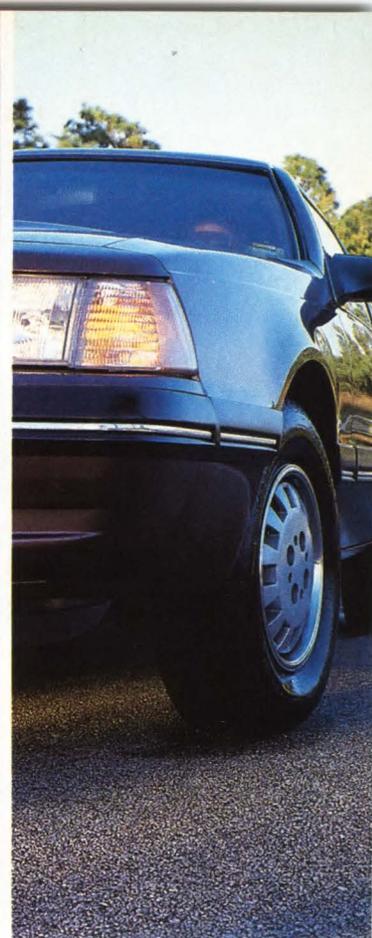
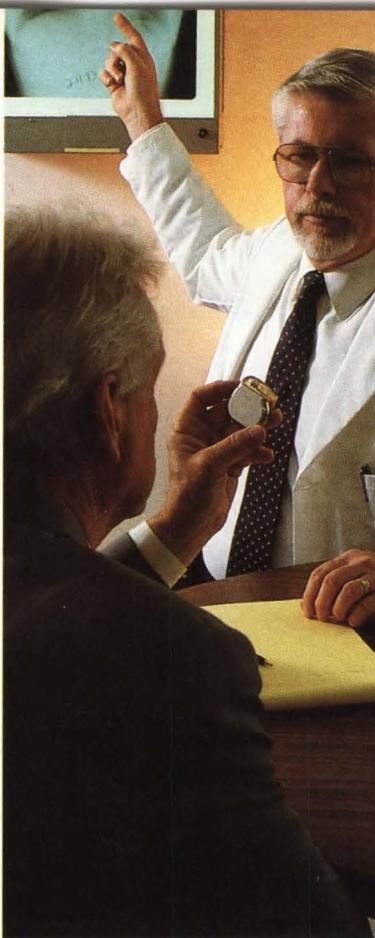
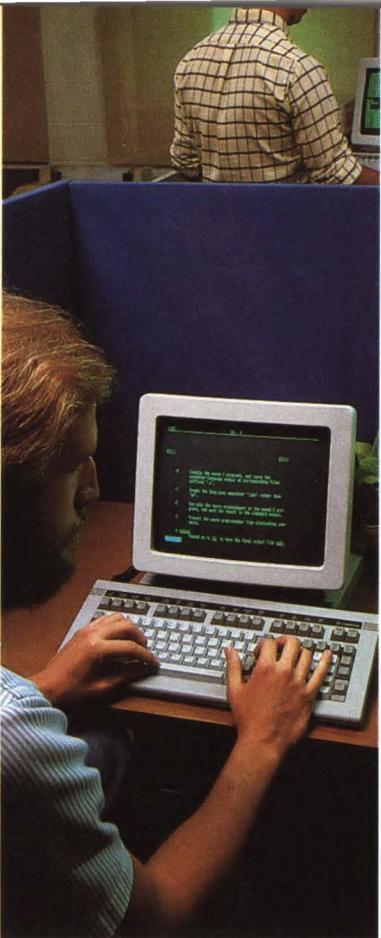
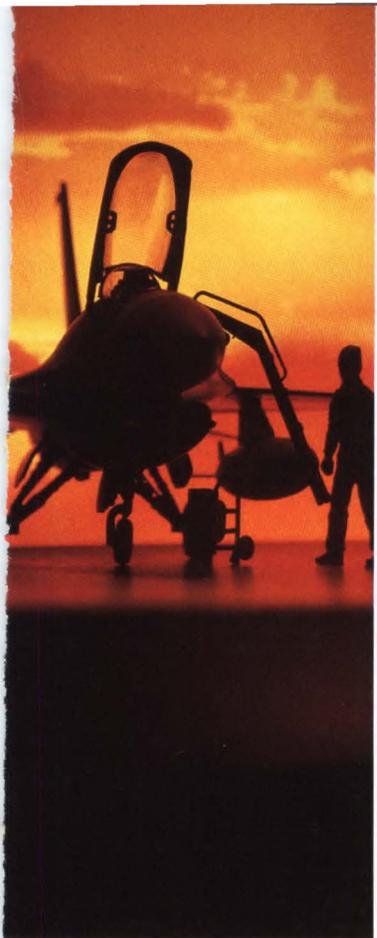
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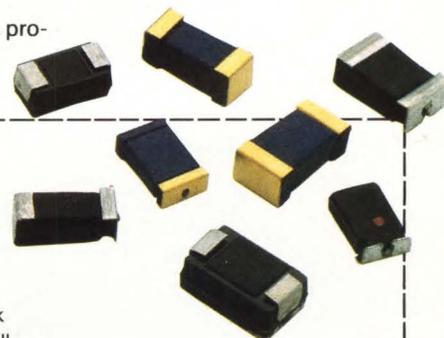
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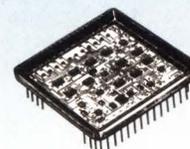
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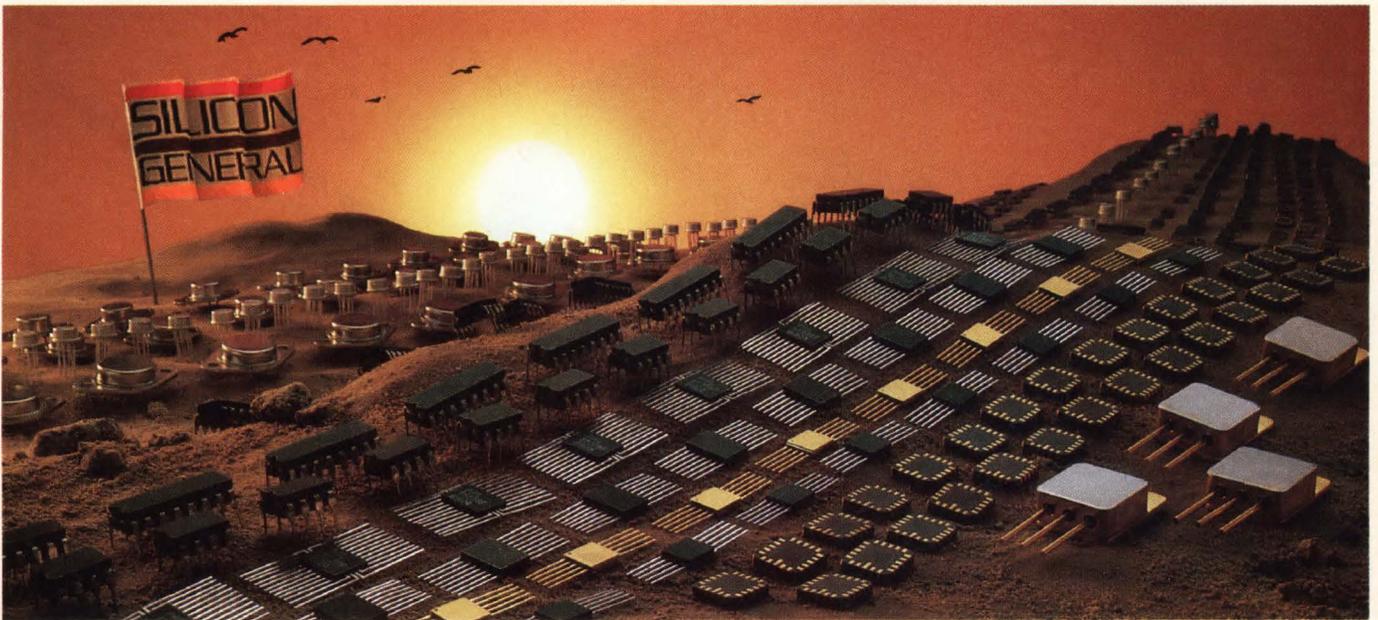


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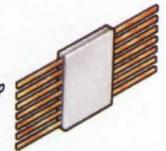
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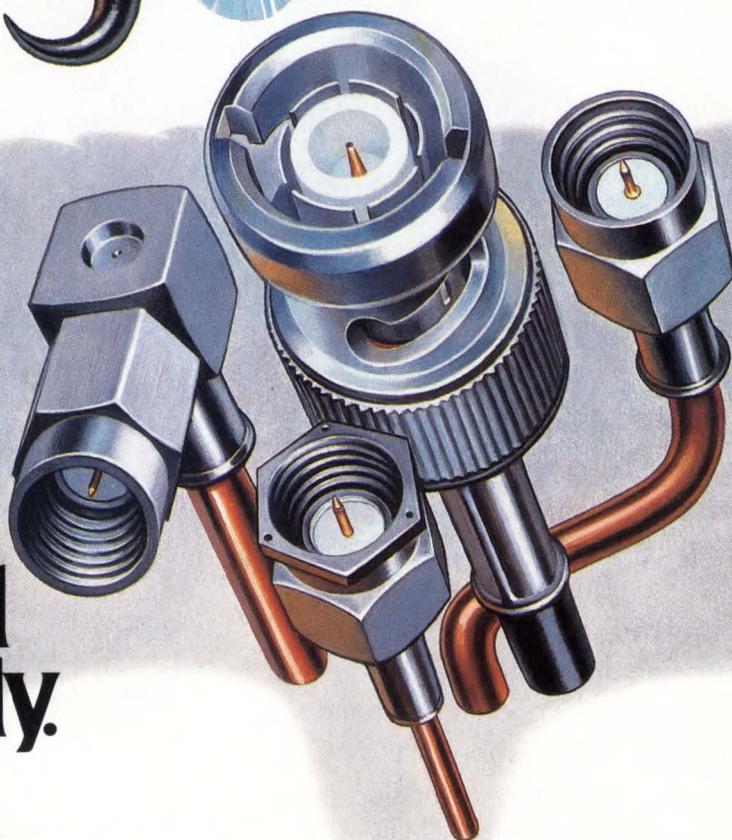
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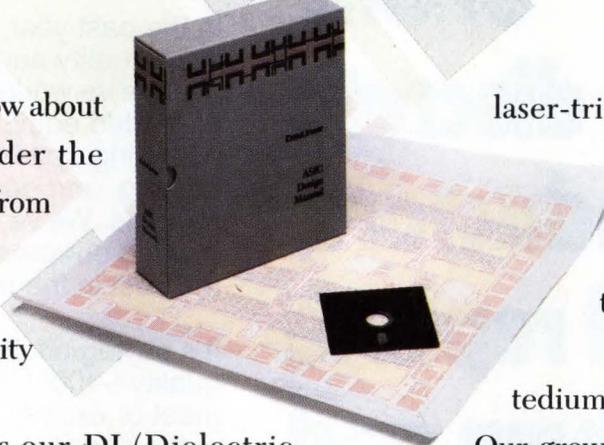
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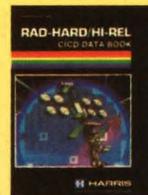
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Peer-to-peer protocol facilitates real-time communications

The low communications overhead of the CSMA/DCR peer-to-peer protocol makes it desirable for real-time network applications. Further, the protocol's guaranteed network-access time relieves the designer from worst-case haunts.

Deif N Atallah, *Intel Corp*

By definition, real-time-communication networks need to transfer information between nodes as quickly as possible. Preferably, these transfers should occur within a guaranteed maximum time limit. Networks have traditionally achieved real-time communications via some type of master/slave protocol, contention-based protocol, or token-based protocol—each with their own advantages and disadvantages. A relatively new contention-based protocol, based on the advantages of each of these methods, enhances the information-transfer rate of a real-time network.

A master/slave protocol is a popular method for real-time communications because it guarantees that all the nodes on the network will gain access. Examples include the Synchronous Data Link Control (SDLC) and High Level Data Link Control (HDLC) protocols. A

master/slave protocol requires the management of a significant amount of overhead, however, which in itself occupies valuable bandwidth. A master node has to first poll the slave nodes to initiate communication, and it must then take control of the link to ensure that communication takes place. If the network has multiple masters, they must arbitrate for control of the network, so that a maximum access time cannot be guaranteed.

Token-passing protocols, in contrast, guarantee a maximum access time for each node on the network by sequentially passing a token around to each node. To avoid contention, each node must acquire the token before transmitting information. Even if the network is quiet, however, a node must wait until the token goes all the way around the network. If there are many nodes on the network, the guaranteed maximum access time can be long. Examples of token-passing protocols are the IEEE 802.4 and 802.5.

A peer-to-peer communication protocol such as the Carrier Sense Multiple Access with Collision Detection (CSMA/CD), which is what Ethernet uses, has low communications overhead. It can't guarantee a maximum access time to the network, however, because it resolves contention problems statistically. The CSMA/CD lets a node monitor the network for a quiet period in which to send its message. If messages from two nodes collide, the two nodes have to wait for a random interval of time and then they attempt to retransmit. Although you can choose network parameters to minimize the

The CSMA/DCR protocol guarantess a maximum access time to the network, yet it has the same low communications overhead as the CSMA/CD.

probability of successive collisions, you can't be guaranteed of a maximum access time because of the protocol's nondeterministic recovery mechanism.

Determinism offers a guarantee

A variation of the CSMA/CD protocol, the CSMA/DCR (deterministic collision resolution), merges the advantages of the aforementioned protocols. The protocol features the same low communications overhead as the CSMA/CD, yet guarantees a maximum access time to the network.

The protocol operates in a peer-to-peer CSMA/CD mode until a message collision occurs. Any node on the network can initiate communications without polling for a response. This lack of polling overhead maximizes the link's bandwidth. Essentially, the physical layer of the OSI (open system interconnection) model looks for opportunities to transmit by monitoring the network's activity. This network-access scheme, coupled with the guaranteed access time of the resolution phase, produces a very efficient network even during heavy traffic conditions.

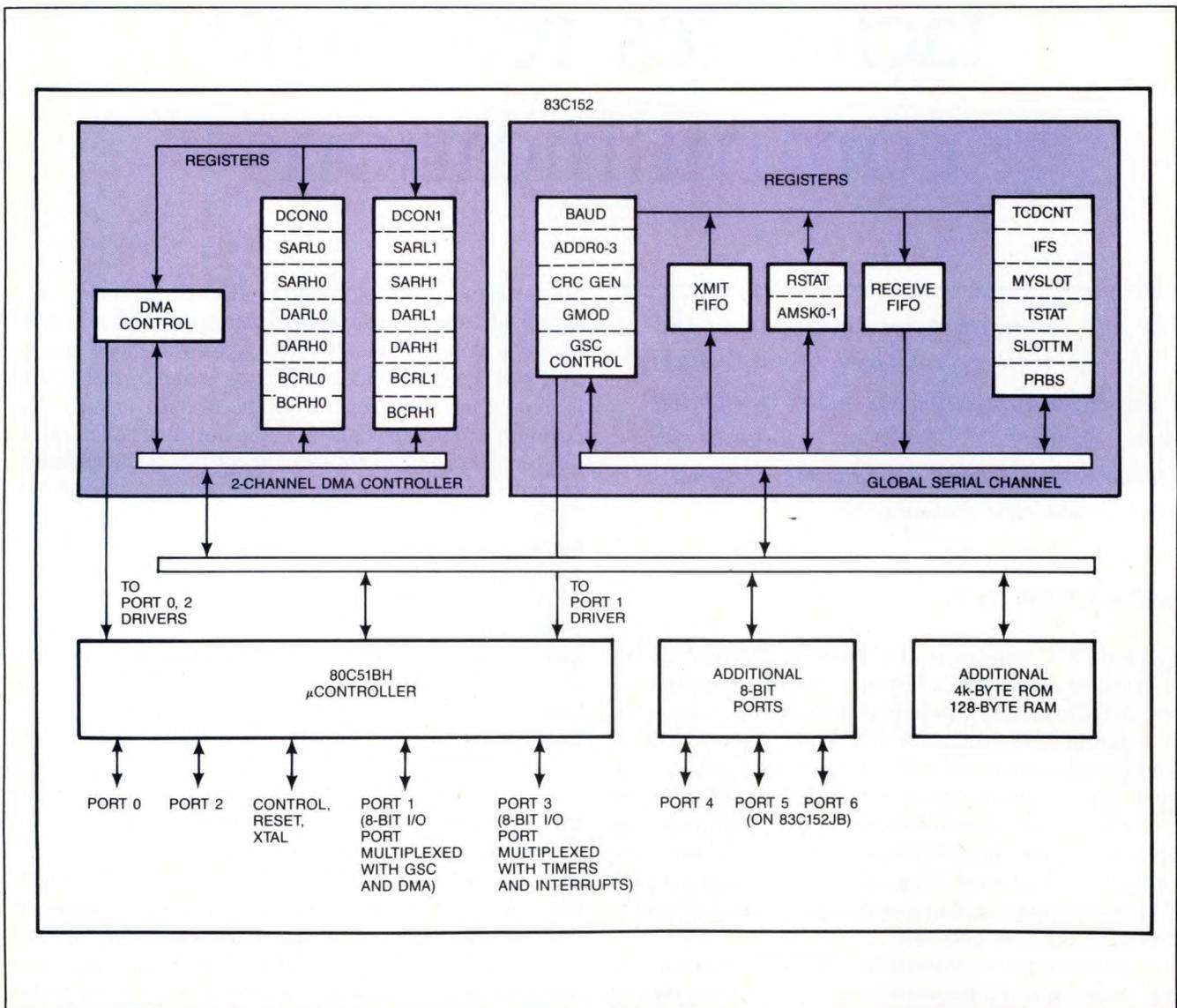


Fig 1—The 83C152 communication controller has a multiprotocol Global Serial Channel (GSC) and two DMA channels functioning as peripherals for the 80C51BH μ controller. Different versions of the 83C152 offer additional ports.

When a collision takes place, all of the nodes on the network, regardless if they are involved in the collision, enter into something called a resolution phase. The worst-case access time is equal to the maximum time of the resolution phase, which you can calculate from the network's configuration and parameters. During the resolution phase, the protocol assigns each node on the network a programmable time slot for data transmission. During its allotted time slot, a node has the option of transmitting a message. The node's maximum allocated frame length determines the length of the message. This type of recovery sequence eliminates the possibility of successive collisions.

A single IC can do it all

The Intel 83C152 is an example of a single-chip VLSI communication controller that implements the CSMA/DCR protocol (Fig 1). (It implements several others as well, including the CSMA/CD protocol.) The IC has an 80C51BH microcontroller core that contains an asynchronous serial port, 4k bytes of ROM, 128 bytes of RAM, four 8-bit parallel-I/O ports, and two 16-bit timer/counters. The IC also has an extra 4k bytes of ROM and an extra 128 bytes of RAM.

The core interfaces to two on-chip peripherals: a 2-channel DMA controller, and a multiprotocol serial channel, the Global Serial Channel or GSC. The DMA channels service both the GSC and the local serial channel. The DMA channels offload the communications overhead from the CPU and arbitrate for shared-memory resources via a hold and a hold-acknowledge bus-access control. The 83C152 interfaces to a serial backplane through open-collector drivers and receivers. To drive larger networks, it uses active drivers such as RS-485 transceivers (Fig 2).

Initially, the user code loads the network parameters, including the nodes' slot position, the interframe space (IFS), the slot time (ST), and the maximum number of slots for the network, into the GSC's internal registers. The controller permits 63 nodes on the network to participate in collision resolution. The network can also have an additional node that doesn't participate in collision resolution. The controller must assign slot number 0 to this additional node to prevent it from transmitting during the resolution phase. A data-gathering station would be a typical example of a node with slot number 0.

During the resolution phase, the slot numbers decrement from the maximum number of nodes on the network to slot number 1. The GSC loads the prepro-

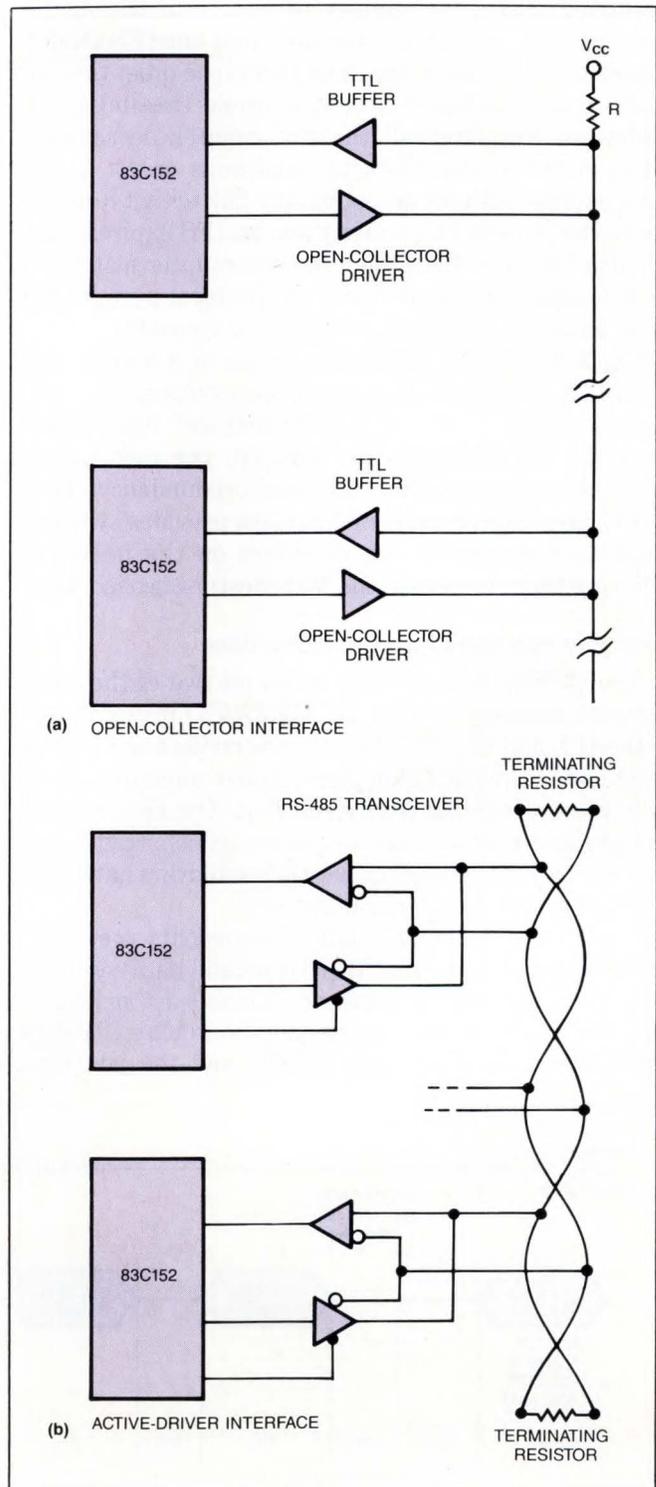


Fig 2—You can interface the 83C152 to a backplane using open-collector TTL buffers (a). The multiprotocol controller can also interface to larger networks via RS-485 transceivers (b).

During the resolution phase, the CSMA/DCR protocol assigns each node on the network a time slot for data transmission.

grammed maximum number of slots into the decrementing slot counter. It must then wait one IFS after it senses that the link is idle. The IFS is the quiet time on the network between successive frame transmissions. Following this interval, the slot counter decrements when either of the following conditions occur: A slot time expires without detecting any link activity, or the controller detects link activity and an IFS expires after the link becomes idle. When the slot counter matches a node's assigned slot number, the protocol permits the node assigned to that slot number to transmit.

Fig 3 depicts the resolution phase of a 6-node network. The CSMA/DCR protocol encapsulates data into frames similar to the CSMA/CD protocol: Each frame consists of a preamble bit pattern, the destination address, a message field, and cyclic-redundancy check (CRC) bits. The preamble bit pattern provides synchronization data for all the receivers on the network, allowing them to decode the Manchester-encoded data.

Now you can calculate the worst case

The CSMA/DCR protocol relies on two of the same network parameters that the CSMA/CD protocol uses—the IFS and the ST. The network nodes must wait at least one IFS while doing peer-to-peer communications and when recovering from a collision. The IFS also lets the physical medium recover after a transmitted frame and ensures that the other network sublayers have time to synchronize data for transmission.

The ST, or collision window, represents the maximum amount of time that there is invalid data resulting from a collision on the network. It is at least as long as the sum of the round-trip propagation delay (RPTD), the collision-detection time (CDT), and the jam time

DATA PROTOCOL	CSMA/DCR
DATA RATE	2M BPS
NETWORK LENGTH	500m
WORST-CASE ACCESS TIME	8 mSEC
INTERFRAME SPACING	96 BIT PERIODS = 48 μSEC
JAM TIME	32 BIT PERIODS = 16 μSEC
COLLISION-DETECTION TIME	1 BIT PERIOD = 0.5 μSEC
SLOT TIME	64 BIT PERIODS = 32 μSEC
ROUND-TRIP PROPAGATION DELAY	4.7 μSEC ≈ 10 BIT PERIODS

(JT). The RPTD is equal to twice the network length divided by the propagation speed (approximately 2.1×10^8 msec). The CDT is the time required for the circuitry to detect a collision. The JT lasts for either a 16 or a 32 bit period, depending on the number of CRC bits you program into the 83C152. The 83C152 detects a collision on every bit by verifying whether the transitions of the Manchester code are valid.

The 83C152 programs the IFS and the ST in multiples of the bit period. (A bit period is the inverse of the bit rate). The controller programs each IFS and ST independently; the maximum length of each can be 256 bit periods. During the resolution phase, the calculated worst-case access time is equal to the ST plus an IFS plus the sum of the maximum frame time allotted for each node and an IFS for each frame. In other words:

$$\text{Access Time(WC)} = \text{ST} + \text{IFS} + \sum(\text{Maximum Frame Time}(i) + \text{IFS}),$$

where the access time(WC) is the worst-case access

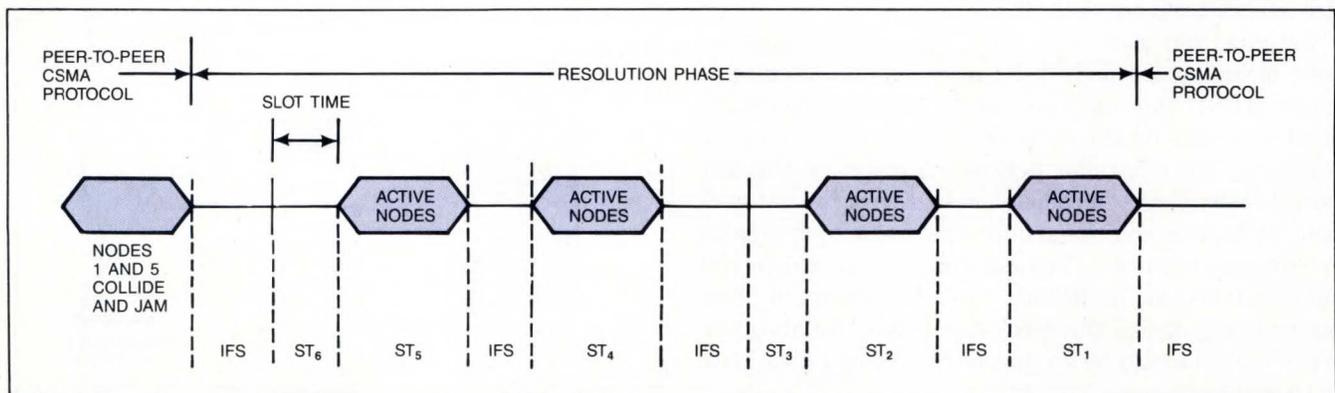


Fig 3—In this sample configuration of a 6-node network operating with the CSMA/DCR protocol, nodes 1 and 5 collide during peer-to-peer CSMA communications. When the network becomes idle, all the nodes on the network enter the resolution phase. After an interframe space (IFS), the slot counter decrements from ST₆ to ST₁. Active nodes transmit frames during their respective slot assignments.

time; the $ST > RTPD + CDT + JT$ as stated above; the sum takes into account all the nodes on the network; and the maximum frame time(i) is the maximum frame time of the *i*th node.

When all of the network nodes have the same maximum frame time size, the worst-case access time is

$$\text{Access Time(WC)} = ST + IFS + n \times (\text{Maximum Frame Time} + IFS),$$

where *n* is the number of nodes on the network. In both formulae, the frame time is equal to the number of bits in a frame divided by the bit rate.

An example will help to illustrate how the network parameters determine the access time. Consider the case of a 2M-bps control network that communicates

over a data link having 32 nodes. Two of the nodes have a maximum frame size of 500 bytes, which is typical of a motor controller. The remaining 30 nodes have maximum frame sizes of 20 bytes, which is typical for devices such as sensors and valves. For this sample network, and for the accompanying network parameters listed in **Table 1**, the worst-case access time is approximately 8 msec.

Because the CSMA/DCR protocol guarantees a maximum access time, you can adjust the network parameters for optimum operation. For the same 2M-bps network, **Fig 4** shows the variations in worst-case access time that result when you manipulate two network parameters—the maximum frame size and the number of network nodes. Curves for other network parameters are similar, and therefore you can custom-

LISTING 1—SAMPLE CODE FOR THE 83C152's GSC

```

MOV GMOD, #7CH           ; select CSMA protocol, Manchester
                          ; encoding, 32-bit preamble, 32-bit
                          ; Autodin CRC, alternate back-off,
                          ; transmitter operation with internal baud
                          ; generator and 16-bit addressing.
CLR DMA
MOV BAUD, #00H          ; select GSC operation without DMA
                          ; set baud rate to 2 Mbps for 16 MHz
                          ; clock
ANL PCON, #0F7H        ; select receiver operation with
                          ; internal baud generator
MOV ADRO, #05H         ; set first station address to 1005H
MOV ADR1, #10H
MOV ADR2, #06H         ; set second station address to 2006H
MOV ADR3, #20H
MOV IFS, #060H         ; set Interframe Spacing to 96 bit times
MOV SLOTTM, #40H       ; set Slot Time to 64 bit times
MOV TCDCNT, #20H      ; set maximum number of stations to 32
MOV PRBS, #0FFH       ; freeze the Pseudo-Random Binary
                          ; Sequence generator for proper DCR
                          ; operation
MOV MYSLOT, #0C5H     ; select station slot assignment to 5,
                          ; select DCR mode and DC-type jam.

```

Depending on the application, the transmitter and the receiver can be enabled when required using the following instructions:

```

SETB TEN                ; enable the transmitter
SETB GREN              ; enable the receiver

```

ize a network to meet a specified worst-case access time.

At first glance, you might think that you could tailor a network so that the nodes with the higher slot numbers would have lower access times than the nodes with lower slot numbers. After all, the slot counter decrements from a high count to a lower one. Consider the following worst-case scenario, though. The network is in a resolution phase and the slot counter is at a count equal to n . At this time, say, the node with an assigned slot number of $n+1$ receives an interrupt and wants to

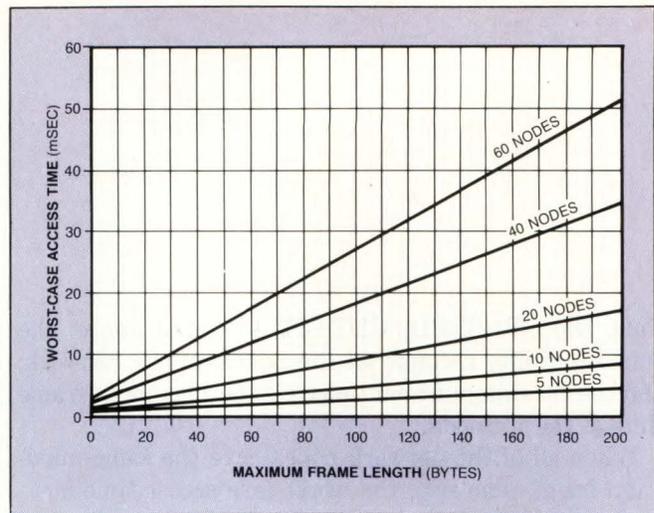


Fig 4—This graph plots the worst-case access time for a 2M-bps CSMA/DCR network having the same length, interframe space, and slot time as the one in Fig 3. As you can see, the worst-case access time varies according to the number of nodes and the maximum allotted frame length per node.

LISTING 2—SAMPLE CODE FOR THE 83C152's DMA CHANNELS

```

SETB DMA           ; select DMA to service transmitter (DMA
MOV DCON0, #88H    ; is a bit in TSTAT register)
                   ; select DMA channel 0 for transmitter,
                   ; DMA demand mode by serial channel and
                   ; external memory as source. The GO bit
                   ; is not set yet.
MOV DCON1, #29H    ; select DMA channel 1 for receiver, DMA
                   ; demand mode by serial channel and
                   ; external memory as destination. The GO
                   ; bit is set.
MOV SARH0, #10H    ; Source for channel 0 is memory
                   ; starting at
MOV SARL0, #00H    ; address 1000H
MOV DARH0, #00H    ; Destination for channel 0 is Transmit
                   ; FIFO
MOV DARL0, #85H    ; Transmit a count of 10 bytes
MOV BCRH0, #00H    ; Source for channel 1 is Receive FIFO
MOV BCRL0, #0AH    ; Destination for channel 1 is memory
MOV SARH1, #00H    ; starting at address 2000H
MOV SARL1, #0F4H   ; receive up to 64 bytes
MOV DARH1, #20H
MOV DARL1, #00H
MOV BCRH1, #00H
MOV BCRL1, #40H

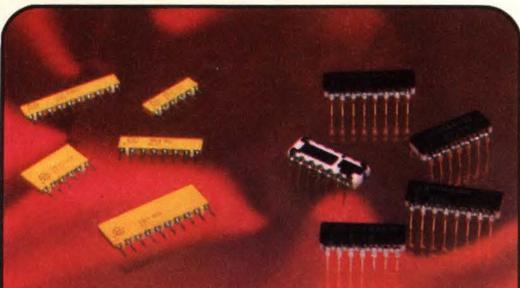
```

Depending on the application, the transmitter and the receiver are enabled when required using the following instructions:

```

SETB TEN          ; enable the transmitter and then set
                   ; the GO
ORL DCON0, #01H   ; bit for the DMA to start
                   ; transmission.
SETB GREN         ; enable the receiver

```



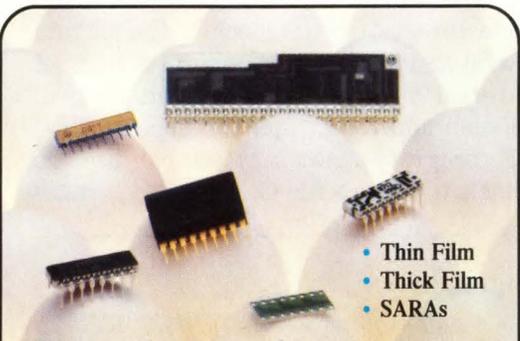
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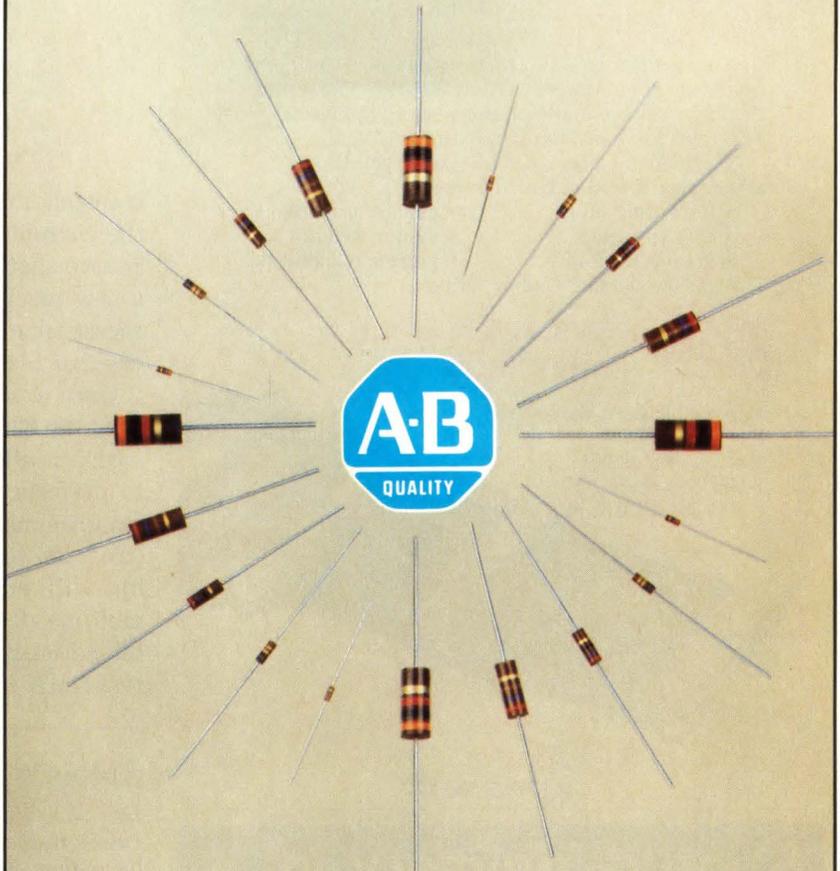
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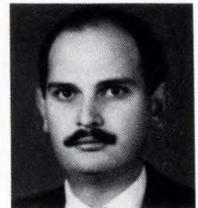
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transmit immediately. Before the node can transmit, the current resolution phase must count out, and if by chance another collision occurs at the end of that phase, a new resolution phase must begin to decrement. The access time for the n+1 node would then be the worst-case calculated value.

Once you've determined your network's configuration, the 83C152 lets you establish network parameters easily. **Listing 1** shows the code that initializes the GSC to perform the DCR operation for a particular node. Programmable features of the GSC include the bit rate (from 2M bps with an internal baud generator to 2.5M bps with an external clock), the preamble bit pattern, multiple destination addresses, and the type of CRC bits. **Listing 2's** program shows how you can use the two DMA channels to service the GSC. **EDN**

Author's biography

Deif N Atallah is a staff engineer with Intel's Embedded Operation Group in Chandler, AZ. He is currently responsible for the product architecture of 32-bit embedded controllers. He obtained his BSEE from Alexandria University, Egypt, and his MSEE degree from Penn State University. Deif enjoys world traveling, camping, and photography.



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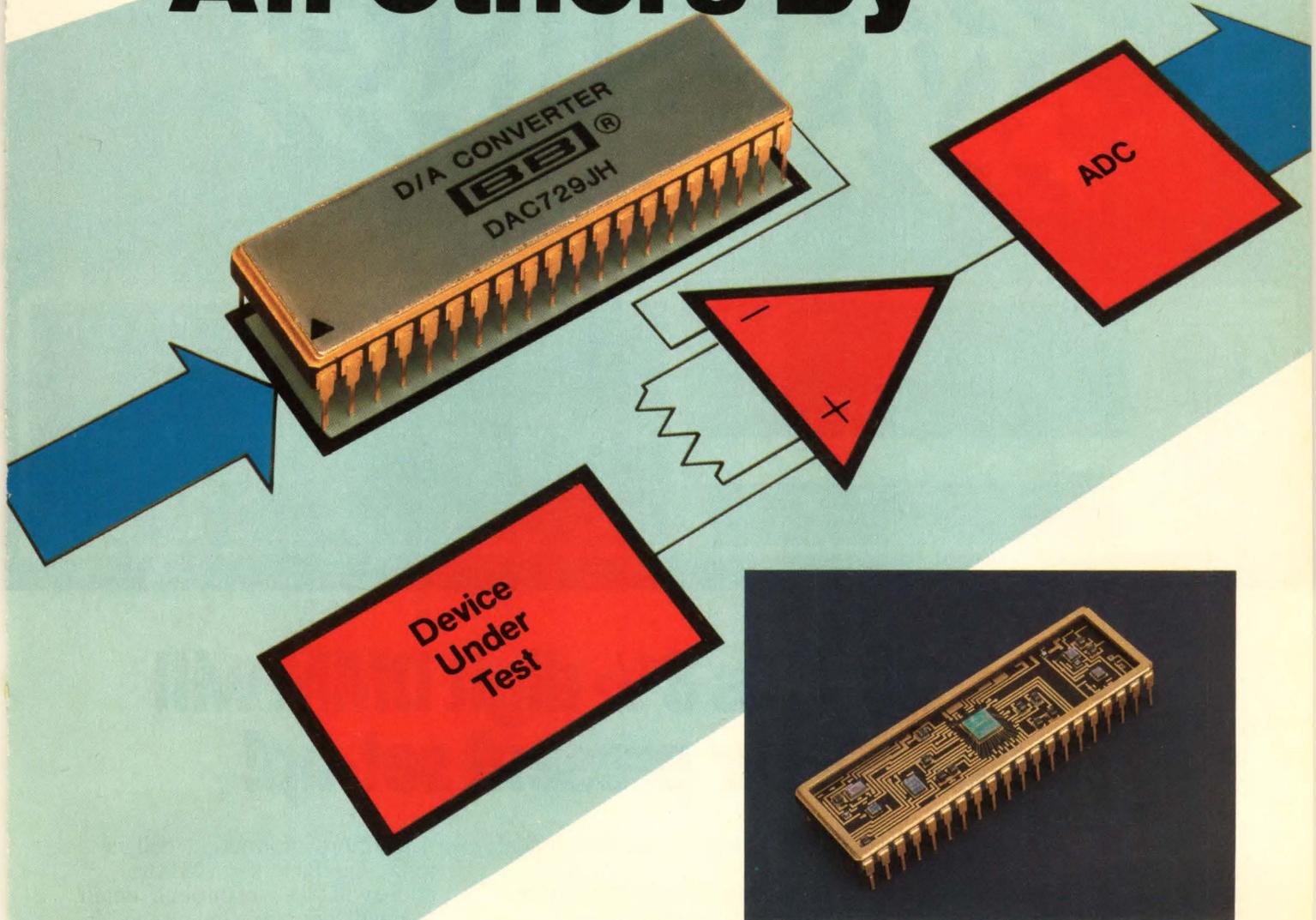
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Testability is crucial in PLD-circuit design

Compared with standard logic parts, PLDs tend to have higher defect rates and require a larger investment in test-program development. As a result, engineers must make testability a prime design goal to ensure that the final product can be manufactured and tested economically.

Peter de Bruyn Kops, *Anvil Software*

In increasing numbers over the past few years, board designers have felt the lure of PLDs. Two basic reasons underlie the devices' popularity. One, PLDs are much more powerful than 7400 Series TTL parts and, two, they are much easier to troubleshoot than gate arrays. A logic error found in a PLD prototype board in the morning can often be fixed by that afternoon—something that gate-array users can only dream of. Today, it's not uncommon for a board to contain 50 or more PLDs.

PLDs do require more test-development effort than standard TTL parts, however, and the reason for this is also quite basic. In standard-logic design, the test department creates a test program, puts it in a library, and then reuses it many times over the years. The test

engineers have easy access to all the standard logic-test programs they need. A PLD test program, in contrast, is not reusable. A 16L8 PLD design test program, for example, is good for only one particular design; any other 16L8 design will require a different test program.

The rationale for testability

To make it worthwhile to design with PLDs, therefore, you have to design with testability in mind and ensure that the test department can test your circuits within a reasonable length of time and for a reasonable expenditure. A PLD is not very testable if it requires a million dollar tester that holds 1 million vectors. A PLD is also not very testable if it takes a genius three weeks to develop an adequate test. For a board with 50 PLDs, a realistic prediction of test-development time is less than a day per device—except in the highest volume manufacturing operations. Simply stated, the effectiveness of the test engineers is inversely related to the sophistication of your design.

For the purposes of this article, assume that your test engineers have been blessed with good documentation and an automatic test-vector generator (ATG) that can create tests for a variety of combinatorial and sequential PLD designs. By comparing the following untestable or difficult-to-test circuits with their enhanced-for-testability counterparts, you will achieve an understanding of how your design practices will hinder or help subsequent testing of the devices. If you decide

A designer's interests are best served when the test engineers have good documentation and a state-of-the-art automatic test generator.

to heed these design tips, you'll decrease manufacturing time and costs and shorten test-development time—and you may also win some friends in the test department.

Oscillator circuits create problems

Oscillators are easy to create with a PLD (Fig 1a), but testing a PLD-based oscillator isn't so straightforward. Whereas PLD testers can readily strobe settled states, oscillator circuits typically require testing of their test frequency and duty cycle. At best, a PLD tester will find such a task difficult, and for many PLD testers it's impossible.

An ATG cannot usually handle an oscillator. Even worse, the oscillator may interfere with the automatic-test generation for other parts of the design. If you want to develop a PLD-based oscillator, you should add an Enable signal so that you can turn the oscillator off (i3 in Fig 1b). Optimally, the Enable signal should be on a dedicated pin. In addition, try to add extra logic, which will allow you to stabilize the oscillator output in both the one and the zero states. This capability will expedite parametric testing.

PLD-based pulse, or glitch, generators (Fig 2a) are just as troublesome to develop tests for as are oscillators. Without proper communication between the design and test departments, the test engineer will have no way of knowing whether the detected signal transition is a legitimate generator output or a system glitch.

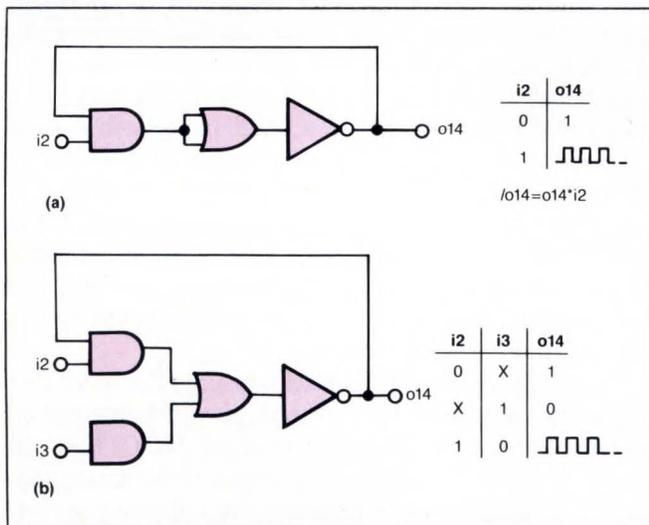


Fig 1—Although it's easy to create oscillators with PLDs (a), the testers commonly used for PLDs cannot easily evaluate the performance of an oscillator. If you redesign the circuit and add an Enable signal (i3), the oscillator can be turned off during testing (b).

If the pulse is indeed a legitimate output, the test engineer will have to develop a special test program and use a more expensive tester to determine that the pulse does indeed occur and that it has the right width.

ATGs typically cannot accommodate glitch generators. And again, the glitch generator may interfere with the automatic-test generation for the rest of the board. As before, try to include additional logic (Fig 2b) that will stabilize the generator output (to both the one and the zero states) to facilitate parametric testing.

Meeting the demands of in-circuit testers

If your PLD design relies on feeding outputs back to inputs on the circuit board, watch out that you don't complicate in-circuit board testing. Depending on how the PLD connects to other devices on the board, external PLD feedback may compound the problem of testing the rest of the board.

Testing the PLD itself may also prove difficult, depending on the ATG's software and the source of any other vectors. If the ATG assumes that two pins can

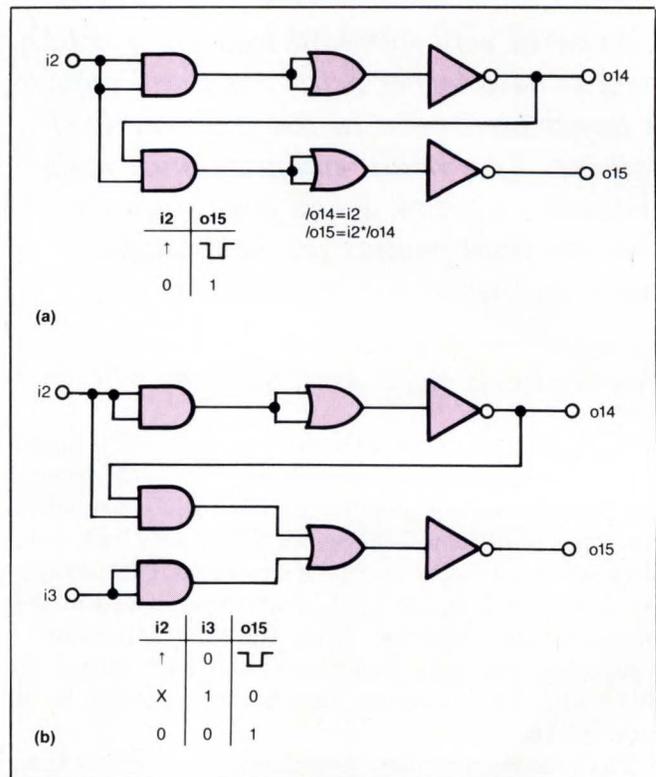


Fig 2—Automatic test-vector generators (ATGs) usually are incapable of testing pulse generators (a). The pulse generator can also hinder the ATG's capability to test other circuitry on the board. By adding logic (b), you can stabilize the generator's output.

move independently, the in-circuit board tester may not be able to use those vectors. Even if the ATG software can abide by the constraint of having two pins tied together, this restriction is still a hassle for the test engineer because it represents one more thing to remember and one more chance to make a mistake. If you need feedback, try to use a PLD with adequate internal feedback paths.

Most PLD-based designs seem to always hard-wire any 3-state outputs in the on condition, thereby creating problems for in-circuit test systems (Fig 3a). A test engineer writing an in-circuit board test program will normally prefer to turn a 3-state output off and drive that output point with the tester. If the output is always on, the test engineer may need to overdrive the pin. Overdriving complicates the test and may make the test more difficult to debug. You can circumvent these problems by controlling all 3-state outputs with an Enable signal (i9 in Fig 3b).

Watch out for race conditions

The exception to this rule are memory elements with 3-state outputs. Memory elements created by feedback around a 3-state type of combinatorial output introduce

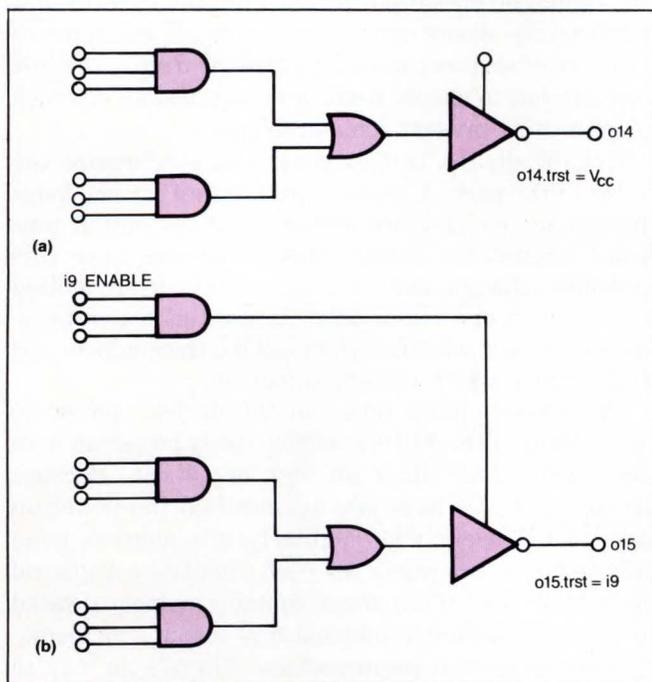


Fig 3—The majority of PLD-based designs pose problems for in-circuit testing (a). You must control 3-state outputs with an Enable pin if system performance is going to be evaluated using in-circuit testing techniques (b).

some special testing subtleties (Fig 4a). This type of design may necessitate that both the tester and the PLD be simultaneously active in order to reliably latch data. Referring to pin o15, when the test vector starts, i2 and i9 are low, and the tester is driving o15. When i9 goes high, the device output will turn on. The driver on a typical PLD tester will stay on for the entire test vector, which means that the tester and the chip will both be striving to establish the same output state.

During functional testing and with bipolar parts, this dual-drive condition isn't usually a problem, but it may prove troublesome with some CMOS devices. Moreover, even some good parts might fail if the tester performs an input-leakage test on that pin for that test vector. Many PLD testers automatically perform input-leakage tests when they initially drive a pin high or low.

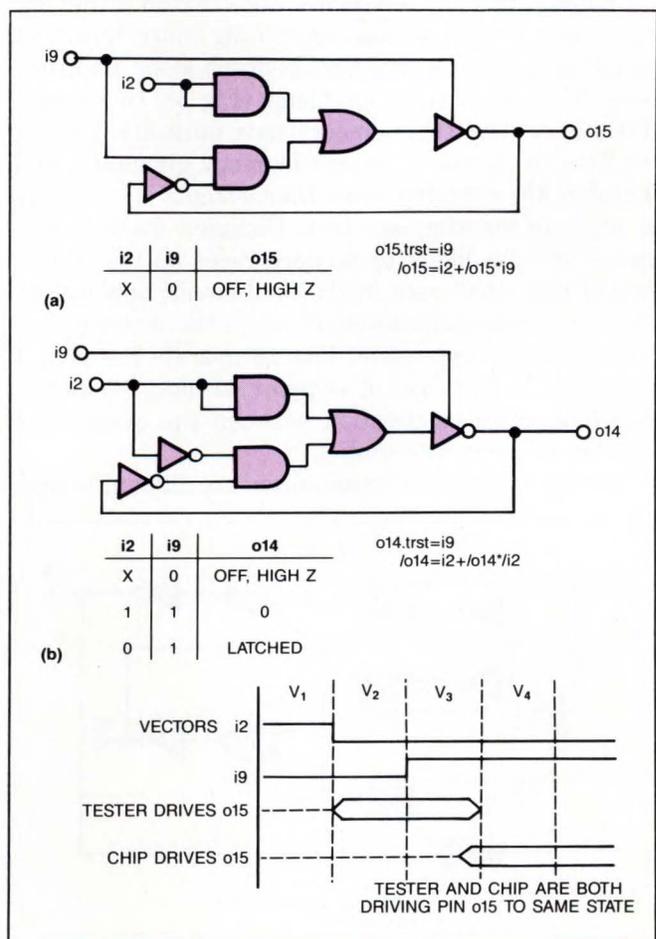


Fig 4—When you create a memory element by using feedback around a 3-state type of combinatorial output (a), you introduce special testing subtleties. If you remove i9 from the feedback path (b), the circuit will be much more testable.

A memory element created by feedback around a 3-state type of combinatorial output introduces some special testing subtleties.

If the PLD is driving the pin at this time, the test engineer will have to manually modify the test.

To avoid the simultaneous-drive situation, the test engineer can write the vectors so that they turn the tester driver on o15 off at the same time that i9 goes high. On most PLD testers, this action causes a race condition and may produce intermittent failures of good parts. If the engineer uses an expensive tester, it will turn the chip drive to o15 off a specified number of nanoseconds after i9 goes high and eliminate the race problem, but it will also require that the test engineer take special effort to modify the test program.

To make the circuit in Fig 4a more testable, you can modify the design to remove i9 from the feedback path (Fig 4b). Once you make this change, the 3-state operation is independent of memory operation.

Complex memory elements are created either by building a feedback loop containing more than one output or by overlapping two feedback loops, and they pose their own peculiar problems (Fig 5). In general, ATGs (as well as test engineers) have difficulty figuring out how to operate complex memory elements, and therefore the circuitry inside the elements is less likely to undergo an adequate test. Complex memory elements are also likely to produce races on the tester, even if they don't race in the final circuit application. These race conditions develop because the vector writer does not fully understand how to operate the circuit correctly. In the case of complex memory elements, therefore, close cooperation between the design and test departments is essential.

Designs that cannot be initialized are difficult to test,

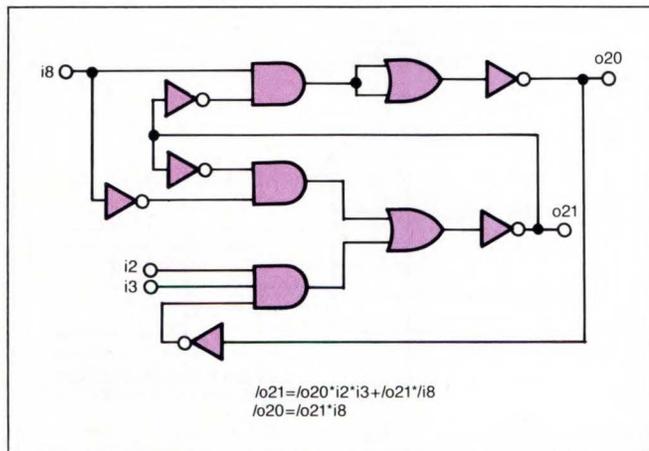


Fig 5—Complex memory elements are tough to test thoroughly because it's difficult for the test engineer—and the automatic test generator—to figure out how to operate the elements.

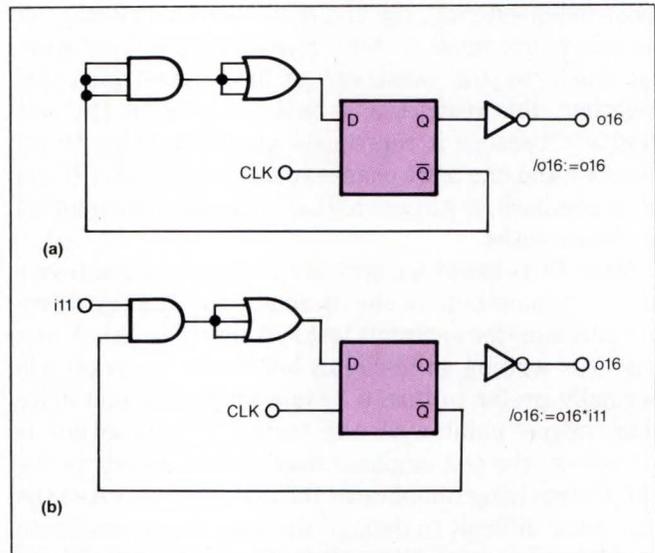


Fig 6—Although circuits that cannot be initialized are fairly common, they are very difficult to characterize (a). The modified flip-flop circuit of b is much easier to test.

but unfortunately such circuits constitute 10%—or more—of existing PLD designs. The toggle flip-flop of Fig 6a is a good example of a simple, common circuit that cannot be initialized. A test program needs to first initialize the device and then test it. If an ordinary sequence of vectors cannot initialize the device, the test engineer has to choose from three options, all of which unfortunately present some problems.

First of all, the test engineer can synchronize the tester to the part. A typical synchronizing scheme loops the test on one or more vectors until the output pins match predefined states. Not all testers have this capability, though, and some testers that do are limited to looping on one vector only. To use this match mode (as some tester manufacturers call it), the engineer has to determine which vectors to loop on.

The second option relies on the device's power-up state. Many of the PLDs available today power-up with the register bits either all high or all low. Because vendors of PLDs have not standardized the power-up state, PLD users who regularly mix sources need different test programs for each vendor—a logistical nightmare. Also, if the device contains memory created by feedback around a combinatorial output, the memory element cannot be initialized: There's no way to reliably know its power-up state. Another problem will surface if the device or the tester requires substantial time (100 msec or more) to power-down and power-up the device. A test that checks parameters (dc or ac) has



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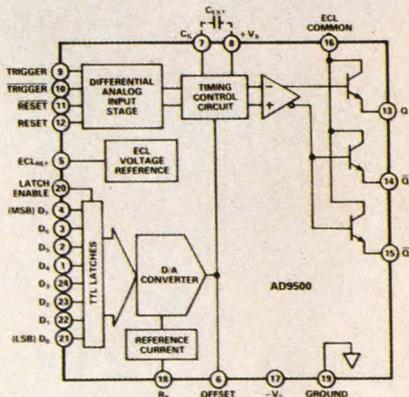
PRODUCT DESCRIPTION

The AD9500 is a digitally programmable delay generator which includes virtually all the circuits needed for generating time delays for digital pulses. It provides 256 programmed delays in a user-specified full scale range which can be varied from more than 100µs to as little as 2.5ns. On the latter scale, it can resolve increments as small as 10 picoseconds.

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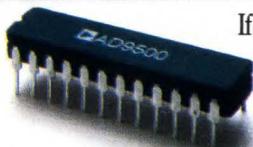


AD9500 Functional Block Diagram

PRODUCT HIGHLIGHTS

1. The AD9500 delay generator is an extremely versatile but remarkable, easy-to-use timing device. A few basic configurations can be expanded and extended into multiple applications.
2. Accurate control of pulse timing is critical for all digital electronic systems, and many systems require that delays be controlled digitally. Until now, the majority of systems using that technique used discrete LSI devices which may consume up to one watt or more of power. The AD9500 performs the same function with 300mW of power.
3. Like a high speed counter, the AD9500 can be programmed with a binary digital word. This makes the unit a variable delay device, in effect, a digital-to-time converter (DTC). The digital input word scales the time reference of the AD9500 in essentially the same way a digital word scales voltage or current references in a DAC.

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And the AD9500 comes in the standard industrial temperature range of -25°C to +85°C, or an extended range of -55°C to +125°C.

In addition, the AD9500 is ECL compatible and usable with analog as well as TTL input levels. These features make it ideal for adjusting cable delays in multichannel ATE systems, or phase correction and timing generation in radar/ECM.

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to run the vectors many times and therefore will need the power-up state to initialize each of these vector runs.

The third option is preloading. Many of today's PLDs support a preload feature that allows the test engineer to apply special voltages (10 to 13V typically) to some output pins. Preloading temporarily converts the output pins to input pins to directly set the internal-register states. The test engineer will encounter several problems with preloading: Each PLD manufacturer has a different protocol; many testers cannot support preload voltages; preloading is incompatible with in-circuit testing because the high voltages can damage other parts; and parametric measurements often are not reliable immediately after preloading.

You can make some of these problems tolerable for the test department if you set the initial state by preloading only on the first vector. However, most test departments prefer not to use preloading for initialization. Some ATG packages will accept starting-state data and generate the test starting from that point. These types of packages allow the test engineer to obtain some valid test data, but they also mean that more vectors have to be generated and they also necessitate more computer time. The increased number of vectors may increase test times, or it may reduce test coverage if the tester cannot hold that many vectors.

The best way to circumvent all of the above problems and improve the testability of a design that can't be initialized is to devote an unused input or combination of inputs to load the initial state (Fig 6b).

Difficult-to-initialize designs also pose problems when it comes time to create test vectors, but they do not cause problems with the tester itself. For example, the following specification describes a particularly difficult-to-initialize design: "When you clock the circuit 10 times, it will wind up in a known state, but the states prior to the tenth clock will be unknown." This type of circuit, where a combination of unknown states is supposed to produce a known state on another gate, mainly causes problems with logic simulators. You can eliminate testability problems resulting from difficult-to-initialize designs in the same manner as circuits that cannot be initialized at all.

Sequentially deep designs cause test difficulties for two reasons. They require a large number of test vectors, and they stipulate that either the test engineer or the ATG software spend a lot of time developing such vectors. A 10-bit counter that can be cleared and then counts up is a good example of a sequentially deep

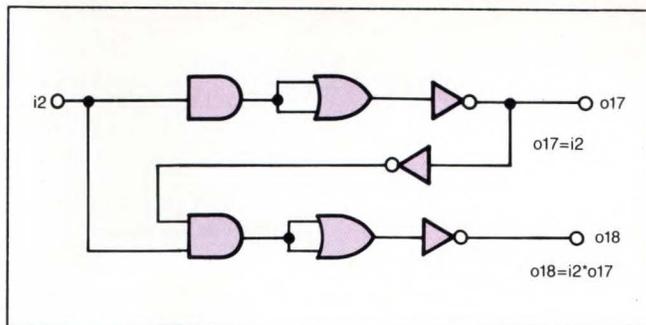


Fig 7—Circuit designers can, with good reason, design in time-sensitive redundancies to achieve a fault-tolerant design. Such designs can prove problematical for test engineers.

design. If a test engineer has to evaluate this part with a tester that is capable of holding only 512 vectors, test coverage will suffer. From the test department's point of view, the best solution is to modify the counter design so that it can be loaded with an arbitrary state. The ATG will then be capable of adequately testing it.

On some testers, sequentially deep designs can also limit the accuracy of ac measurements. These types of testers are most accurate when the transition they must measure occurs within a few vectors of the initialization point. In the 10-bit counter example from above, transitions in the high-order bits occur hundreds of vectors after initialization, which reduces timing accuracy. In a loadable 10-bit counter, these testers can accurately evaluate the transition from count 511 to count 512 with a few vectors by loading count 511 and clocking once.

Watch out for redundancies

Time-sensitive redundancies are another cause of difficulties in testing because test generators and test engineers do not know if they should test the time-sensitive behavior. In ordinary cases, faults in the redundant logic are undetectable (that is, they are faults that cannot affect circuit operation), and some ATG packages can automatically filter them out (Fig 7). Obviously, if the fault can't affect circuit operation, there's no need to test for it.

These fault-tolerant circuits can prove very beneficial in some applications. If you choose to use such a circuit in your next PLD design, make sure you document the redundancy so the test engineer knows that he doesn't have to struggle with it.

EDN

Author's biography

Peter de Bruyn Kops is director of engineering at Anvil Software (Nashua, NH). In this position, he is responsible for developing programmable-logic test generators. Peter holds a Bachelor of Arts degree and a Masters in Science degree from Harvard College.



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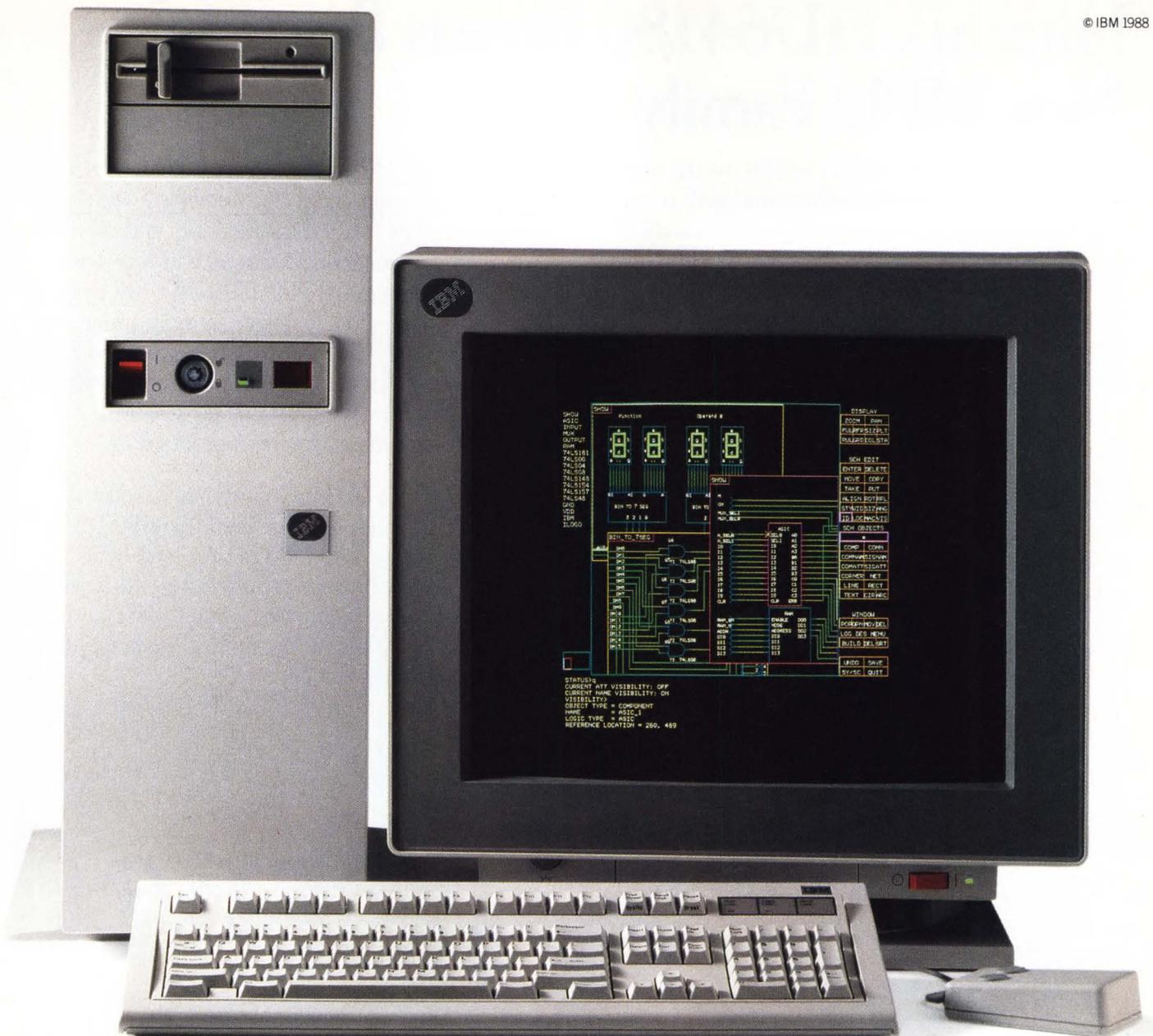
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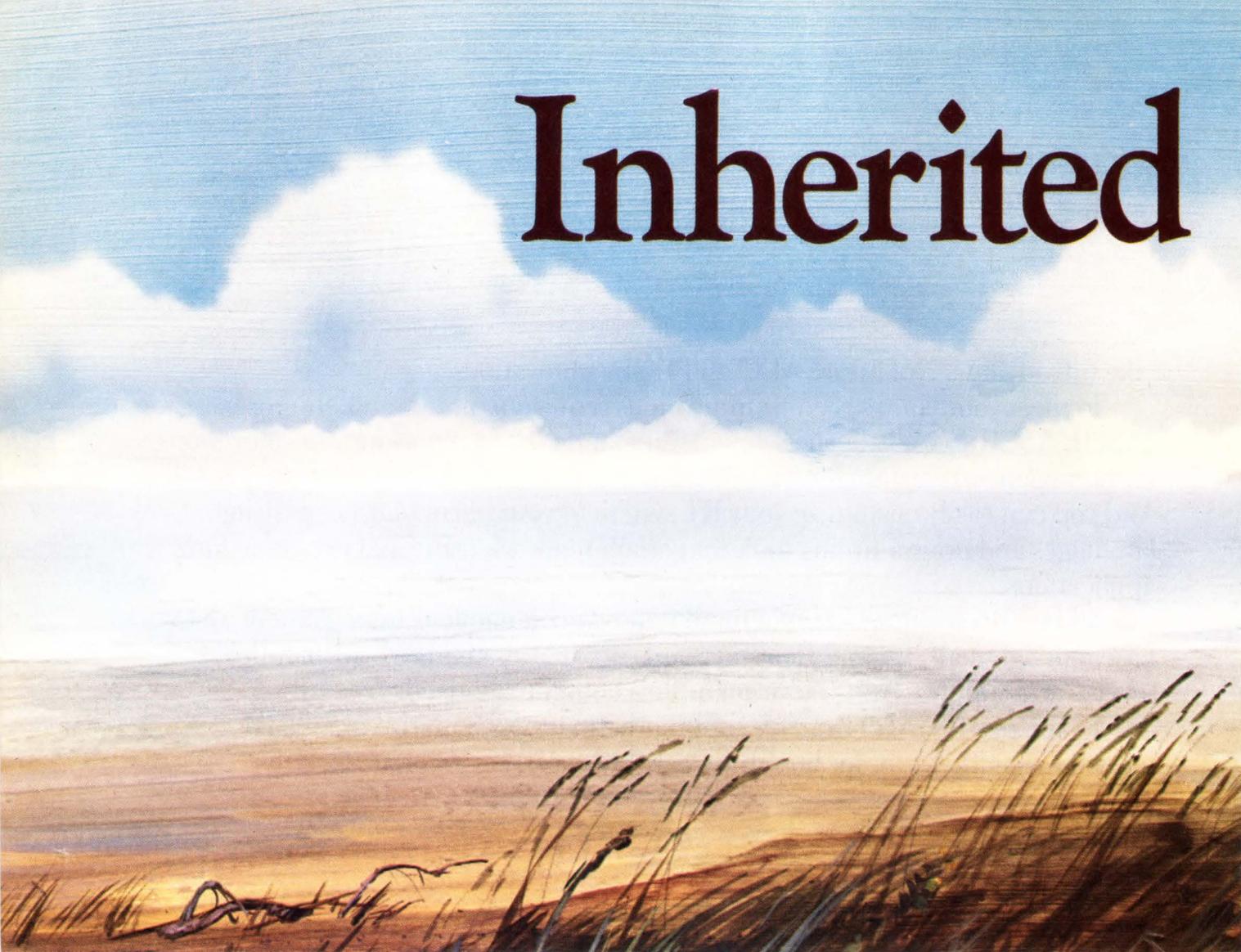
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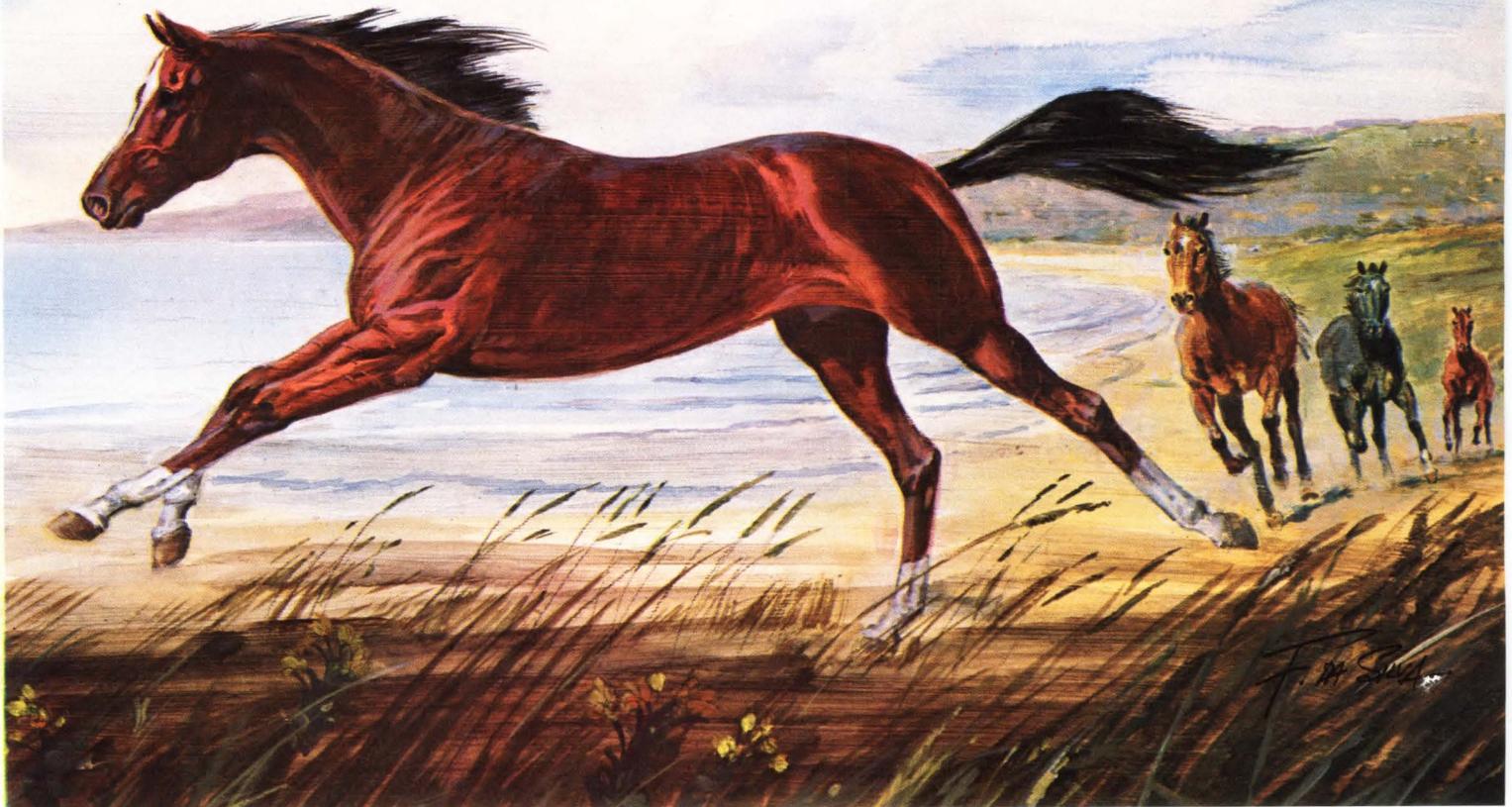
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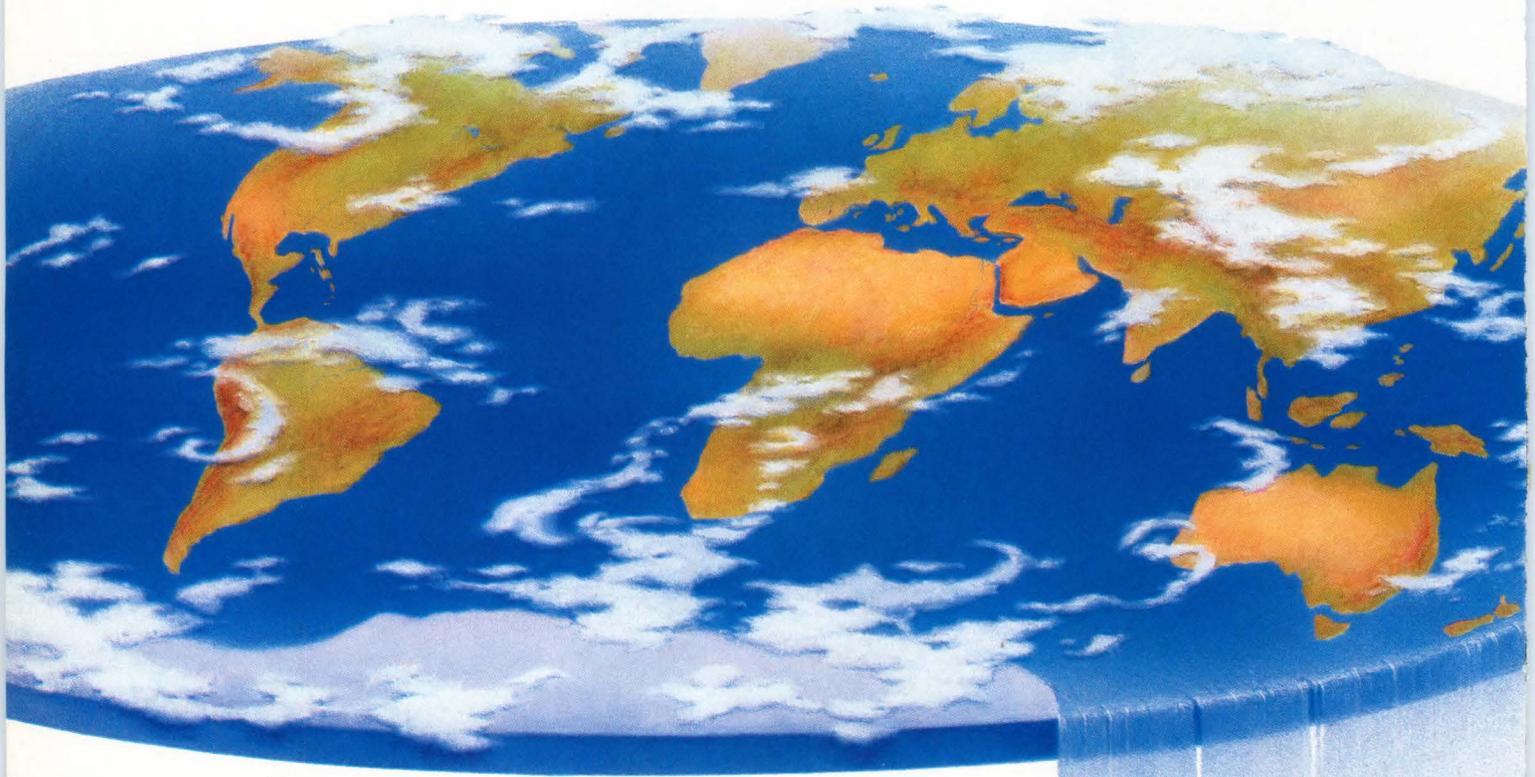
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CIRCLE NO 137

Retargetable tools ease microprogramming of SIMD processors

You can improve your single-instruction, multiple-data processors dramatically by using effective organization and management techniques. Retargetable tool sets can help you program these massively concurrent SIMD processors conveniently, reliably, and inexpensively.

Robert A Mueller and Daniel R Benua,
Quantitative Technology Corp

One way to create programmable parallel computer systems is to use wide-instruction-word, single-instruction, multiple-data (SIMD) processors. But machines with concurrently functioning units require programs that are far more complex than similar programs for conventional sequential computers or microprocessors. Programming at the microcode level is therefore tedious and exacting—it calls for a special combination of talent and patience that not many programmers possess. Until recently, the only alternative was to lower performance and thus create a more manageable machine for the microprogrammers. However, using SIMD architectures is now a feasible option because automated tools for implementing microcode within

those architectures are starting to appear, and these tools offer new methods for resolving the programming difficulties.

SIMD architectures have become the basis of most contemporary high-performance graphics and digital-signal-processing (DSP) systems. Such systems generally consist of custom, application-oriented processors built from a mixture of high-speed arithmetic, floating-point, DSP, and application-specific integrated circuits (ASIC), that provide excellent cost/performance value. In addition, it's possible to design wide-instruction-word SIMD processors in such a way that you can program them in a high-level language (HLL). This advantage becomes significant when optimizing compilers are available to translate HLL programs into *microcode* (for definitions of all the italicized words in this article, see **box**, "Microcode terms decoded").

The wide instruction words used in SIMD processors (from 64 to more than 1000 bits) can be extremely difficult to program efficiently. The reason is that every instruction word contains numerous fields, and every field controls different hardware elements. You must therefore program each field for each clock cycle of an instruction. Furthermore, because you can *pipeline* many hardware elements, one operation can take several instruction cycles to complete, and an operation's later stages may take place concurrently with the early stages of the next operation.

If an SIMD architecture must support large applica-

Programming at the microcode level requires a special combination of talent and patience that few programmers possess.

tion *microprograms*, the hardware designer can take advantage of some powerful chip families to quickly design systems that, because of extensive concurrency and pipelining, can perform exceptionally well. On the other hand, developing software for such an architecture is difficult. In the first place, microprograms are generally not written until after the design is set in silicon, so any early prediction of such a system's performance when running microprograms is just about impossible. Thus the hardware designer must speculate about the software needs, and major design flaws can go unnoticed until it's too late to rectify them. When you add to this the fact that each application program may require 100,000 or more *microinstructions* operating on such an architecture, the intractability of programming those applications is clear.

In fact, most vendors estimate that if traditional microcode development tools are used, writing and debugging microcode on wide-word, SIMD architectures costs between \$1 and \$2 per bit. Thus, an application requiring 100,000 microinstructions, where each microinstruction is 100 bits wide, might cost between \$10 million and \$20 million to develop.

In order to eliminate current design problems without sacrificing a high level of performance, a microcode development system should feature four basic characteristics:

- You should be able to easily *retarget* the tools for different architectures, including hypothetical machines. An automated system is inadequate if it works for only one design, or even for a limited number of designs. Designers must be able to

Microcode terms decoded

Code compaction—The process of scheduling a sequential list of straight-line micro-operations to execute concurrently on a parallel processing machine, without violating resource limitations or data dependencies.

Configure—To adapt retargetable program-development tools for a specific hardware architecture. Configuring involves writing a configuration file and processing it for use by the development tools.

Configuration file—A text file containing descriptions of the hardware and the properties of a target machine. This information is needed to adapt the retargetable program-development tools to a specific hardware architecture. The file is used as input to a configuration program that performs the adaptation of individual tools.

Data dependence—A relationship that involves the reliance of one operation on the data of another. An operation X is data-

dependent on operation Y, if Y writes data that X reads.

Horizontal machine—A machine architecture in which independently programmable operations can occur simultaneously as well as sequentially. Such a machine may have multiple concurrent functional units but only a single program-sequence control unit.

Local compaction—Code compaction.

Microcode—A general term for the machine instructions that directly control the hardware resources of a machine.

Microinstruction (MI)—A source-level assembly-language instruction made up of zero or more micro-operations and corresponding to an object record.

Micro-operation—A primitive operation that controls specific hardware resources of the machine.

Microprogram—A sequence of microinstructions that together perform a specific function. A

microprogram can exist at three levels: source, object, and loadable.

Pipelining—The process of combining operations in such a manner that successive operations are initiated before the first operation is completed. The number of cycle transitions that occur before completion of the first operation defines the depth of the pipeline.

Retarget—To change, or reconfigure, a program for an architecture that is different from the one you last worked on.

Software pipelining—A program-optimization technique that pipelines the operations of a program loop.

Target machine—The computer system for which microcode is written.

Trace scheduling—An optimization that speeds up the program paths that execute most frequently in a microprogram.

LISTING 1—C PROGRAM FOR A 4x4 MATRIX PRODUCT

```
int a[4][4];
int b[4][4];
int c[4][4];

main()
{ int i,j,k;

  for(i=0 ; i<4 ; i++)
    for(j=0 ; j<4 ; j++)
    {
      c[i][j] = 0;
      for(k=0 ; k<4 ; k++)
        c[i][j] = a[i][k]*b[k][j]+c[i][j];
    }
}
```

explore new possibilities in order to make use of the most advanced technology. Limitations on system configuration hamper both their creativity and their ability to exploit new technology.

- You should be able to write microcode in a high-level language. An automated system must allow the reuse of existing microcode on new architectures. Reusability requires that microcode be written in a high-level, machine-independent language. A language that is appropriate, popular, and standardized has added value for the programmer.
- It should automatically (or at least semiautomatically) optimize microcode to effectively exploit concurrency and pipelines. New hardware technology is cost effective only if programming techniques are capable of yielding the full performance potential of the resulting system. Hand coding requires programmers who are both experienced with optimization methods and have an expert knowledge of the target hardware. Even with such expert programmers, hand coding for wide-word SIMD processors is, at best, very time-consuming and expensive. For complex, highly concurrent machines, hand coding can be too difficult for even experts to manage effectively and reliably.
- It should readily provide architectural performance profiles that reveal bottlenecks and other design flaws. The designer must be able to assess the effectiveness of an architecture, when running a representative benchmark suite of microprograms, by means of execution profiles. To obtain such execution profiles, the development system must include a retargetable simulator.

Taking these characteristics into account, let's see what tools you need to automate both the SIMD processor design and the microcode development for such processors. Keep in mind that all of the tools should be retargetable—that is, you are able to adapt them to any architecture, provided that a description of that architecture and its programming rules is available in a *configuration file*.

First of all you need an assembler and a linker that you can easily adapt to various symbolic assembly languages, including those for expressing horizontal instructions and pipelined operations.

Next, to reduce programming time and cost, and to facilitate the reuse of existing code, you need a compiler for a high-level systems-programming language like C. The HLL compiler should generate code for the selected assembly language. To exploit the low-level, fine-grain parallelism, it's critical that you have an optimizer that trace-schedules programs, pipelined loops, and scheduled concurrent operations, both for handwritten and compiled code. HLL compilers can have some built-in optimizing functions, but it's very likely you'll need a separate optimizer tool for fine-tuning the source code generated by the compiler.

A symbolic debugger is also essential, preferably one that shows you the HLL source code as well as the machine code that's currently executing. Debugging a complex single-thread program is often difficult without a source-level debugger—the mind boggles at the thought of debugging parallel or pipelined operations without this aid.

And finally, you need a simulator, not only to test and profile new programs, but to evaluate the performance of the proposed system even before it's committed to silicon.

Powerful chip families allow you to quickly specify systems that can use concurrency and pipelining extensively to achieve high performance.

$$\begin{pmatrix} C_{11} & C_{12} & C_{13} & C_{14} \\ C_{21} & C_{22} & C_{23} & C_{24} \\ C_{31} & C_{32} & C_{33} & C_{34} \\ C_{41} & C_{42} & C_{43} & C_{44} \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} & a_{13} & a_{14} \\ a_{21} & a_{22} & a_{23} & a_{24} \\ a_{31} & a_{32} & a_{33} & a_{34} \\ a_{41} & a_{42} & a_{43} & a_{44} \end{pmatrix} \cdot \begin{pmatrix} b_{11} & b_{12} & b_{13} & b_{14} \\ b_{21} & b_{22} & b_{23} & b_{24} \\ b_{31} & b_{32} & b_{33} & b_{34} \\ b_{41} & b_{42} & b_{43} & b_{44} \end{pmatrix}$$

Fig 1—This general form of a 4x4 matrix multiplication uses the standard approach of cross-product computations. It requires 64 additions and 64 multiplications.

A tool set that includes all these programs offers a new approach to design. For example, you can develop large benchmarks of machine-independent C programs in advance of, or concurrently with, the processor

design. First, you *configure* the entire tool set for that architecture by building a configuration file from which each tool can extract details of the machine-specific properties of the target architecture. Once you have configured the tool set for your design, you can begin the compilation, optimization, and assembly of system and application programs.

To obtain performance profiles and analysis, you run the compiled programs under the simulator. When design flaws or opportunities for improvement crop up, you can make changes and update the configuration file accordingly; the feedback loop then repeats. In situations where you need to compare and contrast alterna-

An integrated set of tools for microcode

The Software Foundry from Quantitative Technology Corporation (QTC) is an integrated family of software development tools that can easily be re-targeted by designers of custom high-speed processors for different architectures. The family consists of six tools.

C compiler

The retargetable SF/C Compiler compiles C source code directly into optimized microcode. It performs the first of two stages of optimization: coarse-grain transformations of the programmer's code. This first optimizing stage includes eliminating common subexpressions, constant propagation, copy propagation, constant folding, strength reduction, and peephole optimizations. It also encompasses code motion, dead code removal, redundant code elimination, and register assignment.

Because it's retargetable, the package can compile machine-independent programs for a large number of architectures. A de-

sign team can thus write application code concurrently with, or even in advance of, the design of the architecture to which the microcode is targeted.

Optimizer

The S/F Optimizer performs the second stage of optimization. This tool reorganizes syntactically correct microcode so that it can do low-level, fine-grain code improvements. It can use any parallelism and pipelining available for a given processor architecture. It improves code efficiency by using compaction, loop folds, and *trace scheduling* optimizations that relate specifically to the target architecture. The SF/Optimizer produces code that typically runs many times faster than the input code.

To improve the microcode's efficiency, the SF/Optimizer operates in both an interactive and an automatic mode. In the interactive mode, the SF/Optimizer provides immediate feedback from the editor-assembler to the operator. This feedback assists the programmer by providing

data-dependency and resource-usage information that is crucial to achieving an optimally written microcode program.

In automatic mode, the SF/Optimizer manipulates the input microcode, using several optimization techniques. One such technique is *code compaction*. Code compaction, operating on straight-line *micro-operation* sequences, produces code that runs more efficiently and takes less space in program memory.

The optimizer also optimizes via *software pipelining*. This operation provides significant speed improvements for sections of code that contain loops. Consider, for example, a simple loop that adds corresponding elements of two large arrays of numbers and stores the results in a third array. For processors that have parallel and pipelined computing resources, the Optimizer increases execution speed in loops by folding the microcode into a number of stages, each of which performs a portion of the total calculation. For example, it might fold a 12-operation

tive designs, you can write several different configuration files and then evaluate the various processors under the benchmark programs.

When your design is completed, you need little extra time for completing the entire microprogrammed system, because you've probably already developed and debugged many of the microprograms with the tool set. If you need to adjust the programs further, you can use the assembler and optimizer to streamline potential program trouble spots for very high performance. This streamlining enhances the quality of your SIMD designs and can dramatically reduce design costs and system development time. The result is better systems

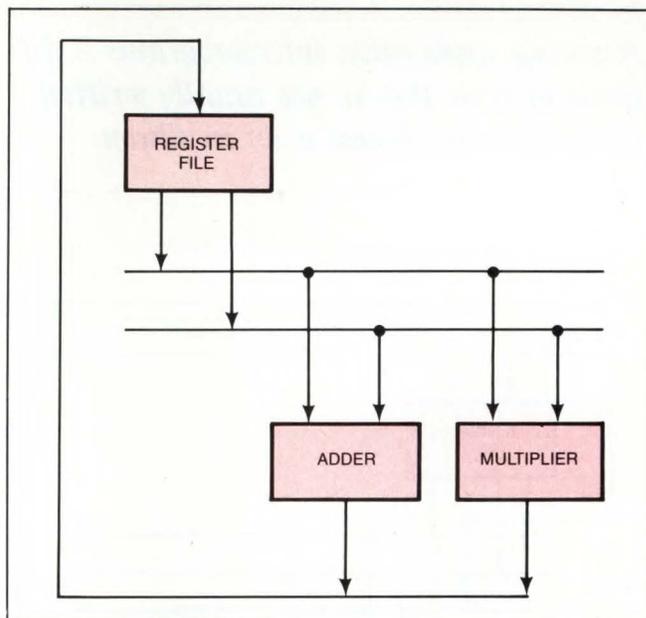


Fig 2—This simple design contains separate adder and multiplier units. The additions and multiplications must be executed sequentially.

straight-line loop into 4 stages, each of which takes only 3 cycles. Thus, when the processor executes the folded loop, only 3 cycles are needed to produce each result. This reduction in cycles improves the performance by a factor of four, compared to that of sequential code.

A third optimization involves *trace scheduling*. This process moves operations around control branches on the basis of the statistics on the relative execution frequencies of the various program paths. The goal is to speed up those program paths that are expected to run most frequently.

Assembler

The QTC SF/Assembler forms the foundation for all the tools in the family. It's a microcode meta-assembler that lets the developer customize a microcode programming language for a specific *target machine*. This tool supports the features found in many modern standard assemblers, like macros, include files, multiple code and data memories, conditional assembly, and

modular, relocatable code.

The SF/Assembler is designed to give the users the flexibility to design syntax that has the attributes and power of a high-level language, while they retain explicit control of the machine resources. The package also accommodates those users who feel more comfortable defining their language syntax at the instruction-field level.

Linker

The SF/Linker allows you to combine object files from a number of separately assembled subprograms into a single program module. The linker then formats modules into one of several selectable standard output formats for loading either into the actual target hardware or into a software simulator of the hardware.

Simulator

The retargetable SF/Simulator runs on the development host and can simulate the execution of an assembly- or microcode-language program as it would run on the target machine. It

uses a description of the target machine's hardware that is based on the same configuration file used by the SF/Assembler and SF/Optimizer. Because the SF/Simulator allows a large number of programmers to develop and check out applications code, regardless of the availability of the hardware, its use can substantially reduce the overall time for completion of a project.

Symbolic Debugger

The SF/Debugger permits the programmer to refer by name to the program variables whose contents he wishes to examine and modify. The SF/Debugger uses the SF/Simulator to execute the compiled code exactly as if it were running on the actual hardware. The SF/Debugger also provides a convenient interface to other programs, so that the user can write his own routines to communicate with actual hardware for hardware system debugging.

Assessing application microprograms is difficult because they're not usually written until after the design is set in silicon.

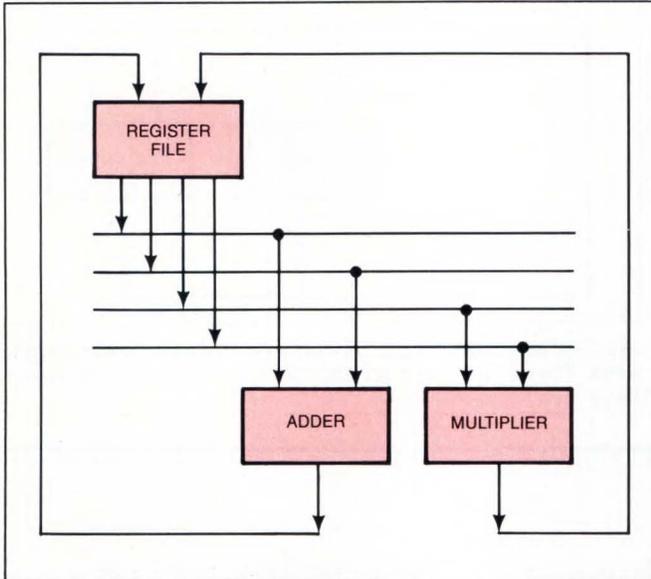


Fig 3—This design contains separate adder and multiplier units. The additions and multiplications can be executed concurrently.

that run faster and cost less.

To illustrate some of the benefits of such a tool set, consider a scenario in which you need to design a computer for fast execution of 4×4 matrix multiplications. This problem is very common in systems designed for high-performance image analysis and rendering. You'll typically work through several versions of the computer from a simple, conventional, sequential bit-slice design to an SIMD architecture.

Along the way, you'll need to know how effective the design is in two respects: First, how programmable is it? That is, will it be possible to write microcode for the machine so as to exploit the features designed to provide greater performance potential? Second, is the performance the machine was designed to provide achievable through microcoding?

Computing a 4×4 matrix illustrates concretely how you actually might use these tools. Matrix multiplica-

LISTING 2—INNERMOST LOOP OF SEQUENTIAL MICROCODE

```
Cycle 1. t = a[i][k] * b[k][j];
2.           ; No-op
3. c[i][j] = t + c[i][j];
```

tion is a very common computation, so the following example touches only on the arithmetic operations and skips over the other issues, such as memory traffic, that a designer would normally have to take into account in the designing process. The example also assumes the presence in the design of all necessary loop operations, variable initialization, addressing, and memory accesses.

Work through a practical example

The problem is to efficiently compute $c = a:b$ (Fig 1). You could just design a bit-slice architecture (Fig 2) that allows a single scalar addition or a single scalar multiplication in any instruction cycle. In this case, a scalar addition would execute in one cycle, and a scalar multiplication in two cycles.

A typical C program that computes a 4×4 product is shown in Listing 1. Simply counting the additions and multiplications reveals that the innermost loop of this program contains one addition and one multiplication, each of which is executed 4^3 , or 64, times. A simple microcoded solution corresponding to the C loop contains the operations shown in Listing 2. If you count the instruction cycles needed to perform these operations, and then count the number of passes through the loop, you'll find that the complete matrix multiplication requires 3×4^3 , or 192, instruction cycles.

Next, you might want to consider an architecture that can perform the scalar additions and multiplications concurrently (Fig 3). To obtain the concurrent operation, you have to change the configuration file (the

LISTING 3—PROGRAM THAT FOLDS THE INNERMOST LOOP

```
PREAMBLE TO THE INNERMOST LOOP:
Cycle 1.   t[1] = a[i][1] * b[1][j]           ;
2.           ; No-op
INNERMOST LOOP BODY (executed for k=2..4):
Cycle 1.   c[i][j] = t[k-1] + c[i][j] # t[k] = a[i][k] * b[k][j];
2.           ; No-op
POSTSCRIPT TO THE INNERMOST LOOP:
Cycle 1.   c[i][j] = t[4] + c[i][j]           ;
```

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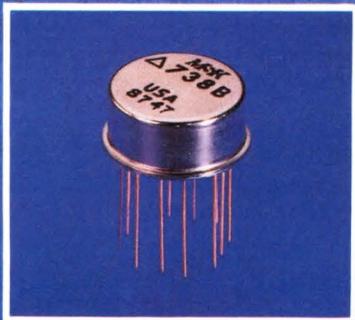
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An automated microcode development system must be retargetable to any hardware architecture if it is to be useful.

LISTING 4—PROGRAM THAT FOLDS BOTH INNERMOST AND MIDDLE LOOPS

PREAMBLE TO THE MIDDLE LOOP:

```
Cycle 1. t[1] = a[i,1] * b[1,1] ;
```

MIDDLE LOOP BODY (executed for j=1...3):

INNERMOST LOOP BODY (executed for k=2...4):

```
Cycle 1. ; No-op
```

```
2. t[k] = a[i,k] * b[k,j] # c[i,j] = t[k-1] + c[i,j];
```

POSTSCRIPT TO THE INNERMOST LOOP:

```
Cycle 1. ; No-op
```

```
2. t[1] = a[i,1] * b[1,j+1] # c[i,j] = t[4] + c[i,j];
```

POSTSCRIPT TO THE MIDDLE LOOP:

```
Cycle 1. ; No-op
```

```
2. t[2] = a[i,2] * b[2,4] # c[i,4] = t[1] + c[i,4];
```

```
3. ; No-op
```

```
4. t[3] = a[i,3] * b[3,4] # c[i,4] = t[2] + c[i,4];
```

```
5. ; No-op
```

```
6. t[4] = a[i,4] * b[4,4] # c[i,4] = t[3] + c[i,4];
```

```
7. ; No-op
```

```
8. c[i,4] = t[4] + c[i,4] ;
```

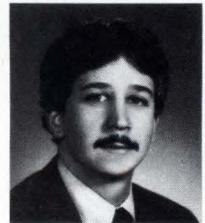
C program, however, can remain the same). If you recompile the program, and the compiler performs only a *local compaction* of instructions (that is, the instructions are not moved around control block boundaries), you would obtain the same microcode.

Because the next scalar multiplication can begin as soon as the addition at the bottom of the loop is done, you can improve the program's efficiency by overlapping the additions with the multiplications. Specifically you can optimize the program by unrolling and folding the innermost loop body to achieve the overlapping operations and then rerolling the innermost part. The result is shown in **Listing 3**. (The # delimiter separates operations that are executed in parallel.) The resulting code performs these arithmetic operations in $(2+(2)\times 3+1)\times 4^2$, or 144, instruction cycles (the parentheses in the arithmetic expression reflect the looping structure of the program).

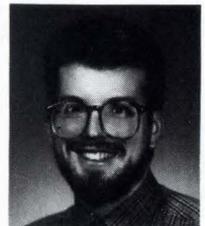
A very powerful optimizer can automatically determine the benefit of performing this optimization, and then take things one step further. The optimizer would unroll, fold, and reroll the middle loop as well, and so reduce the total time still further. Most programmers would probably overlook this possibility, and those who recognized the possible benefits might shy away from it because of the complexity of the required code reorganization. The result of the transformation is shown in **Listing 4**. The highly optimized loop now requires only $1+(2+(2)\times 3)\times 3\llcorner 8)\times 4$, or 132, instruction cycles. **EDN**

Authors' biographies

Robert A Mueller is QTC's director of research. He was previously president and founder of Horizon Research Labs, which was acquired by QTC in July 1987. Bob is currently on sabbatical leave from Colorado State, where he is associate professor and director of the firmware-engineering and micro-architecture design laboratory. He is a recognized expert on microcode optimization, and has published more than 75 papers. Bob holds a BS in computer science and an MS in mechanical engineering from Colorado State University and a PhD in computer science from University of Colorado. He's a member of the ACM and the IEEE. In his spare time, he enjoys bicycling.



Daniel R Benua develops new products for QTC as a senior software engineer. Before joining QTC early in 1984, Dan worked at Spacelabs. He holds an MSEE from Stanford University and a BSEE from Brown University, and is a member of the ACM.



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One if by land...



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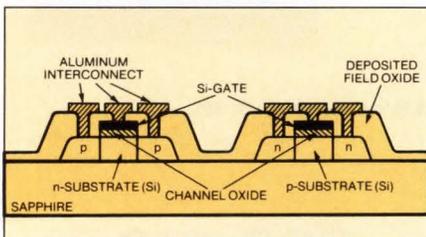
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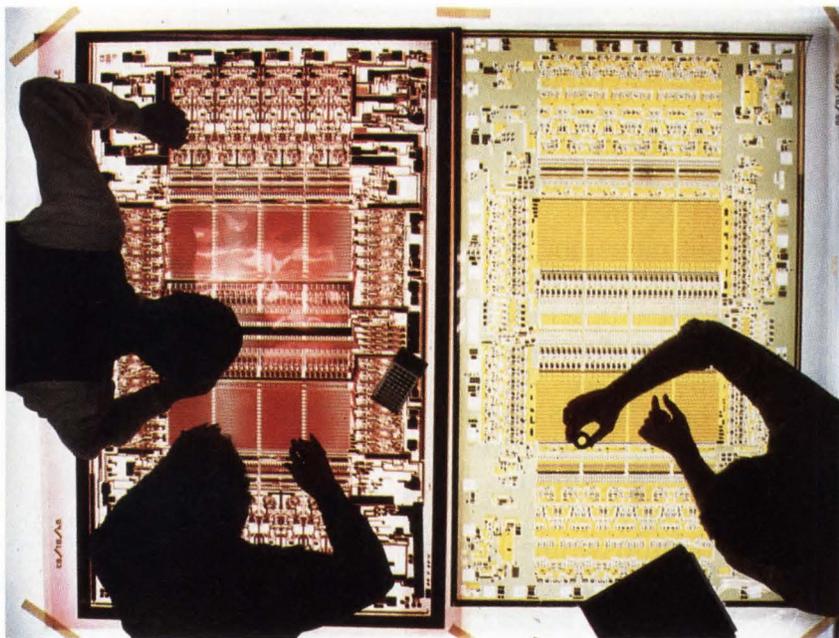
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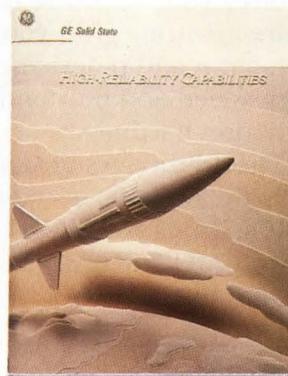
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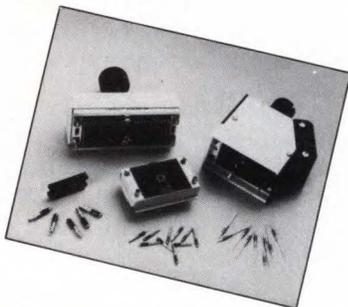


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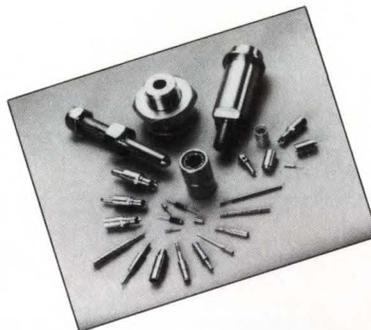


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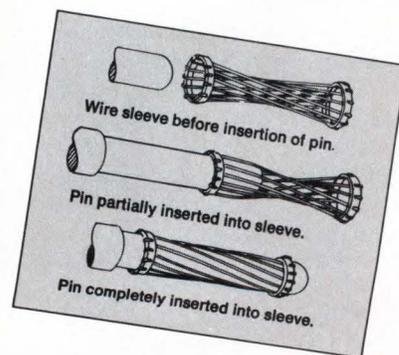
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DESIGN IDEAS

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555 timer triggers phase-control circuit

J N Lygouras
University of Thrace, Xanthi, Greece

The control circuit in Fig 1a allows you to manually adjust the power delivered to a load. By changing the setting of potentiometer R_3 , you change the phase angle at which the thyristor (Q_3) fires (Fig 1b), thereby altering the load current's duty cycle. The adjustment range is about 0 to 180°. Q_3 's off time is linear with R_3 , but of course the resulting load power is not linear with R_3 .

The full-wave diode bridge delivers pulsed-dc voltage to the load, making the circuit suitable for dc-control applications such as dimming. (The circuit can handle ac power if you substitute a triac for Q_3 and make slight modifications.)

IC₁ is a low-power—1 mW—timer configured as a monostable monovibrator. Zener diode D_1 and filter capacitor C_1 , activated by pulses from the voltage divider R_1/R_2 , form a dc supply for the timer. Q_1 turns on and applies a negative-going trigger to the timer (pin 2) each time Q_1 's base voltage approaches 0V. In response, the timer issues a positive pulse that turns on Q_2 and turns off Q_1 , removing load power for an interval equal to $1.1R_3C_2$. To increase the control resolution, you can lower the value of R_3 , substitute a potentiometer with more turns, or add a fixed resistor in series with the potentiometer.

EDN

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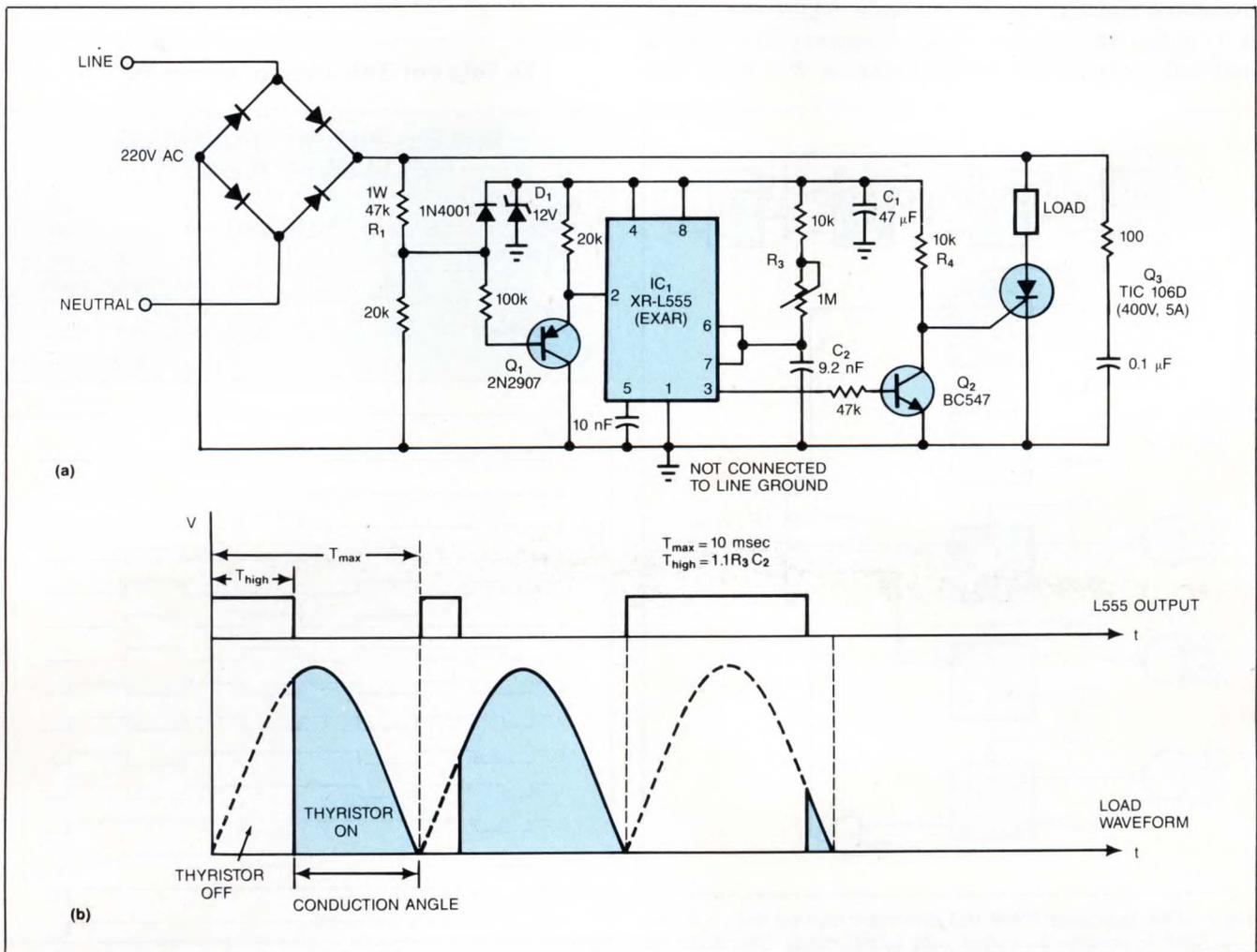


Fig 1—Adjusting this circuit's R_3 (a) varies the percent of each line cycle that power is applied to the load (b).

PWM DAC simplifies output filtering

Roy Sprowl
Litton, Chatsworth, CA

Composed entirely of logic gates, the PWM D/A converter of **Fig 1** is suitable for gate-array designs. The circuit's output signal requires less filtering than that of conventional PWM DACs. A single-pole filter, with a corner frequency (f_0) equal to $\frac{1}{20}$ th of the converter's sample rate, is sufficient to reduce the converter's output ripple to less than 1 LSB p-p. What's more, the filter requirement depends only on the sample rate and not on the converter's bit resolution. For a given level of ripple, a conventional PWM converter would require filtering in proportion to its bit resolution (**Table 1**).

Fig 2's waveforms illustrate the circuit's reduced need for filtering. A conventional PWM converter's maximum ripple occurs at half scale, where the output is a square wave at the sample frequency, but **Fig 1's** half-scale output is a square wave at 2^{n-2} times the

sample frequency. In fact, **Fig 1's** maximum ripple does not exceed $3\times$ that associated with the count 1 waveform of **Fig 2**.

Fig 1 has one potential drawback that conventional PWM D/A converters do not have. Because the rate of output transitions varies with the input code, unequal rise and fall times in the output cause a second-order nonlinearity error. This error value peaks at half scale and is most noticeable in fast or high-resolution versions of the converter.

Although the circuit is similar to a rate-multiplier IC, it has an asynchronous counter that enables its faster operation. You can scale the circuit for other bit resolutions; for an n-bit counter, the bit resolution equals $n+1$ bits. The n input bits are B_0 - B_4 (in this case), and f_{CLK} is a square wave at 2^{n-1} times the sample rate. **EDN**

To Vote For This Design, Circle No 748

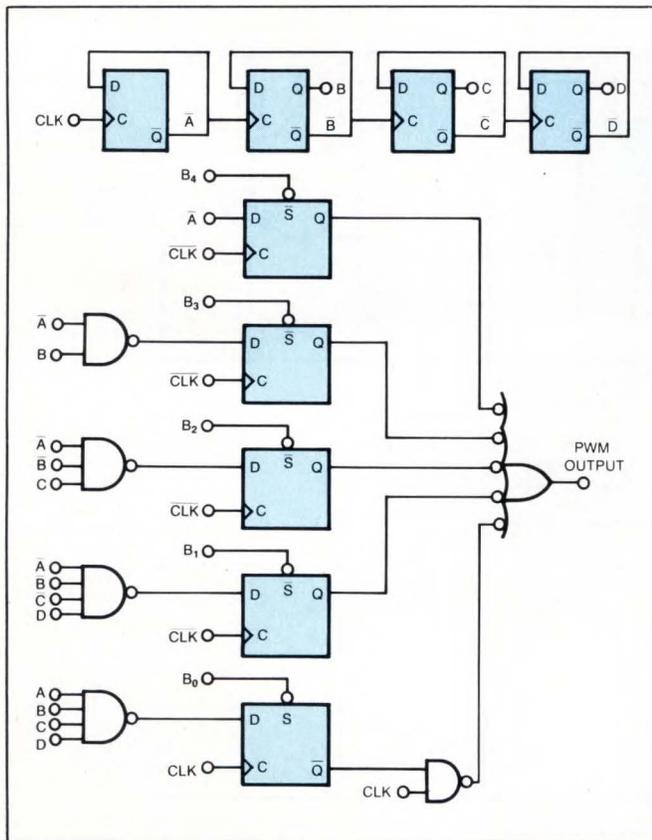


Fig 1—This logic-gate PWM D/A converter requires only a single-pole filter to produce an output with 1-LSB ripple. You make the connections indicated between the counter outputs shown at the top and the left-side input terminals.

TABLE 1—FILTER FREQUENCIES FOR 1-LSB P-P RIPPLE

CONVERTER TYPE	Low-Ripple	PWM	PWM	PWM	PWM	PWM
RESOLUTION	n-bit	4-bit	6-bit	8-bit	10-bit	12-bit
f_0 / f_{SAMPLE}	1/18.8	1/23.5	1/99	1/400	1/1600	1/6400
RIPPLE FREQUENCY	$\times 1$	$\times 1.25$	$\times 5.2$	$\times 21.3$	$\times 85$	$\times 340$

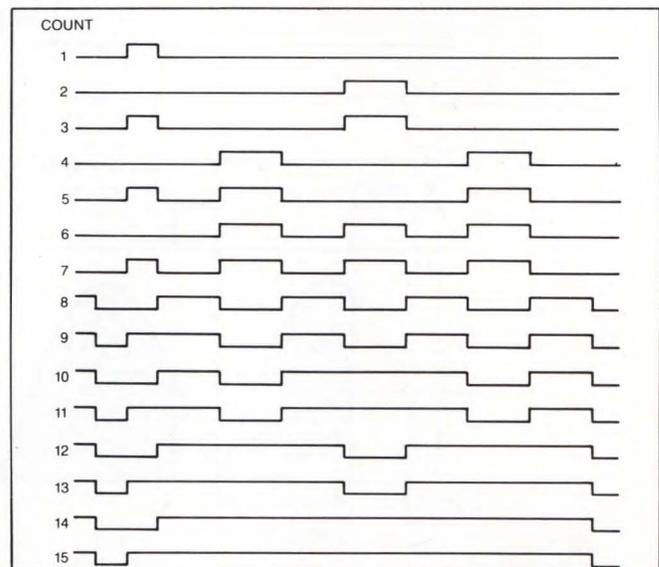


Fig 2—**Fig 1's** circuit produces these output waveforms in response to the counter's 16 output codes.

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MODEL	FREQ. MHz	GAIN, dB			Min. (note)	• MAX. PWR. dBm	NF dB	PRICE \$ Ea.	Qty.
		100 MHz	1000 MHz	2000 MHz					
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8□	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

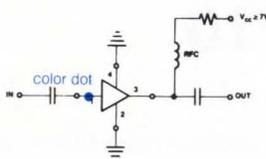
NOTE: Minimum gain at highest frequency point and over full temperature range.

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C113-Rev. D

Add text to composite-video signal

Stephen Tomporowski
Philips Medical Systems Inc, Shelton, CT

The Fig 1 circuit shows a simple way to add text information to a composite-video signal that may be floating at some indeterminate dc level. The text generator and composite-video source must have the same sync signal.

The video-input and -output signals share the same terminal. C_3 couples the video signal to the output of a rectifier circuit that is based on a subvideo-speed op amp. (A faster op amp would clamp on individual sync pulses rather than on the video waveform's average value, as is desired.) C_3 accommodates applications in which the video blanking level is negative (below ground). By adding a second electrolytic capacitor in series, with their negative leads connected, you can eliminate the circuit's sensitivity to the polarity of the

video signal's dc component. R_{11} serves as a pulldown resistor, and feedback resistor R_{10} ensures that TP6 remains at ground level.

Emitter follower Q_1 buffers the text signal, and R_5 serves as a gain control. A simple clamp circuit (Q_2) is sufficient for regulating amplitude because the text signal contains no gray-scale levels. Q_3 couples the text signal into the op-amp clamp circuit. Although a sync-driven clamp would offer higher performance, this type of circuit performs the function required of it—preventing the addition of text from creating a hump or a dip in the video waveform's blanking level. Such aberrations produce unsightly light or dark bars across the monitor screen's text display.

EDN

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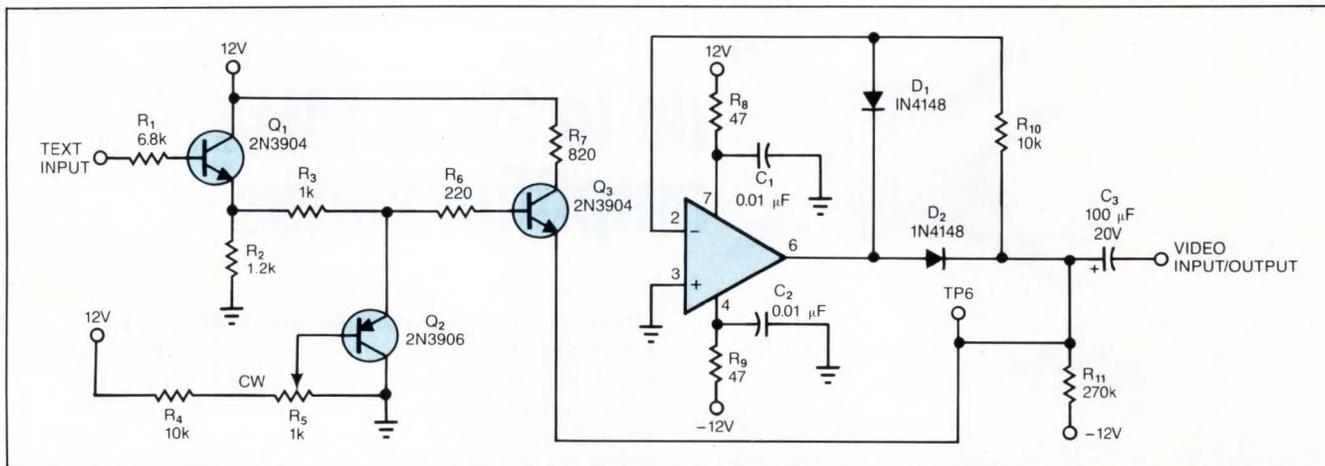


Fig 1—This circuit adds a text-information signal to a composite-video signal of indeterminate dc level.

First-order allpass filter uses an MF10

Kevin Hoskins
National Semiconductor Corp, Santa Clara, CA

You can use a first-order allpass filter to provide compensation for closed-loop control systems, or to remove

the ringing on transmitted square waves by compensating for the transmission line's nonideal phase shift. In addition, you can use such a filter for motor control by creating a quadrature oscillator that generates sine and cosine waveforms. Fig 1a shows a conventional first-

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DESIGN IDEAS

order allpass circuit using an RC network and an op amp; **Fig 1b** shows an equivalent circuit based on ½ of an MF10 dual switched-capacitor filter. (If you don't need the other ½ of the filter section, use an MF5 single-section filter instead.)

For both **Fig 1** circuits, the phase response begins with 0° phase at dc, becomes 90° at the center frequency (f_0), and approaches 180° as the input frequency increases. Just as you would expect for an allpass-filter response, neither of the circuits alters the input amplitude. **Fig 1a**'s transfer function, normalized to $\omega=1$, is

$$\frac{V_{OUT}}{V_{IN}} = -\frac{s-1}{s+1}$$

Fig 1b's realization of this function duplicates **Fig 1a**'s noninverting path by routing the input signal to pin 5, through the first integrator, through R_3 , and back into pin 4. **Fig 1b**'s corresponding inverting path consists of the MF10's op amp, R_2 , and R_1 . The normalized transfer function for **Fig 1b** is

$$\frac{V_{OUT}}{V_{IN}} = \frac{-1 \left(\frac{sR_2}{R_1} \frac{R_2}{R_3} \right)}{s + \frac{R_2}{R_3}}$$

Setting $R_1=R_2=R_3=10 \text{ k}\Omega$ reveals the similarity of **Fig 1b**'s transfer function to the **Fig 1a**'s transfer function:

$$\frac{V_{OUT}}{V_{IN}} = \frac{-1(s-1)}{s+1}$$

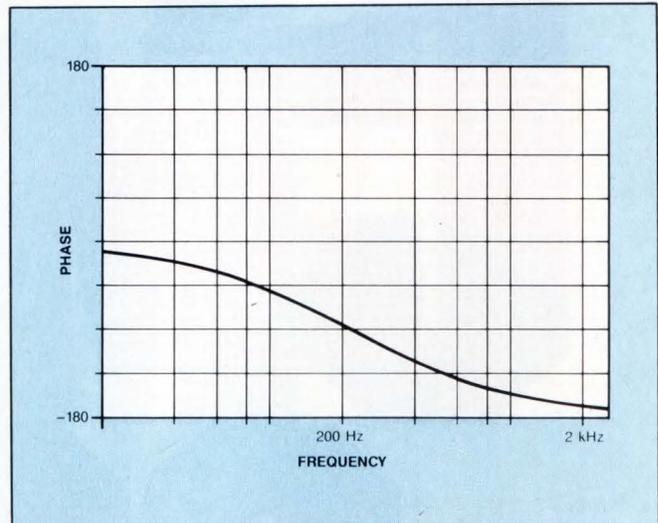


Fig 2—The phase response for **Fig 1b** shows -90° at f_0 (210 kHz).

Fig 2 shows the phase response of the **Fig 1b** circuit when $f_{CLK}=210 \text{ kHz}$. When the circuit uses 1% resistors, the amplitude response is flat to within $\pm 0.3 \text{ dB}$. The center frequency equals $f_{CLK}/50$ or $f_{CLK}/100$, depending on the connection to pin 12. You can change f_0 simply by changing f_{CLK} . Note that **Fig 1b** also provides a first-order lowpass-filter output at pin 2, with a gain of -2 . This output's $-3\text{-dB } f_0$ is the same as that of the allpass-filter output— $f_{CLK}/50$ or $f_{CLK}/100$. **EDN**

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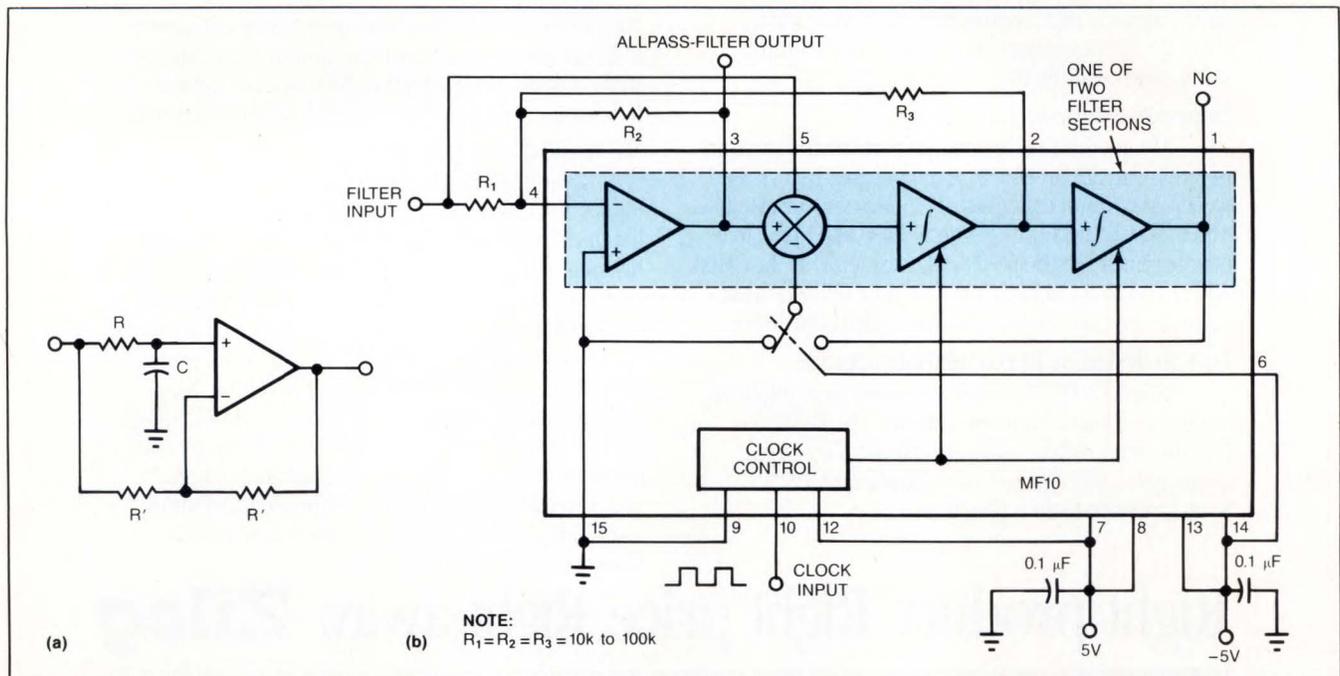


Fig 1—The op amp circuit (a) and the switched-capacitor-filter IC (b) both provide a first-order, allpass-filter response.

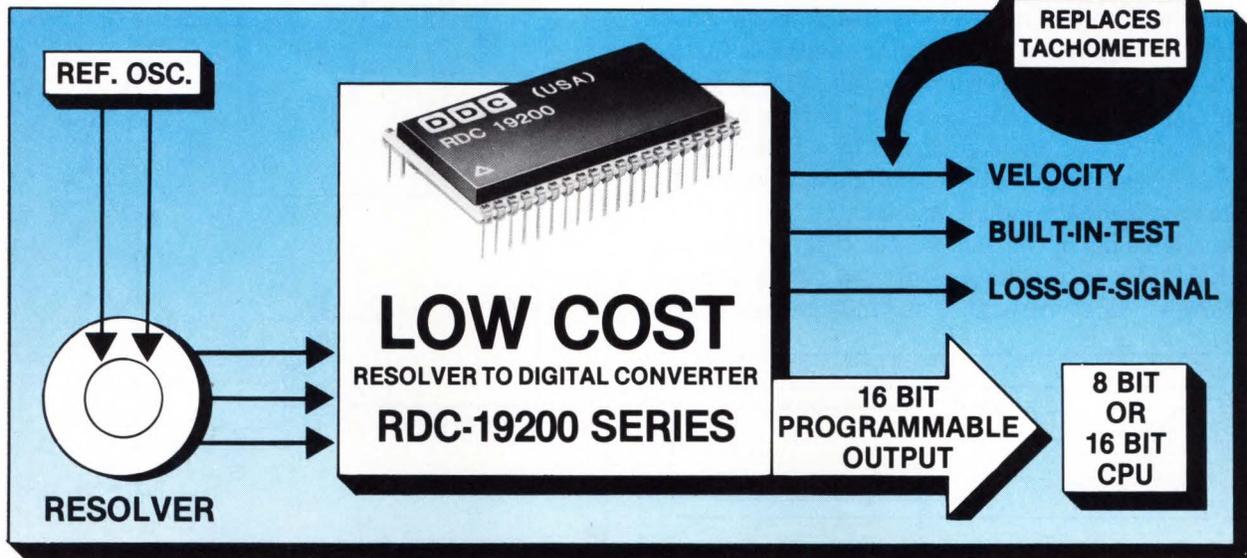
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AUGUST 1988

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Motor controller eliminates tachometer

Barry Friedman
Copley Controls, Newton, MA

Precision motion-control systems use a motor-driven tachometer to generate electronic feedback for the motor's servoamplifier in order to attain 0.1% accuracy. If your application can tolerate 2 to 3% errors, however, you can reduce cost and complexity by eliminating the tachometer and using the servomotor's own back-EMF voltage as a feedback signal instead.

A simple model of the servomotor (Fig 1) shows the back EMF (V_e) as a voltage source in series with the armature winding's resistance and inductance. You can

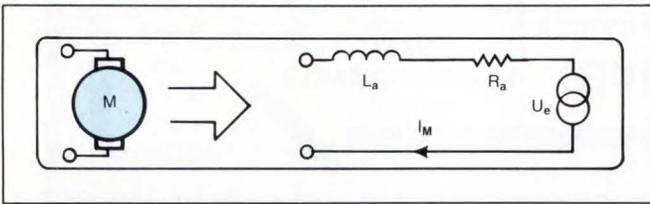


Fig 1—A first-order model of a servomotor includes the motor's armature inductance (L_a), armature-winding resistance (R_a), and back-EMF source (V_e).

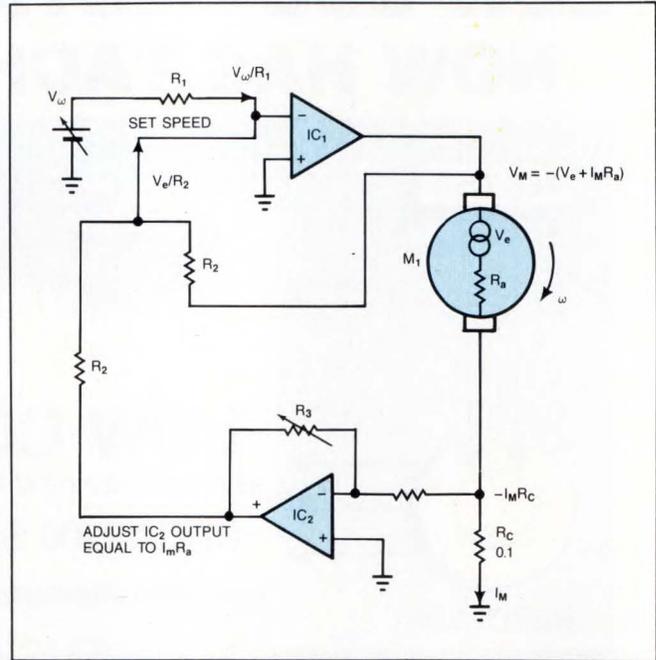


Fig 2—This generalized schematic illustrates the principle of using V_M as a feedback signal, after first subtracting the motor armature's error-producing IR drop.

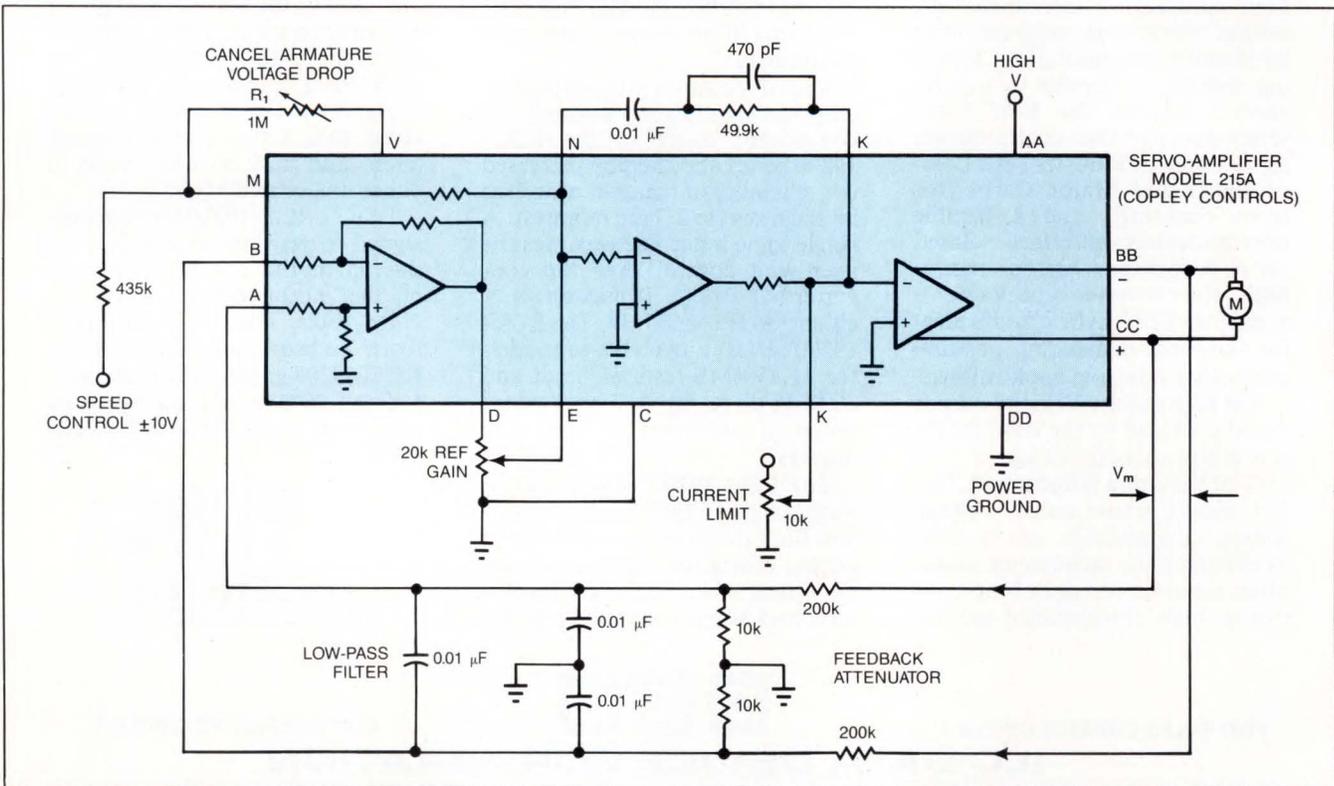


Fig 3—This circuit uses the Fig 2 approach and makes use of a current-sensing circuit internal to the servoamplifier.

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ignore the inductance for steady-state conditions, but the armature current flowing in R_a creates a voltage error in series with V_e . Consequently, the voltage across the armature terminals ($V_e + I_M R_a$) represents pure back EMF only for zero armature current (as, for example, when you turn off the power and let the motor coast to a stop).

Fig 2 shows a circuit that subtracts the error term $I_M R_a$ from the motor voltage V_M , leaving only the desired V_e term for use as a feedback signal. The current-sense resistor, R_C , enables op amp IC_2 to generate the $I_M R_a$ -cancellation voltage; feedback resistor R_3 lets you calibrate the system by adjusting that voltage. The servoamplifier, IC_1 , then produces the drive voltage (V_M) by summing the currents proportional to $I_M R_a$, V_M , and the command variable V_w :

$$\frac{V_w}{R_1} = \frac{V_e}{R_2} \rightarrow V_e = V_w \frac{R_2}{R_1}$$

Fig 3's implementation of this approach incorporates a specific servoamplifier. Because products such as this one, the Copley Controls Model 215A, deliver a differential output (V_M) as high as 150V, you must attenuate the feedback signal with resistive dividers (200 k Ω to 10 k Ω for this example). This type of amplifier also achieves high efficiency by delivering a PWM output. To produce an analog-equivalent signal suitable for feedback to the servoamplifier's input, you need a simple lowpass filter, which you can achieve by adding 0.01- μ F capacitors to the resistor network already in place.

The servoamplifier includes a current-sensing circuit normally used for the remote indication or control of torque, which enables it to cancel the motor armature's $I_M R_a$ term with the help of an external 1-M Ω potentiometer (R_1). R_1 also controls the degree of positive feedback (damping). You should set the potentiometer to its maximum value, and then adjust the system for optimum speed stability by gradually decreasing the resistance setting.

EDN

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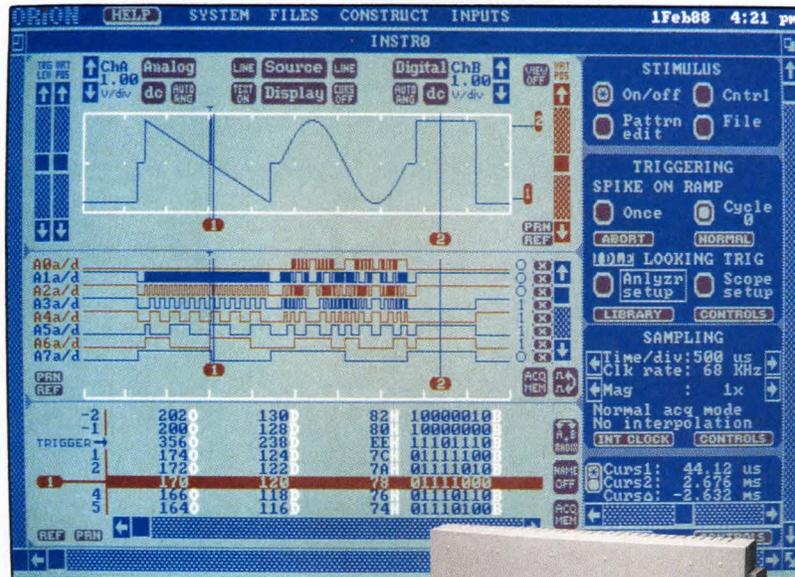
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OmniLab display demonstrates capture of an imbedded analog glitch (in top trace) with time-aligned presentation of the waveform's digitized bit values (center) and numeric states.



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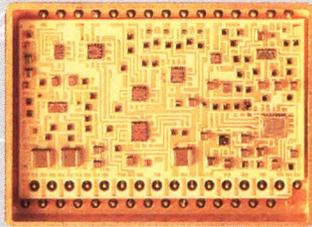
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Repetitive Sampling:	680 MS/s	Repetitive Sampling:	680 MS/s on 48 inputs
Scale Factor:	5 mV/div to 10V/div in 1-2-5 sequence	Synchronous Clocking:	0 to 34 MS/s
Record Length:	4K (16K, 64K optional)	Acquisition Memory:	4K samples (16K, 64K optional)
		Disassembly Options:	Over 150 microprocessors
ANALOG STIMULUS		DIGITAL STIMULUS	
Output:	8mV to 8 V peak-to-peak, 8 bit	Outputs:	24, 74F tri-state drivers
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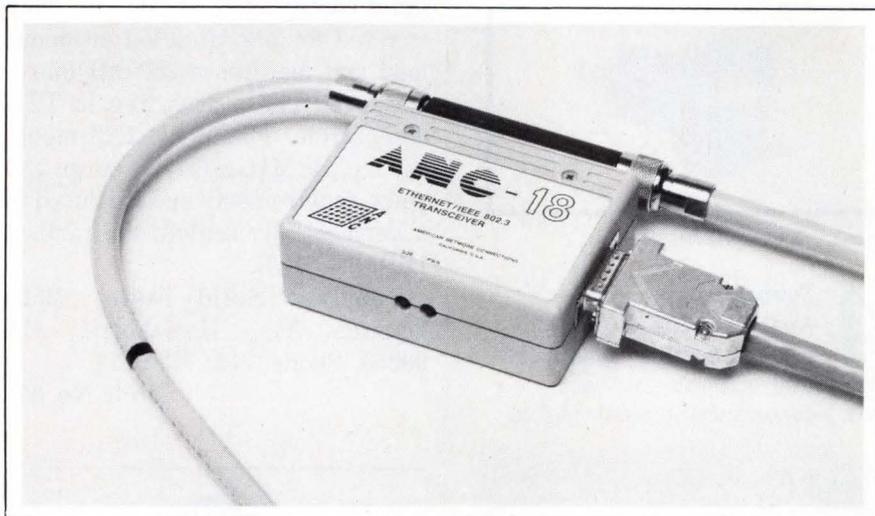
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COMPONENTS & POWER SUPPLIES



TRANSCEIVER

- Connects to a standard Ethernet coaxial cable
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The ANC-18 transceiver connects standard Ethernet-coaxial (10-BASE5) or thin-coaxial (10-BASE2) cable with a choice of three taps—AMP piercing, N-type, and BNC-type. It is designed to comply with Ethernet V2/IEEE

802.3 transceiver specifications and 10M-bps Ethernet CSMA/CD operation. The unit features two indicators for operation and power statuses and is housed in a die-cast aluminum case. The units are UL, CSA, TUV, and FCC certified. \$280.

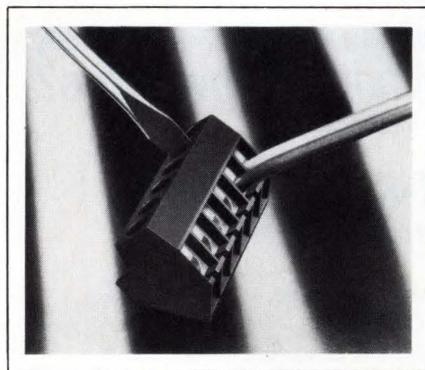
American Network Connections Inc., 462 Oakmead Parkway, Sunnyvale, CA 94086. Phone (408) 737-1511. TWX 650-334-0732.

Circle No 370

TERMINAL STRIPS

- Save space on crowded pc boards
- Captive protectors hold wires securely in place

With 0.197-in. contact spacing, Eurostyle 45° entry terminal strips save space while providing easy, safe access for wiring on crowded pc boards. In addition to a small footprint and easy wire access, the terminals have touch-proof recessed terminals and wire-ready captive screws that won't fall out and cause shorts. The terminal strips carry a 15A UL-recognized current rating and will accommodate voltages to 300V. Other features include a large wire-entry design that will accept 14 AWG wires, a closed side that acts as a wire stop, and thermoplas-



tic insulator material that has a 130°C temperature index and carries a 94V-0 UL flame-retardant rating. \$0.18/circuit (500).

Vernitron Corp., Beau Products Div, Box 10, Laconia, NH 03247. Phone (603) 524-5101. TWX 710-364-1843.

Circle No 371

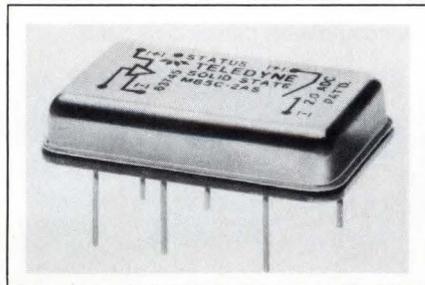
LASER DIODES

- Designed for long-haul applications
- Feature 0.2-nsec response time

DFB laser diodes are designed for long-haul, high-speed communications applications. Available in hermetically sealed metal packages, the diodes feature a typical side-mode suppression ratio of 33 dB. They operate in a stable transverse mode and feature a 0.2-nsec pulse-response time. All six devices in the line have a 20-mA typ operating threshold current and output 5 mW typ. Three of the units—ML7912, ML7612, and ML7702—operate at a 1310-nm optical wavelength. The ML9912, ML9612, and ML9702 feature a 1550-nm output wavelength. \$1787 to \$2112.

Mitsubishi Electronics America Inc., 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 372

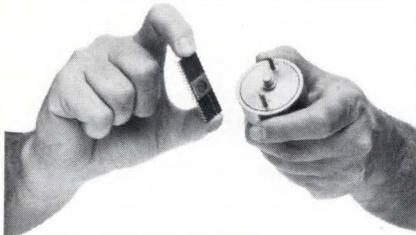


SOLID-STATE RELAY

- Features output-status feedback
- Senses a short-circuit condition and shuts down

The M85C-2AS solid-state relay features true output-status feedback as well as short-circuit and current-overload protection. An output-status pin indicates that the output is on and conducting current. The short-circuit protection provided will sense a short-circuit condition and initiate a shutdown within 5

Solenoid control design tips



Microprocessor turns snap action solenoid into a smooth positioner. It's quiet, too. See below.

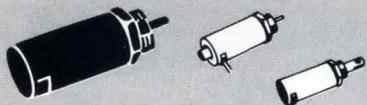
Solenoids are used to control the performance of devices such as valves, gates, and dampers. New research and development provides better design capability over solenoid parameters and characteristics to make them a system designer's dream come true. Designers are specifying solenoids in applications that once used other actuators.

1 Some hot solenoid applications

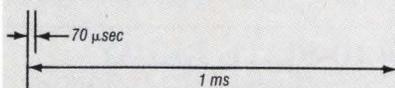
■ Variable, repeatable positioner ■ Fly-by-wire ■ High speed liquid metering ■ Safe-arm locks ■ Fuel injection

2 Design benefits

The simpler control required by solenoids means faster product development cycles, higher reliability from fewer interfaces, high force and speed capabilities. A solenoid is practically made for digital control because it's a pulsed device. And its few components can be optimized.



Example: Want higher speed actuation than a given solenoid allows? Consider using two or more smaller, faster solenoids and take advantage of their multiplied force.



Example: A designer wanted a solenoid to operate within a millisecond, in a window only 70 microseconds wide. With a specified life of 500 million cycles! Lucas Ledex solenoids are repeatable, predictable, reliable.

3 Workhorse.

Lucas Ledex Soft Shift™ variable positioning solenoid starting force is 3 to 5 times conventional, using the same power. It can actuate in milliseconds, or its plunger velocity can be controlled smoothly and noiselessly if you ramp

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Soft Shift™ solenoid. Stock models in five sizes.

4 Solenoid package size

Need low profile? Minimum volume? Smallest frontal area? Lucas Ledex solenoids can pack more work per cubic inch than motors.

Lucas Ledex solenoid configurations

Rotary —High torque, compact.
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Linear —Short, medium, long stroke types.
Push or pull.
Open Frame—High performance at least cost.

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Look at the variety of parameters and characteristics the designer can optimize: ■ Force ■ Speed ■ Life ■ Acceleration ■ Quality ■ Noise ■ Repeatability ■ Reliability. Design flexibility also comes by using controls, such as: ■ Current limiting ■ Pulse (A to D) ■ Position sensing ■ Packaged switches. Call on us to discuss your application. Often just a phone call will start a shelf-stocked solenoid on its way.

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Request catalogs.

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Lucas Ledex Inc.
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Vandalia, Ohio 45377-0427 U.S.A.
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Lucas Ledex

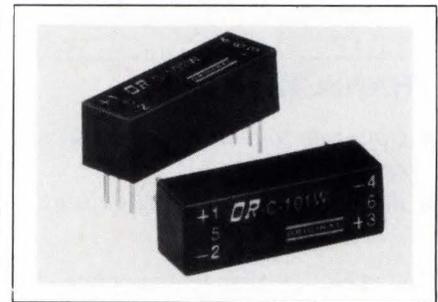
helpful motion control technology

COMPONENTS & POWER SUPPLIES

μsec. The relay will block the short-circuit condition indefinitely until the short circuit is removed and the input control is recycled. The relay is rated for a 2.1A/60V continuous load and features a 280-mΩ on-resistance. The status line is TTL compatible. The M85C-2AS meets the 28V dc MIL-STD-704 surge and spike requirements and is housed in a hermetically sealed, militarized DIP. \$90 (100).

Teledyne Solid State, 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077.

Circle No 373



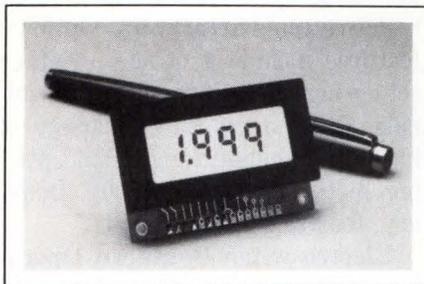
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- Designed to meet high-density packaging requirements
- Features a -30 to +60°C operating range

Measuring only 0.394×0.375×1.157 in. for a 1 Form A type, the OR-C Series reed relays meet the high-density packaging requirements of applications in instrumentation, audio and telecommunications equipment, and security and control systems. Contact configurations of 1B, 2A, 2B, 3A, and 3B are also available. The relays are available in both open and enclosed versions and operate over a -30 to +60°C range. Switching capability specs at 1A at 3 to 24V dc. Coil sensitivity ranges from 100 to 280 mW. The relays have a 2-million-operations lifetime at the rated load. \$1.36 (1000) for 1 Form A relays.

Original Electric Mfg Co Inc, 123 Lincoln Blvd, Middlesex, NJ 08846. Phone (201) 271-5770.

Circle No 374



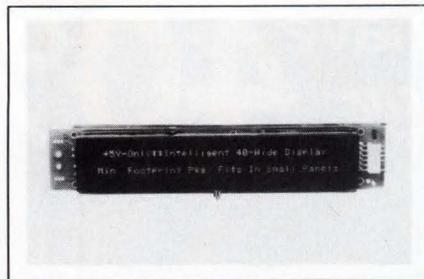
DIGITAL PANEL METER

- Supports all 4- to 20-mA transmitters
- Adjustable for both the zero and full-range spans

The DP-670 supports all 4- to 20-mA transmitters and interfaces directly to any 4- to 20-mA process loop. The meter draws operating power from the loop. The DP-670 features full differential input, 86-dB min CMR, and a dual-slope integrating A/D converter. As shipped from the factory, it is calibrated for a reading of 0 at 4 mA and 2000 at 20 mA. Both the zero and full-range spans are adjustable to permit users to fine tune the full-scale display ranges. You can momentarily freeze the display by strapping the hold-display pin to 5V dc. \$95.

Acculex, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (617) 880-3660. TLX 503989.

Circle No 375



DISPLAY

- Flicker-free operation under data-loading conditions
- Onboard μ P controls all display functions

The 3601-54-080 intelligent vacuum-fluorescent display provides two lines of 40 5x7 dot-matrix characters measuring 5.05 mm high. It

offers flicker-free operation under all normal data-loading conditions. An onboard μ P controls all the display functions and easily interfaces to an 8-bit parallel TTL data bus. The module displays the full 96-character ASCII font and additional European characters, scientific symbols, and user-programmable characters. The brightness level is

typically 165 fL; software-control allows you to dim the display to approximately 50 fL. The display operates from a single 5V supply. From \$177 (100). Delivery, four to six weeks ARO.

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 376

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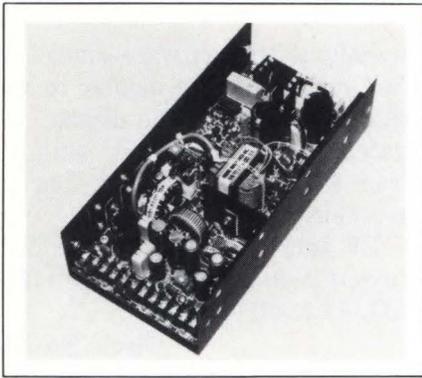
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CIRCLE NO 148

COMPONENTS & POWER SUPPLIES



POWER SUPPLIES

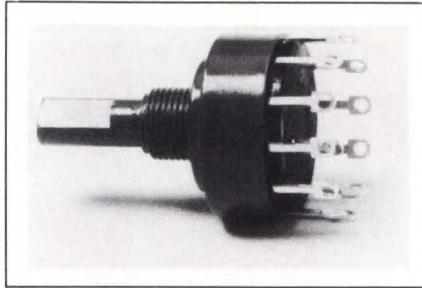
- Provide four fully isolated outputs
- Suitable for tight-space applications

Having dimensions of 5×2.5×10.5-in., NQF-200 Series 200W switch-mode power supplies are suitable for enclosures where space is at a premium. The units provide four fully isolated outputs. The main output is preset to 5V at 25A and features a remote-sensing capability. Users can specify the three auxiliary voltages in any combination. Standard values are 5, 12, 15, or 24V, but custom voltages are also available. Outputs 1, 3, and 4 are fully regulated. Output 2 is semiregulated and features a 10A surge-current rating. All outputs are fully protected against overload and short-circuit conditions. The supplies are

designed to meet VDE, UL, CSA, IEC, BS, and FCC safety standards and contain VDE-standard RFI line filters. \$252 (50).

Intelligence Power Technology Inc., 2111 Howell Ave, Anaheim, CA 92806. Phone (714) 937-1301. TWX 910-591-1893.

Circle No 377



ROTARY SWITCHES

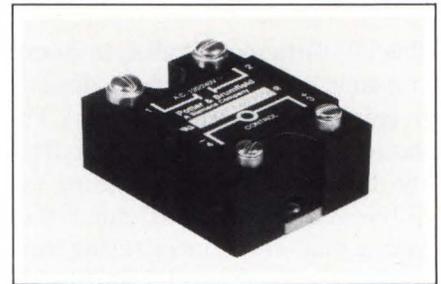
- Molded silver-plated terminals lock out flux
- Will carry 5A

Series 900A rotary switches are available in single-deck designs with 1- through 4-pole switching configurations. Standard features include a detent mechanism for a positive feel; insert-molded, silver-plated terminals for strength and flux lock-out; water-resistant housing-to-deck construction; 30° indexing; and an adjustable 2-through 12-stop position selector.

The units will switch 1A at 125V ac resistive and will carry 5A. Optional features include a choice of either solder-lug- or pc-board-type terminals, fixed stops, and a variety of bushing and shaft lengths and plating materials. \$0.90 (1000). Delivery, four to six weeks ARO.

Electroswitch Southern Operations, 2510 North Blvd, Raleigh, NC 27604. Phone (919) 833-0707. FAX 919-833-8016.

Circle No 378

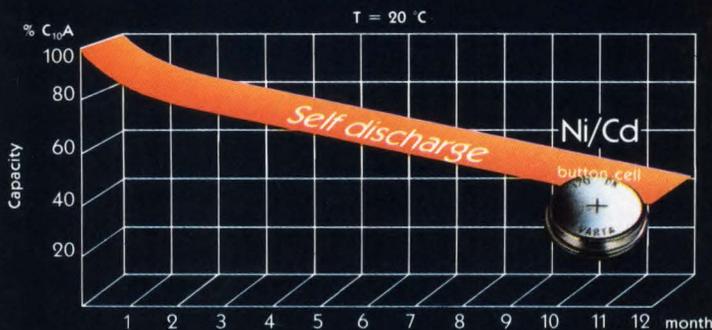


RELAYS

- Available in 10 and 25A versions
- Feature 4000V rms isolation

SSRT Series solid-state relays feature an spst NO contact configuration and are available in 10 and 25A versions for loads on 120 and 240V ac lines. Housed in the traditional hockey-puck package, they use a triac for the output device. A dv/dt

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CIRCLE NO 149



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snubber network on the output protects against false triggering by restricting voltage-transient rise times. The zero-voltage-turn-on units are available with control voltage ranges of 3 to 32V dc or 90 to 280V ac. The relays employ optical coupling to develop 4000V rms input-to-output isolation. The relays are UL-recognized and CSA-certified. From \$15. Delivery, stock to 10 weeks ARO.

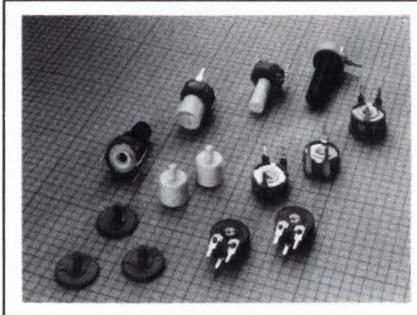
Potter & Brumfield Inc, 200 S Richland Creek Dr, Princeton, IN 47671. Phone (812) 386-2194.

Circle No 379

TRIMMERS

- Incorporate carbon-ink or cermet tracks
- Available with a variety of adjustment arrangements

The CP10 Series trimming potentiometers are available with either

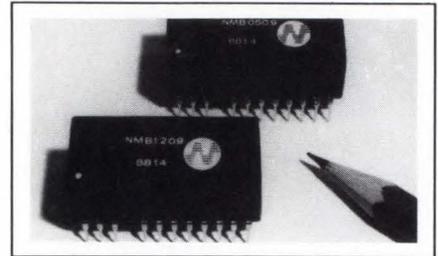


carbon-ink or cermet tracks. The carbon-ink versions use a Mylar film substrate that achieves a better humidity characteristic than conventional paper-phenolic materials. They are available with nominal resistance values between 100Ω and 10 MΩ, and have an end resistance of less than 3% of their nominal value. The cermet versions have a 0.5W power rating at 40°C, and a temperature coefficient of 100 ppm/°C. The nominal value tolerance is 20%, but tighter tolerance parts are available on special order. You can order versions with top,

side, or underside adjustment controls. From £0.06 (1000).

Bicc-Citec Ltd, Westmead, Swindon, Wiltshire SN5 7YT, UK. Phone (0793) 487301. TLX 449112.

Circle No 380



DC/DC CONVERTERS

- Generate -9V from 5 or 12V dc inputs
- Suitable for use with Cheapernet transceivers

Producing a -9V/250-mA output from a 5 or 12V dc input respectively, the NMB0509 and NMB1209 pc-board mounting dc/dc converters



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You remember what semicustom used to be: all that time and money with no assurance your ICs would withstand hi-rel environments. Now Harris gives ASICs a change for the better. With advanced cell libraries...an open-system CAE/CAD toolset...integration with industry standard workstations (Daisy, Mentor, Sun and other UNIX-based platforms).

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CIRCLE NO 253

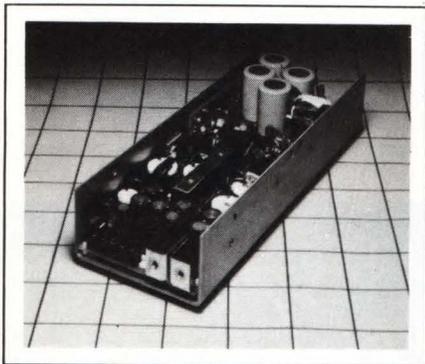
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COMPONENTS & POWER SUPPLIES

are designed for use in LAN equipment that conforms to the Ethernet or Cheapernet specification. They are suitable for use with a variety of transceiver chip sets. The converters have an input-to-output isolation of 500V dc, and an operating efficiency as high as 80%. They do not require additional heatsinking or derating over their operating temperature range of 0 to 70°C. The converters are housed in 24-pin DIPs with a height above the pc board of 10.8 mm. Around £8 (1000).

Newport Components Ltd, Tanners Dr, Blakelands North, Milton Keynes MK14 5NA, UK. Phone (0908) 615232. TLX 825621.

Circle No 381



POWER SUPPLY

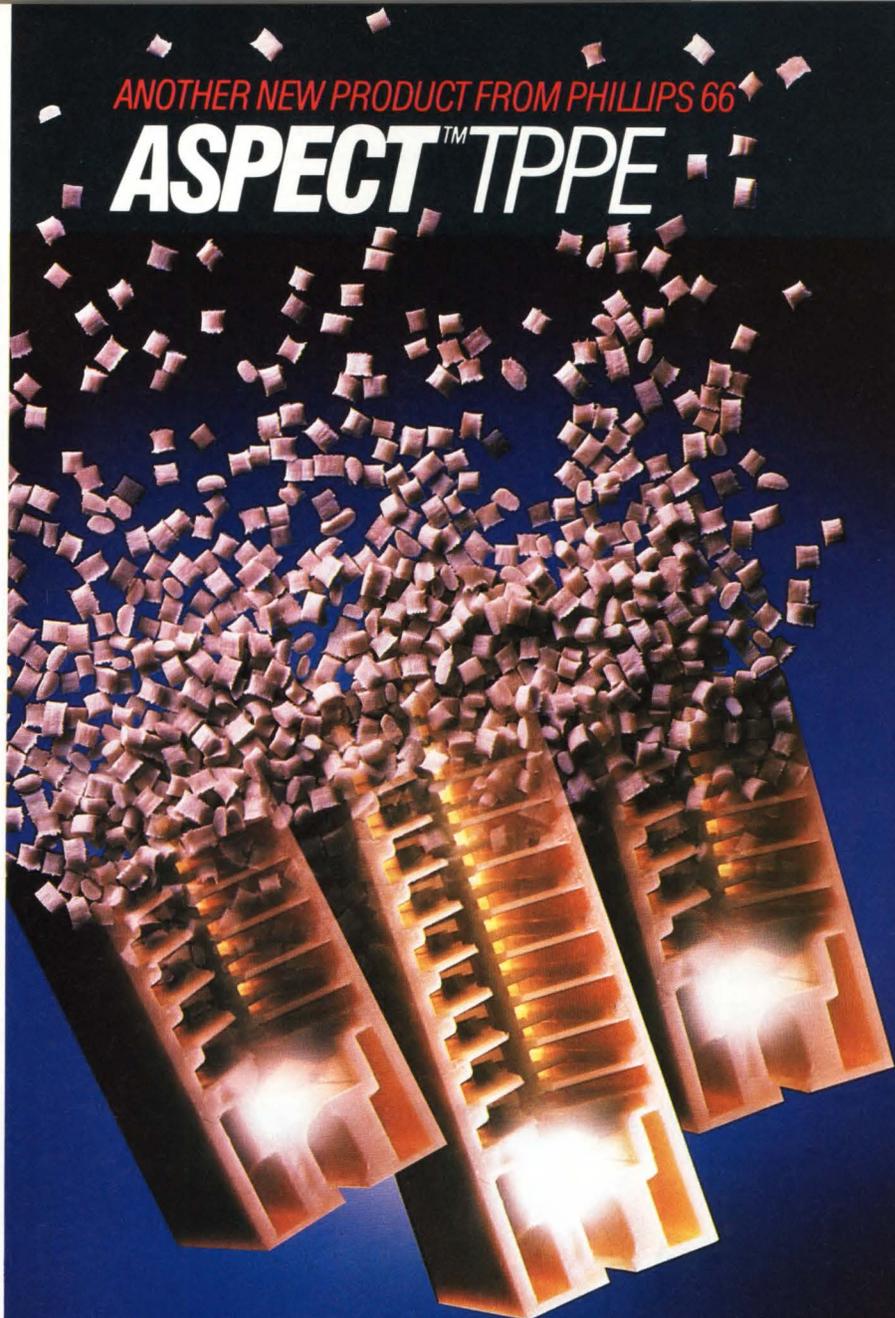
- *Delivers 700W*
- *All outputs are user-adjustable*

The MAX-704 delivers 700W and provides 100A at 5V for logic and memory applications. As many as three auxiliary outputs provide regulated 12 or -5.2V at 20A max. All outputs feature a $\pm 5\%$ user-adjustment range. Overload protection is provided on all outputs as is over-voltage protection on the 5V main output. Remote inhibit is standard, and power-fail is available as an option. MTBF specs at 80,000 hours. The supply meets international safety requirements such as UL 478, CSA 22.2, IEC 380 and 435, and the Class A RFI standards of FCC and VDE 0871. The supply features creepage and clearance distances of 4 and 8 mm, respectively,

EDN August 18, 1988

ANOTHER NEW PRODUCT FROM PHILLIPS 66

ASPECT™ TPPE



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ASPECT™ TPPE from Phillips 66 can bring a new dimension to your electronic components: a thermoplastic polyester with outstanding processibility, excellent toughness, and superior long-term thermal aging. Consider the cost-efficiency and results you can achieve with excellent flow properties, low molding pressure and high temperature performance.

Phillips 66 ASPECT™ TPPE is available in both natural and flame-retarded grades with two levels of glass reinforcement. It is the first in a line of Application Specific Thermoplastics from Phillips 66 that can meet your unique requirements. For more information about ASPECT™ TPPE and the full line of Phillips 66 Plastics, call **1-800-53-RESIN**.



ASPECT™ TPPE
PLASTICS WITH POWER TO WIN.™

CIRCLE NO 152

COMPONENTS & POWER SUPPLIES

to meet SELV requirements. \$549 (100). Delivery, stock to six weeks ARO.

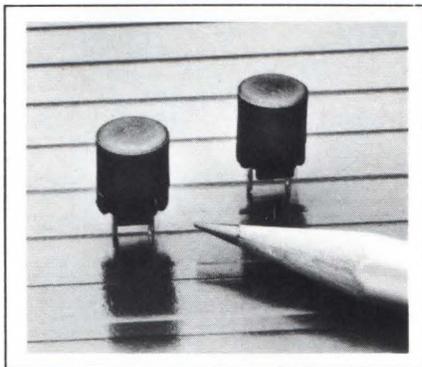
Todd Products Corp, 50 Emjay Blvd, Brentwood, NY 11717. Phone (516) 231-3366. TWX 510-227-4905.

Circle No 382

INDUCTORS

- *Internal capacitor conserves pc-board space*
- *Can accommodate wave-soldering processes*

Model 8RBC fixed inductors are designed for noise-filtering and trapping applications. They feature an internal matched capacitor that provides a stable temperature coefficient, conserves pc-board space, and reduces design and assembly time. Inductance values range from 1 to 45 mH, and the operating frequency range spans 50 to 200 kHz. Values for the internal capacitor range



from 5 to 6800 pF. The inductor base features pedestals that protect the winding terminations during assembly operations. The base is molded from UL 94V-1-grade phenol for heat protection during wave-soldering processes. All terminals are presoldered to provide reliable pc-board bonds. \$1. Delivery, six to eight weeks ARO.

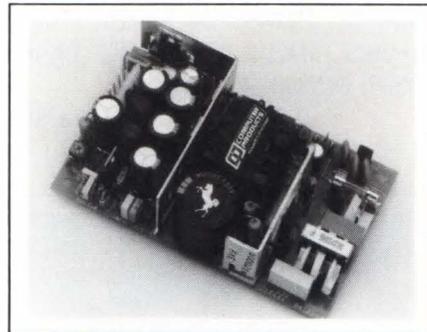
Toko America Inc, 1250 Feehanville Dr, Mount Prospect, IL 60056. Phone (312) 297-0070.

Circle No 383

POWER SUPPLIES

- *Accept any input from 85 to 264V ac without jumpers*
- *Available in single- and triple-output versions*

NFS40 40W switching power supplies will accept any input from 85 to 264V ac without the need for jumper wires or a switch. Versions are available with single outputs (5, 12, 15, or 24V) and triple outputs (various combinations of 5, 12 and 15V). The supplies will regulate down to zero output load and feature a



VME Dream Card

The HK68/V30 is the card you've been dreaming of.

This fully-loaded single-board VME microcomputer combines the highly sought-after qualities of high speed and advanced on-card functionality. Now you can have high-end performance for UNIX and real-time applications. Standard equipment:

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- Up to 1 MB of EPROM
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- Single 8-bit parallel port
- Mailbox interrupt support.

Optional equipment includes on-board 68881/68882 FPP, SCSI interface and Time-of-Day clock with battery back-up.

HEURIKON CORP

Take Heurikon's HK68/V30 for a grand tour today.
Call toll-free: 800-356-9602 (ext. 503).
Telefax: 608-251-1076
3201 Latham Drive ■ Madison, WI 53713

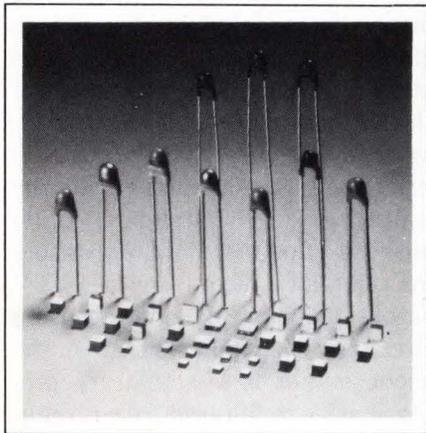
CIRCLE NO 153

COMPONENTS & POWER SUPPLIES

160,000-hour MTBF. Line regulation is $\pm 0.5\%$ max and efficiency specs at 70%. The supplies are approved by UL, CSA, and VDE, and provide sufficient line filtering to meet FCC limit B and VDE limit A line-conducted noise specs. Of the eight models making up the line, only the NFS40-7608 is stocked as a standard product. From \$59 (1000).

Computer Products Inc., 2900 Gateway Dr, Pompano Beach, FL 33069. Phone (305) 974-5500. TWX 510-956-3098.

Circle No 384



THERMISTORS

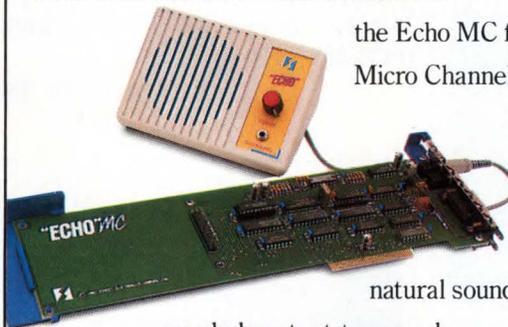
- Feature a 0.75% beta-value tolerance
- Provide low-thermal-conductivity leadouts

NTC thermistors in the 640-6 and 645-0 stable-line families have a 0.75% beta-value tolerance and a 25°C resistance (R25) with a 3% tolerance. These tolerances allow the units to achieve an accuracy of 1.5°C at 85°C. The 640-6 family comprises 16 devices with R25 values between 2.7 and 470 kΩ. The 645-0 family offers four devices with R25 values of between 5 and 10 kΩ and 38-mm low-thermal-conductivity nickel leads. The thermistors operate from -40 to +125°C. When operating at their maximum rated power of 250 mW, the units function over a reduced range of 0 to +55°C. Gld 0.38 (10,000) for thermistors

SPEECH

For over seven years the Echo™ speech output products from Street Electronics have set the standard for reasonably priced voice equipment.

There are now two new Echo speech boards for MS DOS®-based machines:



the Echo MC for the IBM Personal System/2 Micro Channel™ products, and the ECHO PC+ for the IBM PC and compatibles. These products utilize the new Echo speech chip which processes digitized voice; natural sounding LPC voice, and unlimited vocabulary text-to-speech.

OEM quantity pricing for all these products is under \$100.

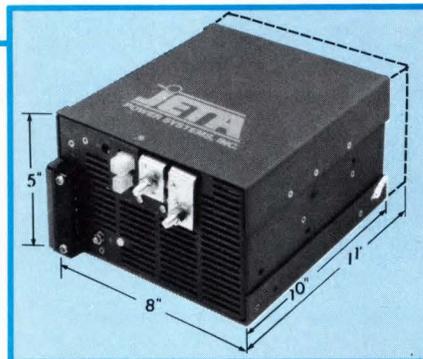
The Street CMOS speech processing chip, custom LPC vocabulary generation, and technology licensing are also available.

Street Electronics Corporation

6420 Via Real, Carpinteria, CA 93013 (805) 684-4593

CIRCLE NO 154

We'll give you
an inch...
and
**1200
WATTS**



Where other manufacturers require 11" or more in a 1200 watt design, JETA gives you the same output power ratings *plus* an extra inch. So you can fit even more into your CAD/CAM/CAE systems, mini-main frames or communications products.

For compact high-current single and multiple output power supplies from 500 to 2200 watts, contact JETA.

See EEM pages D1706-1708



POWER SYSTEMS, INC.

2675 Junipero Avenue ■ Signal Hill, CA 90806
Tel: 213/427-0095 ■ TWX: 510-101-1804 ■ FAX: 2134262417

CIRCLE NO 155

NEW! SWITCHMODE POWER SUPPLIES FROM STOCK

- 2 to 48 VDC Outputs
- Automatic Current Sharing On All Outputs
- N+1 Capabilities



MULTIPLE OUTPUT



- 350 to 1500 Watts
- 3 to 15 Outputs

SINGLE OUTPUT



- 400 to 3000 Watts in 5" x 8" Standard Package
- 155,000 Hrs. Demonstrated MTBF

Hot Plug-In FAULT TOLERANT (N+1) POWER SYSTEMS



- Two to Six Supplies
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- Internal Isolation Diodes (Option)

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(818) 882-0004 • FAX (818) 998-4225

CIRCLE NO 156

COMPONENTS & POWER SUPPLIES

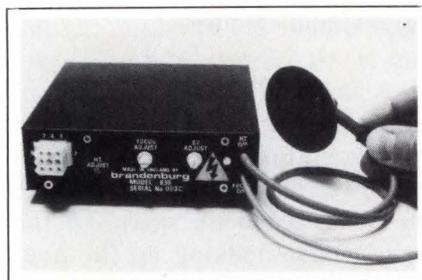
with a 5% R25 tolerance.

Philips, Components Division, Box 523, 5600 AM Eindhoven, Netherlands. Phone (040) 757189. TLX 51573.

Circle No 385

Mepco/Centralab Inc, Box 760, Mineral Wells, TX 76067. Phone (817) 325-7871.

Circle No 386



HV SUPPLY

- Powers high-resolution CRTs
- Features full regulation

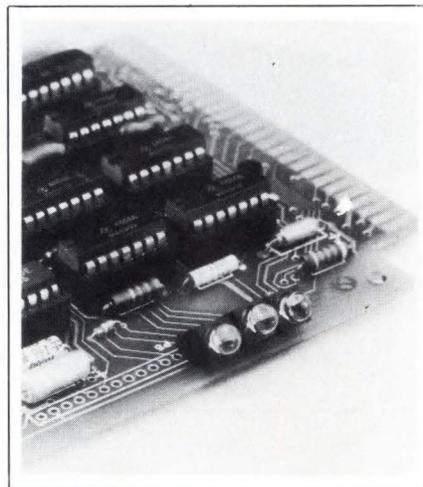
You can employ the 836A shadow-mask supply for high-resolution monitors. The fully-stabilized dc/dc converter operates from a 20 to 30V input. The supply provides a 22 to 28 kV output voltage at currents as high as 1.2 mA for the final anode of the CRT; the adjustable output voltages for the CRT's focus and G2 grids; and a -200V output for the control grid. The standard model includes a floating, stabilized supply for the CRT's heater and a +400V output to power dynamic focusing circuitry. The ripple voltage on the anode output is less than 5V p-p. Static zero- to full-load output regulation on the anode output is 15V. Around £70 (1000).

Brandenburg Ltd, 939 London Rd, Thornton Heath, Surrey CR4 6JE, UK. Phone 01-689-0441. TLX 946149.

Circle No 388

Astec (USA) Ltd, 2880 San Thomas Expressway, Suite 200, Santa Clara, CA 95051. Phone (408) 748-1200. TLX 6839191.

Circle No 389



INDICATORS

- Mount at a 45° angle for better visibility
- Meet UL94V-0 requirements

PC45 Series LED indicators mount on pc boards with the LED at a 45° angle. This design makes the devices well-suited for applications requiring viewing from an elevated position. Designed for use on the edge of boards positioned low in a cabinet or rack, the LEDs are compatible with side-by-side or front-to-back mounting. The indicator housings meet UL94V-0 flammability requirements and are available in red, green, amber, and yellow, all with a choice of diffused or nondiffused encapsulation. Typical operating current and voltage drop spec at 20 mA and 2.1V, respectively. From \$0.22 (1000). Delivery, stock to six weeks ARO.

Data Display Products, Box 91072, Los Angeles, CA 90009. Phone (800) 421-6815; in CA, (213) 640-0442.

Circle No 387

CHASSIS

- Delivers full PC/AT functionality
- Includes a filtered cooling system

The 7515-24H chassis is designed for installation inside a standard 19-in. rack. When appropriately configured, the chassis can serve as a node, server, or gateway in a network. With its 15-slot backplane,

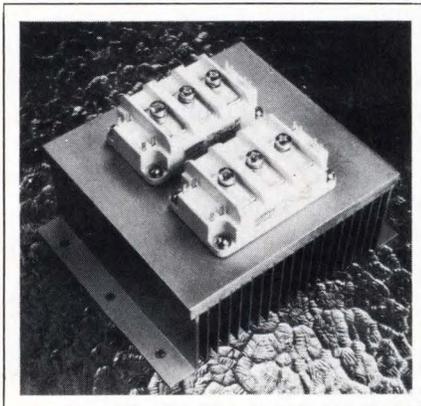
COMPONENTS & POWER SUPPLIES



the chassis delivers full PC/AT functionality. The rugged steel enclosure includes a disk-carrier assembly that can hold as many as four half-height drives, a drive-area cover door, a system reset button, and a 200W power supply with a filtered cooling system. A positive-pressure buildup inside the chassis prevents dust particles from damaging any installed drives. From \$1395.

Industrial Computer Source,
5466 Complex St, Suite 208, San
Diego, CA 92123. Phone (619) 279-
0084. FAX 619-541-1138.

Circle No 390



HEAT SINKS

- For natural-convection and forced-air applications
- Achieve 0.024 to 0.08°C/W thermal resistance

Series 6760 bonded-fin heat sinks are designed for both natural-convection and forced-air applications. Available in nine standard sizes, the heat sinks feature mounting-hole patterns that accept all standard-power-module packages. Forced-air models are designed to

More than just another pretty interface... *this keyboard is intelligent.*

If you're designing electronic instrumentation for medical, aerospace, military or industrial applications, a Foster designed Application-Specific User Interface Terminal (ASUIT™) can increase functionality, simplify design and lower your total costs.

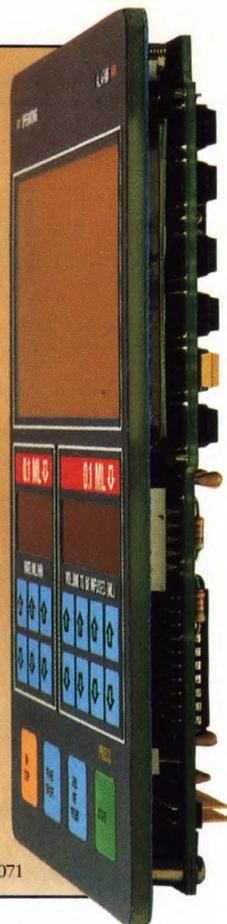
Foster manufactures embossed, snap-action, tactile keyboards which can include second board systems (piggybacks) to interface with your host instrument, providing functions such as:

- keyboard encoding
- display and display control
- system controller functions

Eliminate multi-vendors and "over design" of your instrument. Foster Engineering offers complete product support, from engineering to production and testing for standard systems, custom systems, custom keyboards and graphics. Send for our Designer's Guide or call today.

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1 West Lone Cactus Drive, Phoenix, Arizona 85027 (602) 492-0071



CIRCLE NO 157

with 5 outputs... to **2200** WATTS



Main output to 300A. Our 2200 watt, UL/CSA/VDE/IEC compliant, power supply offers 1 to 5 outputs. Standard features include DC OK, FCC EMI filter, power fail, remote inhibit, remote margining, electronic soft start and more—many of which would be costly options elsewhere.

High reliability is derived from a reduced component count, high-voltage transistor V-I load reshaping for maximum SOA and careful thermal management to ensure the best operating environment for critical components.

For reliable high-current single and multiple output power supplies from 500 to 2200 watts, contact JETA.

See EEM pages D1706-1708

JETA POWER SYSTEMS, INC.
2675 Junipero Avenue ■ Signal Hill, CA 90806
Tel: 213/427-0095 ■ TWX: 510-101-1804 ■ FAX: 2134262417

CIRCLE NO 158

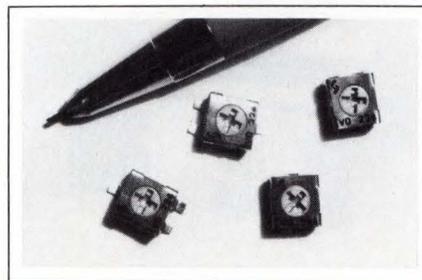
COMPONENTS & POWER SUPPLIES

accept standard muffin fans with a 4.12-in.-square mounting hole pattern. These models are 5.25 in. high and have mounting surfaces ranging from 7×4.78 to 16×10.78 in. Thermal resistance ranges from 0.024 to 0.08°C/W. Natural-convection models are 3.130 in. high and available in 7- and 12-in. lengths. These units have a 7.375-in.-wide mounting sur-

face and are available with or without mounting flanges. Thermal resistance ranges from 0.22 to 0.30°C/W. \$39.37 (100) for the 7-in. natural-convection model. Delivery, eight to 12 weeks ARO.

Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400.

Circle No 391



TRIMMERS

- Have a temperature coefficient of 50 ppm/°C
- Provide surface mounting

The TS5Y-series single-turn, miniature, surface-mounting trimmer potentiometers feature automatic and manual adjustment. A clutch mechanism prevents damage to the trimmers. For nominal values of 100Ω or higher, the trimmers feature a ±50 ppm/°C temperature coefficient. They come with nominal resistance values between 10Ω and 1 MΩ with either ±10% or ±20% tolerance. The trimmers have a power rating of 0.2W at 85°C and an operating temperature range of -55 to +155°C. Housed in a sealed package, the trimmers can withstand vapor-phase or reflow soldering, and water cleaning. \$0.20 (1000).

Sfernice, 199 blvd de la Madeleine, 06021 Nice Cedex, France. Phone 93446262. TLX 470261.

Circle No 392

Ohmtek, 2160 Liberty Drive, Niagara Falls, NY 14304. Phone (716) 283-4025. TWX 710-524-1653.

Circle No 393

CIRCUIT BREAKERS

- Address the problem of nuisance tripping
- Current ratings of 5 to 20A

To address nuisance tripping problems, S Series circuit breakers incorporate a solenoid. To reset a remote breaker, you simply actuate the solenoid. The solenoids will operate from 24V ac, 120V ac, or 24V dc. The devices are available in 250V ac and 50V dc versions with

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Designed for military applications where vibration and sudden impact may occur

• Ideal for airborne and shipboard equipment.
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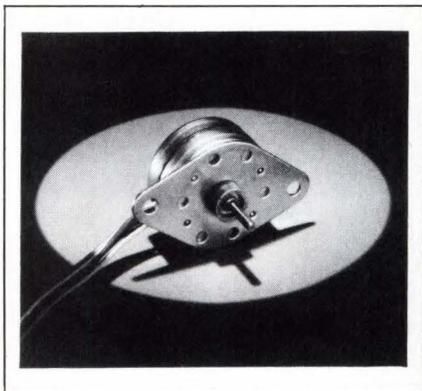
CIRCLE NO 254

COMPONENTS & POWER SUPPLIES

current ratings of 5, 10, 15, and 20A. At 200% of rating, tripping time is 6 to 30 sec. Acceptable solenoid-actuation techniques range from a simple switch to a radio-receiver signal. \$85 (10).

Casco/Maitland, Box 947, Roswell, GA 30077. Phone (404) 475-3192.

Circle No 394



STEPPER MOTORS

- Operate from either 5 or 12V dc supplies
- Suitable for portable equipment

With a housing that measures only 1-in. in diameter, Series M82100 and N82100 stepper motors are well suited for portable equipment where space is at a premium. The motors have step angles of 7.5 and 15°, respectively. Both operate from either 5 or 12V dc supplies and are available for unipolar or bipolar operation. The PM motors come equipped with permanently lubricated bronze sleeve bearings. Holding torques for unipolar or bipolar units spec at 1.3 and 1.5 oz-in. on 7.5° models, and 0.7 and 1.0 oz-in. on 15° models. M82100 motors have a 1.1×10^{-4} gm² rotor moment of inertia and a $\pm 0.5^\circ$ step-angle tolerance. These parameters equal 4.5×10^{-5} gm² and $\pm 1^\circ$, respectively, for N82100 motors. Bipolar motor, \$5.35 (500). Delivery, four to 12 weeks ARO.

Airpax Co, Box 868, Cheshire, CT 06410. Phone (203) 272-0301.

Circle No 395

EDN August 18, 1988

the unlimited design benefits of miniature metal tubing.



design benefits number 107 and 108

PUNCHING/NOTCHING

Round, square, rectangular and elongated holes can be punched or notched in miniature tubing to tight tolerances. Single or multiple configurations are available depending upon tube diameter and wall thickness. Check the know-how, fabrication expertise and alloy selection at Uniform Tubes. Phone toll free 1-800/321-6285 or send for our design packed folder.

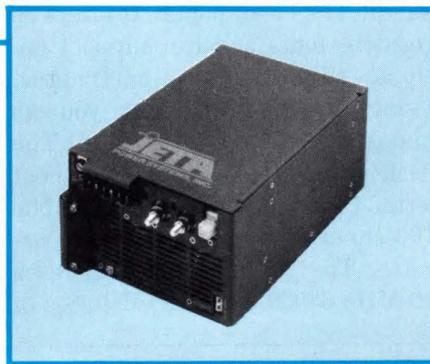


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CIRCLE NO 264

...and we'll back
it up!
750 WATT
multiple output
battery backup
supply.



For safe and orderly system shutdown in the event of blackout or even brownout situations, choose our battery backup switching power system.

JETA's proven multiple output power supply technology combines with a dual-stage charger, boost converter and 48V battery to provide your system with unlimited holdup time (depending on battery capacity) in the event of AC line failure.

2-YEAR WARRANTY on all models

At JETA, we back up all our power supplies with a full two-year guarantee. After we beat them up and then burn them in, we're confident that you'll receive the finest high-current power supplies built.

For single and multiple output power supplies from 500 to 2200 watts, contact JETA. We back them up.

See EEM pages D1706-1708



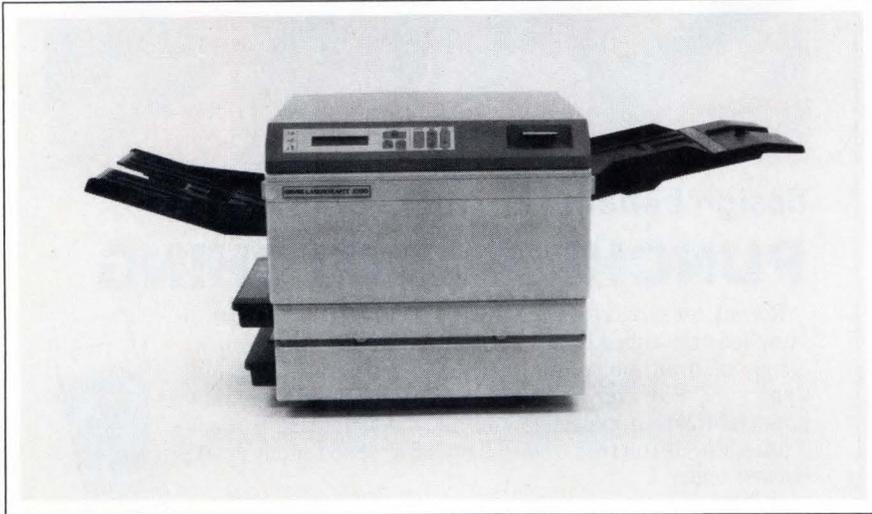
POWER SYSTEMS, INC.

2675 Junipero Avenue ■ Signal Hill, CA 90806
Tel: 213/427-0095 ■ TWX: 510-101-1804 ■ FAX: 2134262417

CIRCLE NO 177

NEW PRODUCTS

COMPUTERS & PERIPHERALS



LASER PRINTER

- Prints 22 pages/minute
- Offers 36 resident fonts

The Lasergrafix 2200 laser printer prints at 22 pages/minute and can handle 11×17-in. paper. It offers 36 resident fonts and can support optional slim-card font cartridges. Using an HP-GL emulator, you can make B-size CAD drawings. The desktop printer has two 250-sheet letter-size paper cassettes and one 100-sheet ledger/letter paper cassette. The print engine includes a 16-MHz 68000 μ P and 7M bytes of

RAM. The engine can concurrently process two B-size pages of bit-mapped graphics at a 300×300-dot/in. resolution. An optional QMS 80-VE interface connects to a Versatec parallel interface on a CAD workstation to emulate the Versatec V-80 electrostatic printer. Another optional printer interface lets the printer attach to IBM 3276, 3274, or 3174 controllers for printing on the IBM 3270 network. \$14,995.

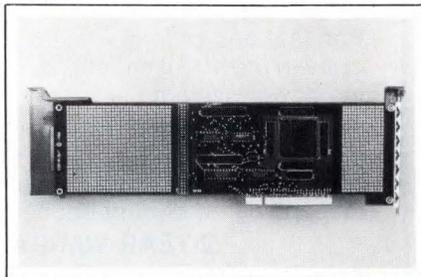
QMS Inc, 1 Magnum Pass, Mobile, AL 36618. Phone (205) 633-4300.

Circle No 351

PROTOTYPE BOARD

- For the Micro Channel in IBM's PS/2 model 70 computer
- Features the One Chip Plus interface chip

The One Chip Plus add-in prototype development board for the IBM PS/2 model 70 computer features the company's 88C01 interface chip for the Micro Channel. You can program the chip to decode addresses for extended memory, expanded memory, ROM, and multiple I/O ports. It also supports the Micro Channel DMA arbitration and burst-mode DMA. The chip sup-



ports all speeds of the model 70: 16, 20, and 25 MHz. The hardware kit includes the board with decoded memory and an interface for connecting a logic analyzer. The software kit includes the extended and expanded memory driver (LIM 4.0 specification), design utilities, and

sample adapter-description files. An acquisition engine provides high-level programming commands for data acquisition and I/O control. Kits range from \$495 to \$995.

Capital Equipment Corp, 99 S Bedford St, Burlington, MA 01803. Phone (617) 273-1818.

Circle No 352



MULTIPLEXER

- Adds four buffered ports to any RS-232C or RS-422 port
- Transmit and receive buffers

The DP4 is a 4-port multiplexer for RS-232C or RS-422 interfaces. Each of the four ports contains a 4992-byte transmit data buffer and a 4992-byte receive data buffer. The unit lets the user simultaneously communicate with as many as four devices operating at the same or different baud rates from 75 to 38.4k baud. You can individually select the baud rates, parity, and word length. The unit supports XON/XOFF and hardware handshaking techniques. It is one of the company's CMCNet II system products and can create a system that supports as many as 6400 users via multidrop. Menu-driven control software for IBM PCs and compatible computers is included free of charge. \$695.

Connecticut MicroComputer Inc, Box 186, Brookfield, CT 06804. Phone (203) 354-9395. TWX 710-456-0052.

Circle No 353

68030 - VME

The Real *Single Board Computer*

The TP32V from Tadpole

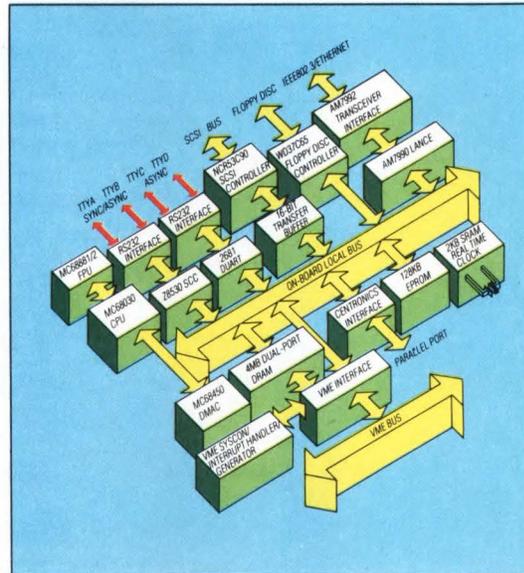
• The Philosophy •

Designed for optimum system performance from a single full IEE 1014 VME board, the TP32V needs no other cards, piggy-backs or mezzanines to deliver the full potential of the 16-33 MHz MC68030. To maximise overall throughput, all the on-board I/O facilities were designed to take advantage of hardware transfer buffers, DMA facilities and advanced DRAM arbitration techniques between competing resources.

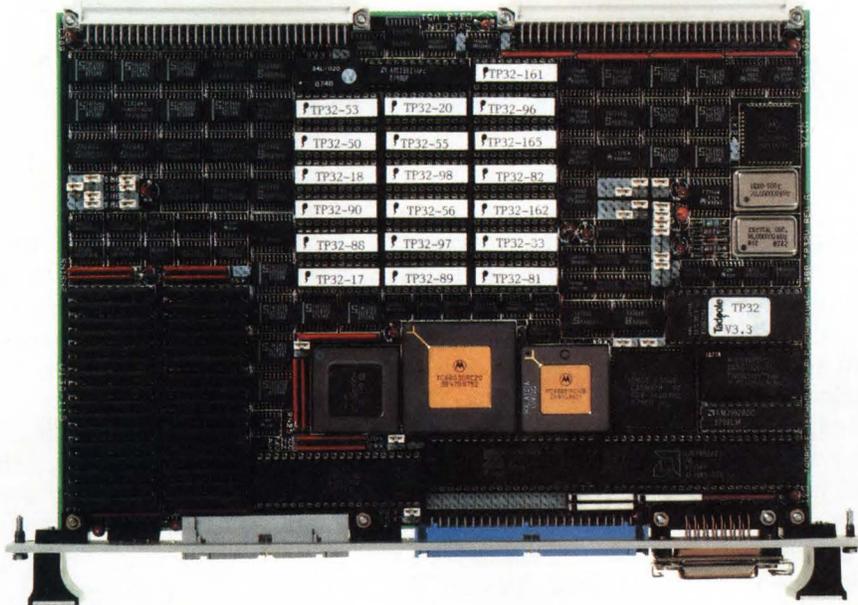
• The Specification •

- MC68030 16-33MHz
- MC68450 4-channel DMA controller
- 4Mb multi-ported nibble-mode DRAM
- AMD Lance IEEE 802.3 Ethernet with DMA
- Z8530 SCC giving two DMA-driven RS232 sync/asynchronous ports and two further RS232 asynchronous ports
- NCR 53C90 DMA-driven synchronous or asynchronous SCSI interface
- Floppy disk controller
- Full VME Rev C.1 IEEE 1014 interface
- 64-512Kb EPROM
- Battery-backed RTC/SRAM
- Full debug monitor
- Optional MC68881/2 FPU
- TP-IX/68K version of UNIX V.3.1*
- NFS, RFS, TCP/IP

• The Design •



• The Evidence •



Tadpole Technology
the driving force in 32-bit design

Tadpole Technology plc

Titan House, Castle Park,
Cambridge, CB3 0AY, UK.
Tel: 0223 461000
Fax: 0223 460727

Tadpole Technology Inc

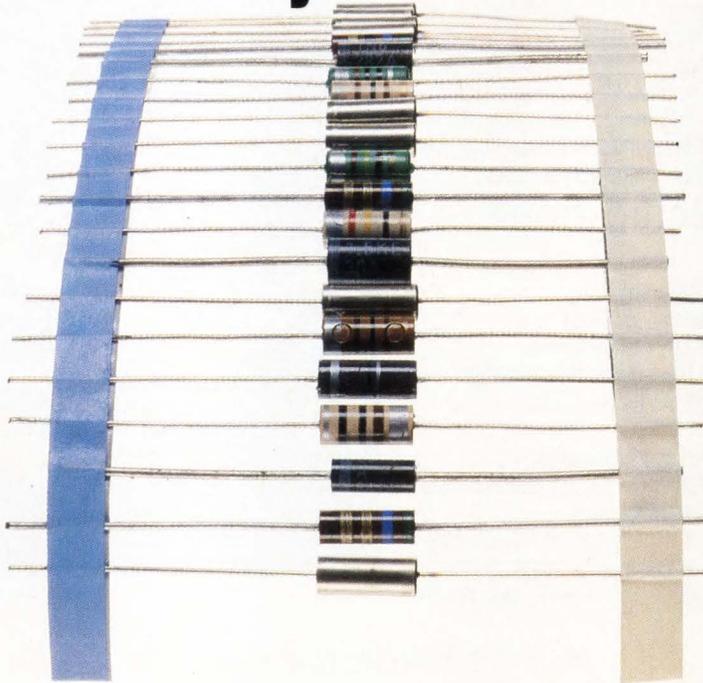
Reservoir Place,
1601 Trapelo Road, Waltham,
Massachusetts 02154, U.S.A.
Tel: 0101-617-890-8898
Fax: 0101-617-890-7573

2157 O'Toole Avenue,
Suite F, San Jose,
California 95131, U.S.A.
Tel: 0101-408-435-8223
Fax: 0101-408-435-8432

T A D P O L E

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VRTX is a trademark of Ready Systems *TP-IX V.3.1 is derived from UNIX V.3.1

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1421 Clarkview Road Baltimore, MD 21209-9987, USA Telephone (301) 296-7000 ext 304 Telex 898095 CATALYST

WORKSTATIONS

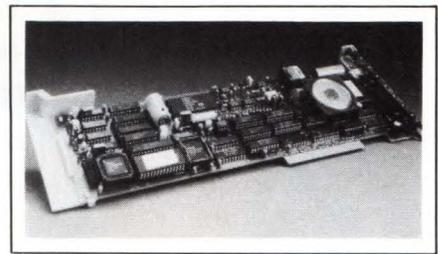
- Six models for the VAXstation 2000 family
- Feature an 8-bit plane graphics coprocessor

The VAXstation 2000 family has six new models of desktop workstations. They incorporate the company's MicroVAX II CPU and floating-point unit along with a choice of a 15- or 19-in. color monitor. A graphics coprocessor module supports 8-bit planes and offers 256 simultaneous colors from a palette of 16M colors. A 12M-byte memory-expansion module provides a total of 14M bytes of memory. The models are available with either a VMS or an Ultrix operating system. Optional main storage comes in 42M-, 71M-, or 159M-byte hard disks. Backup options include a 96M-byte streaming tape and a 1.2M-byte floppy-disk drive. Applications developed for the VAXstation II/GPX,

3200, and 3500 workstations are fully compatible with the new systems. A system with an 8-bit plane coprocessor, 6M bytes of memory, and a 15-in. color monitor costs \$13,830.

Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Phone (617) 493-4297.

Circle No 354



operates at 4800 bps. This version conforms to V27-ter specifications. The modem's software indicates the condition of the modem-interface signals. Along with the modem's onboard speaker, the software provides information on call progress. In addition, the software provides autodial and autoanswer facilities using commands based on the AT and CCITT V25-bis standards. You can use the autodial software with synchronous communication packages that don't feature autodial functions. You enter dial commands via an independent control channel, which lets you monitor the call's status. A nonvolatile RAM stores

MODEM CARD

- Allows microcomputer-to-mainframe communication
- Includes autodial and autoanswer facilities

The Syncro-24-PS add-in synchronous modem for IBM-PS/2 computers or Micro Channel Architecture systems lets these systems access mainframe computers. The modem transmits at 2400 bps. It complies with CCITT V26-bis specifications. Another version, the Syncro-48-PS,

spectron

Gravity Referenced
Measures: Slope, Tilt Angle, Pitch
37 Years Experience

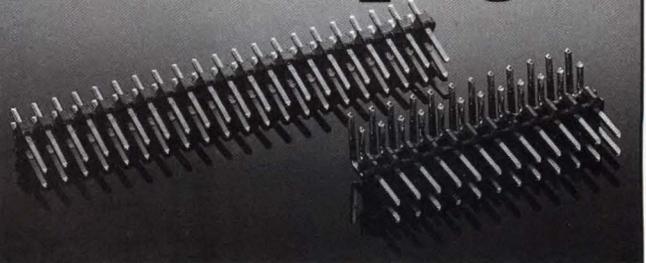
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4000 Via Pescador, Camarillo, California 93010-5049
Phone: (805) 484-4221 • TWX 910-343-6468 • FAX: (805) 484-4113

the modem's configuration data. Syncro-24-PS, £545; Syncro-48-PS, £645.

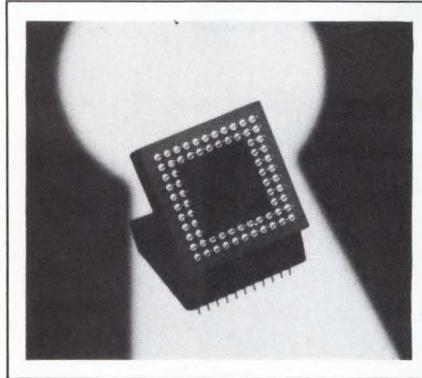
Mayze Systems Ltd, Delta 900, Great Western Way, Swindon, Wiltshire SN5 7XQ, UK. Phone (0793) 511789. TLX 445707.

Circle No 355

ENCRYPTION KEY

- Protects against unauthorized access of data
- Meets NSA's communication security requirements

The Smart Key encryption device prevents unauthorized data access. This key-like device provides eight pairs of redundant gold contacts that plug into a 16-pin socket. It contains a 12-MHz CMOS μ P with ROM for program storage and a 16k- or 64k-byte EEPROM. With the key inserted in a system, you can initialize a new key number,



write a record into memory, read a record from memory, read a status register, compute a checksum, read the key number assigned during initialization, and erase the data storage area. The unit measures 5.08x2.54x1.27 cm and weighs less than 12g. It meets NSA's communications security (COMSEC) requirements. \$375 (OEM).

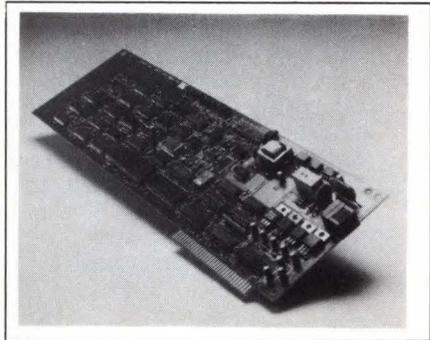
Tracor Inc, 6500 Tracor Lane, Austin, TX 78725. Phone (512) 926-2800.

Circle No 356

VOICE PROCESSOR

- Has an 8k-sample/sec μ -law codec
- Compresses voice data 2 to 1, using 32k-bps ADPCM encoding

The AVA (Automated Voice Administrator) single-slot IBM XT and AT board for processing voice communications has an 8k-sample/sec μ law codec; it compresses voice data 2 to 1, using adaptive differential-pulse-code modulation (ADPCM) encoding. It compresses data further by deleting silent periods and



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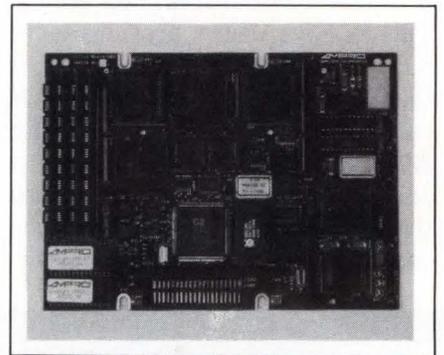
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COMPUTERS & PERIPHERALS

restoring them on transmission. A telephone interface has ring detection, DTMF reception and dialing, and call progress tones. Its features include an unattended answering routine, unattended directory assistance, personalized messages, call screening, and an information bulletin board. Customized software lets you adapt the system to user protocols. \$1100.

Zymacom Inc, 2 Lyberty Way, Westford, MA 01886. Phone (617) 692-4500.

Circle No 357



MOTHER BOARD

- Performs IBM PC/AT motherboard functions in 46 in³
- Employs a 3-chip set and consumes 8W

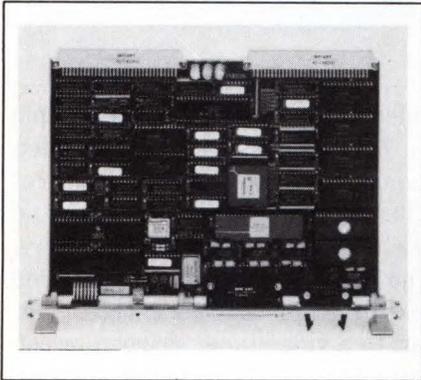
The Little Board/286 mother board performs the functions of an IBM PC/AT computer in 46 in³. It measures 8x5¼x1 in. The board employs a 3-chip set, called the 286 AT, which permits the integration of an AT-compatible system with 13 ICs. The board consumes 8W and operates from 0 to 70°C. It lets you substitute bubble memory, EPROM, and nonvolatile RAM for disk drives in embedded applications and harsh environments. The board comes with an 8- or 12-MHz 80286 CPU, an AT-compatible BIOS, a 512k- or a 1M-byte dynamic RAM, and a floppy-disk controller for two 5¼- or 3½-in. disk drives. In addition, it has two RS-232Cs serial ports, a parallel port, a keyboard port, three counter/timers with

COMPUTERS & PERIPHERALS

seven DMA channels, and 16 levels of interrupts. \$739 (OEM).

Ampro Computers Inc, 1130 Mountain View, Alviso Rd, Sunnyvale, CA 94089. Phone (408) 734-2800. TLX 4940302.

Circle No 358



COMM BOARD

- Provides X.25 communication over wide-area networks
- Implements layers 1 to 3 of the OSI communications model

Simplifying the software that you have to write during systems integration, the CC-125 VME Bus X.25 communications card conforms to the X.213 specification for data transfer to layer 4 functions of the OSI (open systems interconnection) model. The board implements layers 1 to 3 of the OSI model. Layer 1 operates according to the X.21 bis (V.24/V.28) standard, and layer 2 to the LAPB (link access procedures balanced) protocol standard. The board's layer 3 software handles the X.25 packet-level protocol and imposes flow control to prevent the communications link from overloading. Messages are passed between the CC-125 and the VME Bus system's layer 4 functions via dual-port RAM on the CC-125. These messages, coded according to X.409 recommendations, are transferred to the dual-port RAM in the form of network-service data units that can be as much as 4k bytes long. The 68000-based board is suitable for transmitting packet-switched data over public or private data networks

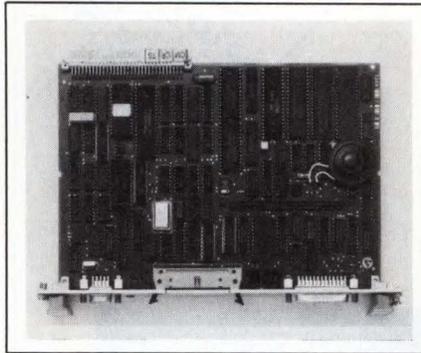
at bit rates as high as 64k bps. \$3675.

Compcontrol bv, Stratumsedijk 31, 5600 AD Eindhoven, The Netherlands. Phone (040) 124955. TLX 51603.

Circle No 359

Compcontrol Inc, 15466 Los Gatos Blvd, Suite 109-365, Los Gatos, CA 95032. Phone (408) 356-3817. TWX 510-601-2895.

Circle No 360

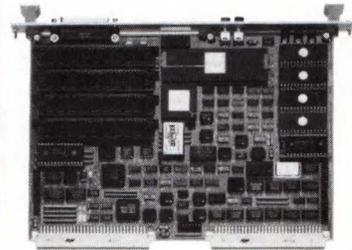


INDUSTRIAL PC

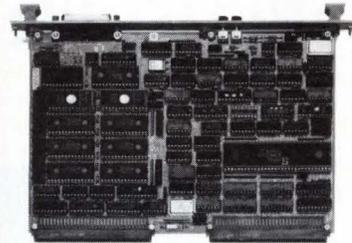
- Puts an IBM PC/AT-compatible in VME Bus systems
- Allows memory expansion to 16M bytes

The PX4000 VME Bus module allows you to implement an IBM PC/AT-compatible computer in VME Bus systems. The 2-board sandwich runs an 80286 μ P and an optional 80287 math coprocessor at 8 MHz. It includes all the ports you'd expect to find on a standard PC/AT—that is, a keyboard, a monitor, a printer, and floppy-disk interfaces—and runs the MS-DOS operating system. However, the module's video output provides an IBM CGA-compatible interface as standard. In addition to accessing the board's 512k bytes of onboard dynamic RAM, processor and DMA channels can transparently access additional memory via the VME Bus. If you use the μ P's protected addressing mode, it can access as much as 16M bytes of memory. The onboard RAM is also accessible to other VME Bus masters. A hard-disk controller board that operates in conjunction with

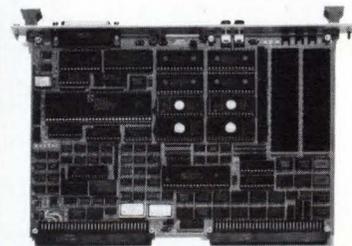
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Industries Inc.

TL Industries, Inc.
2541 Tracy Rd.
Toledo, OH 43619
Call Meg Niehaus
1-800-227-8144 (outside Ohio)
or 419-666-8144
FAX 419-666-6534

the PX4000 is also available. \$2500.

Philips, Industrial and Electro-Acoustic Systems Div, 5600 MD Eindhoven, The Netherlands. Phone (040) 788620. TLX 35000.

Circle No 367

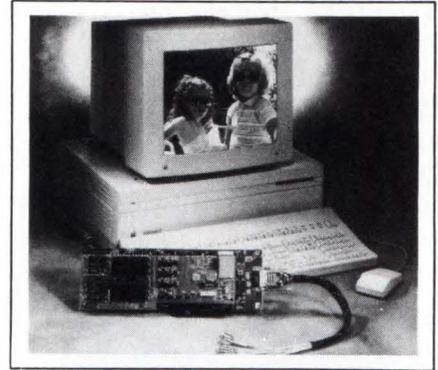
Philips Electronic Instruments Inc., 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800.

Circle No 361

FRAME GRABBER

- Displays color motion pictures on the Macintosh II
- Captures 640x480-pixel images with 32,768 colors

The ColorCapture plug-in frame grabber board for the Macintosh II computer captures color images from video cameras, VCRs, or still-



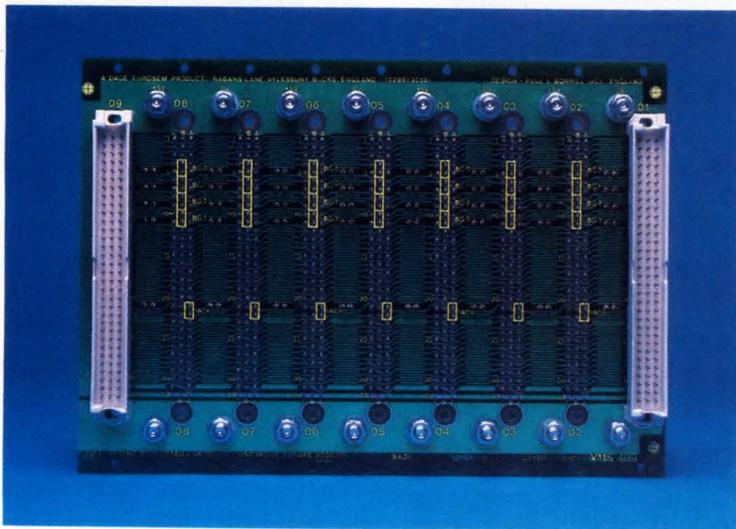
video equipment. It displays them in 1/30 sec (real time) on a video monitor. The board captures 640x480 square-pixel images and can display them in 32,768 colors. The board lets you edit images, add text or graphics to color video, output to a video tape, sharpen or soften edges, build multiple images, and perform animations. An external trigger lets you synchronize captured images with other events. A zoom, pan, and scroll controller provides real-time magnification. The 60-Hz DT2270 version comes with an NTSC composite output and outputs for the three RS-170 RGB signals. The 50-Hz DT2270 version provides PAL composite output and the three CCIRR RGB outputs. \$2995.

Data Translation Inc., 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700. TLX 951646.

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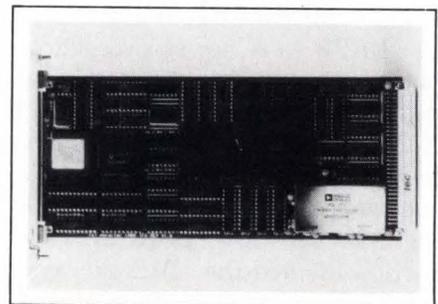
- Impedance - 60Ω (±2)
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- Crosstalk - <200 mV



DAGE PRECISION INDUSTRIES, Inc.

46701 Fremont Blvd.
Fremont, CA 94538 (415) 683-3930

CIRCLE NO 180



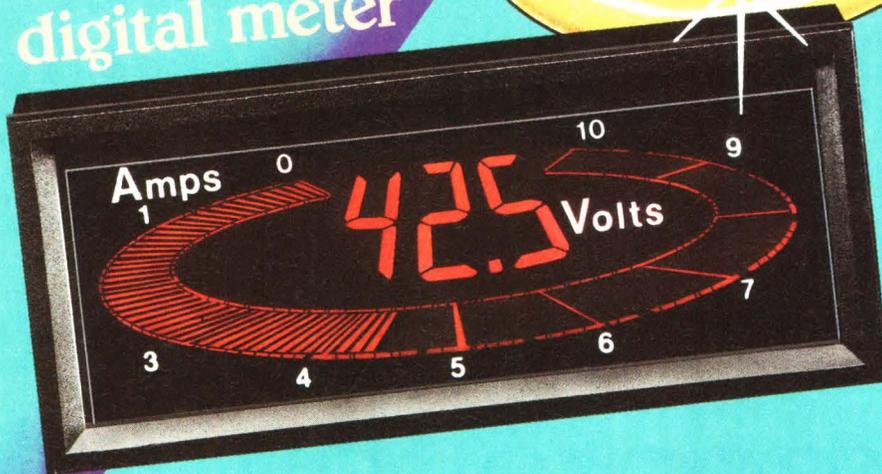
IMAGING BOARD

- Digitizes up to 256 gray-scale levels
- Provides 768x512-pixel max resolution

The TFG single-Eurocard image processing module includes a frame grabber, a frame store, a

A MARRIAGE MADE IN NEW HAMPSHIRE!

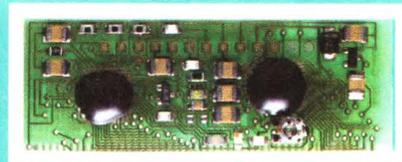
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The inside story! Modutec's chip-on-board technology.



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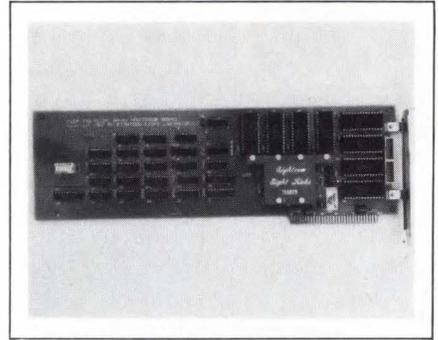
CIRCLE NO 181

Transputer to process the image, a color look-up table, and video output. The board accepts CCIR and RS-170A video signals and digitizes them to 256 gray-scale levels with a 768x512-pixel max screen resolution. You can externally or internally synchronize the frame grabber and cascade boards to capture RGB color inputs. The board stores the image on a 0.5M-byte video RAM. It provides an additional 1M byte for the onboard T800 or T414 Transputer. The color look-up table lets you generate color images containing 256 colors from a palette of 262,144 colors. Four 20M-bps Transputer links allow the Transputer to communicate with other processors. By using adapter modules you can insert the board into an IBM PC, or couple it to a VME Bus, a Q bus, or a Nu bus. The vendor's software support includes compilers for Occam, C, Fortran, Pascal, Parallel Prolog, and the He-

lios Transputer operating system. DM 7800.

Parsytec GmbH, Juelicher Strasse 338, 5100 Aachen, West Germany. Phone (0241) 166000. FAX (0241) 1660050.

Circle No 363



ARRAY PROCESSOR

- Provides 8M 32-bit flops on IBM PCs and compatibles
- Contains a 60k-byte cache for program and data

The PL800 is an array-processing board for the IBM PC, PC/XT, PC/AT, and compatibles. A floating-point engine contains a 32-bit floating-point multiplier, a 40-bit ALU, and four 40-bit accumulators. The multiplier and ALU are in a pipeline and operate in parallel. This combination can perform 8M 32-bit flops. The board also contains a 16-bit RISC (reduced instruction set com-

puter) Integer Processor, a 60k-byte cache for program and data, a host interface processor, and an auxiliary interface processor. A 32-bit instruction fetch, two 32-bit data fetches, and a 32-bit store occurs within 244 nsec. You can use from one to eight boards by writing control programs in Fortran, C, or Pascal. PL800 with support software, \$1995.

Eighteen Eight Laboratories, 771 Gage Dr, San Diego, CA 92106. Phone (619) 224-2158.

Circle No 364

Thermography enters

With the advent of the Hughes Aircraft Company Probeye® 7300 Thermal Video System, thermal imaging has entered a new age—the Age of Information.

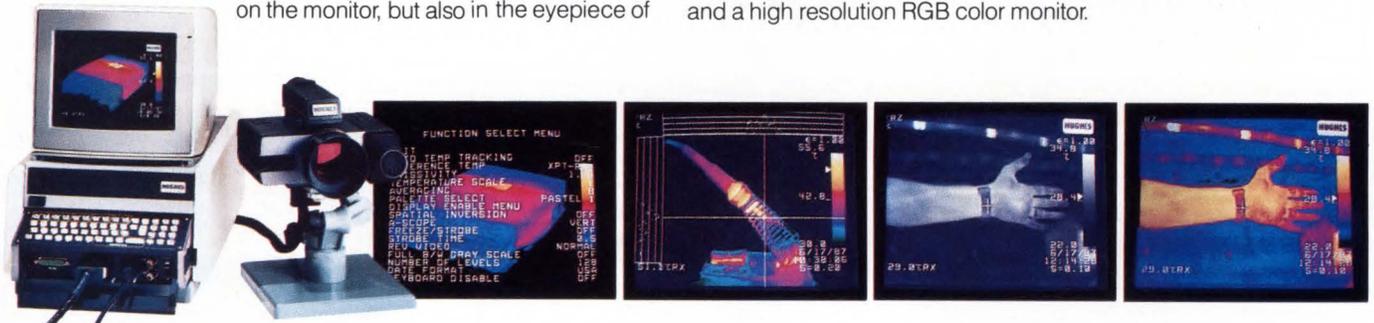
In a single package, the Hughes Probeye 7300 Thermal Video System gives you a powerful, intelligent laboratory system with instant field diagnostic capability. Immediately select, store, quantify and analyze. And, most importantly, *understand* the information—with more speed and accuracy than ever before! Hughes has leapfrogged the competition with state-of-the-art features that can't be matched by any other system.

Start with superior resolution—240 infrared lines. Not just on the monitor, but also in the eyepiece of

the portable imager. Which means you can perform on-the-spot detection and analysis in up to 128 distinct levels.

All-electric operation does away with liquid nitrogen or argon gas. The imager uses ac or battery power for full field portability—it goes wherever the information originates.

Fully automatic operation allows you to concentrate on detection and analysis. Precise comparisons are facilitated by built-in features. There's no exhaustive training process. No delays. Just point and read. And, the design is extremely functional—in addition to the portable imager and attached CRT viewfinder, the system includes a processor with built-in, full-function keyboard and a high resolution RGB color monitor.



VME BUS SBC

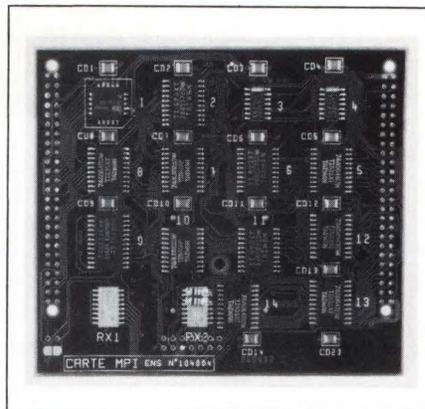
- Features a 33-MHz 68030 CPU and a VSB interface
- An 8-bit extension bus lets you add plug-in modules

The 68-31 single-board computer for the VME Bus in a single-slot, double Eurocard form factor features a 33-MHz 68030 CPU and the VME Subsystem Bus (VSB) interface. The additional interface lets you dedicate different operations to either the VSB or the VME Bus for optimum bus utilization. The board contains 4M bytes of dual-ported dynamic RAM, an optional 68882 floating-point coprocessor, a cache capable of burst fills with zero wait states, two synchronous or asynchronous serial ports, mailbox interrupts, and a Processor EXtension bus (PEX). The PEX bus is an 8-bit asynchronous bus linked to the CPU that lets you add more functions via plug-in modules. Modules with

SCSI or floppy-disk interfaces are available. The board complies with the VME Bus IEEE-1014 standard and operates as a 32-bit address/data bus master. \$4295.

Radstone Technology, 1 Blue Hill Plaza, Pearl River, NY 10965. Phone (800) 368-2738; in NY, (914) 735-4661.

Circle No 365



INTERFACE MODULE

- Lets you interface I/O boards to the iPSB bus
- Sends and receives iPSB messages

The MPI module lets you interface I/O cards to the Multibus II iPSB. This 81.3x80x12.3-mm module needs two I/O card connectors. It occupies a single slot. The module's iPSB interface can send or receive normal or broadcast messages without data fields. In the I/O space, the

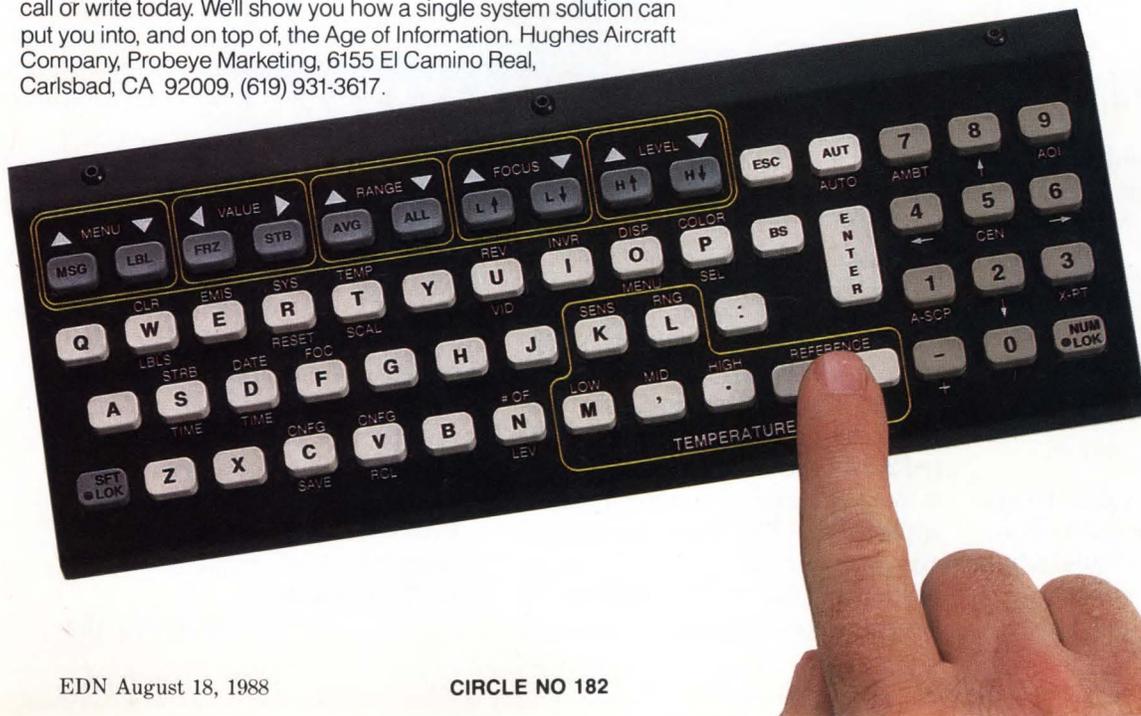
board provides for 8- or 16-bit data transfers and a 2k-byte board address region. In the interconnect space, the module provides 32 header registers, which you can program using an EEPROM. The interface module doesn't require I/O-board firmware. Approximately \$220.

Centralp Automatismes, 16 rue Gabriel Péri, 92120 Montrouge, France. Phone (1) 42533617. TLX 632380.

Circle No 366

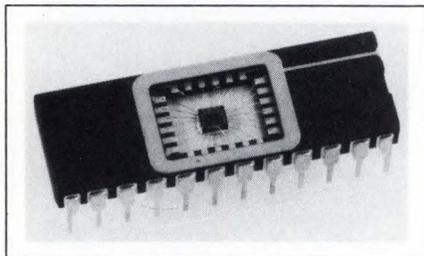
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NEW PRODUCTS

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GaAs DIGITAL ICs

- Pin-compatible with 100K ECL
- Minimized propagation delay

Fabricated in the company's depletion-mode GaAs process, the G100113 quad driver, G100141 8-bit shift register, G100179 carry-lookahead generator, and G100180 6-bit adder are all drop-in replacements for 100K ECL types. Typical propagation delays are 500 psec for the quad driver, 1150 psec for the 8-bit shift register, 1000 psec for the carry-lookahead generator, and 1450 psec for the 6-bit adder. All of these high-performance digital ICs are compatible with ECL single power supplies of $-4.5V$ (100K systems) and $-5.2V$ (10K systems). Each is fully compensated for voltage and temperature variations. Samples are available now in 24-pin DIPs; flat-pack versions will be available in the fourth quarter of 1988. \$25 (G100113 and G100179), \$26 (G100141), and \$32 (G100180), (100).

Microwave Semiconductor Corp., 100 School House Rd, Somerset, NJ 08873. Phone (201) 563-6300. TLX 833473.

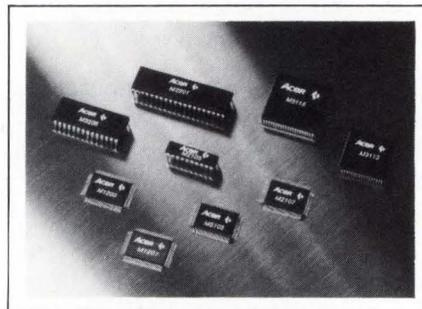
Circle No 400

PS/2 CHIP SET

- Contains 8 chips
- For IBM Models 25 and 30

The PC86 chip set provides the system-, graphics-, and peripheral-control functions needed to build a fully compatible PS/2 Model 25 or 30. The chip set's architecture and partition-

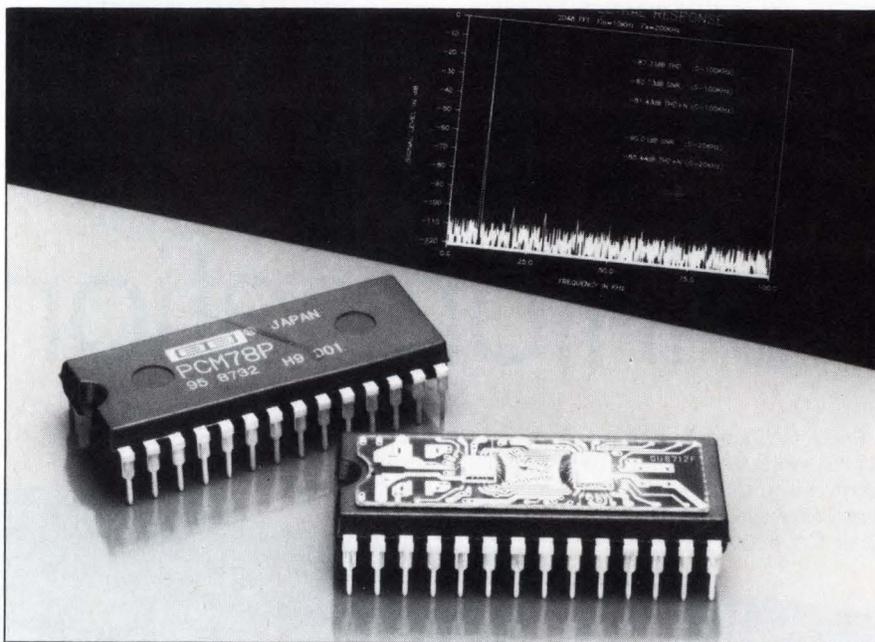
ing simplify manufacturing and reduce costs by making it possible to use only a few chips to build a range of systems. The set consists of the M1201 system controller for the 8086 and V30; the M1203 address and data buffer; the M2107 input/output controller; the M3113 and M3115 MCGA and Hercules graphics controllers; the M3205 50-MHz, 256×18 -color palette; the M2201A bidirectional printer interface; and the M5103 floppy-disk-drive interface. You can use the graphics-control and peripheral-control chips separately for PC/XT and PC/AT



computers. A PC86 sample set costs \$88; \$77 (1000).

US Sertek, 926 Thompson Pl, Sunnyvale, CA 94086. Phone (408) 733-3174.

Circle No 401



16-BIT AUDIO ADC

- 4- μ sec conversion time
- Typical THD+N of -88 dB

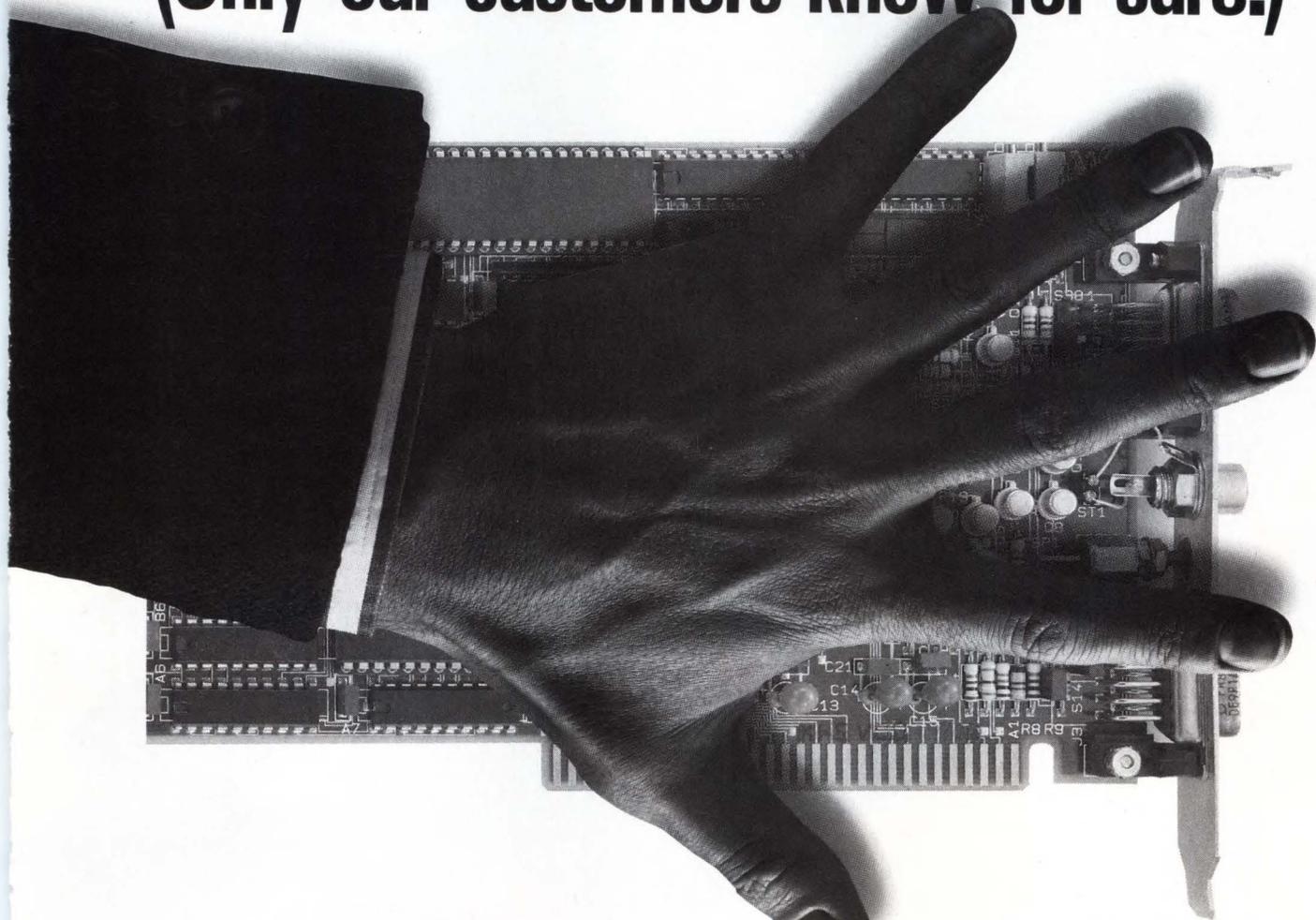
The PCM78P 16-bit successive-approximation A/D converter has a typical total-harmonic-distortion-plus-noise (THD+N) spec of -88 dB (-82 dB max) at full scale. The chip is designed and tested for dynamic applications. The chip uses bipolar circuitry for its precision analog portion and low-power CMOS for its logic and clock functions. It features

a typical 4- μ sec conversion time (5 μ sec max). The PCM78P's $\pm 3V$ input range interfaces to S/H amplifiers, and its two serial-output modes facilitate interfacing. The chip includes an internal clock and reference, is 100% tested to data-sheet specifications, operates from ± 5 to $\pm 12V$ supplies, and dissipates 600 mW. \$39.90 (100).

Burr-Brown Corp., Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 402

What's so special about our 8 BIT microcontrollers? (Only our customers know for sure.)



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Not only is MHS one of the world leaders in CMOS microcontroller technology, with over 7 million units delivered to date. We're also one of the fastest suppliers, delivering both standard and customized parts to our customers' doorsteps - anywhere in the world - in no time flat.

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80C52	8	256	3	Quick ROM 18 MHz
83C154	16	256	3	Extra modes
83C158	32	256	3	Extra modes
80C752	4	128	2	Keyboard controller

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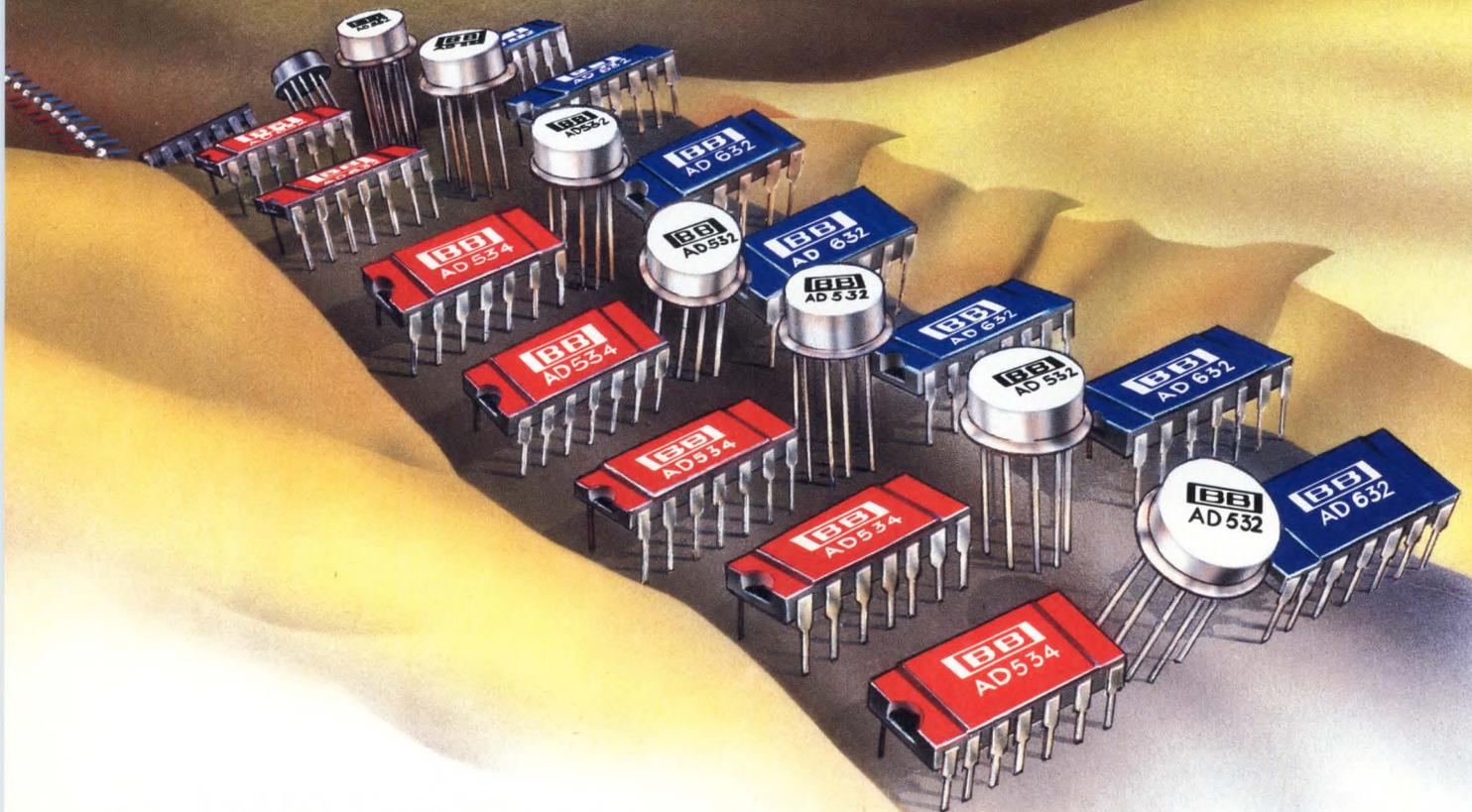
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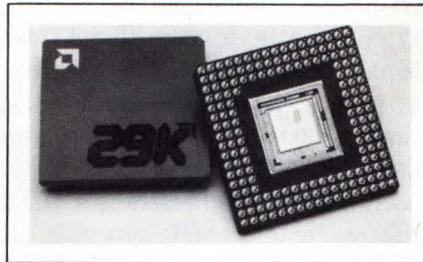
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617-273-9022 Burlington, MA
313-474-6533 Farmington, MI
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Aspen Sales, Inc.
801-467-2401 Salt Lake City, UT



CIRCLE NO 184



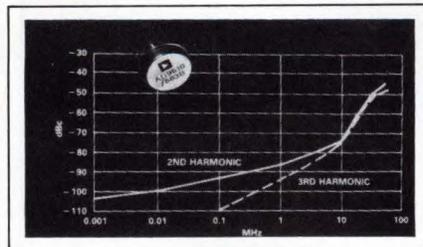
32-BIT RISC μ P

- 16- to 25-MHz versions
- 11- to 17-MIPS performance

The Am29000 32-bit, RISC μ P is now available in three different speeds: 16 MHz (11 MIPS), 20 MHz (14 MIPS), and 25 MHz (17 MIPS). The company is also supplying samples at beta sites of a 30-MHz (20-MIPS) version. The 25-MHz version delivers 36,000 dhrystones, using the V1.1 benchmark with 8k bytes of instruction and data cache. It delivers 15 MIPS at 24,000 dhrystones using V1.1 with an inexpensive video RAM. The dhrystone benchmark represents the typical mix of instructions anticipated for large-integer applications. 16-MHz version, from \$174 (100).

Advanced Micro Devices Inc.,
Box 3453, Sunnyvale, CA 94088.
Phone (408) 732-2400.

Circle No 403



100-MHz OP AMP

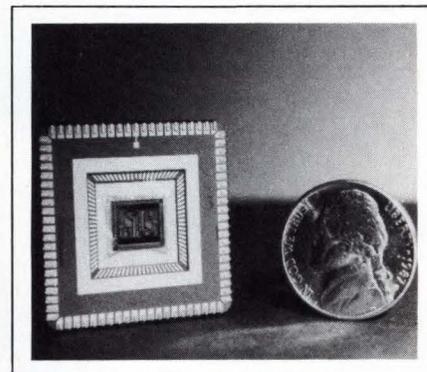
- Conforms to MIL-STD-883B
- Has 3000V/ μ sec slew rate

The AD9610 current-feedback operational amplifier is now available in a MIL-STD-883B version that is specified over the -55 to $+125^\circ\text{C}$ temperature range. The AD9610TH/883B offers a minimum -3 -dB bandwidth of 80 MHz and a maximum total-harmonic distortion

of -50 dB with a 20-MHz input tone. Rise- and fall-times are <4 nsec with a 5V step; the settling time is 25 nsec (max) to 0.1%. A minimum slew rate of 3000V/ μ sec is guaranteed. Maximum dc specifications at 25°C include: ± 1 -mV offset voltage, ± 15 - μA inverting-node bias current, and ± 50 - μA noninverting-node bias current. The AD9610TH/883B operates from ± 15 V supplies and comes in a TO-8 metal can. \$125 (100).

Analog Devices Inc., Box 9106,
Norwood, MA 02062. Phone (617)
329-4700. TLX 924491.

Circle No 404



SYNTHESIZER

- Has a resolution of 0.01 Hz
- 30-MHz input reference

The Q2334 single-chip digital frequency synthesizer provides a μ P interface to control variable frequency and phase signals that are synthesized from a master reference. It includes two independent frequency synthesizers for use in full-duplex systems, spread-spectrum analysis, or quadrature oscillator applications. The chip provides a resolution of more than 0.01 Hz with an input signal clocking the phase accumulator at 30 MHz. Signal-to-noise ratios are 72 dB for quantization noise and 76 dB for phase noise. The Q2334 is available in 68-pin packages. \$98 (1000).

Qualcomm Inc., 10555 Sorrento
Valley Rd, San Diego, CA 92121.
Phone (619) 587-1121.

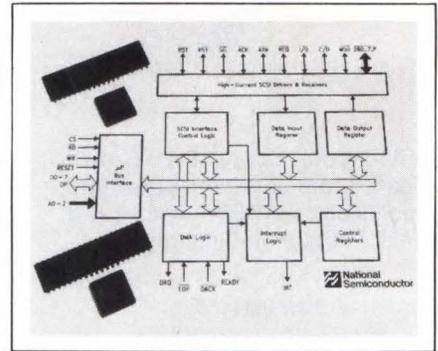
Circle No 405

CMOS SCSI ICs

- Pin-compatible with NMOS types
- 10-mA max supply current

Targeted at new and upgraded system designs, the DP8490 and DP5380 are CMOS devices that comply with the SCSI standard and are pin-compatible with the NMOS

NCR5380 device. The DP8430/5380 types operate from a 10-mA max supply current. The devices feature a typical acknowledge-to-request time of 60 nsec, and a typical request-to-acknowledge time of 30 nsec. The DP8490 features a DMA rate as high as 4M bytes/sec. It powers up as a 5380 device until an enhanced mode opens three regis-



ters. Two registers control interrupts, and a third register, Extra Mode, has a sophisticated arbitration scheme that controls the use of the SCSI bus; μ P polling, as used with 5380 devices, is not required. A loop-back test mode allows users to fully test the device's functions, including DMA operation. The DP8490 also includes a phase-mismatch interrupt that detects a phase mismatch in any information transfer, decreasing dead-time on the SCSI bus. For users not making software changes, the DP5380 is available; it has the same speed and power features as the DP8490. The devices are available in 40-pin DIPs and 44-pin PLCCs. DP8490, \$8; DP5380, \$7.50 (100).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-4960. TLX 346353.

Circle No 406

Where CMOS Ends, DMOS Begins.

Enter the dimension of superior performance with the high-speed and high-voltage capabilities of DMOS from Topaz Semiconductor.

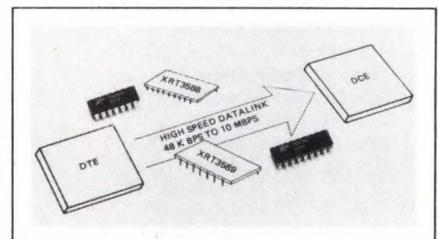
Our DMOS devices go beyond CMOS to provide the versatility you need for a wider range of applications, from subnanosecond switching to high-voltage power requirements. DMOS can speed through your toughest applications, or surpass the 40-volt reach of CMOS to extend your system capabilities up to 800 volts.

And Topaz has the DMOS products you need in a variety of configurations, from high-voltage DIP arrays to high-speed, surface-mount discrete devices.

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Topaz Semiconductor, 1971 N. Capitol Avenue, San Jose, CA 95132-3799
TEL (408) 942-9100 TWX 910-338-0025 FAX (408) 942-1174



INTERFACE CHIP SET

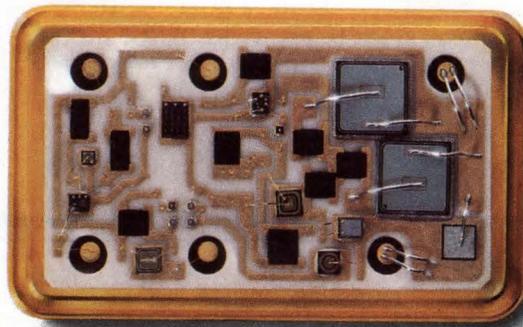
- CCITT V.35/Bell 306 compatible
- Data rates to 10M bps

The XR-T3588 (driver) and XR-T3589 (receiver) provide a communications link between data-terminal and data-communications equipment at rates from 48k bps to 10M bps. The XR-T3588 contains three independent drivers; the XR-T3589

SOLID STATE RELAY

Short Circuit Protection and True Output Status

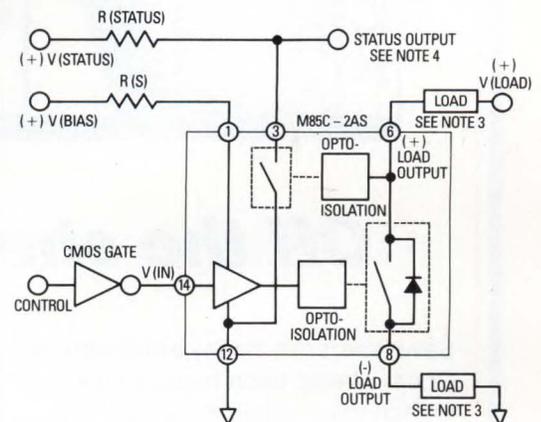
- Current Overload Protection
- Optical Isolation
- TTL & CMOS Compatible Control
- DESC Drawing Number Pending



PART #M85C-2AS

ELECTRICAL CHARACTERISTICS (-55°C to +105°C unless otherwise noted)				
	Min	Max	Units	
Bias Voltage (V_{BIAS})	3.8	32	V_{DC}	See Note 1
Bias Current (I_{BIAS})		15	mA	$V_{BIAS} = 5V_{DC}$
Control Voltage (V_{IN})	0	18	V_{DC}	
Control Current (I_{IN})		250	μA	$V_{IN} = 5V_{DC}$
Turn-Off Voltage	3.2		V_{DC}	-55°C to +25°C
$V_{IN(OFF)}$	2.8		V_{DC}	+25°C to +105°C
Turn-On Voltage		0.5	V_{DC}	-55°C to +25°C
$V_{IN(ON)}$		0.3	V_{DC}	+25°C to +105°C
Continuous Load Current		2.0	A	-55°C to +25°C
I_{LOAD}		400	mA	+105°C
Output Trip Current (I_{TRIP})	8 (TYP.)		A	+25°C, 100 ms
Continuous Load Voltage (V_{LOAD})		60	V_{DC}	
Output Leakage Current (I_{LEAK})		2	mA	
On-Resistance (R_{ON})		0.28	Ohms	
Turn-On Time (T_{ON})		3.0	ms	
Turn-Off Time (T_{OFF})		1.0	ms	
Status Voltage (V_{STATUS})	1	18	V_{DC}	
Status Current (I_{STATUS})		0.6	mA	See Note 2

- Notes: 1. Series resistor is required for bias voltages above 6V_{DC}. $R_S = (V_{BIAS} - 5V_{DC})/15 \text{ mA}$
 2. A pull up resistor is required for the status output. $R_{STATUS} = V_{STATUS}/600 \mu A$
 3. Output will drive loads connected to either terminal (sink or source).
 4. Status output is low when the load output is off.



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Teledyne Solid State, 12525 Daphne Avenue, Hawthorne, California 90250.

contains three independent receivers. Both ICs are TTL compatible and feature a power-down mode for each of the drivers and receivers. According to the company, the chip set is the first monolithic version to fully meet the CCITT V.35 requirements. The XR-T3588 comes in a 14-pin ceramic DIP; the XR-T3589 in an 18-pin ceramic DIP. \$4.18 (5000).

Exar Corp., Box 49007, San Jose, CA 95161. Phone (408) 434-6400. TWX 910-339-9233.

Circle No 407

18-BIT AUDIO DAC

- Includes deglitcher and reference
- Features 4x oversampling

Serving as the back-end of a digital audio system, the ZDA1801A 18-bit D/A converter includes a built-in deglitcher circuit and a voltage reference. The chip's guaranteed



front-to-back total harmonic distortion plus noise (THD+N) is 98 dB over the full 20-Hz to 20-kHz audio range. The ZDA1801A operates at a 4x oversampling rate. The DAC module comes in an electrostatic- and electromagnetic-shielded package with dimensions of 3.0x1.6x0.45 in. \$99 (100). Delivery, stock to six weeks ARO.

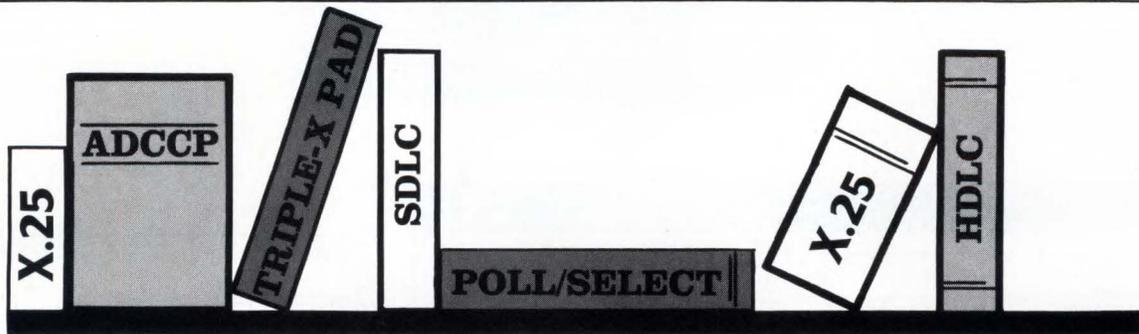
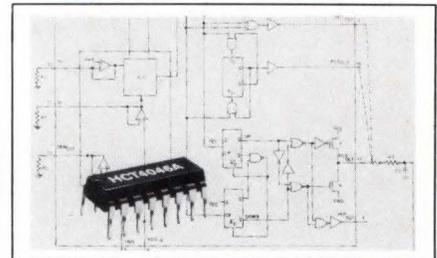
Analog Solutions, 85 W Tasman Dr, San Jose, CA 95134. Phone (408) 433-1900.

Circle No 408

PLL IC

- Has three phase comparators
- 0.4% frequency linearity

The CD54/74HC/HCT4046A PLL IC contains three different phase comparators—an exclusive OR gate, a J-K flip-flop, and an R-S flip-flop. Its VCO characteristics include a frequency linearity of 0.4% and a typical frequency stability of 0.11%/°C. The VCO operates at frequencies as high as 38 MHz, and a VCO-inhibit pin provides on/off control and limits power consumption when the PLL is in standby mode. A signal input and a comparator



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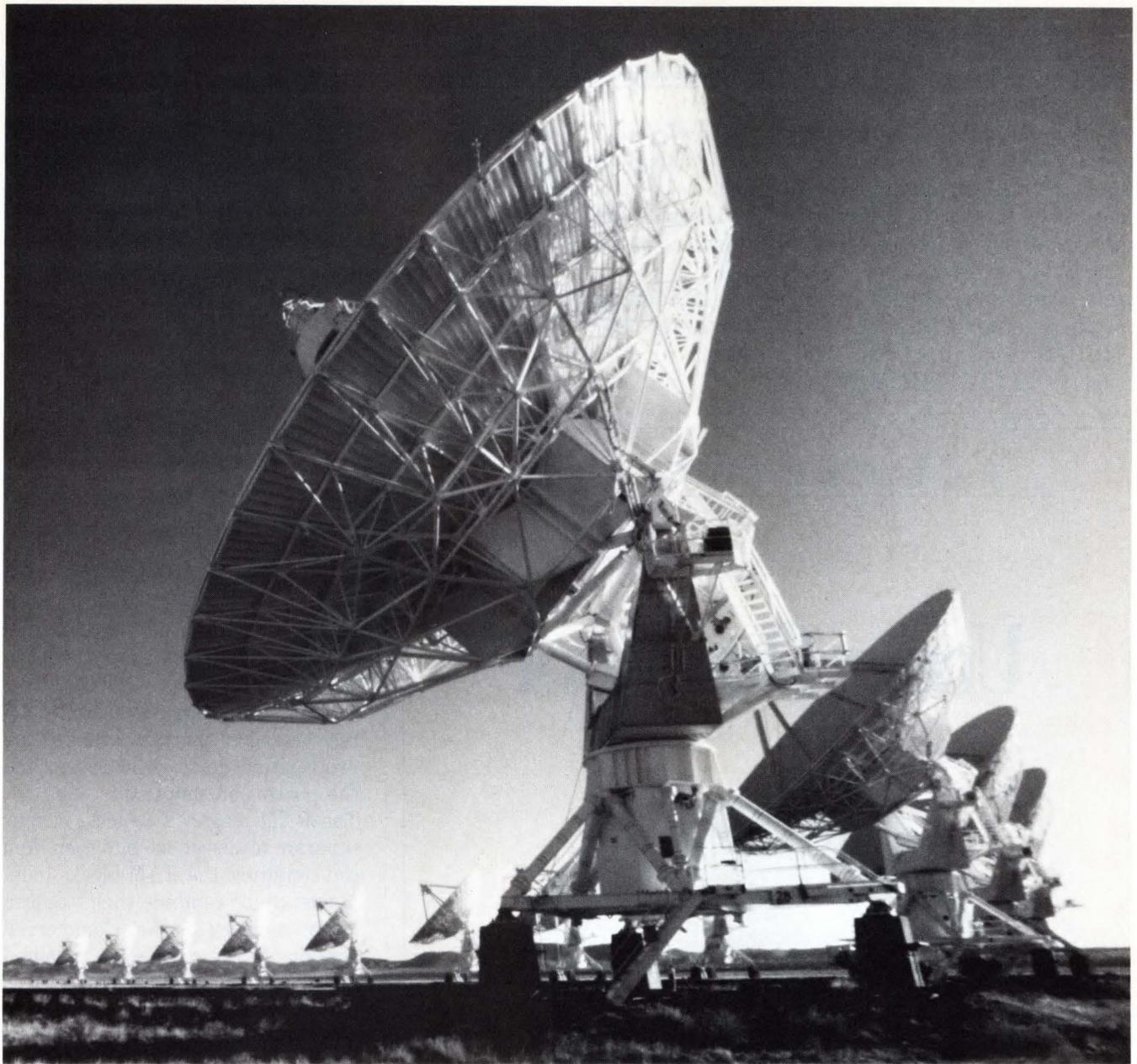
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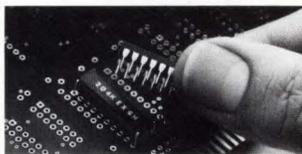
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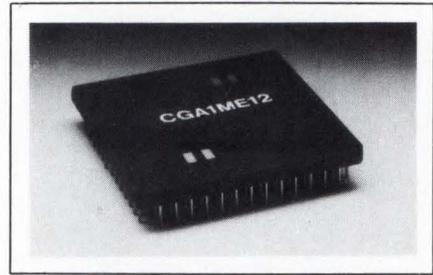
OUTSIDE THE U.S. CONTACT: Europe: Mektron NV, Ghent, Belgium Japan: Rogers Inoue Corp., Nagoya
Brazil: Rogers Coselbra, Sao Paulo Singapore, Hong Kong, Taiwan: Dynamar

input are common to all three phase comparators. You can couple the signal input directly to logic-level voltages or indirectly to millivolt-level signals through a series capacitor. The chip's self-bias circuit keeps small signals within the linear range of the input amplifiers. The CD54/74HC4046A operates from a 2 to 6V supply; the CD54/74HCT4046A op-

erates from a TTL-compatible 4.5 to 5.5V supply. Available packages include 16-pin ceramic and plastic DIPs and a 16-pin surface-mount version. In 16-pin plastic DIP, \$1.62 (100).

GE Solid State, Box 2900, Somerville, NJ 08876. Phone (201) 685-6562.

Circle No 409



ECL GATE ARRAY

- 4584 equivalent gates
- 3.5-nsec typical access time

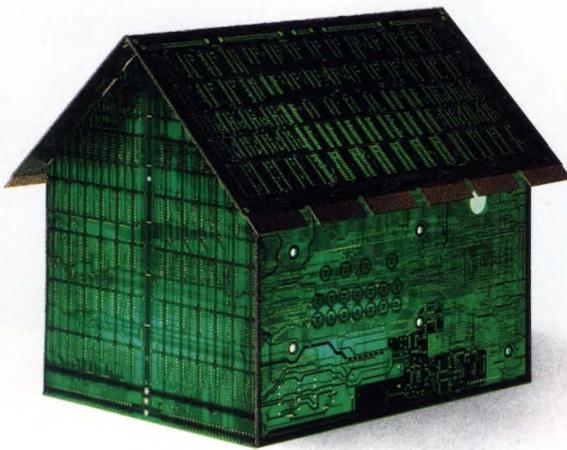
Featuring a typical access time of 3.5 nsec, the CGA1ME12 ECL gate array contains 4584 equivalent gates max, 1280 bits of configurable RAM, and 120 I/O cells. Interfaced among the I/O cells are 34 dedicated power pins. The gates are laid out in 12 contiguous rows with each row containing 1320 transistors and 1320 resistors. For the typical gate, the propagation delay is 300 psec, and the power consumption is 300 μ W. The RAM megacell consists of four separate blocks of 320 bits each. You can configure the RAM blocks independently or combine them to form larger memory blocks. Commercial versions of the device are specified for operation over the 0 to 70°C temperature range. Depending on gate utilization, quantity, and test requirements, prices start at \$150. Nonrecurring engineering costs range from \$40,000 to \$60,000.

Raytheon Company, Semiconductor Div, 350 Ellis St, Mountain View, CA 94043. Phone (415) 966-7639.

Circle No 410

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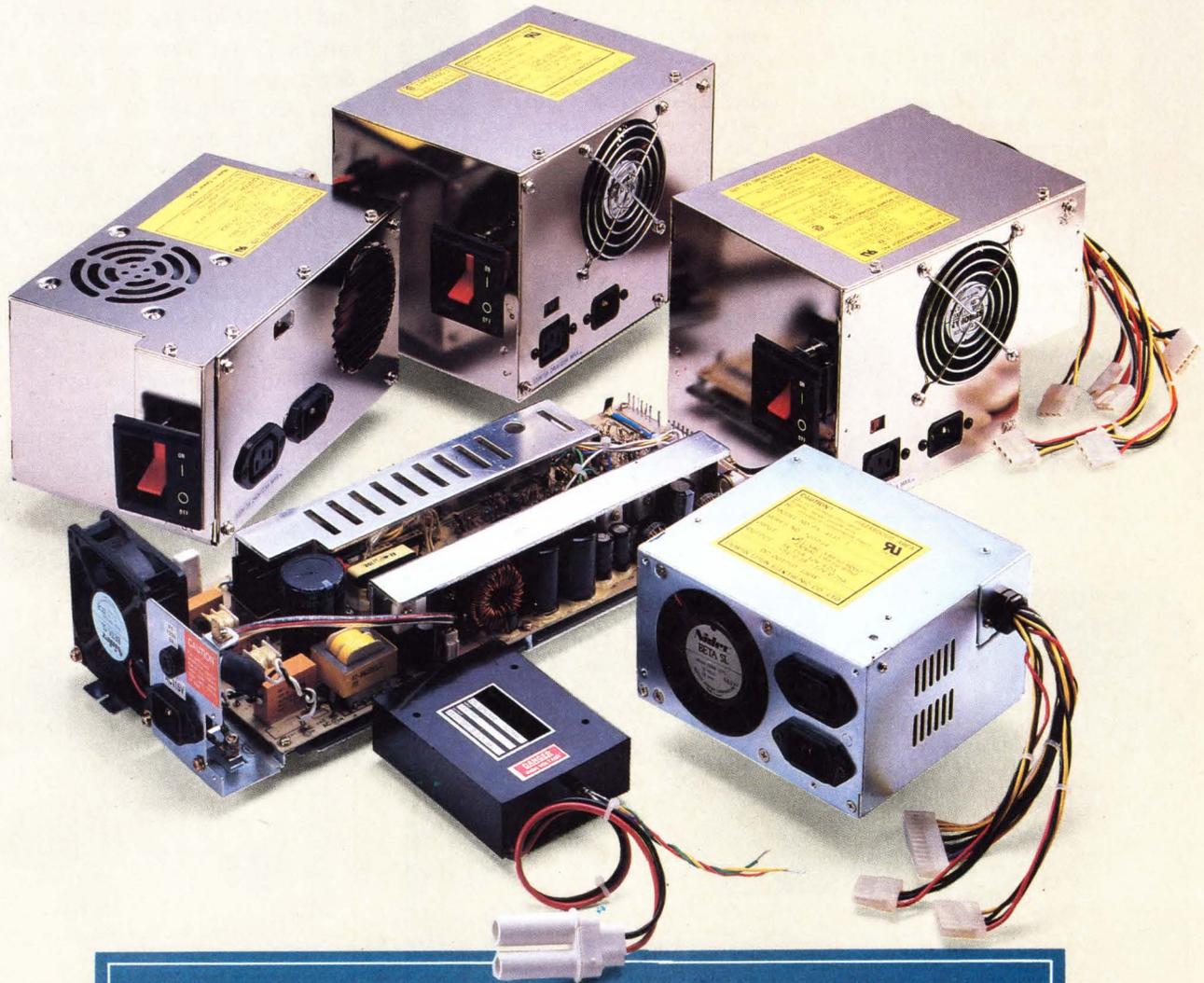
CHIP SET

- Includes multiplier and ALU
- Performs 60M flops

The B3110A-50 floating-point multiplier and B3120A-25 floating-point ALU comprise an ECL 10KH-compatible chip set that offers double-precision (64-bit) multiply operations in 50 nsec and add or subtract operations in 25 nsec. TTL-compatible versions are also available

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Systems Division Attn: Sales Manager
726 South Hillview Drive, Milpitas, CA. 95035
Tel: (408)946-4873 · Fax: (408)942-1527

CIRCLE NO 190

Taiwan Liton Electronic Co., Ltd.
12Th Fl., 25, Tunghua South Road, Taipei, Taiwan, R.O.C.
Tel: (02) 2226181-8 Telex: 34266 TWLITON Fax No.: (02) 2212780

with all general-purpose EL display applications, including IBM PC and PS/2 formats. The chip is available in either plastic or ceramic 44-pin J-lead packages. Plastic package, \$9.96 (1000).

Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94088. Phone (408) 744-0100. TLX 6839143.

Circle No 412

BUFFER AMPLIFIERS

- 125- and 200-MHz bandwidths
- 1500V/ μ sec slew rate

The EHOS-100 and EHOS-200 are high-speed, unity-gain buffer amplifiers with bandwidths (-3 dB) of 125 and 200 MHz, respectively. The EHOS-100 operates from $\pm 15V$ supplies; the EHOS-200 from $\pm 5V$ supplies. Included in each of the 2-stage amplifiers are bypass capacitors that improve the transient response. Both amplifiers feature a slew rate of 1500 V/ μ sec and can deliver 100 mA of output current. The buffer amplifiers come in TO-8 metal packages and are available in commercial and military versions. EHOS-100, \$10.13 to \$24.75; EHOS-200, \$9.38 to \$24 (100).

Elantec Inc, 1996 Tarob Ct, Milpitas, CA 95035. Phone (800) 821-7429; in CA, (408) 945-1323.

Circle No 413

PLDs

- 12-nsec propagation delay
- 100 erase/write cycles

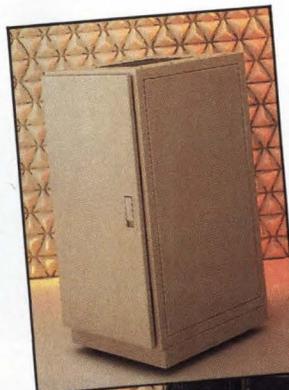
The GAL16V8A-12 and GAL20V8A-12 are CMOS PLDs (programmable logic devices) with a maximum propagation delay of 12 nsec. As with all of the company's Generic Array Logic (GAL) products, these devices can replace any common 20-pin or 24-pin (PAL) device. The GAL16V8A-12 is a 20-pin device; the GAL20V8A-12 is a 24-pin device. The E²CMOS technology allows complete ac and dc testing during the manufacturing pro-

cess. The company guarantees the devices for a minimum of 100 erase-write cycles; it guarantees data retention for more than 20 years. Available packages are plastic DIP and plastic leaded chip carrier (PLCC). In plastic DIPs, the GAL16V8A-12 costs \$8.32; the GAL20V8A-12, \$9.51 (100).

Lattice Semiconductor Corp,

5555 NE Moore Ct, Hillsboro, OR 97124. Phone (503) 681-0118. TLX 277338.

Circle No 414



When your specs call for emission control, call for Emcor's EMI/RFI series



Emcor offers a choice of shielding solutions, all of which are tested to MIL STD 285. These enclosures combine high strength with modular options and attractive esthetics. Emcor's commercial EMI/RFI enclosures are fabricated from 14-gauge cold-rolled steel and are fully zinc-plated. Our Tempest-style enclosures provide even higher levels of attenuation. They are fabricated from 12-gauge cold-rolled steel, nickel-plated and feature a unique latching system and door design (patent pending).

Contact Emcor to discuss your EMI/RFI needs. Our engineering staff has the knowledge and experience to help solve shielding problems. We can also design modified and custom products.



Crenlo, Inc.

1600 - 4th Ave. N.W.
Rochester, MN 55901
Phone 507-289-3371
FAX #507-287-3405

EMCOR

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CIRCLE NO 193

269

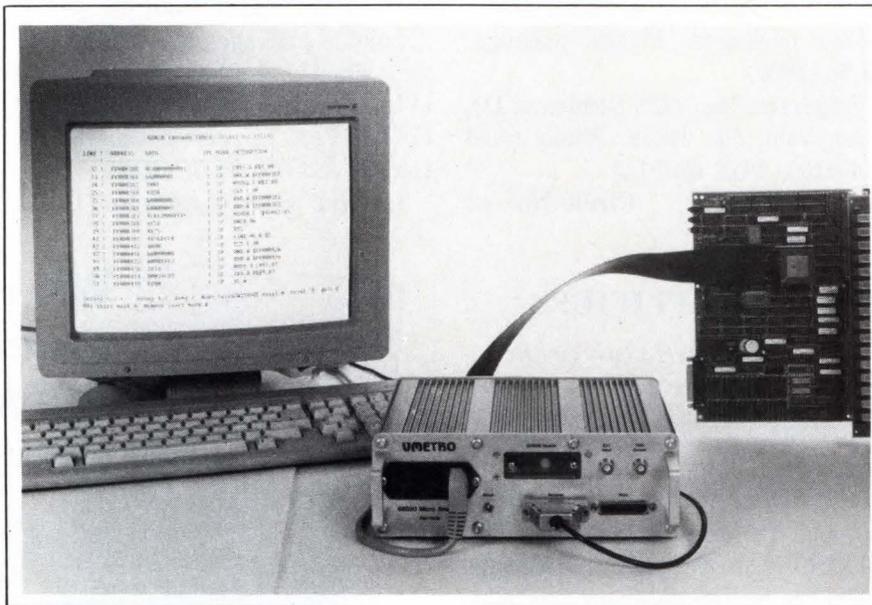
NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

68020 ANALYZER

- *Disassembles code and traces program flow*
- *Measures cache hits and interrupt-level distribution*

The PMA-020A microanalyzer stand-alone development tool tests, debugs, and evaluates 68020-based systems. A short cable connects it to the target μ P socket. An RS-232C port links the analyzer to an ASCII terminal to provide the operator interface. A second RS-232C port lets you use the same terminal as the operator interface for the target system. The specialized 88-channel logic/software-performance analyzer was optimized for developing and debugging modules such as drivers and operating-system kernels. The analyzer disassembles 68020 code, traces program flow, and determines the cache hit rate



and the distribution of interrupts on the μ P's interrupt levels. \$7900.

Vmetro A/S, Sognsvn 75, N-0855 Oslo 8, Norway. Phone 47 2 39 46 90. FAX 47 2 18 39 38.

Circle No 420

Vmetro Inc, 2500 Wilcrest, Suite 530, Houston, TX 77042. Phone (713) 266-6430. FAX (713) 266-6919.

Circle No 421



TROUBLESHOOTER

- *Memorizes analog signatures at good boards' circuit nodes*
- *Lets you compare unknown boards with good boards*

The Tracker 5100DS uses analog-signature analysis to help you troubleshoot analog and digital pc boards. You employ this PC-hosted instrument to force small ac currents into circuit nodes. It measures the ac voltages that appear at the nodes, digitizes them, and stores them on disk. You can recall the signatures from disk and display as many as eight on the PC's display.

By recording the signatures from a good board and comparing the corresponding signatures from a board under test, you can find inputs with marginal-breakdown voltages, out-of-tolerance components, and gates and capacitors with high dissipation. \$9500.

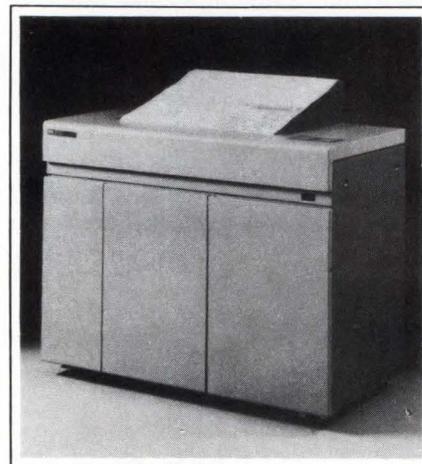
Huntron Instruments Inc, 15720 Mill Creek Blvd, Mill Creek, WA 98012. Phone (800) 426-9265; in WA, (206) 743-3171. TLX 152591.

Circle No 422

PLOTTERS

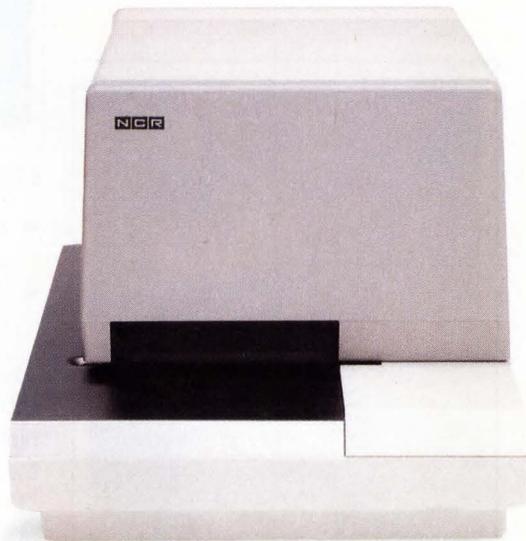
- *Use electrostatic imaging to resolve 406 dots/in.*
- *Produce D- and E-size drawings in under 1 minute*

The HP 7600 Series Models 240D and E are electrostatic plotters that produce monochrome output on D- and E-size coated paper at a rate exceeding 1 page/minute. Though the plotters' only moving parts are



the paper and the paper-drive mechanism, the plots, whose resolution is 406 dots/in., are as sharp as those produced by electromechanical pen plotters. The plotters incorporate a vector-to-raster converter and accept input in HP-GL/2, a superset of the vendor's earlier HP-GL (graphics language). Because of HP-GL/2's total compatibility with HP-GL and the wide support of HP-GL by vendors of CAD and CAE software,

. One is twice as good as two.



Introducing the NCR 2208. The one, and *only* 40-column printer that has the functionality of two.

And that's twice as good because now one printer can handle just about any retail transaction. Three print modes and 90° font rotation provide horizontal receipt printing as well as horizontal and vertical slip printing. This makes the 2208 the first printer in the world that can handle both EFT and credit authorizations with equal ease.

You also get more design flexibility. The 2208 is available in either a standalone unit or as a print mechanism only. And both configurations are lightweight and offer an extremely small footprint.

And when you use one printer to do the work of two, you can reduce your inventory and

service—practically in half.

The final point of comparison—cost. Obviously buying one printer is better than buying two. It's like getting one printer free. And that gives you either better margins or more aggressive pricing on your systems.

The only thing that could make this printer better is that it's from NCR—the world's leader in POS products.

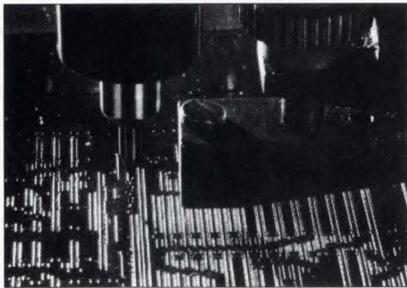
If you're looking for a way to be twice as good as the competition, call the NCR Technology Marketing Division at 1-513-445-7443 for a demonstration. The new 2208 Slip/Receipt Printer—only from NCR.

NCR

Creating value

NCR is the name and mark of NCR Corporation.
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Now in-house prototyping is truly affordable.



Mills and drills circuits in minutes.

There's no reason to waste time and money sending out for prototype circuit boards any longer. With the new BoardMaker, you can make your own prototypes in your own lab directly from your PCB CAD—as fast as you need them.

No delays or rush charges.

BoardMaker engraves single and double-sided boards, forming conductor lines as small as 5 mil. (There is a throughplate option too.)

A 2" x 3" board with medium density, for example, takes about 15 minutes. So you can save a week or more *at every level* of design development. You also save the money spent on outside sources, along with costly charges for rush service that can't compare with BoardMaker speed.

No chemicals.

BoardMaker is totally *mechanical*. There are no chemicals, no fumes, and no toxicity problems.

At \$5,000, pays for itself fast.

BoardMaker is revolutionary because it costs *one-sixth* the price of first generation prototype machines—and literally pays for itself after about a dozen boards. For more information, call (415) 883-1717 or use the reader card.



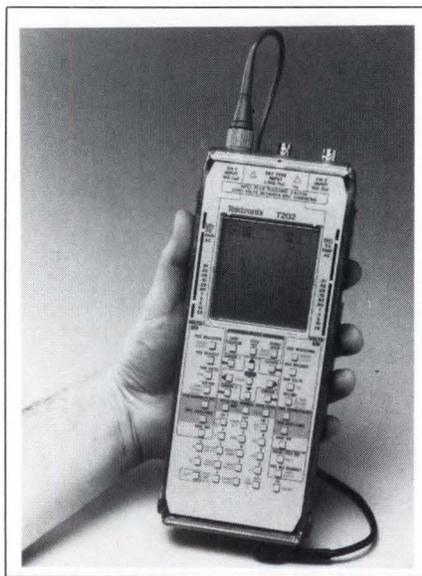
20A Pamaron Way
Novato, CA 94948

TEST & MEASUREMENT INSTRUMENTS

existing software packages already support these plotters. The vendor claims that you can simply plug in the electrostatic plotters in place of HP-GL-compatible pen plotters and start producing drawings in minutes. 24-in.-plot-width model, \$22,900; 36-in.-plot-width model, \$27,500. Delivery, four to six weeks ARO.

Hewlett-Packard Co., 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

Circle No 423



PLD TEST GENERATOR

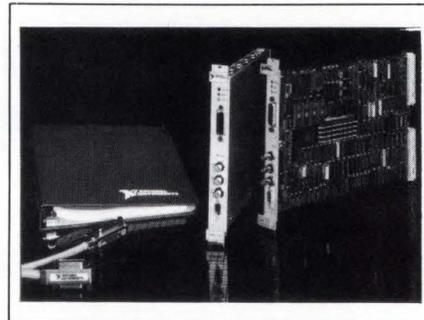
- Allows in-circuit testing of devices on pc boards
- Supports devices that you can't initialize

Version 2 of the vendor's ATG (automatic test generation) software runs under MS-DOS and creates test routines for PLDs, including those already mounted on pc boards. According to the vendor, the tests provide very-high-fault coverage during in-circuit testing where you can't preload initial conditions into devices. The software models ICs the way you actually use them—with some pins connected together or to V_{CC} . It also lets you enter information on constraints imposed by the circuitry that surrounds the device under test. The

vendor will upgrade existing installations at no charge. \$4950.

Anvil Software, 427-3 Amherst St, Suite 341, Nashua, NH 03063. Phone (603) 891-1995. TWX 910-250-3381.

Circle No 424



GPIB/VXI INTERFACE

- Plugs into VXI bus and links it to the IEEE-488 bus
- Transparently routes messages between the two buses

The GPIB-VXI circuit card plugs into the VXI bus (VME Bus extension for instrumentation). With its two backplane connectors, this "C-size" board conforms to the VXI standard. The card edge opposite the backplane supports an IEEE-488 connector; a 9-pin, D-subminiature connector used for an RS-232C port; and BNC connectors for triggering input, output, and an external clock input. A 32-bit 68070 μP has 512k bytes of dual-ported RAM that you can increase to 4M bytes. The μP runs under a firmware-resident version of the pSOS operating system and makes the board and all the IEEE-488 devices connected to it appear to the VXI subsystem as a VXI device with its own command set. The μP manages the VXI bus resources; controls communication between the VXI and IEEE-488 buses; and lets you download custom instrument-control software modules. \$3000.

National Instruments Corp., 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737.

Circle No 425



THE SIMPSON 560 MENU DRIVEN MULTIMETER. SOMETHING NEW ON THE MENU.

From microvolt transducer measurements to high voltage work, Simpson's new *Professional Series Model 560 Digital Multimeter* is designed to quickly give the answers you need—without elaborate signal conditioning.

Diagnostic functions such as MIN/MAX Hold and Peak Hold let you find and display transient amplitudes, while the bar graph continues to monitor the incoming signal. Programmable data logging on any range or function and a built-in 500 KHz frequency



counter, further expand the acquisition capabilities of the Simpson 560.

What's more, it's now possible to speed up routine tests—saving only the measurements of interest—because the 560 offers real-

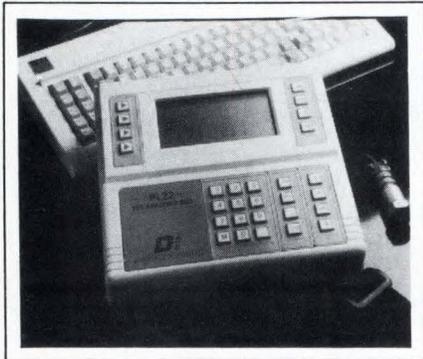
time comparison to stored test limits. Permanent records of the captured data can be generated by computers or printers connected to the optional interfaces (Centronics, RS-232 or IEEE-488). Displayed menus make it quick and easy to set the measurement parameters. And ultra-fast autoranging inputs instantly calculate the proper scale.

Order from our menu. The Simpson 560 Menu Driven DMM. You'll agree that it's done quite tastefully.

Simpson Professional Series products are made in USA.

SIMPSON

Simpson Electric Company 853 Dundee Ave., Elgin, Illinois 60120-3090 312/697-2260 FAX: 312/697-2272



FFT ANALYZER

- Has a bandwidth of 20 kHz
- Is battery powered and portable

Weighing 4 kg and measuring 256x250x82 mm, the battery-powered PL21 single-channel and PL22 dual-channel FFT analyzers are suitable for a variety of field and lab test applications in mechanical, structural, acoustic, and electrical engineering. The instruments analyze frequencies in the range of 0 to 20 kHz and produce frequency spec-

trums with as many as 1600 lines and a resolution as high as 62.5 mHz. They have input voltage ranges between ±5 mV and ±5V, which you can autorange or manually range in a 1-2-5 sequence. An accelerometer input allows you to connect the instrument to accelerometers with built-in charge amplifiers without a separate accelerometer power supply. Eight input frequency ranges, between 100 Hz and 20 kHz are provided, and the analyzers have a data record length selectable between 256 and 4096 points. Triggering facilities allow pre- and post-trigger recording. The instruments have 256k bytes of nonvolatile memory in which you can store as many as 250 measurements. Signal-processing functions include autospectrum, cross-spectrum, autocorrelation, cross-correlation, transfer function, coherence, and averaging functions. You can dump measured data through the

RS-232C interface. PL21 \$5900; PL22 \$8900.

Diagnostic Instruments Ltd, 264 W Main St, Murraysgate Industrial Estate, Whitburn, West Lothian EH47 0LB, UK. Phone (0501) 43031. FAX (0501) 43933.

Circle No 426

PS/2 I/O CARDS

- Plug into Micro-Channel bus
- Provide analog and digital I/O capability

The MC-MIO-16 is an analog, digital, and timing I/O board for the IBM PS/2 Micro-Channel bus. The MC-DIO-32F is a 32-bit parallel digital I/O interface card for the same bus. It achieves high speed by implementing DMA. The MC-DIO-24 is a lower-cost and lower-speed 24-bit parallel digital I/O card for interrupt-driven applications. The MC-MIO-16 incorporates a 12-bit A/D

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CIRCLE NO 197



The Complete UNIX/Real-Time Connection.



OS-9 utilizes common UNIX features:

- Multi-user, Multi-tasking
- UNIX I/O model
- UNIX task model: (fork, set priority,...)
- Pipes and Signals
- Shell User Interface
- Hierarchical Disk File System

...and more to connect you to Real-Time:

- Fast task switching
- Data modules
- Easy system generation and reconfiguration
- Fast interrupt servicing
- Events and semaphores
- Resident OS-9 compilers, assemblers and debuggers

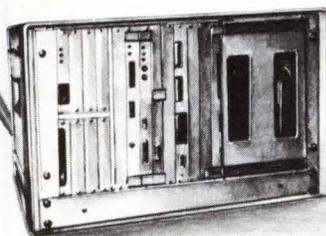
OS-9 UniBridge

Integrating UNIX and C applications into VMEbus systems has just been made easier with Microware's introduction of UniBridge. UniBridge is a complete development and communications package that allows you to connect your SUN 3, DEC VAX, HP 9000 or Motorola Delta workstation, to the world's premier real-time operating system: OS-9.

UniBridge provides a gateway so you can utilize UNIX in every phase of VMEbus system integration. From hosting C application development to monitoring large real-time networks, UniBridge connects UNIX to your OS-9 target system; whether it's ROM-based, disk-based, networked or stand alone.

UniBridge contains three high performance software modules that link UNIX and OS-9:

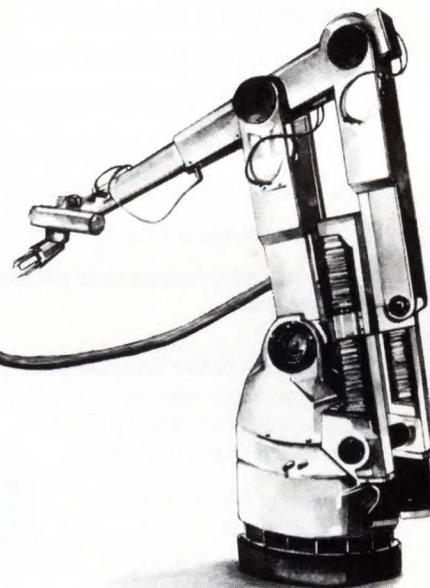
- OS-9/XCC Cross C Compiler allows you to produce compact, re-entrant and position independent C applications on your workstation for high speed execution on your OS-9 target.
- OS-9/ESP Ethernet Support Package provides industry standard BSD 4.2 sockets for TCP/IP communications with full FTP and Telnet support. UniBridge lets your workstation become a real-time server.
- OS-9/SRCDBG debugs resident VMEbus applications at the C source level, all interactively, across the Ethernet network from your UNIX terminal. And UniBridge makes all file access and transfer transparent from system to system while you debug.



And no other operating system complements UNIX with real-time functionality better than OS-9. OS-9, like UNIX, is a complete operating system to provide extensive C and math libraries, independent file managers, inter-process communications, debuggers and resident compilers. Yet OS-9 is 100% ROM-able and executes in real-time to host thousands of imaging, process control, data acquisition, communications and robotics projects worldwide.

Best of all, every module of UniBridge and OS-9 is written entirely by Microware to provide you one source for technical support and service.

From UNIX and C, to OS-9 and VME, contact Microware today and let your next real-time application shine with UniBridge: The Complete UNIX/Real-Time Connection.



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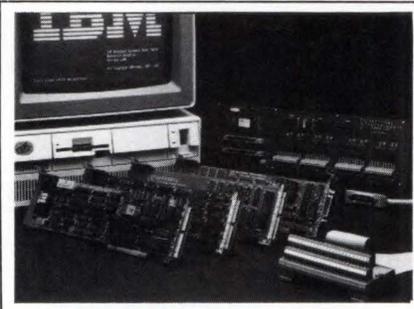
microware® OS-9

Microware Systems Corporation
1900 N.W. 114th Street
Des Moines, IA 50322
Phone: 515-224-1929

Microware Western Regional Office — Santa Clara, CA 408/980-0201;
Microware Japan 0474 (22) 1747

Distributors: West Germany 06221-862091; France (1) 43-33-96-38; Italy (6) 762221;
Switzerland (056) 83-3377; Sweden (018) 138595; Australia (02) 919-4917

converter preceded by an amplifier that provides software-controlled gain and an analog multiplexer with 16 single-ended inputs. The board also contains a pair of 12-bit D/A converters with double-buffered digital inputs, eight TTL-compatible digital I/O lines, and three 16-bit counter/timer channels. Other features include a FIFO buffer for A/D



conversion results, an automatic channel sequencer for the analog multiplexer, and a timer and interrupt generator. You can obtain the board in three A/D-conversion speed grades: 9, 15, and 25 μ sec/conversion. The fastest grade permits a throughput of 100k conversions/sec. MC-MIO-16, from \$1195. MC-DIO-24, \$245. MC-DIO-32F, \$595.

National Instruments Corp,
12109 Technology Blvd, Austin, TX
78727. Phone (800) 531-4742; in TX
(800) 433-3488. TLX 756737.

Circle No 427

Your Logic Analyzer Really Needs The PI-6500 Pattern Generator.

Here's Why:

1. The new Pulse Instruments PI-6500 Pattern Generator and your Logic Analyzer are a cost effective alternative to high-priced test systems.
2. Working together they offer you general-purpose digital signal send-receive capability.
3. You won't have to kluge digital signals or build special circuits any more—the PI-6500 Pattern Generator and your Logic Analyzer will do it for you.
4. You can now create interactive functions between the DUT, PI-6500 Pattern Generator and your Logic Analyzer.
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The PI-6500 Pattern Generator features specs like: 16 to 112 Channels, 256 Trigger/Flag Combinations, Easy Programming, Serial/Parallel Modes. And it is ideally suited to large digital test systems and military applications.

Want more information?
Call Pulse today at:

(213) 515-5330.



Pulse Instruments PI-6500 Pattern Generator.

Pulse Instruments

1234 Francisco Street • Torrance, California 90502 • (213) 515-5330



BOARD TESTER

- Performs time-phased analog and digital generation
- Can sample at equivalent of 1 GHz

The Expertest 2000 automatic test system is hosted by an 80386-based PC. The system tests loaded pc boards. It runs the vendor's diagnostic expert system software and uses a bed-of-nails fixture. The unit generates coordinated, time-phased, analog and digital patterns. Its high-speed channels can sample continuously at 200 MHz or can achieve an effective 1-GHz sample rate on repetitive waveforms by programmable edge shifting. According to the vendor, you don't have to write any code. The artificial-intelligence-based test-generation software tests with 1000 channels and, the vendor maintains,

MILITARY 256K RACE

EDI—First from the Start

Since 1983, when EDI introduced the first Military 64K SRAM, the company has been first in the race to market with the latest generation, highest density, CMOS MIL-STD 883 devices.

With a new family of fast 256K Monolithics, DESC qualified devices, and a new JEDEC standard Megabit Module, EDI is maintaining its' leadership position with the widest array of Military CMOS Static RAMs available today.



EDI's 256K Gold Medalists

256Kx1 35, 45, 55ns
64Kx4 35, 45, 55ns
32Kx8 45, 55, 60ns

And, all are available in a variety of ceramic, JEDEC standard DIP and LCC Packages.

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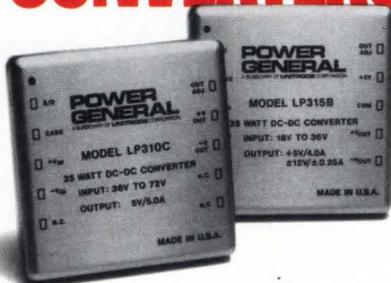
Corporate Headquarters: 42 South Street, Hopkinton, MA 01748 USA (617) 435-2341, TFX: (617) 4356302, TLX: 948004

Electronic Designs Europe Ltd.,

Shelley House, The Avenue, Lightwater, Surrey GU18 5RF United Kingdom, 0276 72637, TFX: 0276 73748, TLX: 858325

CIRCLE NO 200

ULTRA LOW PROFILE WIDE INPUT 25W, DC/DC CONVERTERS



Got an "on card" power distribution problem? Not enough real estate for a big modular supply? Don't want to use two card slots for any of the readily available "high profile" converters?

Well, Power General has the LP-310/315 solution. These compact converters utilize surface mount manufacturing, high frequency design and unique thermal management techniques to achieve performance features such as:

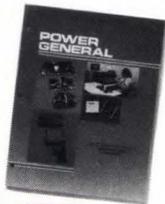
- 0.375 inch height
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FAX: 617-828-3215

INSTRUMENTS

thousands of diagnostic messages. From \$17,985 to \$49,985. Delivery, 30 to 45 days ARO.

Array Analysis, 200 Langmuir Lab, Brown Rd, Ithaca, NY 14850. Phone (607) 257-6800. TWX 490-000-1912.

Circle No 428

TEST GENERATOR

- Generates device- and board-test programs
- Uses waveform database derived from simulator output

The VectorBridge software package produces device- and board-test programs. It uses files generated by logic-simulation programs in the vendor's standard-events format. The test programs created comply with restrictions imposed by the target tester's hardware. The software's programs are compatible with Hewlett-Packard's 3065 and 16500, Integrated Measurement Systems' Logic Master, and Schlumberger and Semiconductor Test Solutions' systems that use the Factor language. The package runs on workstation platforms that support the vendor's other software products. Starts at \$10,000 for upgrades; \$15,000 for new installations.

Test Systems Strategies Inc, 8205 SW Creekside Pl, Beaverton, OR 97005. Phone (503) 643-9281.

Circle No 429

5-DIGIT DMM

- Incorporates 52-segment bar-graph display
- Includes 500-kHz frequency counter

The model 560 digital multimeter makes dc-voltage measurements with a basic uncertainty of 0.0035%. It measures dc voltage from 10 μ V to 1 kV, ac voltage from 10 μ V to 750V, resistance from 10 m Ω to 50 M Ω , dc and ac current from 10 nA to 10A, and frequency from 5 Hz to 500

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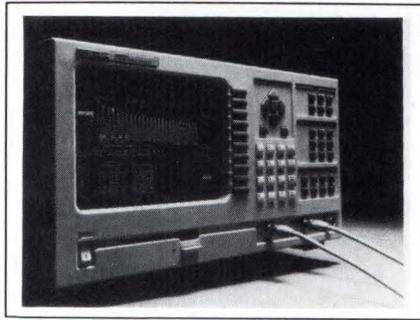
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grams developed by third parties into the internal computer. These programs utilize the vendor's disk-based HP 35680A Instrument Basic language interpreter; they customize the analyzer for specialized applications such as diagnosis of electric-motor problems from vibration spectra. You can write your own programs in Instrument Basic and

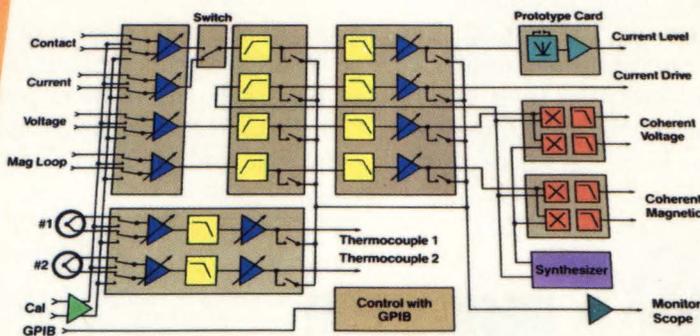


develop them on an MS-DOS-based PC. Using an ASCII keyboard, you can type in your programs, or you can enter them from the analyzer's front panel by keystroke recording of Basic keywords. HP 35660A, \$12,500; HP 35680A, \$500. Delivery, eight weeks ARO.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone local office.

Circle No 432

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CIRCLE NO 205



IN-CIRCUIT EMULATOR

- Supports 80C196, 8096-90, and 8096-BH μ Ps
- Shares memory with host PC at 12 MHz max

The EMS96 in-circuit emulator supports the 8096-90 and 8096-BH microcontrollers. It allows multiple hardware breakpoints on instruction fetch, data read, write, address or pattern matching. The emulator plugs into the IBM PC bus and provides full-speed emulation. You place the 8096 code and data in the PC's memory, where both the PC and the 8096 can share it. The emulator maps this RAM space to shared or user memory in 64-byte blocks. It allows your PC-resident programs to access, display, and modify variables without affecting the microcontroller's operating speed. The unit supports the host processor's speeds from 4.77 to 12 MHz and the 8096's speeds from 3 to 18 MHz. It allows for symbolic debugging in ASM96, PL/M96 and C96. \$2995.

Annapolis Micro Systems Inc, 612 3rd St, Suite 301, Annapolis, MD 21043. Phone (301) 269-8096.

Circle No 433

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CLR-69	M39006/21	TXX
CLR-10/14/17	Mil-C-39006/18/19/20	XT
CRL-01/02	Mil-C-83500	W13
	Silver Tubular	MTPH
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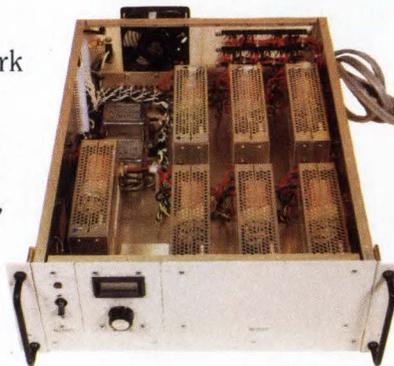
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 - + 28 VOLTS & 2.15 AMPS
 - 28 VOLTS & 2.15 AMPS
 - 28 VOLTS & 2.15 AMPS
 - ± 15 VOLTS & 0.4 AMPS
 - ± 15 VOLTS & 0.4 AMPS



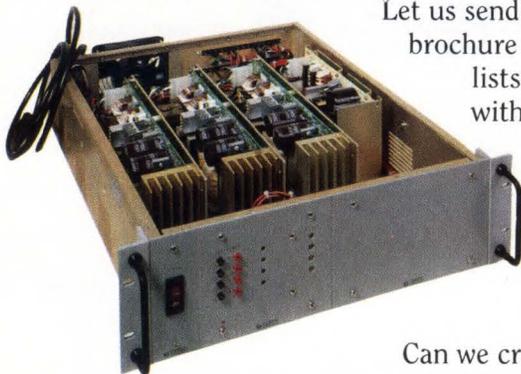
TYPICAL ASSEMBLY

- OUTPUTS
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 - + 5 VOLTS & 6 AMPS
 - + 5 VOLTS & 6 AMPS
 - 5 VOLTS & 6 AMPS
 - 2.1* VOLTS & 0.25 AMPS

*Modified Standard Unit

TYPICAL ASSEMBLY

- OUTPUTS
- + 5 VOLTS & 10 AMPS
 - + 5 VOLTS & 10 AMPS
 - 5 VOLTS & 10 AMPS
 - 5 VOLTS & 10 AMPS
 - + 28 VOLTS & 2.15 AMPS
 - 28 VOLTS & 2.15 AMPS



TYPICAL ASSEMBLY

- OUTPUTS
- + 24 VOLTS & 10 AMPS
 - 24 VOLTS & 10 AMPS
 - + 5 VOLTS & 48 AMPS
 - + 12 VOLTS & 10 AMPS

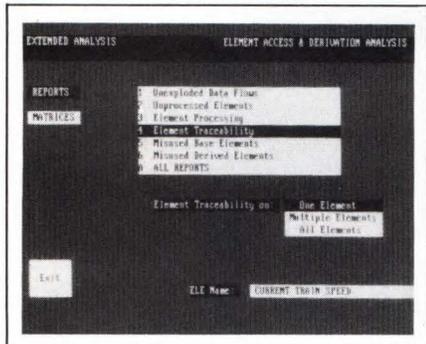


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NEW PRODUCTS

CAE & SOFTWARE DEVELOPMENT TOOLS



CASE TOOL

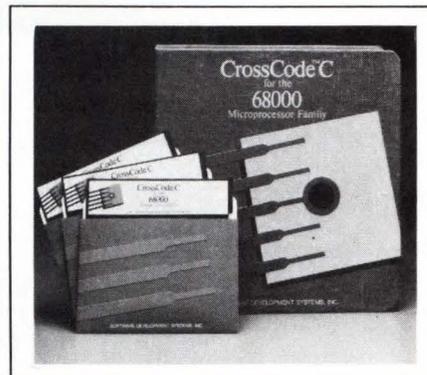
- Analysis and workbench tools for real-time systems
- Semantic and syntactic validation of specifications

Excelerator/RTS version 1.8A software lets you develop specifications for embedded and real-time systems. It works with the IBM PC/XT, PC/AT, PS/2, and compatibles. The software supports the

Ward-Mellor and Hatley techniques for system design. You can adapt graphics and a central dictionary using the vendor's customizing software. The software provides semantic and syntactic validation of specifications. Its new features include 33 analysis reports with 25 matrices that let you check system design. An element-trace report lets you find logic errors in the design. The software's graphical-analysis facilities match your system design against 50 specified rules. \$8400. If you own a prior version of the software and have a warranty or maintenance plan, the upgrade is free; the upgrade is available to other users for \$500.

Index Technology Co., 1 Main St., Cambridge, MA 02142. Phone (617) 494-8200. TWX 910-380-7014.

Circle No 435

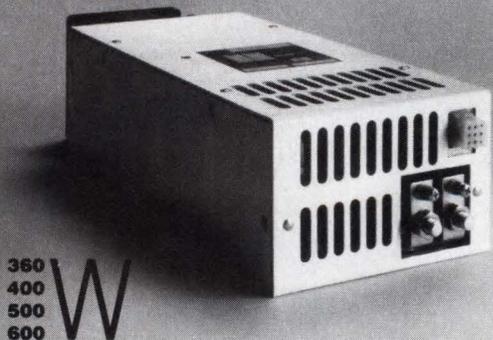


C COMPILER

- Generates ROMable code for the 68000 μ P family
- Can split output code into five memory sections

The CrossCode C compiler generates ROMable code for the 68000 μ P family and conforms to the ANSI C standard. The compiler package comprises a macro assembler, a

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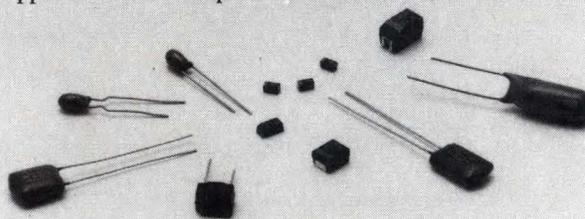
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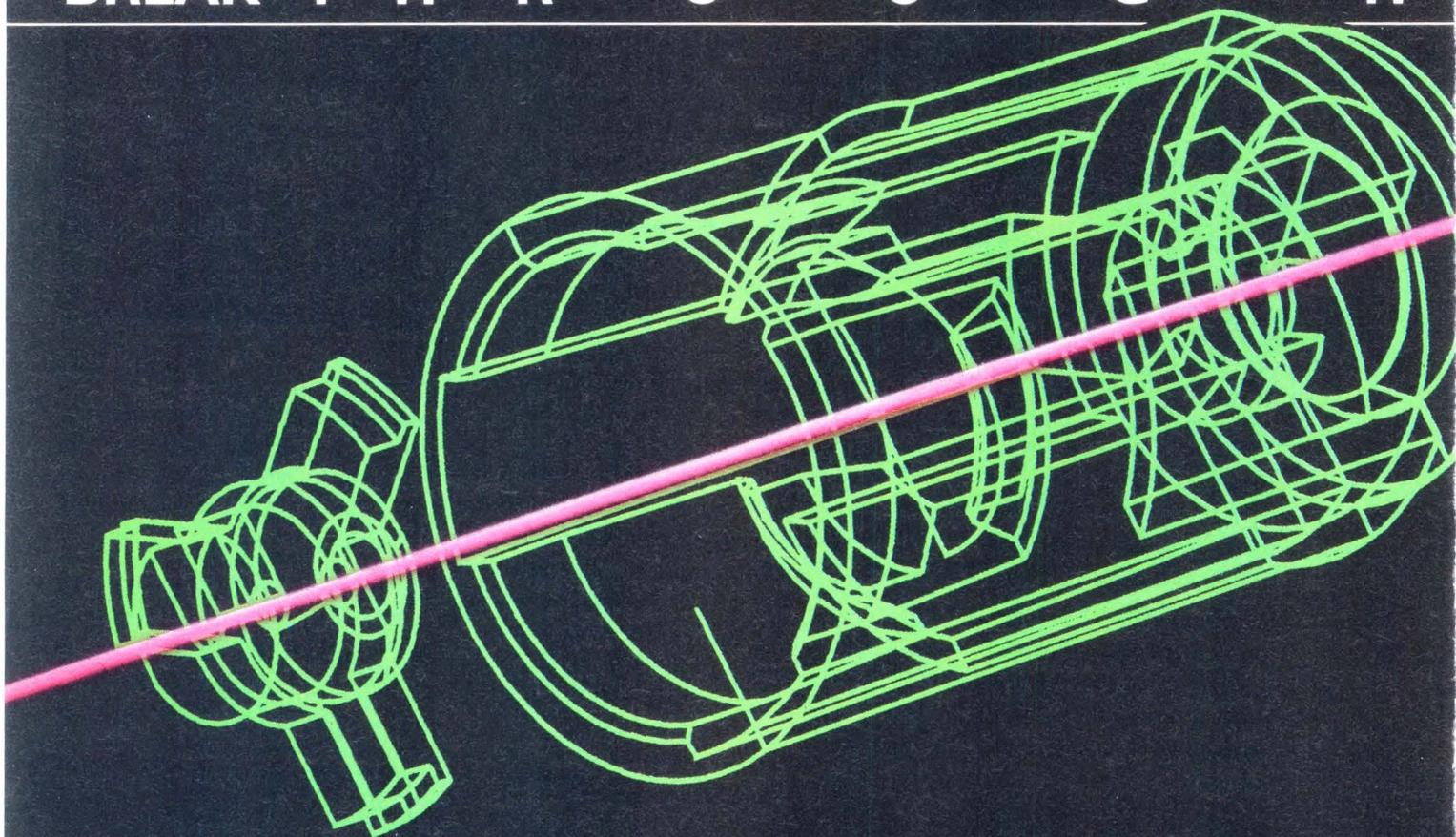
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CIRCLE NO 210

CAE & SOFTWARE DEVELOPMENT TOOLS

linker, and a C library. Using the compiler, you can split output code into five RAM or ROM sections and define integer and pointer sizes over a 16- to 32-bit range. The linker lets you partition and allocate the required memory. The compiler's C library provides the source for more than 47 functions. The package also features a downloading utility that communicates with EPROM programmers, allowing you to convert compiled code into Motorola S records and other file formats. This utility also allows you to create binary images. The compiler lets you use a maximum of 64 characters for symbol names. MS-DOS or Xenix version, \$1595; Unix version, \$4795.

Software Development Systems Inc., 3110 Woodcreek Dr, Downers Grove, IL 60515. Phone (800) 448-7733; in IL or outside USA, (312) 971-8170. FAX 312-971-8513.

Circle No 436



SOFTWARE PACKAGE

- Lets you design and run process-control functions
- Includes PLD and stepper-drum functions

The PCI-20073S-1 software package is an enhanced version of the industry-standard RD1000/PC relay-ladder software. In conjunction with the vendor's PCI-20000 data-acquisition system, the software simplifies the design of process-monitoring and -control functions. You can use the PC first as a development system to configure a data-acquisition and -control algorithm, and then as a controller

that runs the algorithm. A screen editor displays conventional and enhanced relay-ladder symbols that you can select and enter with single keystrokes. You can at any time access an on-line help screen. The editor allows you to perform forward and backward searches for rungs, and you can delete or insert rungs. You can monitor, and even modify, a running program. The software also provides password-security protection. The enhancements include the ability to program the logic equivalent of as many as 32 16x16 stepper drums; each drum can step 16 times and selectively open or close as many as 16 contacts at each step. \$995.

Burr-Brown, 1141 W Grant Rd, #131, Tucson, AZ 85705. Phone (602) 746-1111.

Circle No 437

FORTRAN FOR 80386

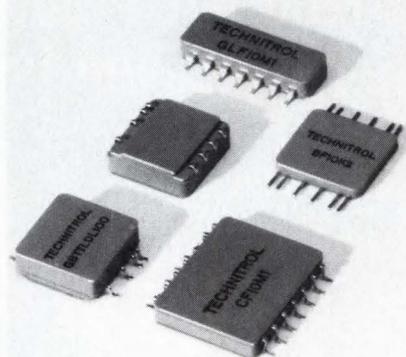
- Makes full use of 32-bit architecture for speed
- Lets you compile programs as large as 4G bytes

The F77L-EM/32 full implementation of the ANSI Fortran 77 standard includes a number of popular extensions, which makes it easier to adapt minicomputer and mainframe applications to the 80386 architecture. The compiler can use both 80287 and 80387 math coprocessors, and a future release will also work with the Weitek 1167; it will run in protected mode. The package comes with a source-level debugger, a library manager, and a 32-bit linker. To run the compiler, you need an 80386-based machine, PC-DOS 3.0 or higher, at least a 1M-byte extended memory, and either OS/386 or Developers' Kit OS/386—the two DOS-extender systems from AI Architects (Cambridge, MA). \$895.

Lahey Computer Systems Inc., Box 6091, Incline Village, NV 89450. Phone (702) 831-8123. TWX 910-240-1256.

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CIRCLE NO 211

CAD SOFTWARE

- Features 3-D polyline with five types of surfaces
- Works simultaneously with 2-D and 3-D elements

The AutoCAD software package, release 10, now runs on the Apple Macintosh and uses pull-down menus and icons to guide you. Fea-

turing a 3-D polyline with five types of surfaces, the software performs simultaneously with 2-D and 3-D elements. A coordinate-system icon provides visual feedback. The software's interactive viewing lets you display multiple on-screen views. Its standard features include zoom, clip, pan, and project facilities. The software employs a proprietary ver-

sion of Lisp for programming. A graphics exchange facility lets you communicate with other CAD systems. \$3000.

AutoDesk Inc., 2320 Marinship Way, Sausalito, CA 94965. Phone (415) 332-2344. TLX 275946.

Circle No 439

Frequency Products for Aerospace, Military and Industrial Markets

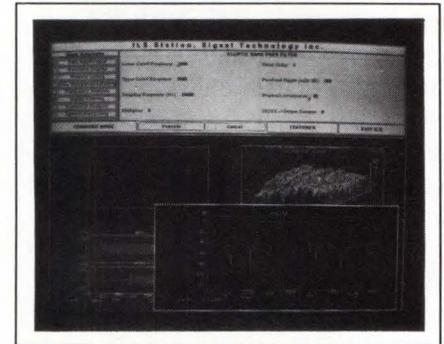
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SIGNAL ANALYSIS

- Performs DSP analysis of time-series data
- Supports Apollo user-interface and graphics standards

The ILS (Interactive Laboratory System) signal-analysis package is now available for the Apollo 3000 and 4000 workstations. The software operates on digitized signal data stored in computer files. It lets you analyze the data using DSP techniques such as frequency analysis, digital filtering, numerical analysis, speech processing, and other forms of data manipulation. This version uses the Apollo Domain/Dialogue user-interface design and management system to provide a menu-driven operation for most DSP functions. You can easily modify and customize the menus. The multiple-window facility lets you view several different analysis steps simultaneously. The software conforms to the Apollo GMR (Graphics Metafile Resource) standard, which allows you to direct graphics output to any Apollo-supported output device. If you store graphics in a metafile, you can edit the file, share the file with other applications, or view the file on any Apollo workstation on the Domain local-area network.

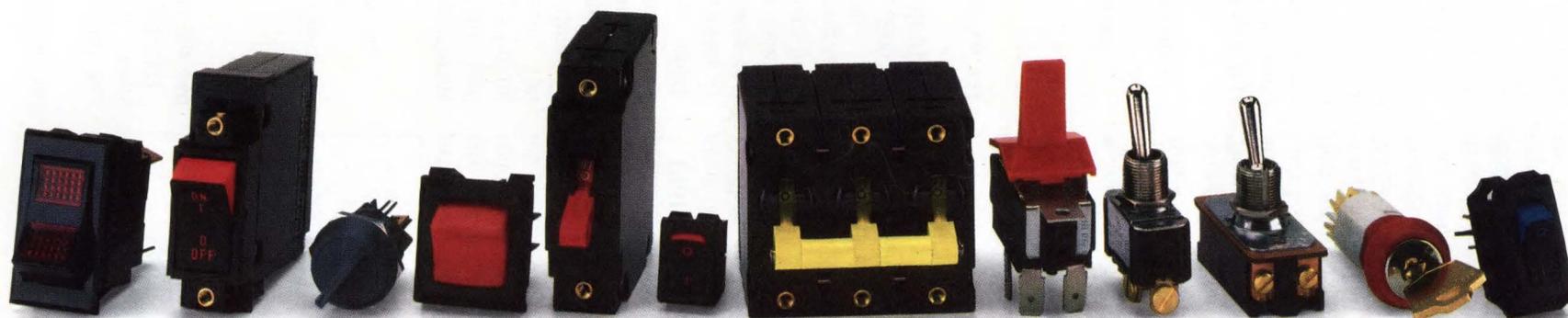
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CIRCLE NO 214

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\$5100 to \$12,500, depending on host's configuration.

Signal Technology Inc., 5951 Encina Rd, Goleta, CA 93117. Phone (805) 683-3771. TWX 910-334-3471.

Circle No 440

TIMING ANALYZER

- Performs worst-case analysis on ASIC and board designs
- Displays timing problems on schematic designs

The QuickPath analyzer performs worst-case analysis on ASIC and board designs, and displays timing problems on the schematic. You don't have to create vector stimuli in order to find setup and hold problems. The analyzer calculates path delays, then compares them to clock specifications. It supports multiphase and multifrequency clocks. In addition, the analyzer locates fast and slow components on pc boards. Its algorithm works with gate-level, functional, behavioral-language, and hardware models. \$9900.

Mentor Graphics Corp., 8500 SW Creekside Pl, Beaverton, OR 97005. Phone (503) 626-1231.

Circle No 441

CASE TOOL

- Lets you develop structured programs for PLCs
- Runs on an industry-standard PC

The PDS5 software package lets you develop programs for the company's PC20 and MC30 programmable logic controllers (PLCs) on an industry-standard PC. The package supports the graphic Sequential Function Chart (SFC) language. SFC employs embedded ladder-diagram and functional-block diagram languages. In addition, you can program using text coding. The SFC language obtains the program structure from a flow chart of the main control functions. This feature lets you develop structured pro-



grams at shop-floor level. For on-site test purposes, you can download code to a PLC. The debug facilities let you monitor program execution at any level. The package includes pull-down menus, on-screen help, and documentation facilities. Approximately gld 5000.

Philips, Industrial & Electroacoustic Systems Div., 5600 MD Eindhoven, The Netherlands. Phone (040) 788620. TLX 35000.

Circle No 442

Philips Electronic Instruments Inc., 85 McKee Dr, Mahwah, NJ 07430. Phone (201) 529-3800.

Circle No 443

CAE TOOL

- Checks pc-board designs for environmental reliability
- Analysis conforms to MIL-STD-217 standards

When combined with the vendor's Allegro pc-board design system, ThermoStats provides environment analysis. It allows you to analyze board-spacing, part-selection, air-flow velocity, noise, and thermal conditions. The tool indicates the MTBF of a pc board by checking the board's conduction, convection, and radiation effects. By examining driver/receiver pin pairs, the tool identifies components that are susceptible to noise. The tool takes 30 sec typ to process an analysis and display the results on a color-coded line graph, and provides a library with 1200 thermal models. The reli-



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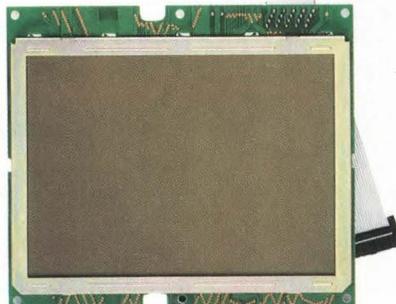
“Whether between two people, or two companies, trust is what makes partnerships work.”

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“Hitachi defines quality the same way we do—meeting customers’ needs.”

“Hitachi gives Techsonic the technological edge, and more. We’ve learned it’s a waste of time to do incoming testing on Hitachi LCDs. And when we sold over three times our forecast, they were flexible enough to come through for us. Whatever support we need, we get.



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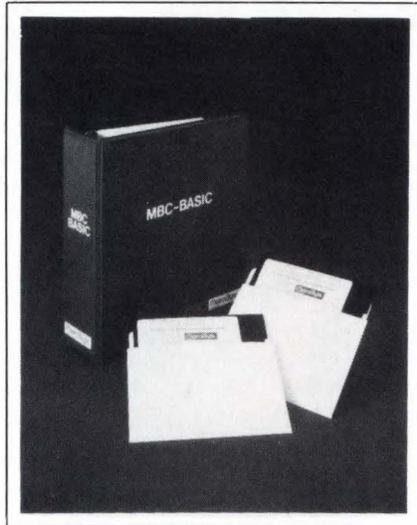
To learn about how partnering with Hitachi can benefit your company, call Tom Klopce or David Ross at (312) 843-1144. Or write to Hitachi America, Ltd., Electron Tube Division, 300 N. Martingale Road, Suite 600, Schaumburg, IL 60173.

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 Electron Tube Division

ability analysis conforms to the requirements of MIL-STD-217. The ThermoStats package runs on Sun 3, 4, and Digital 3000, GPX II workstations. \$15,000.

Valid Logic Systems, 2820 Orchard Parkway, San Jose, CA 95134. Phone (408) 432-9400. TLX 3719004.

Circle No 449



STRUCTURED BASIC

- Includes statements for data acquisition
- Provides structured-programming format

The MBC-Basic high-level programming language is compatible with GW Basic and BasicA. However, the language has extensions that let you tailor programs to the needs of a specific data-acquisition and -control application. New control-flow

keywords let you create structured procedures and functions similar to those of C or Pascal. You can declare variables as either global or local to a procedure. You can create libraries of pretested, error-free code for repeated use. The language also lets you create your own keywords, and the package comes with a number of

these special keywords that are created specifically for the vendor's Metra-bus family of process-control and data-acquisition devices. Unlike other Basic implementations, which are restricted to 64k bytes of memory, MBC-Basic allows you to access the full 640k bytes available to DOS. \$195.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. TLX 503989.

Circle No 444

NUMBER GENERATOR

- Generates double-precision random numbers
- Lets you select various probability distributions

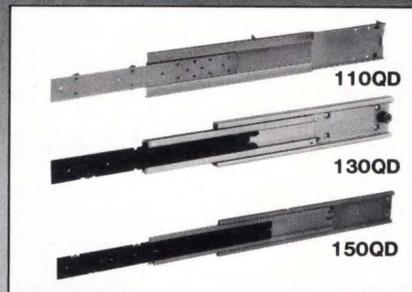
The RanGen software package performs high-speed generation of double-precision random-number sequences with uniform, Gaussian

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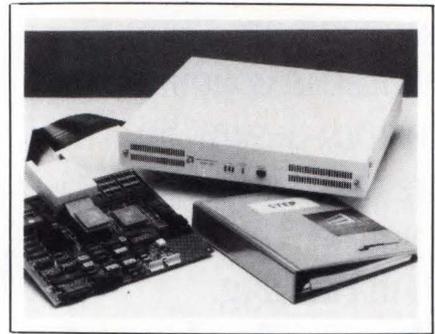
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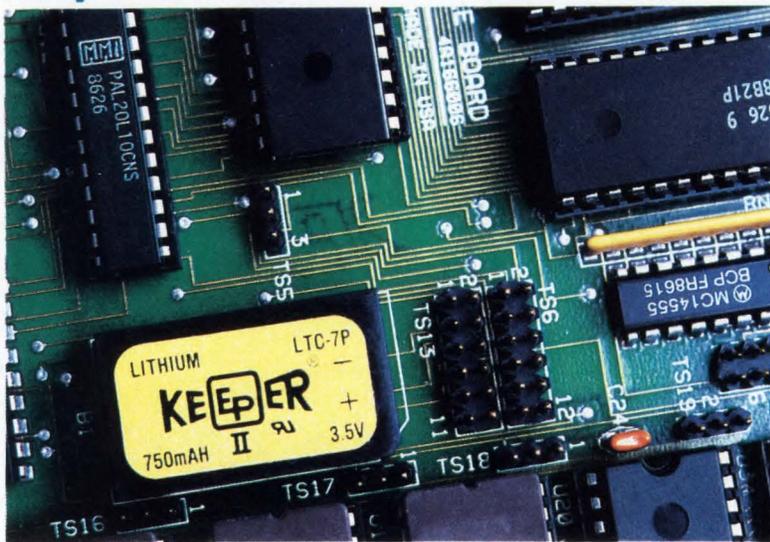
ters such as the mean and the variance of the distribution needed; if you don't specify these parameters, the program uses the defaults of zero-mean and unit variance. \$29.95.

Signal Analysis Research, 8301 Thomas Ave N, Minneapolis, MN 55444. Phone (612) 560-8166.

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DEBUG TOOL

- Provides hardware and software debug facilities
- Runs in real time without speed problems

The Adapt29K, a RISC (reduced instruction set computer) μ P development tool, provides both hardware and software debug facilities. According to the vendor, it runs in real time without encountering speed problems. The tool supports a 29k-byte max development project and provides ROM-resident software with an assembler. The software allows you to set eight breakpoints; to read from and write to I/O lines; to trace code execution; and to download files. Running on ASCII terminals and host computers, the tool catches bus signals at 40 MHz max. It plugs into the CPU socket and runs directly on the target processor. \$8500.

Step Engineering, Box 3166, Sunnyvale, CA 94088. Phone (800) 538-1750; in CA, (408) 733-7837. TWX 910-339-9506.

Circle No.446

CAE SYSTEM

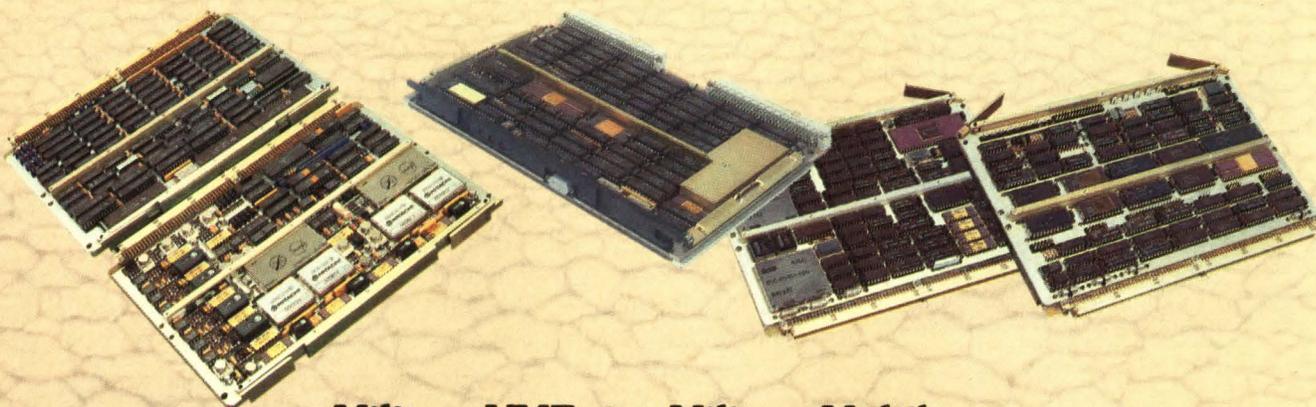
- Lets you design and simulate in an interactive mode
- Allows you to work on more than 30,000 gates

The Workview 3000 provides an ASIC design system for 386-based computers that lets you design and simulate in an interactive mode. The schematic capture lets you use the mouse, the keyboard, or macros for your instructions. The system provides 60 primitives that operate at

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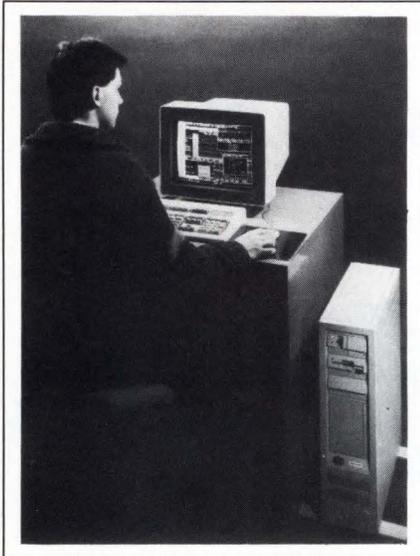
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Circle No 447

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- Has a battery-backed RAM with eight inputs

The D100 PLD provides a controller with interface modules and ladder-logic software. The software runs on the IBM PC, PC/XT, PC/AT, and compatibles. The controller comes with a battery-backed RAM with eight inputs. The device's features include six 24 to 240V ac/dc outputs; a 2-kHz max counter with 32 presets; and two 8-bit A/D channels with 12 presets/channel. The ladder-logic software lets you make in-

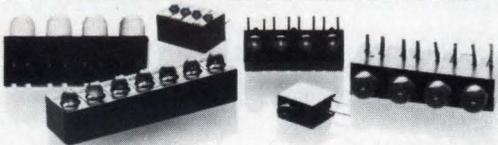


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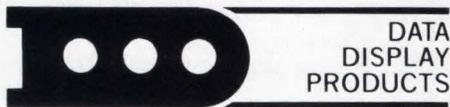


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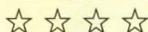
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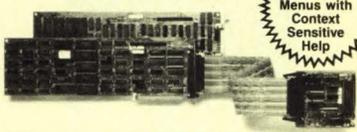
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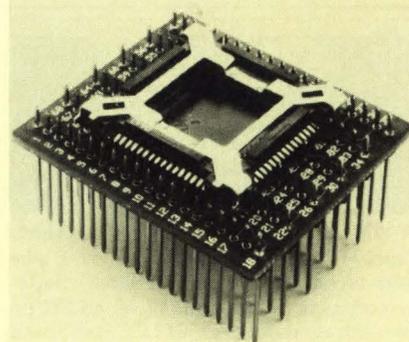
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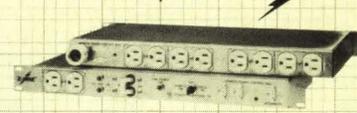
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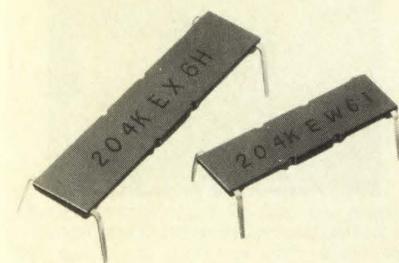
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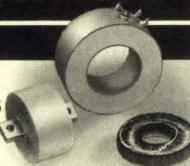
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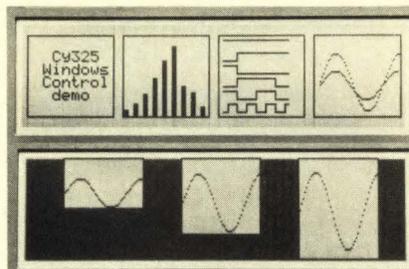


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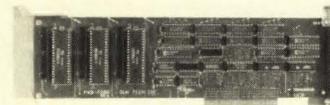


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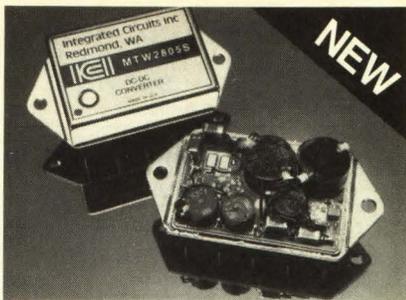
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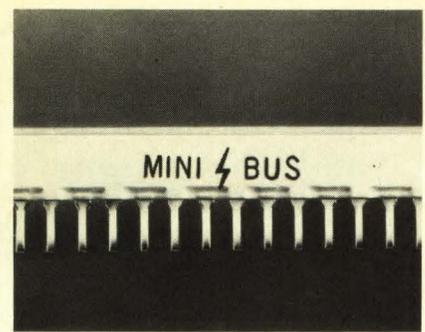


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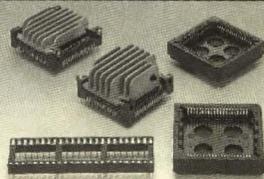
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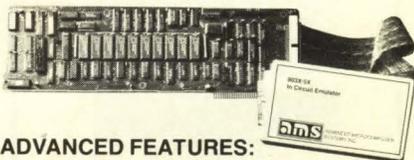
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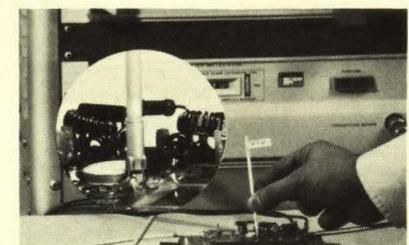
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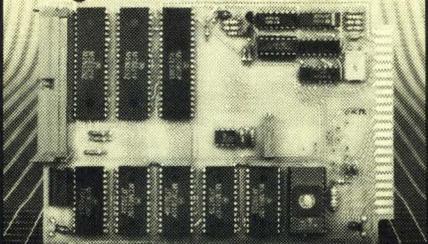
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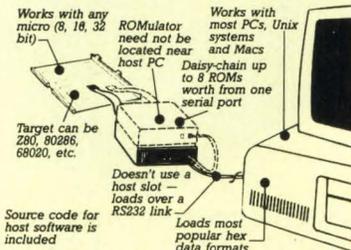
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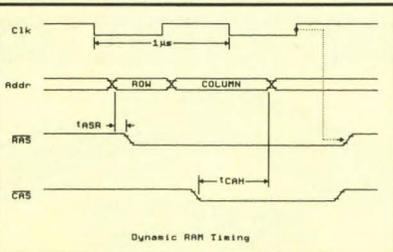
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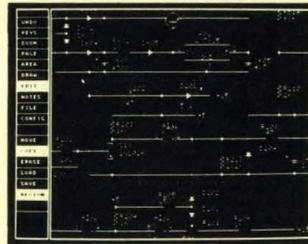
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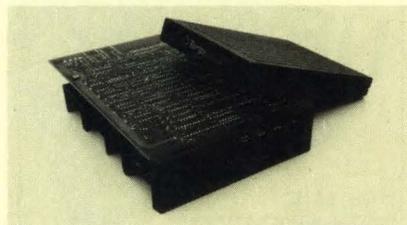
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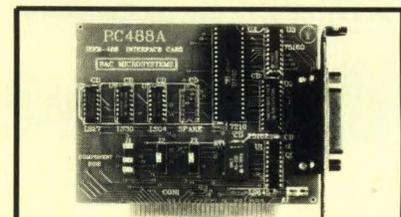
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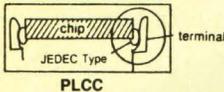
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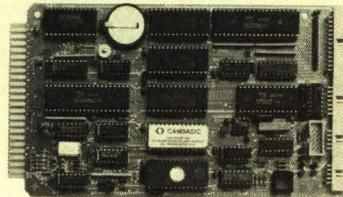
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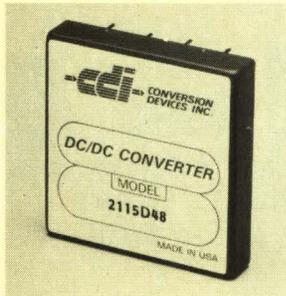
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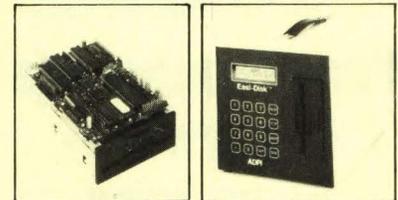
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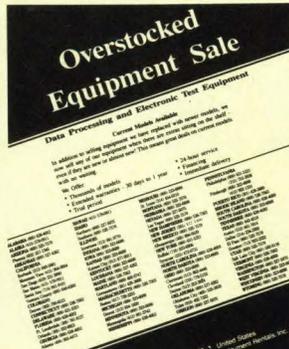
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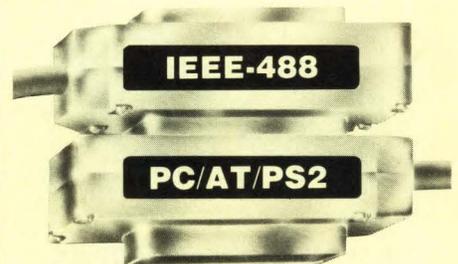


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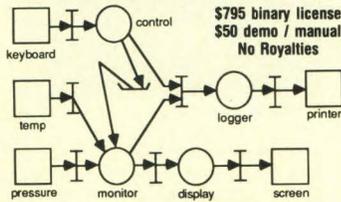
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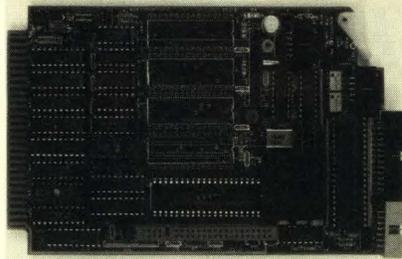
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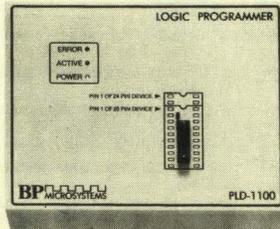
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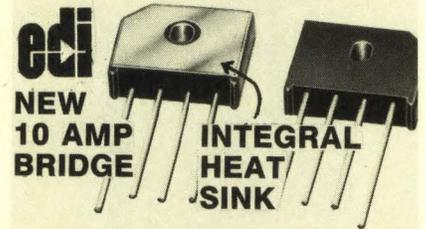


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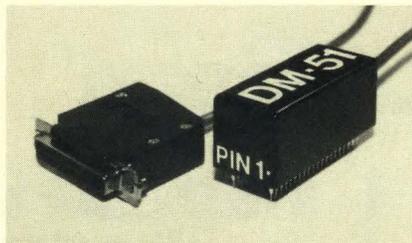
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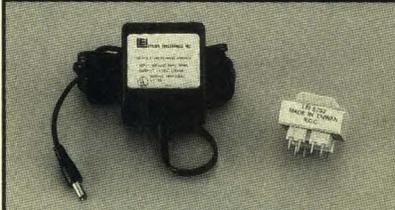
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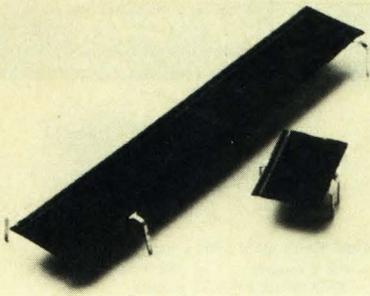
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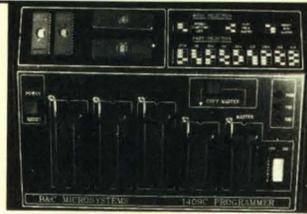


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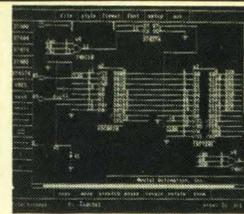
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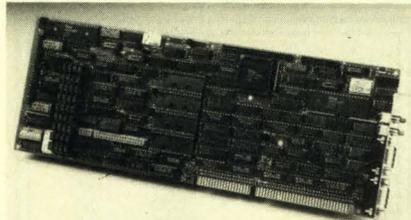
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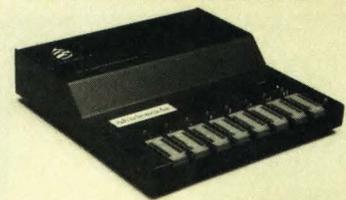
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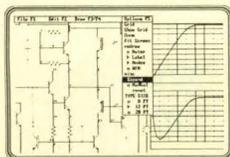
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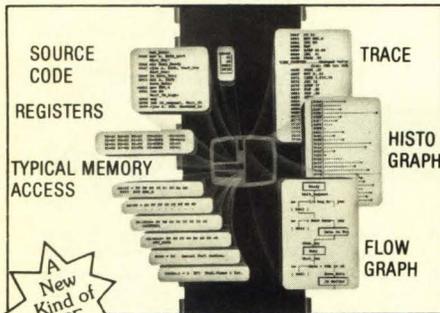


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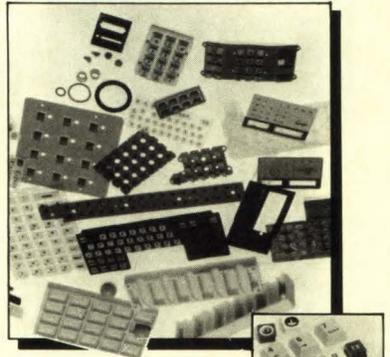
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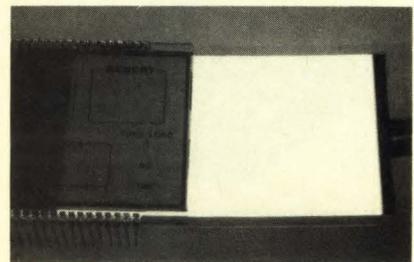
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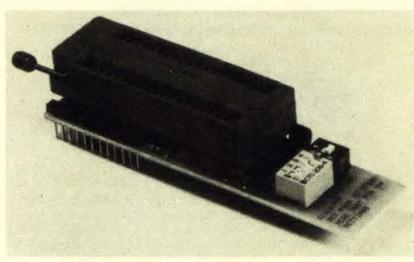


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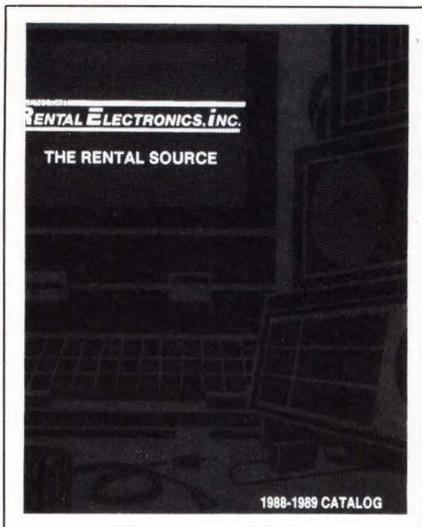
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This 1988-89 Rental Catalog presents electronic test equipment that's available for rent. The 36-pg listing includes products from major instrumentation manufacturers, such as Hewlett-Packard, Tektronix, Intel, and Fluke. The instru-

ments for rent fall into 26 categories, including analyzers, meters, generators, oscilloscopes, desktop computers, and telecommunications. Rental terms and conditions, illustrations, and a product index complete the publication.

GenStar Rental Electronics Inc., 6307 DeSoto Ave, Suite J, Woodland Hills, CA 91367.

Circle No 450

Catalog unveils software for VAB and HP-UX

The vendor's 200-pg Publication 5951-6794 deals with software for value-added-business (VAB) and proprietary-software solutions for its HP-UX operating system. The catalog lists more than 400 technical and commercial software packages for the vendor's HP-9000 workstations and servers. Using the market keyword index, you can look for products in specific application

areas. A range of application areas are available, from aerospace simulators to water-utilities operation. Business application areas include financial management, sales analysis, and accounting packages. The 200 VAB software packages listed in the publication are part of the HP Plus Program that assists third-party software suppliers with marketing the products.

Hewlett-Packard Co., Customer Information Center, Inquiry Fulfillment Dept, 19310 Pruneridge Ave, Cupertino, CA 95014.

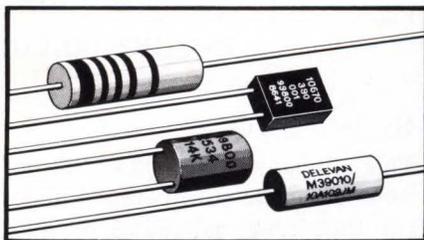
Circle No 451

Survey analyzes repair record of personal computers

The report, *Opportunities in Personal Computer Servicing: A National Survey of Malfunction and Repair*, is the second in a series of analyses outlining the personal-computer industry. It provides an

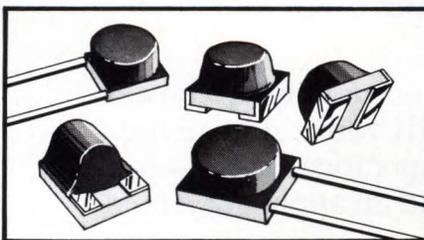
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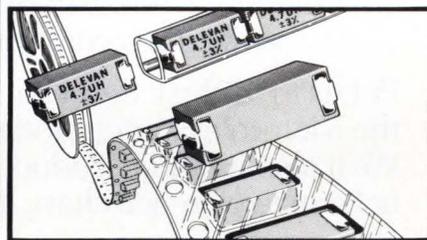
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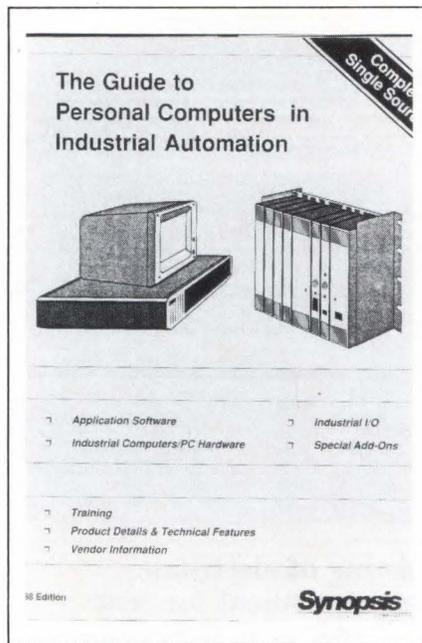
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technology. Entries include application software, PC hardware, industrial computers, industrial I/O devices, and peripherals. The guide also provides applications in process monitoring and control, data acquisition, PLC (programmable logic controller) programming/documentation, statistical quality control, manufacturing resource planning, operator interface, and cell control. A training section provides application training and technology reviews that include charts, photos, and diagrams. \$39.95.

Synopsis Corp, 2708 Salisbury Plain, Raleigh, NC 27612.

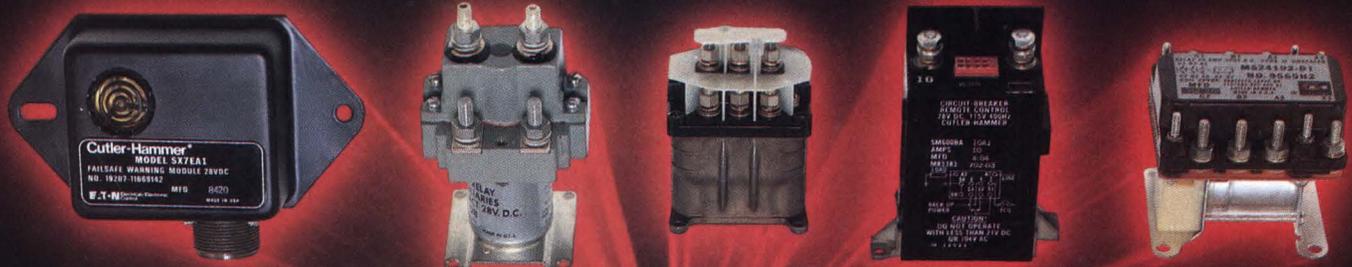
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IC data book

This company's 1988 data book presents all of the information found in the 1987 issue, as well as technical specifications and application notes for all the company's products released during the past year. It also features previews of many products to be released during 1988. New sections describe electrostatic discharge sensitivity and provide information about the sale of products in die form.

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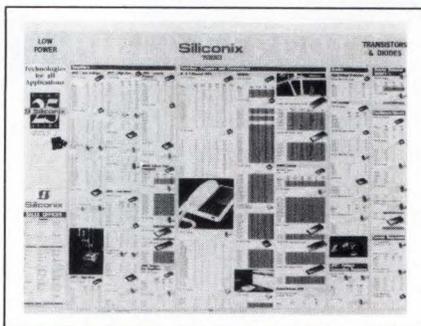


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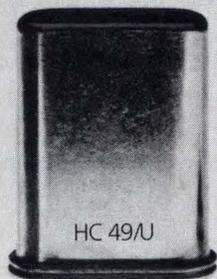


FETs. For easy reference, the chart is organized by major circuit categories, such as amplifiers, switches, choppers, commutators, diodes, current regulators, oscillators, mixers, and voltage-controlled resistors. Within each application area, the parts are sorted according to selection criteria—for example, amplifier FETs are sorted by critical parameters and by package options.

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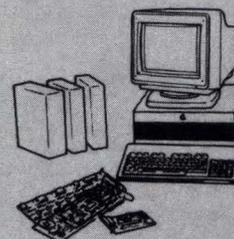


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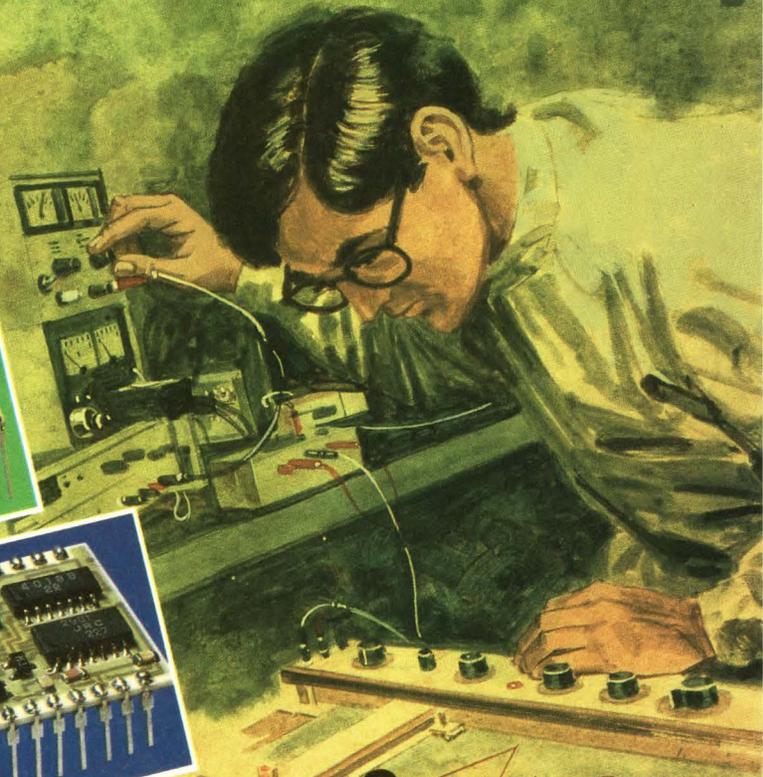
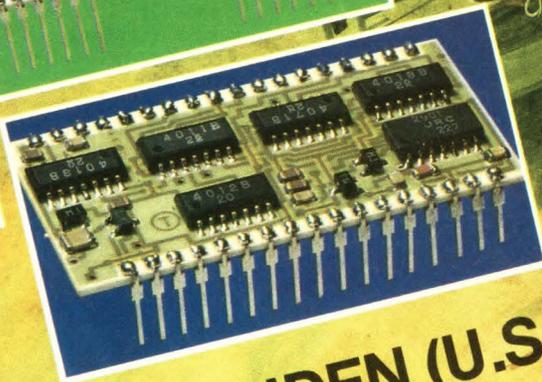
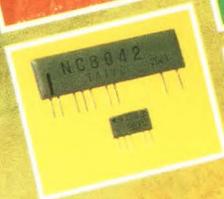
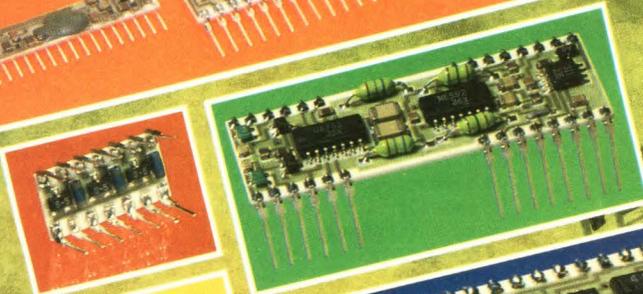
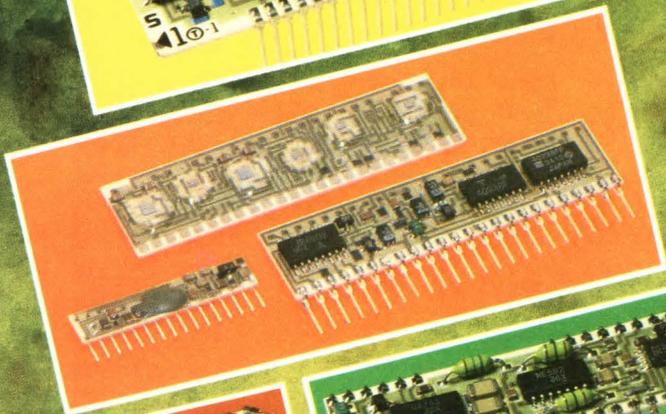
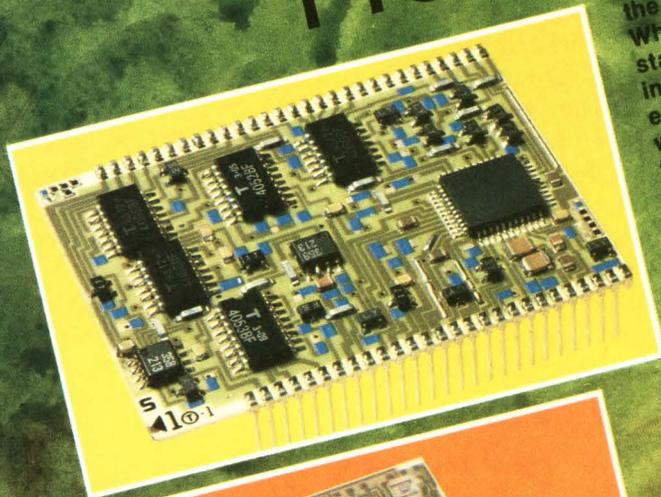
Manual targets IBM PC/XT and PC/AT users

Aimed primarily at engineers, scientists, and other professional IBM PC/XT and PC/AT users, *The 1988 PC Technical Source-Book* is a collection of hardware and software facts and data about the IBM PC family and its operating system. The 76-pg manual provides an introduction to the IBM PC for the beginner and a ready reference for the experienced user. It includes among its topics: I/O Bus 62-Pin Connectors, Bus Signal Summary, Memory Map, I/O Map, DMA Channels, Switch Settings, and DOS Commands. Further topics are AT CMOS Memory, 8237 DMA Controller, Keyboard Scan Codes, IBM PC/XT and PC/AT I/O Card Dimen-

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These three case studies discuss the use of artificial intelligence in electronics manufacturing. The 336-pg *Artificial Intelligence Applications in Manufacturing* presents more than 200 commercial expert systems and case studies for specific applications such as CAD/CAM, maintenance, production scheduling, and energy management. The 198-pg *Artificial Intelligence in the Computer/Electronics Industry* explains the aspects of AI used for in-house applications: expert systems, artificial vision, voice recognition, and intelligent robots. Finally, the

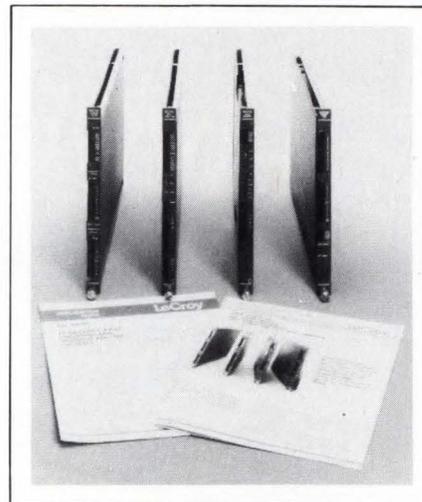
176-pg *Artificial Intelligence in the Semiconductor Industry* discusses the research being done by major manufacturers in the design of VLSI circuits. Each publication costs \$135.

Lion Publishing, Box 1869, Los Gatos, CA 95031.

INQUIRE DIRECT

Publications clarify ADC and TDC systems

This technical data sheet and application note explain the FERA/FERET fast-encoding and readout data-acquisition systems. The 4-color, 8-pg data sheet details the features of these modular systems and describes units for fast A/D conversion (Model 4300B), time-to-digital conversion (Model 4303), and fast access memory (Model 4302). It also reports on modules that provide logic decisions based on analog and time information. The application

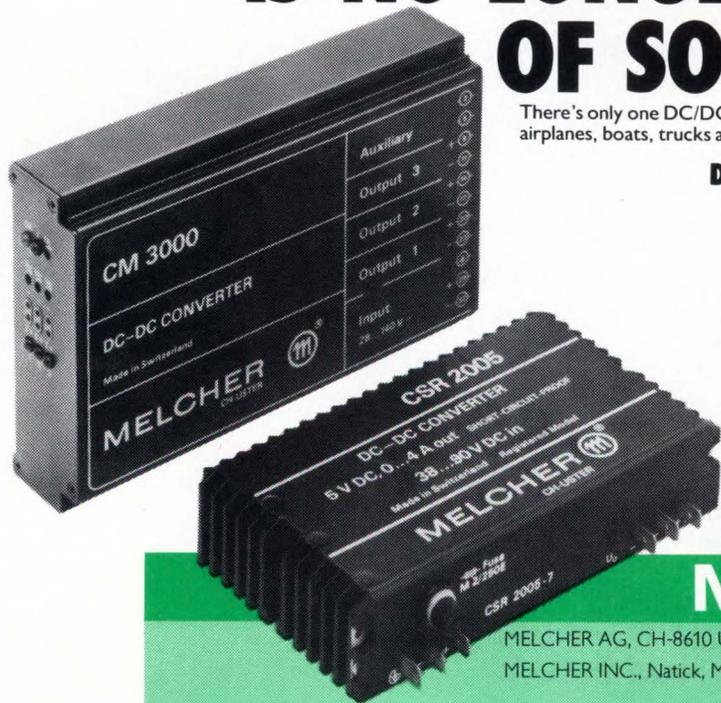


note, *FERA/FERET-Fast Encoding and Readout ADC/TDC Systems (AN 4004A)*, presents the systems, using text, tables, and diagrams, and discusses several configurations.

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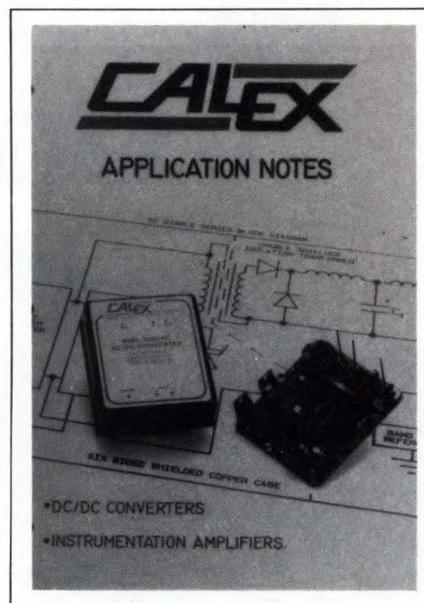
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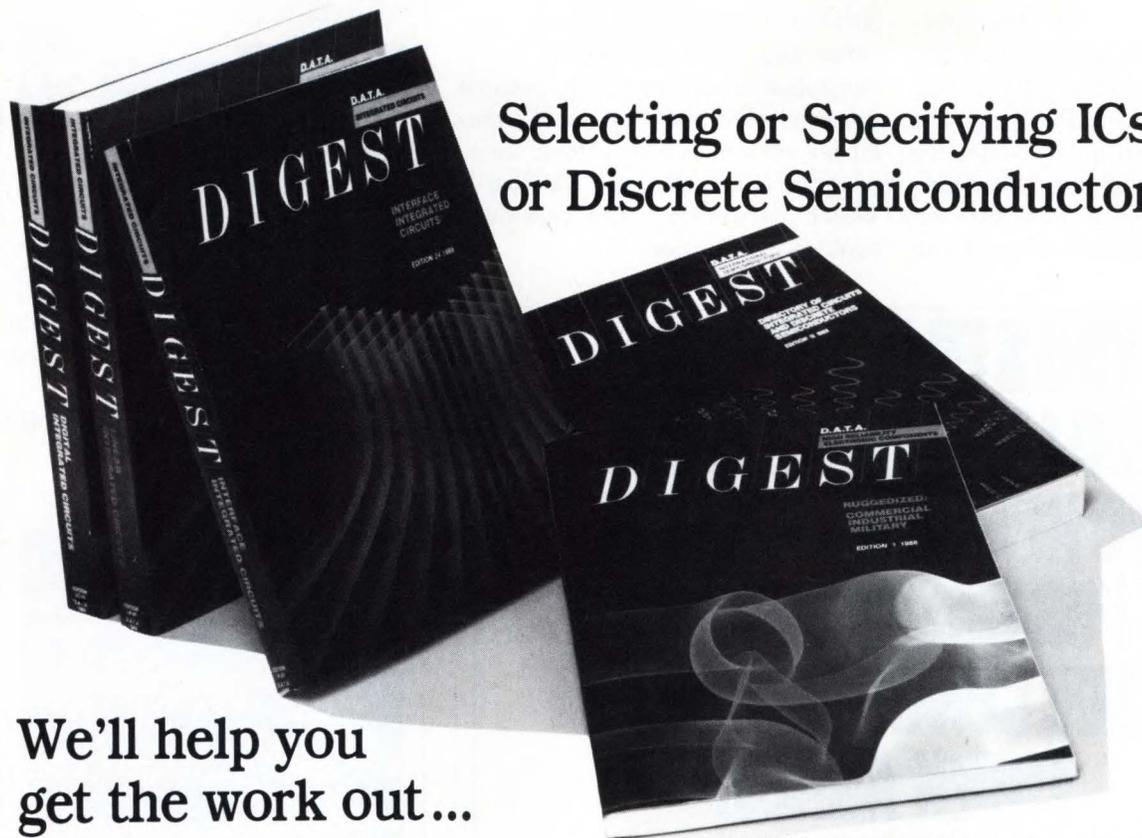
INTEGRATED CIRCUIT	MAXIMUM OPERATING TEMPERATURE	MINIMUM OPERATING TEMPERATURE	DC VOLTAGE	AC VOLTAGE	DC CURRENT	AC CURRENT	ESR	ESL
74181	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74182	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74183	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74184	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74185	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74186	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74187	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74188	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74189	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74190	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74191	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74192	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74193	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74194	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74195	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74196	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74197	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74198	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74199	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF
74200	125°C	-55°C	5V	5V	100mA	100mA	100mΩ	100pF

Data sheet deals with decoupling capacitors

This data sheet examines the vendor's Micro/Q decoupling capacitors. It gives you product specifications, standard and special configurations, and electrical performance. Finally, it provides installation and ordering information.

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Brochure surveys VLSI board-test systems

This 12-pg, 4-color brochure provides an overview of the five members of the vendor's L200 VLSI board-test systems. Discussing the features that provide cost-effective solutions to individual test requirements, the brochure elaborates on the modular architecture and the

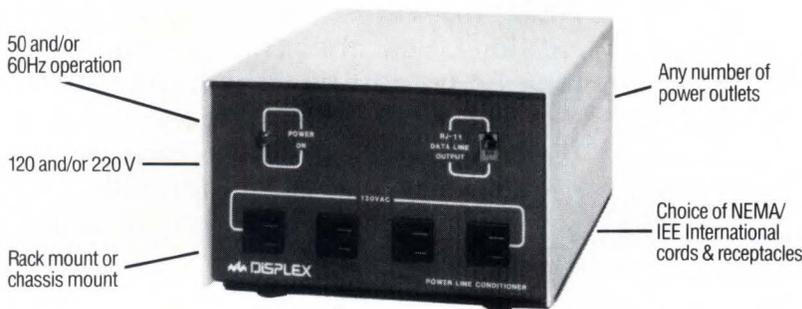
use of the VAX/VMS platform. Further, the pamphlet describes the software support for all the systems: the L200 test-development environment and in-circuit pattern libraries, the Lasar Version 6 simulation system for functional test-program generation, and the Board-Watch networking and test-data management system.



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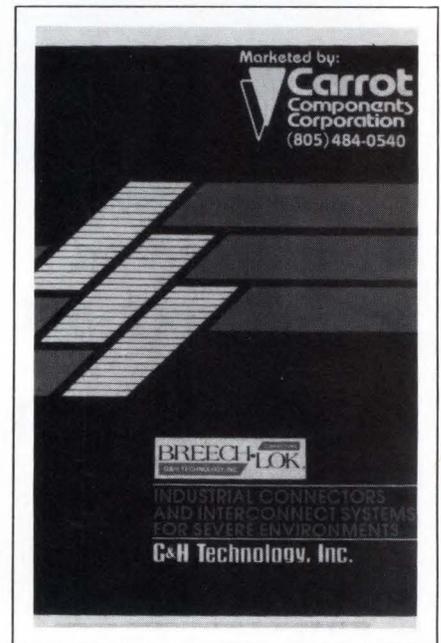
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CIRCLE NO 232



Listing of connectors

The vendor's 12-pg catalog of BLC Breech-Lok connectors features specifications, mechanical drawings, contact arrangements, and information about backshell accessories, crimp contacts, and service tools. Also included is information about straight plugs; mounting, in-line, and jam-nut receptacles; and protective covers.

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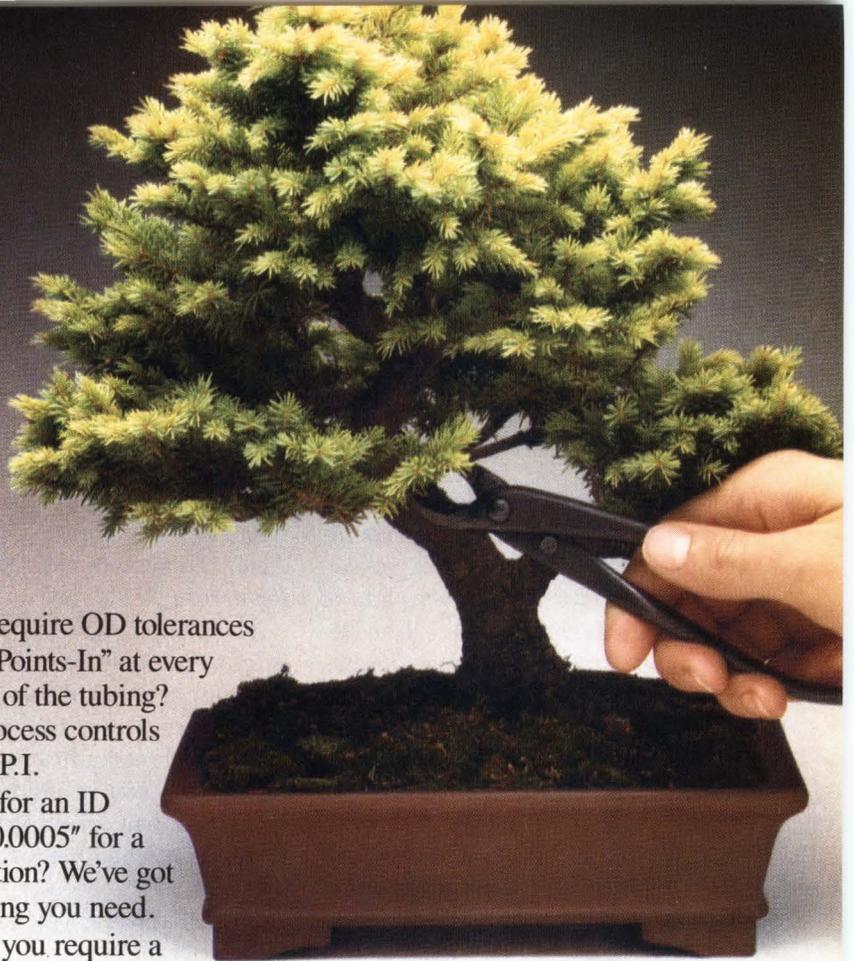
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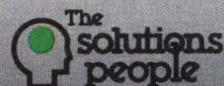
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SOFTWARE REVIEW

Filter-design package offers a variety of filter types

Filter Design and Analysis System. Momentum Data Systems, 1666 Newport Blvd, #115, Costa Mesa, CA 92627. Phone (714) 548-3257. Version 2.0, \$895; code generation, \$200.

Designing filters is easier when you don't have to calculate filter coefficients. It's even easier when you can try various filters and view plots of their characteristics. The Filter Design and Analysis System allows you to design, evaluate, and create code for a variety of digital filters. The system is well documented, easy to use, and very flexible.

The package runs on IBM PC, PC/XT, PC/AT, PS/2, and compatible computers. It supports most popular graphics interfaces, printers, and plotters. The graphs displayed on the CRT and the hardcopy devices provide a higher quality

than most filter-design packages—high enough for use in reports and manuals. You can use a graphics-interchange file that lets you incorporate the plots in various desktop publishing systems. The software is easy to install; the manual provides easy-to-follow instructions. Operating the system is also easy—its menu-driven operation guides you. Also, the system checks your input for errors while you're entering it.

The main menu lets you design an infinite-impulse-response (IIR), finite-impulse-response (FIR), or equiripple filter; analyze a digital system; or read a filter-specification file. After you've made selections from the menu, the program accepts the screen when you press function key F10.

For IIR filters, you can employ a bilinear-transformation or impulse-invariance design method to design a lowpass, highpass, bandpass, or

bandstop filter. You enter the characteristics of the filter by filling in blanks. The system then calculates the estimated order for four types of filters: Butterworth, Chebyshev, elliptic, and Bessel. You then select the filter type and order.

Next, the output-options screen is displayed. This screen allows you to select from a wide variety of plots on the screen and on the hardcopy. You can "zoom" by selecting start and stop ranges. The plot options include magnitude, log 10 magnitude, poles and zeros, impulse and response, group delay, phase, and step response.

In addition, the output-options screen allows you to quantize the filter coefficients over the 8- to 32-bit range. All of the internal calculations provide 64-bit, floating-point precision. The quantization option allows you to vary word sizes and determine the effects of the

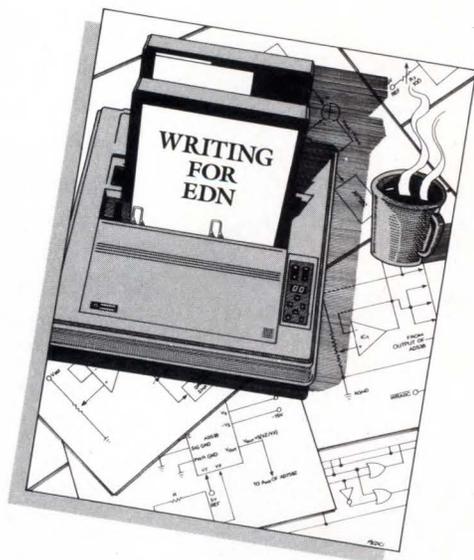
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*Rev. C, Paragraph 1.2.2

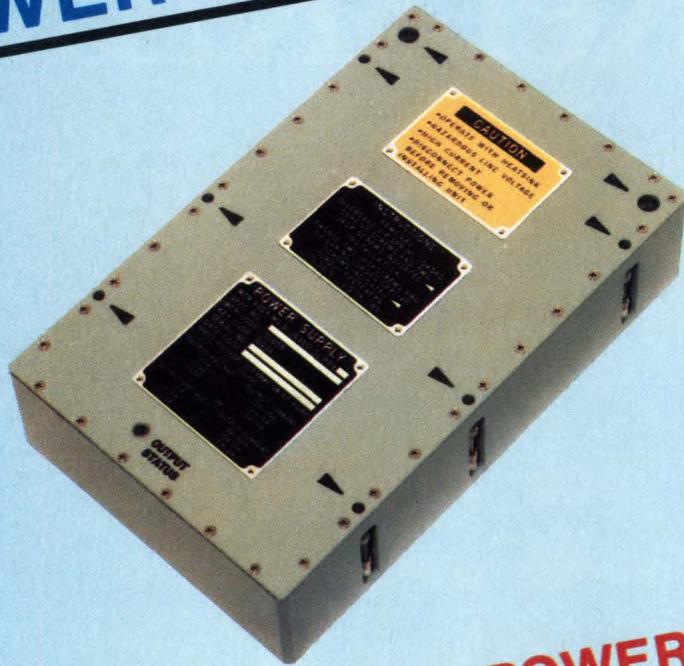


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SOFTWARE REVIEW

resolution. Other options allow you to create files for code generation, for future use, and for graphics interchange.

The FIR-filter design option works in a similar way. It supports lowpass, highpass, bandpass, bandstop, and differentiator filters with rectangular, triangle, Hanning, Hamming, Blackman, and Kaiser window functions. Once you've entered the filter characteristics, the system gives an estimated number of taps for each filter type. As in the IIR option, an output-options screen controls the output; however, it supports only magnitude, log-10-magnitude, impulse-response, and step-response plots.

The equiripple FIR-filter design is based on the Parks-McClellan algorithm; it helps you design lowpass, highpass, bandpass, bandstop, differentiator, multiband, Hilbert-transform, and arbitrary-magnitude filters. The use of this section is similar to that of the FIR option, except that in the equiripple option, you have to enter each band. The characteristics you use should be realistic: If your band transition is too steep, the system will not produce a result.

The analysis system also lets you analyze digital systems. You enter the transfer function in either the s or the z domain. You can then use an output-option screen similar to the one the IIR filter provides.

Two code generators take the filter you designed and convert it to source code. One generator creates code for the Motorola DSP56000, and the other produces code for the Texas Instruments TMS32010, TMS32020, and TMS320C25.

—David Shear

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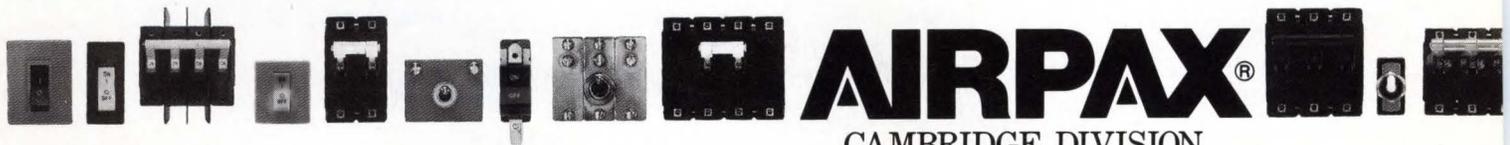
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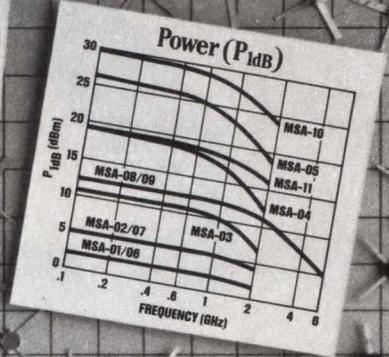
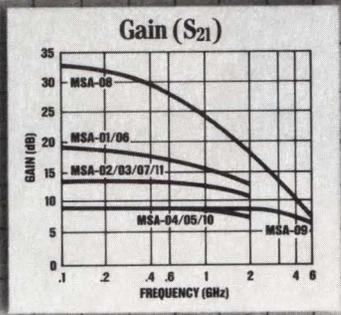
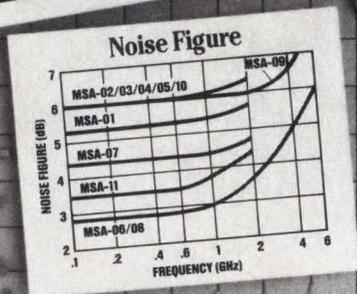
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BOOK REVIEW

A "civilized" look at the engineering profession

The Civilized Engineer, by Samuel Florman. 258 pgs; \$15.95. St Martin's Press, 175 Fifth Ave, New York, NY 10010.

Richard Simonelli,
Engineering Consultant

Are you a civilized engineer? Do you know something about the history of our profession? Do you know what motivates us as professionals? Have you thought about the profession's strengths and weaknesses?

Samuel Florman raises these prickly questions and many more in his controversial book, *The Civilized Engineer*. If you missed the book when it was first published in 1987, then read it now. Florman, a practicing civil engineer, provocatively discusses engineering's place in modern society and our values. He covers the ethics, the responsibili-

ties, and the risk-taking issues posed by the Challenger disaster.

The author's arguments are direct—neither pedantic nor abstract. His tone expresses a deep pride in the profession, but at the same time, acknowledges that something is amiss.

Metaphorically, Florman argues, engineers are "uncivilized." To Florman, civilization refers to a broadening of horizons and a deepening of cultural awareness. Are we too narrowly educated and focused on our work to be effective as well-rounded citizens in the complex future?

The author traces the roots of engineering back to toolmaking. He follows the trail through ancient Greece and Rome, on to the Middle Ages and the Renaissance. Finally, he places modern engineering's origins in the tradition of Western craftsmanship.

During the industrial revolution

of the 17th and 18th centuries, the British took a hands-on approach to engineering, while the French and continental approach emphasized polytechnic education and cooperation among government, industry, and academia. However, both approaches are alive today in North American engineering.

Florman points out that the term "ethics", as it applies to engineering, means something quite different from its meaning in other contexts. He writes: "A conscientious engineer, by definition, can not falsify test reports or intentionally overlook questionable data, cannot in any way evade the facts." As engineers, our ethics and viewpoints result from the black-and-white nature of our products: Things must work.

Florman always renders criticism with respect. His purpose is not to shock or denigrate the engineering

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BOOK REVIEW

profession, but to ask the unaskable. But some of his conclusions are grim:

- As engineers, our interests are narrow, and our specialties are all-consuming; we can't afford to be curious about areas outside our work.
- We are often insensitive and indifferent to human rela-

tions, finding them to be too much of a gray area.

- Compared with other professions, we are poorly educated in the humanities, and we are contemptuous of such learning.

As a result of these shortcomings, Florman contends, we fail to comprehend the cultural and social im-

plications of our work, preferring to look the other way. As psychological types, he adds, we are often wooden, rigid in areas outside of technology. Florman maintains that we're easily manipulated as a group, and that we contribute less than our share to community and national leadership. It is courageous and timely of Florman to air this subject.

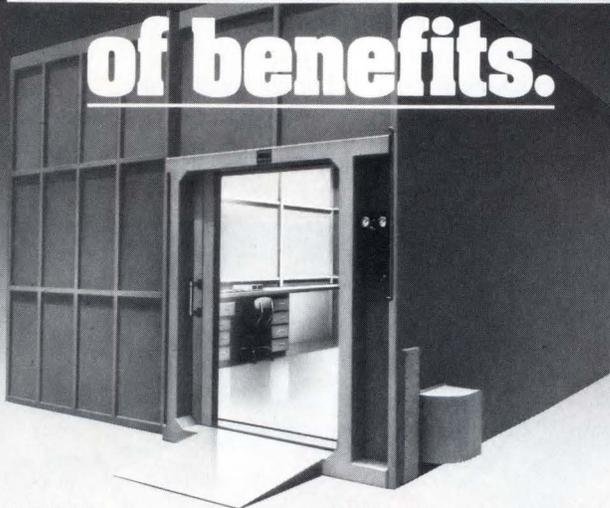
Florman encourages us to improve the humanities education available to those engineering students desiring it. Current accreditation standards require engineering students to take 12.5% of their courses in liberal-arts areas, yet, Florman says, most students show disdain for such studies. "Most of the young engineering students I meet these days want to take technical courses that will maximize their chances in the job market," he laments. "They don't want to spend a day or a dollar more than necessary in pursuing their degrees, and they are not at all convinced that the humanities are relevant to their concerns."

Florman believes that a better grounding in the humanities and social sciences would prepare more students for an engineering career involving leadership and communication skills. The idea of encouraging some students, and not others, to prepare for a leadership role naturally leads to cries of elitism. However, he argues that each person should have the opportunity to rise to the full extent of his or her abilities.

An engineer will come away from this book with both a sense of pride and a challenge not to rest on his or her laurels. It places the profession in perspective and makes concrete proposals for changes that will benefit the individual engineer, the profession, and our society. **EDN**

Richard Simonelli is an engineering consultant in Boulder, CO.

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CIRCLE NO 238

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CIRCLE NO 239

Design firms: A little bit of engineering heaven

Deborah Asbrand, *Associate Editor*

Independent design firms differ from traditional manufacturing companies in many ways. For one thing, they don't require engineers to perform product-support tasks or to prepare voluminous amounts of paperwork. They're strictly no-frills environments—no thickly carpeted, color-coordinated offices. Instead, the emphasis is on engineering. When clients are footing the bill, designs that are "good enough" aren't good enough. A client-driven, deadline-oriented environment isn't for everyone, but for engineers who enjoy that atmosphere, it can be a little bit of engineering heaven.

Engineer Bernard Daines founded Tidewater Associates, a Union City, CA, design house, in 1984. After having worked for two years as an independent consultant, Daines was anxious to take on meatier assignments. "I had a hunger to do bigger projects than I could on my own," he says. In 1981, he invited his younger brother, Nolan, to join his consulting practice, and three years later, they incorporated to form Tidewater.

The concept of a "full-service development firm," as Bernard Daines likes to call it, is new. Independent consultants and job shoppers are fixtures in the electronics industry. But the idea of a service company that maintains its own facilities and equipment and uses them to develop products for other companies is a new twist. Many people, Daines admits, aren't sure quite what to make of this recent addition to the electronics sector. To help remedy the situation,

Daines recently hired a public-relations firm to promote not only Tidewater's services but also simply the idea of a full-service development firm.

Consulting companies such as Tidewater are sometimes referred to as "hired guns." Daines doesn't appreciate the

"All we have to offer is hard work and interesting projects."



Tim Davis

Bernard Daines, Founder, Tidewater Associates

“Clients’ engineers need to support and manufacture a product. They want to maintain a close link with the designers.”

comparison. The company emphasizes that its working style is cooperative. “Clients’ engineers need to support and manufacture a product,” sales and marketing director Mike Gifford asserts. “They want to maintain a close link with the designers.”

Tidewater’s perseverance as a full-service development firm has paid off—its business is booming. In the company’s early days, a \$150,000 contract was a large one. Now, says general manager

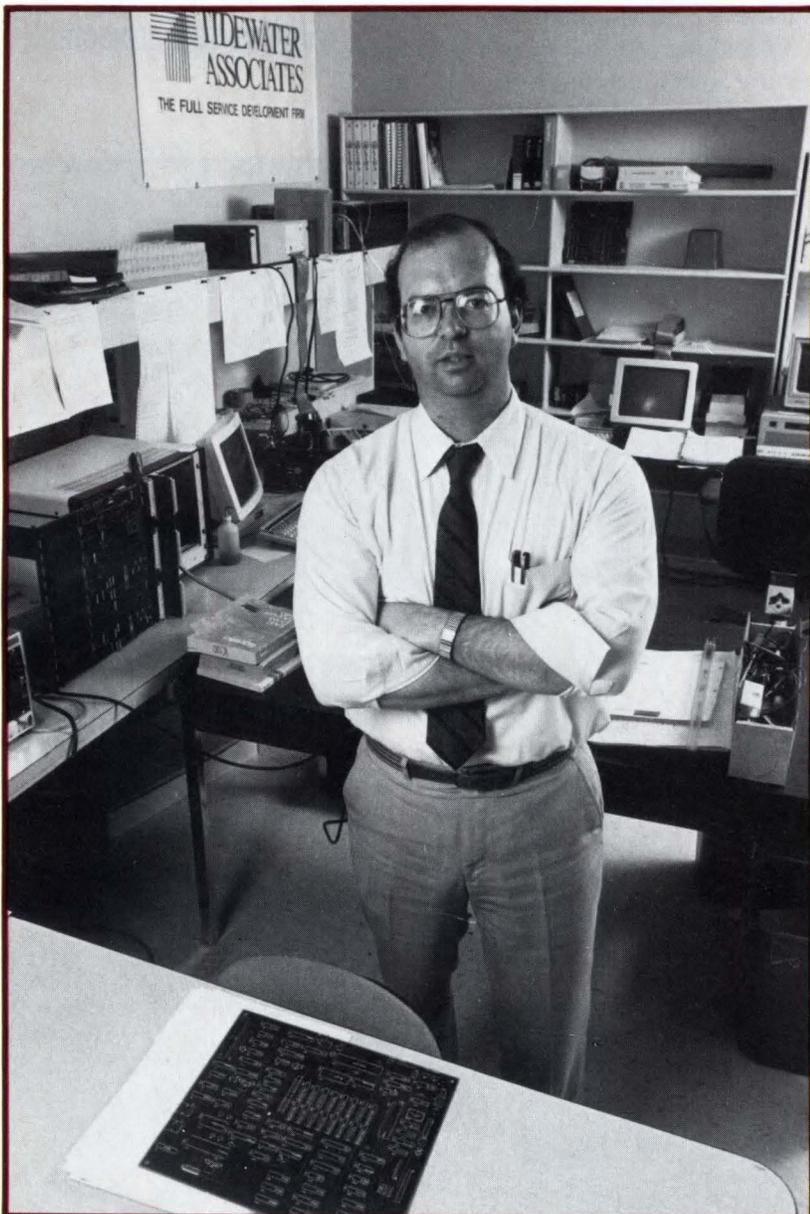
Larry Heaton, that’s about the smallest contract the company will accept. This year, the company expects to pull in \$8 million in revenue.

Tidewater’s Union City location typifies its no-nonsense attitude. Union City is short on local color; it got its inauspicious start 20 years ago when area townships filled in the marshy, southernmost tip of San Francisco Bay. Today, it’s a city made up largely of industrial parks. Work is the order of the day.

The firm currently occupies 15,000 square feet of space, which it has leased since 1981, when the Daines brothers moved their operation out of their garage. The space, once mostly vacant, is now nearly filled, as a result of the company’s growth. The company’s quarters feature few of the usual corporate props. Instead of finding the typical roomy lobby with floor plants, couches, and an oversized version of the company logo behind a receptionist’s desk, visitors to Tidewater squeeze into a small, plain waiting area. In contrast, generous amounts of space have been set aside for design, assembly, and manufacturing. Four cavernous bays, allow ample room for work on clients’ products.

Notably absent from the structure are the ubiquitous modular cubicles that pass for office space in most companies. Tidewater maintains genuine offices for its engineers and technicians alike. Individual work spaces are walled off, and incandescent lighting softens the interior atmosphere. Also noticeably missing, however, are doors to each office. Bernard Daines chose to keep the offices doorless as “a compromise between openness and privacy.”

Clients retain Tidewater, and other design houses like it, for a number of reasons. Some engineering departments, for example, have come up with new ideas, but are too busy with existing projects to undertake the new ones. In other companies, the development of a



Tim Davis

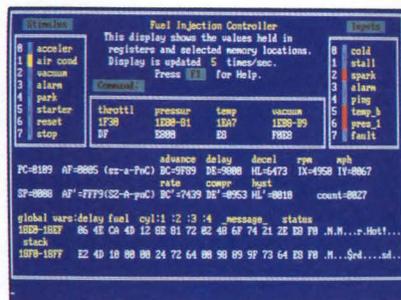
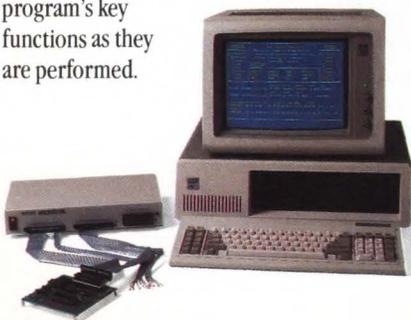
Mike Gifford, Sales and Marketing Director

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new product requires engineering expertise in an esoteric area, and rather than recruit and hire an engineer with the necessary knowledge, the company turns to a service company. Start-up companies that as yet lack their own engineering departments are also customers.

For some companies, the decision to approach a design firm for assistance can be gut-wrenching, particularly for firms that have gone to great expense to hire talented engineers only to load them with so much work that they're unable to proceed with the development of a new-product idea. "We may talk to a vice president of engineering who feels guilty about coming because he's got a staff full of engineers," says Gifford. "He also may be wrestling with the not-invented-here syndrome."

For the engineers who work at Tidewater, the client-driven atmosphere can be a pressure cooker. At any given time, Tidewater's engineers are working on 20-odd projects of varying sizes. The company bills its clients for its engineering services, and each engineer must keep meticulous track of the time spent on various projects. With clients footing the bill, deadlines take on new meaning. Says general manager Heaton: "At most companies, you have a deadline you don't make and you go in and ask for another six weeks. Here you can't do that."

Like employees of any service-oriented business, Tidewater's engineering staff must acquire a certain amount of finesse in working with their clients. "We once ran into a 3-week delay while a client decided on the color of a keyboard," sighs Heaton.

With each engineer juggling several projects at once and facing constant deadline pressures, there's little time for conversations at the water cooler. Tidewater's growing business keeps the engineers' between-project time to a minimum. Paul O'Connor, who joined Tidewater in 1987, says that his previous jobs with defense contractors always

included a cooling-off period between contracts. It's not so at Tidewater, he says; there's always a new project to be tackled.

That kind of intensity isn't for everyone. Tidewater has lost several talented engineers who simply felt that the required level of involvement was too much for them. Mukesh Patel had similar thoughts when he joined the company in 1985. Battle weary from years of negotiating Silicon Valley's congested freeways, Patel's criterion for a new job had been reduced to one simple requirement: He wanted a commute of no longer than 15 minutes. Tidewater, located just a short distance from his home, fit the bill. Though he loved the short commute, he had originally planned to stay just one year. "I thought this place would be a sweatshop," he concedes. Since joining the company, he's worked on a project in video imaging, one in voice synthesis, and Project Victoria, an ISDN project. Now, he enthuses, there are few engineers in Silicon Valley who can match his resume. Agrees Nolan Daines: "We get to do the stuff that really raises the hair on the back of your neck."

The charged atmosphere results from Bernard Daines' business savvy rather than any desire to create an engineering utopia. "It wasn't structured to be a mecca for engineers, because all we have to offer is hard work and interesting projects," explains Daines, who is himself a veteran of Hewlett-Packard and IBM. "The thing that makes working here interesting is that the engineers don't have to live with a project for three years. I'm not knocking that, but I think there are a lot of really creative people who are banging out logic designs and feeling very frustrated."

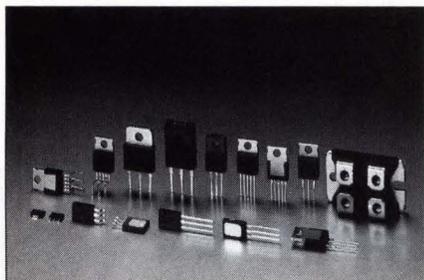
Indeed, a single recruitment ad for Tidewater typically produces 50 resumes. Tidewater is selective, and not everyone makes the grade. Heaton estimates that 20 to 25 of the inquiries are from qualified applicants, and of those,

A client-driven, deadline-oriented environment isn't for everyone, but for engineers who enjoy that atmosphere, it can be a bit of engineering heaven.

High Performance N-Channel PowerMOS Transistors

A new family of nearly 200 n-channel PowerMOS transistors from Philips Components offers the highest performance available, yet costs no more than existing devices. The BUK family of transistors spans low, medium and high voltages (up to 1000 V), and includes devices for use in such applications as automobiles and inverters.

The low-voltage transistors have cell densities of 1.6 million cells per square inch, which results in drain-source on-resistances as low as 25 m Ω . This feature is a key measure for PowerMOS devices, and corresponds to drain currents up to 56 A. Philips' new BUK family includes 14 low-voltage logic-level devices for 12 V battery operation in automotive and industrial applications, and 13 high-voltage FREDFETs for bridge or half-bridge applications in motor control, uninterruptible power supplies and inverters.



There are 74 low-voltage transistors with crystal sizes between 6 mm² and 20 mm², and with maximum drain-source voltages between 50 V and 200 V. Even the lowest voltage transistors in the family, such as the 50 V BUK453-50A, can carry up to 22 A drain currents because of $R_{DS(ON)}$ values as low as 80 m Ω .

There are 72 medium-voltage devices with drain-source voltages between 400 V and 600 V. These devices include 400 V transistors with $R_{DS(ON)}$ values of 400 m Ω and maximum drain-source currents of 14 A, and 600 V devices with $R_{DS(ON)}$ values of 800 m Ω , passing currents of 10 A.

Thirty-eight high-voltage transistors withstand between 800 V and 1000 V. These include 800 V devices with $R_{DS(ON)}$ values down to 1.5 Ω and corresponding drain-source currents above 8 A, and 1000 V transistors with $R_{DS(ON)}$ values of 2 Ω , passing currents of nearly 7 A.

Switching times are in the low tens of nanoseconds, allowing the transistors to operate at frequencies up to 10 MHz in resonant power supplies, for example. The devices are available in a choice of

five packages, from the SOT-186 – a fully isolated version of the TO-220, which dissipates up to 30 W – to the SOT-93 (TO-218), which dissipates up to 250 W. Devices in other packages are in development.

CIRCLE NO 259

Range of SensorFETs Provides "Loss-less" Load Protection

By dedicating a few of its cells to current sensing, this range of SensorFETs from Philips Components provides "loss-less" overcurrent, or short-circuit, protection for a wide variety of automotive and industrial applications.

Unlike most power MOSFETs, which detect load currents using a high-power resistor, these new SensorFETs use some of their current-carrying cells to direct a proportion of their current – a few milliamps – to an external control-regulation circuit.

The four SensorFETs that make up the BUK700 series can be used whenever current limiting is needed to protect equipment – such as motor drives – from damage. The BUK793 and BUK795 have maximum drain-source voltages of 50 V or 100 V.

These SensorFETs have densities of 1.6 million cells per square inch, the highest in the industry for these types of devices. This density cuts the drain-source on-resistance to between only 40 m Ω and 800 m Ω , depending on the device, and leads to current-handling capacities of up to 40 A for the 50 V devices and up to 25 A for the 100 V devices.

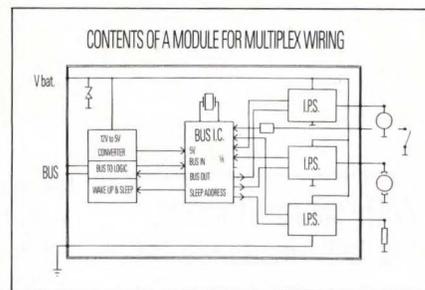
The SensorFETs come in TO-220 Pentawatt packages. Samples are available.

CIRCLE NO 260

11 A High-side Switch for Automotive Applications

A new MOS Intelligent Power Switch has a drain-source, on-resistance $R_{DS(ON)}$ of only 33 Ω , four to eight times lower than that of other such devices. Called the BUK196-50, the new device from Philips Components passes a drain-source current of only 11 A and its $R_{DS(ON)}$ matches the low contact resistance of mechanical relays, making it a suitable replacement for such relays in a variety of automotive and industrial applications.

The BUK196-50 is an n-channel transistor that fits on the battery-side (high-side) of the load. It incorporates short-circuit and thermal protection, and features current-sensing circuits. An integ-



ral charge pump boosts the car-battery voltage to ensure that the MOSFET saturates fully, even when the battery voltage falls to 6 V. A status indicator signals that the device is functioning, thus closing the feedback loop between the drive and switch.

The device connects directly to the industry standard decoders for the multiplexed bus systems that will appear in the next generation of automobiles.

The low on-resistance comes from the high cell density – 1.2 million cells per square inch – of the BUK196-50. The high cell density also leads to the device's 11 A rated current, which is maintained even with a case temperature of 85 °C and battery voltage as low as 6 V. The low on-resistance also leads to low losses – the device has a low quiescent current of less than 10 μ A.

The transistor also has a maximum drain-source voltage rating of 50 V. Its projected MTBF is as good as the standard Philips MOSFET.

The BUK196-50 comes in a TO-220 Pentawatt package. Samples will be available in November.

CIRCLE NO 261

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With clients footing the bill, deadlines take on new meaning. Says general manager Heaton: "At most companies, you have a deadline you don't make and you go in and ask for another six weeks. Here you can't do that."

no more than six make the second cut and are interviewed. "We get people who come in and say they've been doing 68000 work for 15 years," says Heaton. "But their involvement has been taking a small segment and passing it on. Those people don't have the global understanding of the product that we need here."

John McGinnis is an industry veteran and specialist in image recognition. He's now director of engineering for Tidewater. He characterizes the company's environment as "very, very different" from the other companies he's worked for. In the engineers he hires he looks for "a willingness to take chances—not someone who wants to analyze something forever."

Despite the breadth of his managerial responsibilities, Bernard Daines manages to remain an active team member

on about four projects at a time. He enjoys the thrill of the new-product chase, he says, and he looks for that same enthusiasm in the engineers he hires. "I'm excited about every new project that we start. If the same enthusiasm to build things and make things work isn't there, then the person isn't suited to this thing." **EDN**

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EDN

Editorial Emphasis

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News
Sept. 15	Aug. 25	Data Acquisition, Data Communications, Digital ICs	Closing: Sept. 1 Mailing: Sept. 22
Sept. 29	Sept. 8	DSP, Graphics, Optoelectronics	
Oct. 13	Sept 6 22	Test & Measurement Special Issue, Instruments, Computers & Peripherals	Closing: Sept. 29 Mailing: Oct. 20
Oct. 27	Oct. 6	CAE, Computers & Peripherals, Integrated Circuits, Wescon '88 Show Preview	
Nov. 10	Oct. 20	Programmable Logic Devices, Integrated Circuits, Test & Measurements, Wescon '88 Show Issue	Closing: Oct. 27 Mailing: Nov. 17
Nov. 24	Nov. 3	Microprocessor Technology Directory Graphics, CAE	
Dec. 8	Nov. 16	Product Showcase—Vol. I, Power Sources, Software	Closing: Nov. 21 Mailing: Dec. 15
Dec. 22	Dec. 1	Product Showcase—Vol. II, Computers & Peripherals, Test & Measurement	

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CV/ CADD System Administrator

This position is responsible for the operations and support of Computervision CADD4X Systems. BS in Computer Science with at least 3 years experience with CV/CADD System Management, knowledge of CADD4X/CGOS environment is required. SUN/UNIX systems knowledge is desired.

MANUFACTURING

(When writing in response to the career opportunities listed in this category, please use address listed below, attention: MANUFACTURING)

Industrial Engineer

B.S. degree in Industrial Engineering or Industrial Technology. Substantial knowledge of manufacturing processing in at least one of the following areas: forming and bending, machining, welding, heat treat, chemical processing and painting. Analyze and interpret engineering drawings and

specifications for production application. Estimate all standards for bids and production floor operations. 2 to 3 years experience required.

Quality Control Engineer

B.S. degree in Engineering, Industrial Technology, or Quality Assurance. Five years minimum experience in a Quality Engineering function with a strong working knowledge of MIL-Q-9858 and MIL-STD-1520. Involves extensive investigation of failure analysis and problem resolution. Must possess good verbal and written communication skills in interactions with customer representatives.

FMC offers an excellent salary and a comprehensive benefits package. For prompt consideration please send resume, including your salary history and requirements addressed to either Engineering, Technical Computing or Manufacturing at: FMC Corporation Ground Systems Division, 328 W. Brokaw Road, P.O. Box 58123, Dept. 17-88-05, Santa Clara, CA 95052. We are an Equal Opportunity Employer.

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FMC

ARE YOUR IDEAS AHEAD OF OUR TIME?

Stonehenge, one of the most famous of all the classical megalith monuments, has long been an important part of the popular and scientific imagination. Its origin has been the cause of speculation for years, as scientists try to discern who had the intellect and ingenuity to create a celestial observatory of such astronomical significance and exactness.

What is clearly understood and shared these 4,000 years later is man's unceasing fascination with the heavens and his need to explore them for a better understanding of his place in time and space.

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You can now be a part of our exciting time in history. Your ideas and accomplishments could be chronicled for future generations to study as hallmarks of a brilliant epoch in space exploration.

We currently have opportunities available in the areas listed below for individuals with a technical degree or the equivalent combination of formal education and related experience. Government or aerospace industry background is preferred. If you are interested in one or more of these areas, please send your resume to: Professional Staffing, GENERAL DYNAMICS SPACE SYSTEMS DIVISION, MZ C2-7143-I252, P.O. Box 85990, San Diego, CA 92138.

(Opportunities also exist in Huntsville, AL and Harlingen, TX.)



AVIONICS

- EMI/EMC
- Electrical Power
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- RF Systems
- Parts Engineering
- Harness Design/Installation
- Liaison
- Analog/Digital Circuit Design
- Avionics Systems
- Mechanical Packaging
- Control Systems
- Guidance & Navigation

QUALITY ENGINEERING

- Tool Design/Proofing
- Software Quality Assurance
- Process Control
- Radiographic Inspection

FLUID SYSTEMS DESIGN

- Pneumatic
- Hydraulic
- Propulsion
- Cryogenics

STRESS ANALYSIS

- Hand Analysis
- Finite Element Modeling
- Structural Test Support
- CAE
- Methods
- Advanced Composites

SYSTEMS

- Systems Requirements
- Systems Safety
- Environmental Engineering
- Security Engineer
- Software

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- Tank Structures
- Adapters
- Fairings
- Materials & Processes
- Pre-Design
- Mechanical Liaison
- Superconducting Magnets
- Drawing Checkers

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- Environmental Dynamics
- Acoustics
- Jettison Trajectory
- IRAD & CRAD
- CAE

THERMAL/FLUIDS ANALYSIS

- Systems Modeling
- Space Environments
- Propulsion
- Cryogenics

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PROCUREMENT

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PRODUCTION

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Careful strategic planning has provided Martin Marietta with the diversified and solid contract base needed to thrive in the years to come. Some of the contract victories won by Martin Marietta and being worked on at Aero & Naval Systems in Baltimore, are the Vertical Launching System, MK 50 Torpedo, Titan and WAA.

Other current program activity includes work in:

- **Autonomous Underwater Vehicles**
- **Advanced Lightweight Sonar**
- **Remotely Piloted Air Vehicles**
- **ASW Research & Technology**
- **Surface Weapons Systems**
- **Combat Systems Engineering**
- **Robotics**

These and other exciting projects require us to seek out experienced engineers with a technical MS/PhD or at least one year experience in:

Manufacturing Engineer

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- Cutter Specialist

Production Control

- Planners
- System Programmers

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- Test & Evaluation
- EMI/EMC Definition
- Systems Test Requirements
- Interface Integration

Systems Analysis

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- Simulation & Modeling
- Mission Analysis
- Sensor Performance

Software

- Discrete Simulation
- ATE Software Design
- State Table Design
- Test and Evaluation
- Autonomous Underwater Vehicle Software

Robotic Systems

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- Supervisory Vehicles
- Manipulator Design

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- Microprocessor Applications

- VLSI Design
- ATE/Teradyne
- Analog & Digital Design

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- Noise Control Engineer

Logistics Engineering

- Systems Safety

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- Electronic Process Engineer
- Welding Engineer

We also have opportunities for these professionals:

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- **Contract Administrators**
- **Master Program Planners**
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Help us do what GE does best...

If you are intrigued with the idea of working years in advance of current technology with some of the industry's leading engineering professionals, you should consider a career with GE System Engineering. Positions are available with our operations across the United States including **VALLEY FORGE, PA, WASHINGTON, DC, HUNTSVILLE, AL, COLORADO SPRINGS, CO AND LOS ANGELES, CA.**

The GE System Engineering Team.

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System Simulation
Survivability/Vulnerability
Spacecraft Systems Engineers
Ground Station Systems Engineers
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Launch Operations Engineers
System Requirements Engineers
Mission Analysis Engineers
Advanced Systems Engineers
Communications Systems Engineers
Control Systems Engineers

Systems Serviceability Engineers
Senior EMI/EMC Engineers
Radiation Effects Engineers
Interface Development Engineers
Configuration Control Engineers
Program Control Engineers
System Verification Engineers
System Test Engineers
Reliability/Availability Engineers
RF Engineers
Antenna Systems Engineers
Structural Dynamics Engineers
Power Systems Engineers
Software Systems Engineers
Data Systems Engineers
Computer Systems Engineers
Information Systems Engineers
System Analysis Engineers
Command & Control Systems Engineers
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Orbit Analysts
Trajectory Estimation Analysts

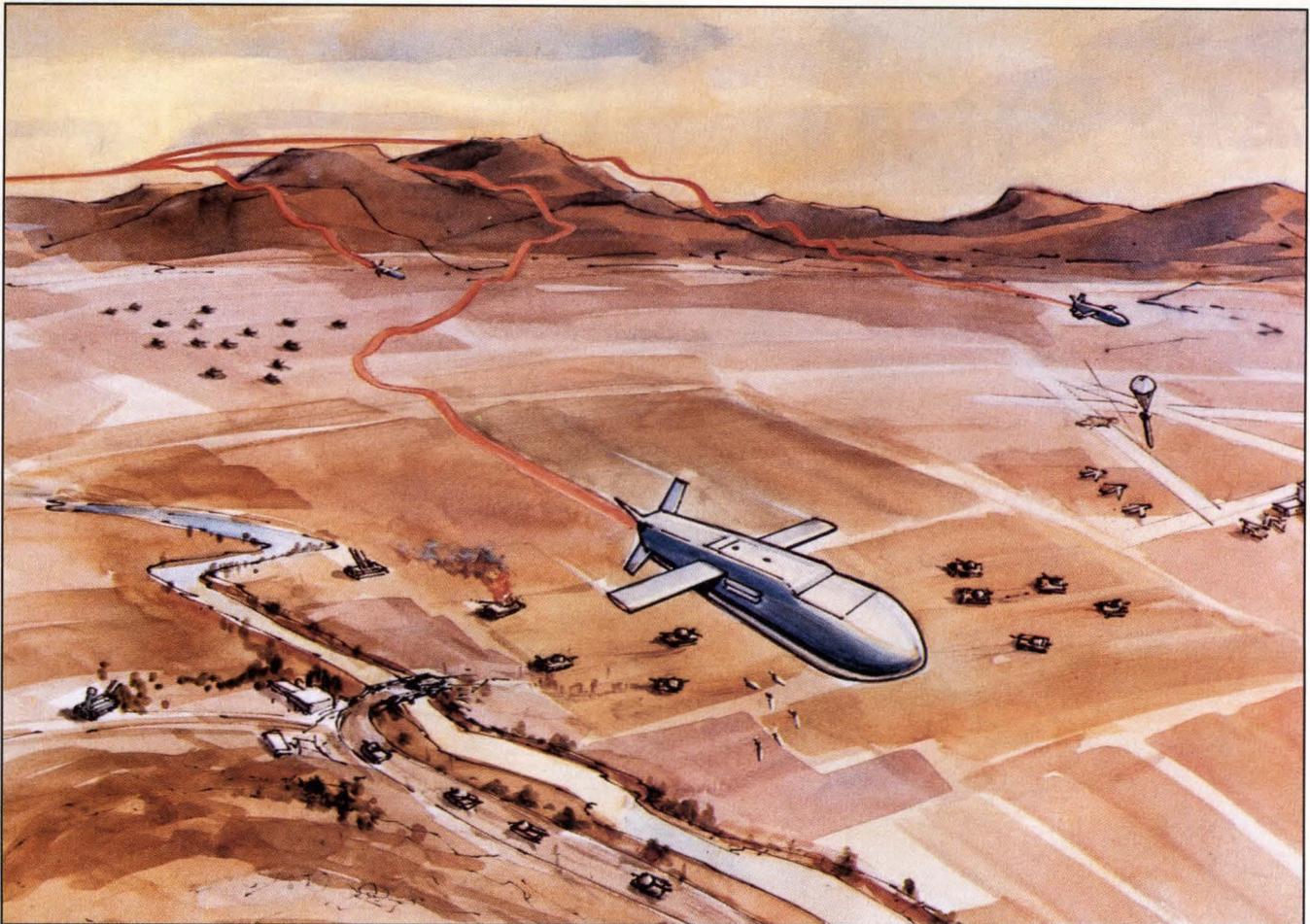
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Textron Defense Systems combines the strength of superior resources with advanced design, research and manufacturing achievements. We offer people with talent, leadership and imagination the unique opportunity to put their best ideas into action. We are able to support outstanding performance in every way, from advanced design tools to our leading edge technical commitment.

These positions require educational levels from BS to PhD in a technical discipline and upwards of 3-15 years related experience. All openings require U.S. citizenship. For consideration please forward your resume to: Paul Smith, 3 AV 14 Textron Defense Systems, 201 Lowell Street, Wilmington, MA 01887. An equal opportunity employer

TEXTRON Defense Systems

A Tale of Two Cities

Join the engineers working on the AN/BSY-2
...the remarkable, fully integrated combat system
for the Navy's new SSN-21 Seawolf



With One Mission.

SYRACUSE, N.Y.

At GE Government Electronic Systems Division in Syracuse, we're taking undersea technology to new heights. And you can be part of it.

Exciting positions are now available to work on the SSN-21 Seawolf submarine project...developing systems architecture and providing overall program management for the AN/BSY-2. This marvel of sensor, processing and command hardware and software is our greatest achievement yet, confirming our position as a world leader in sonar and ASW.

Surface ship acoustic technology is another area of GE leadership in which we have a whole range of challenging opportunities.

To be part of this tremendous effort, see if you qualify for one of the following positions.

Software Architecture

Requires 7+ years experience in large systems design involving embedded programmable processors (68000 or similar processor). Familiar with top down structured design in ADA or Fortran.

Combat Systems Engineering

Requires 5+ years in analysis, design and development of large scale shipboard ASW systems. Must be knowledgeable in weapons control systems engineering, reliability/maintainability and human factors.

Acoustics/Signal Processing

Systems engineers with 5+ years design experience involving towed and remote sonar arrays. Sensor systems design and algorithm development are key requirements, also target motion analysis.

Sonar Array Hardware

Project engineers with 8+ years experience in advanced architecture and design of sonar hardware. Will lead a development team in all related functions: wide aperture array design, transmitter design, electronics packaging, cabinet design, simulation and modeling, etc.

Program Management

Must have 10+ years in-depth experience in ASW systems development. Broad ranging software/hardware knowledge. Experience in large program prime contractor environment. Subcontractor management experience.

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Software engineers with 7+ years military electronic systems experience, including knowledge of MIL-S-483/2167/2168.

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MOORESTOWN, N.J.

Deep thinking continues at RCA Electronic Systems Division in Moorestown, where our top-notch team of engineers continue to make major contributions to the design of the AN/BSY-2...a fully integrated combat system.

This highly impressive hardware/software with superior automated command/communication functions and unsurpassed time saving data information processing, represents some of the most sophisticated ASW technology ever developed for the U.S. Navy.

The specific positions now available will afford engineers the opportunity to work on these vital system challenges for the SSN-21 Seawolf...the submarine of the future. See if you qualify for one of the following positions.

Senior Engineers, Combat Control

- BSEE
- 5+ years in Combat Control performance definition, design and test for real time Combat Control Systems.
- Knowledge of U.S. Navy systems, preferably submarine systems.

Senior Digital Design Engineers

BSEE, with 5+ years experience in the digital/firmware design of digital sub-systems. Should also have experience in the design of special purpose digital processors with strength in current custom design and simulation techniques.

Senior Software Design Engineers

BSEE or BSCS with 5+ years direct experience in the design and development of large real time Command and Control Systems which utilize sensor data input. Experience with the following:

- Fault location/fault detection with a plus for automatic configuration design experience.
- Real-time data base design experience with Ingress or Oracle.
- Motorola 68020 assembly language, and/or real time operating system experience.

Senior Engineers, Command & Decision

BSEE with 5+ years in Command and Control performance definition, design and test for real time Command and Control Systems. Should have knowledge of U.S. Navy systems, preferably submarine systems.

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Develop systems and subsystems, test requirements, and design validation. Requires specialization in anti-armor launching, fire support or target acquisition and the ability to communicate requirements to design engineering. BSEE and 5 years in optics, electro-stabilization, electronic design, or real-time software are desirable.

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Break new ground in optics, electro-optics, laser, radar, and land navigation products and programs. Requires BSEE (MSEE/MBA preferred) and 10 years experience with all aspects of anti-armor

missile launching and guidance systems and/or fire support target acquisition systems. Prior military experience would be a definite plus.

SENIOR TEST ENGINEER

Perform environmental and functional test planing, preparation, and conduct tests; design test fixtures, setups, and write test plans; and have lead responsibility for test programs. Position requires 5 years related experience with MILSPECS and formal documentation in analog, digital and RF systems.

SENIOR STAFF ENGINEER (POWER)

Generate, implement and monitor EMI, NEMP, ESD plans for electronic programs. Provide source data for filter procurement specs. MSEE or Applied Physics and 10 years specialized experience with MILSTD-461 and 462 EMI Control required. NEMP and nuclear effects experience desired.

DIGITAL DESIGN ENGINEERS

Requires BSEE and 5 years experience either designing control units, or working with real-time computerized signal processor and image processing with radar interfacing. Design experience with VHSIC and/or ASIC desirable.

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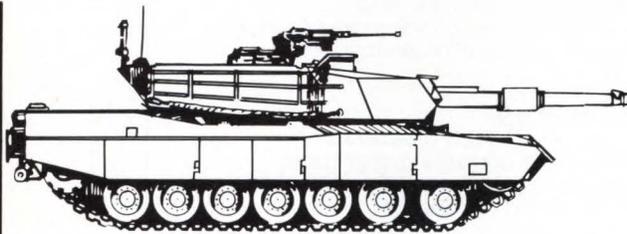
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Reliability Group Manager

You will manage reliability design engineering and product support activities, as well as failure analysis lab functions. Requires a minimum of 7 years related experience, including some at the supervisory level. BSEE or BS Physics expected.

Senior Reliability Engineer

Project coordination responsibilities in engineering and product support. Requires a minimum of 5 years related experience, and strong leadership and communication skills. You must be familiar with FMEAS, MIL-Specs, and reliability modeling, predictions and testing. BSEE or BS Physics necessary.

Mechanical Engineer

Your challenges will demand at least 6 years experience in the design, development and testing of dynamically tuned gyros, with an orientation toward project responsibility. BSME required.

Staff Engineer

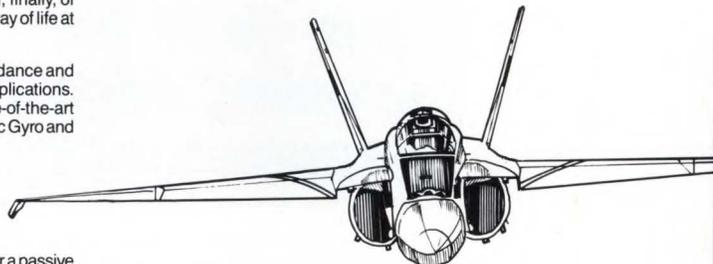
Sales support engineering will be among your challenges. Requires systems project technical experience in the design, development and testing of Strapdown Inertial Navigation Systems. Strong math and analytical skills are a must. BSEE necessary.

Materials Engineering Section Manager

Requires 7+ years experience, to include some at the supervisory level. Materials engineering experience in an aerospace instrument or electronic systems environment is preferred, with knowledge of printed wiring board fabrication and assembly, metal finishing, heat treatment and general metallurgy. BS in Metallurgy, Chemistry or Materials Science expected.

Senior Data Systems Engineer

Qualifications include a minimum of 5 years experience in military avionics system design, with strong hardware and software experience. You must be familiar with MIL-490 and MIL-2167 system requirements documentation; background in structural analysis is preferred, as is the ability to formulate interface control documents, white papers, proposals, etc. BSEE or equivalent.



Senior Software Engineer

Requires 5+ years experience in real-time, embedded, computer-based system development, involving system requirements specification, architecture design, function design and programming. Knowledge of formal development methods and the DEC VAX/VMS environment is essential. Familiarity with CASE tools is preferred, as is teaching/ training experience. Advanced degree in Computer Science or Electrical Engineering desired.

DTS Engineer

You must possess at least 5 years experience with data transfer systems, and a strong digital hardware background involving microprocessors. You must be able to write software requirement specifications, and to analyze system software/ hardware trade-offs. Presentation and communication skills are essential. BSEE or equivalent.

Process Engineer

You will be instrumental in improving yields and capabilities in circuit board assembly. Requires an Engineer with process experience (wave solder, touch-up, coating, etc.)

Electromechanical Manufacturing Engineer

Your responsibilities in our dynamically tuned gyro area will demand strong electro-mechanical skills.

Producibility Engineer

Our producibility improvement/cost reduction team will make full use of your expertise.

Logistics Engineer

Requires a minimum of 3 years logistics planning experience for avionics equipment, with knowledge of the LSA process, MIL-STD-1388 LSAR database, and military logistics/acquisition or USAF concepts. BSEE or equivalent.

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You will provide process engineering support to hi-rel assembly operations. Responsibilities will also include developing, monitoring and writing applicable specifications for yield enhancement. To qualify, you should have a BS in Chemical or Electrical Engineering and a minimum of 2 years' related experience.

Product/Test Engineering

You will provide product and test engineering support to ASIC product development activities. You will also provide test programs, evaluate test hardware and test program debug correlation evaluations. To qualify, you should have a BS in Electrical Engineering and a minimum of 2 years' ASIC product and/or test engineering experience. In addition, experience in Automated Test Program Generation (ATPG) would be a plus.

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You will provide front end design support at field offices and customer locations. You will also assist customers in the use of Harris design tools and CAD capabilities. **Positions available are in northern and southern California, Southeast U.S. and Northeast U.S.** To qualify, you should have a BS in Electrical Engineering or Computer Science and a minimum of 4 years' related circuit design experience. In addition, experience with cell-based or custom design automation tools is highly preferred.

Reliability Assurance Engineering

You will evaluate reliability characteristics of new processes by providing test structure designs, test procedures, data analysis techniques, failure mechanism models, and development of reliability design rules. An MSEE with an emphasis in solid state physics and a minimum of 2 years' related engineering experience are preferred. Experience in reliability theory, statistical analysis and modelling techniques is highly desired.

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 - Micro Processor
- Senior Electronics Optical System Engineer
- Senior Tactical Systems Engineer
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- RF Design
- Senior DOD Program Manager for Large Instruments
- Senior Optical Engineers
- DOD Marketing
- Electronic Optics Design
- IR Sensor Systems
- Hardware Systems Safety
- Reliability
- Spacecraft Systems
- Senior Spacecraft Systems Test
- Senior Signal Processing Engineer
- Senior Software Engineer

Send your resume to Ball Aerospace Systems Group, Human Resources, Dept. 53761, P.O. Box 1062, Boulder, Colorado 80306, or call 1-800-678-9030.

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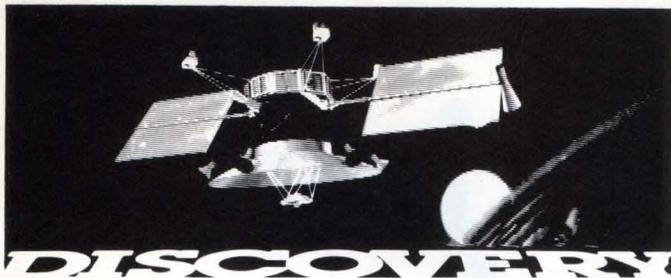
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- **MAN/MACHINE INTERFACE DESIGNERS** — design and implement man/machine interface software.

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- **SYSTEMS ENGINEERS** — technical monitoring and implementation of subcontracts.
- **SYSTEMS ENGINEERS** with experience in system level design and implementation trade-offs.
- **SYSTEMS ENGINEERS** with experience in Configuration Management development of documentation and modification process.
- **SYSTEMS ENGINEERS** with understanding of system level RAM and FMECA issues.
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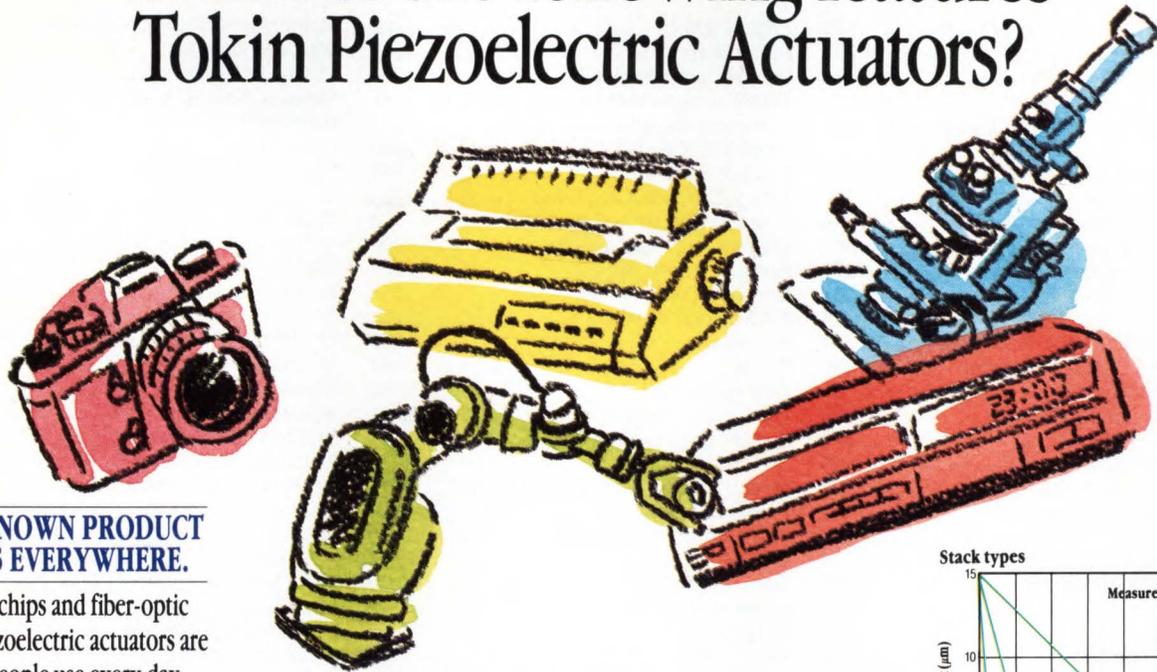
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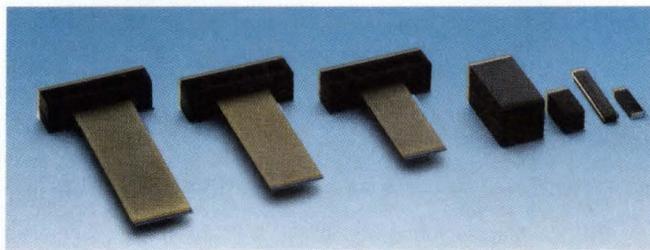
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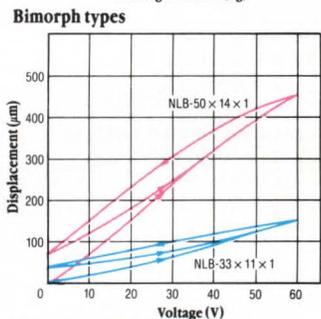
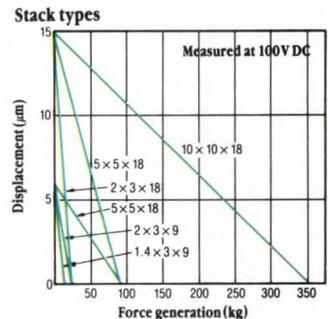
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NLA-5 × 5 × 18	15.0	87.0
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Bimorph types	(µm/60V) ±20%	(g/60V) ±20%
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"I COUNT ON **EDN MAGAZINE** AND **EDN NEWS** TO CREATE WORLDWIDE BRAND AWARENESS FOR OUR POWER SUPPLIES."

John R. Belden
Marketing Manager
Glassman High Voltage, Inc.

Glassman High Voltage designs and manufactures high-voltage DC power supplies with a difference. The most striking difference is that they're insulated with air, and contain no oil or potting compound.

Marketing Manager John R. Belden has watched Glassman grow from a small shop with a lot of innovative ideas to an industry leader. And EDN magazine and EDN NEWS have helped along the way. "The two publications get us the brand recognition and prestige we need," he says. "They go right to the engineers and engineering managers who make the buying decisions."

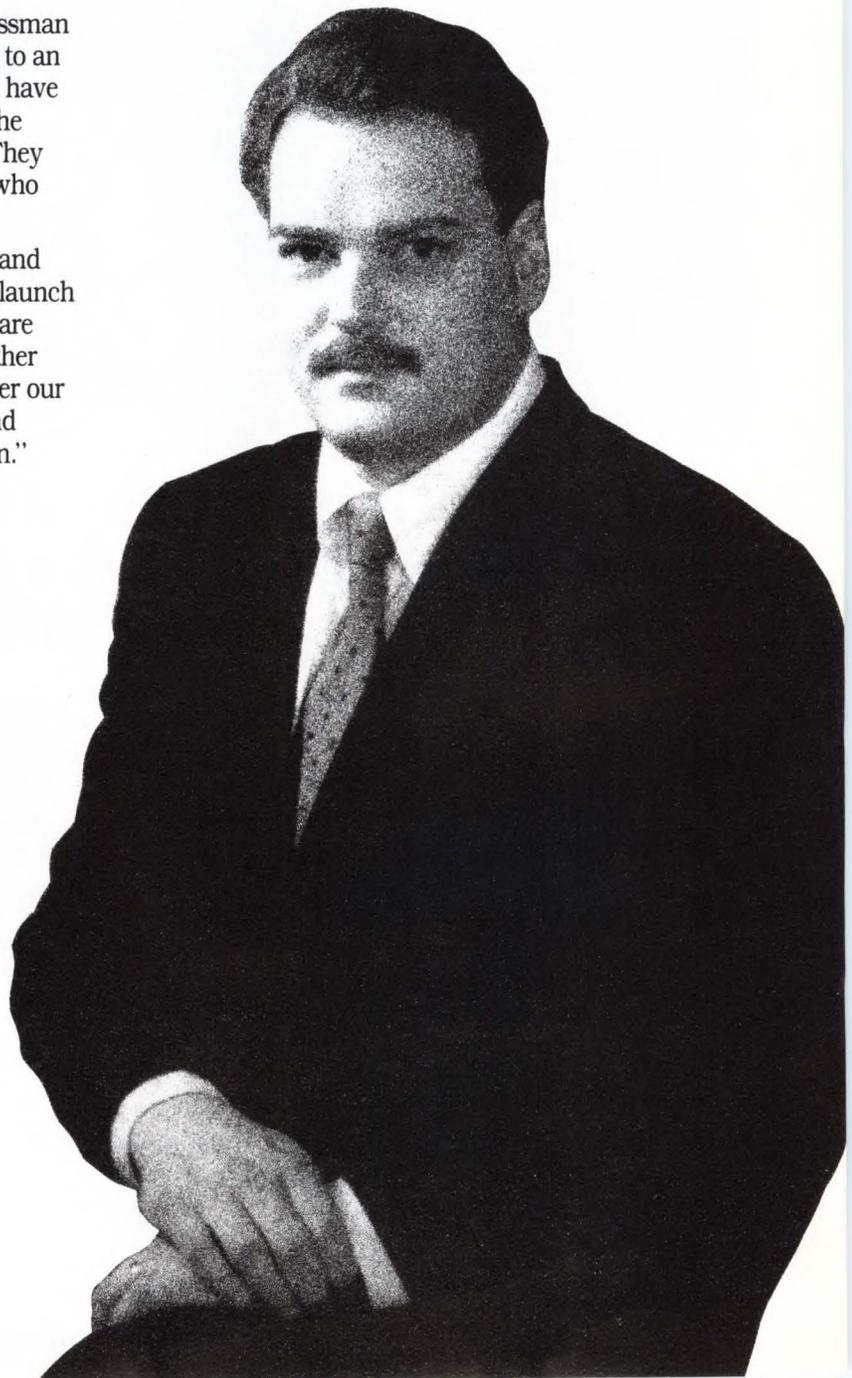
John Belden believes in the power of EDN magazine and EDN NEWS. So much so that he's relying on them to launch a series of new product lines. "EDN and EDN NEWS are sure to get them off the ground," says Belden. "No other pair of publications can provide the influence to deliver our message to as many markets, both geographically and demographically, in a cost-effective and timely fashion."



EDN magazine and EDN NEWS work for Glassman High Voltage. They can work for you.

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*EriPower™ is a trade mark for standard power products from Ericsson Components AB's power department, formerly known as RIFA Power Products.

LOOKING AHEAD

EDITED BY CYNTHIA B RETTIG

Manufacturers praise JIT logistics

In response to a survey recently conducted by Touche Ross (Chicago, IL), 90% of a group of manufacturers and distributors said just-in-time (JIT) logistics were strategically important to developing or maintaining a competitive advantage. Once companies have put JIT plans into effect, they can deliver products in a short period of time while investing minimally in inventory needs. Companies have found that producing just what is needed and delivering exactly the right quantity at precisely the right time not only lowers inventory requirements but also improves a manufacturer's or distributor's relationships with both vendors and customers. About 25% of the nearly 200 respon-

dents already had operational JIT programs; another 50% or more are in the planning or start-up stages.

Operational JIT programs reduce the number of primary vendors any individual company deals with by an average of 42%, Touche Ross found. And when companies purchase more goods from fewer vendors, they have a better opportunity to influence those vendors' quality-control programs and to reduce purchase lead times. As companies thus reduce the number of vendors and improve their relations with them, the companies become much more satisfied with the quality of the goods and services received. Sixty percent of those with operational JIT programs stated that they were very satisfied with vendor quality; only 18% of those in the planning

stages for JIT said they were as pleased.

Manufacturers with JIT programs also benefited from improved relationships with their customers. Those companies found they could reduce costs while providing better customer service—including more frequent, as well as more timely, deliveries.

Touche Ross found that implementing just-in-time programs is not without its obstacles, however. Some manufacturers, for example, faced internal organizational resistance, lack of systems support, and limitations in manufacturing facilities. Others encountered difficulties defining service levels, inadequate amounts of purchased goods, and generally poor implementation of JIT planning.

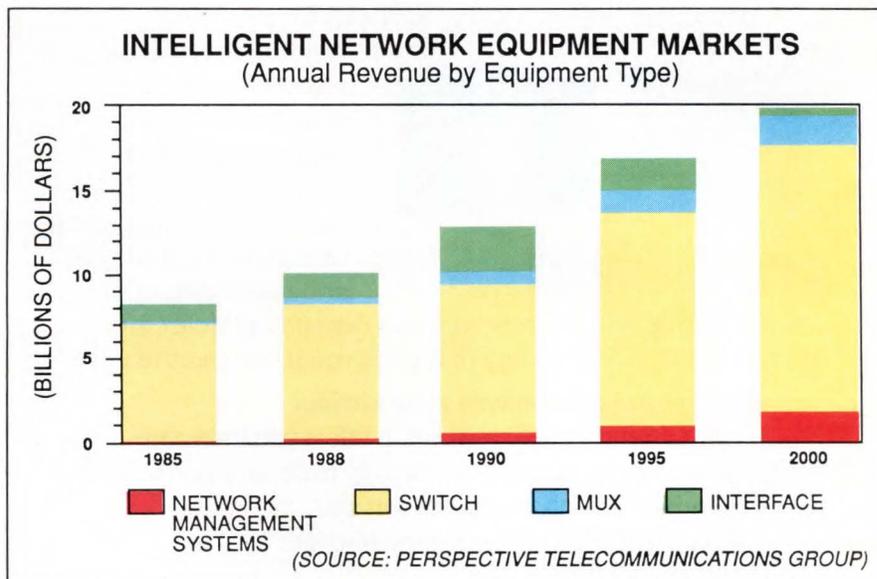
\$20B market predicted for smart network equipment

Annual sales of equipment for intelligent telecommunications networks should reach \$20 billion by the year 2000, according to the Perspective Telecommunications Group, a marketing research and management consulting firm specializing in telecommunications (Franklin Lakes, NJ). Prospective buyers will be looking for different qualities in different types of products. The extent to which intelligent switching gear improves system performance, for instance, will be critical to its success. On the other hand, customers will judge network management systems by ease of use. The market-research firm also points out that not all kinds of intelligent network equipment will flourish. Some products, like protocol converters, will actually decline in sales between the

years 1990 and 2000.

Perspective also identifies specific areas where opportunities in public as well as private network development exist, including switch manu-

facturing, data-communication equipment, LANs, computer manufacturing, and other vendors of equipment, information, and services.



Making the Connection Between...

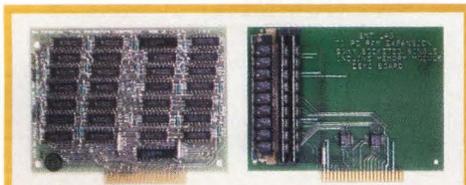
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Molex SIMM socket (right) takes up dramatically less board space than DIP packaging (left).

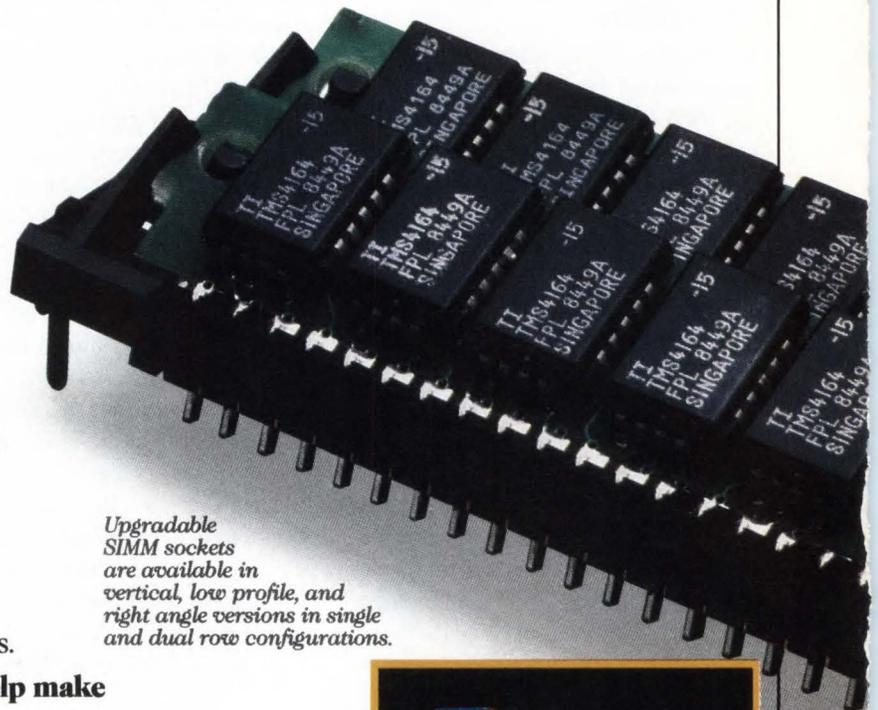
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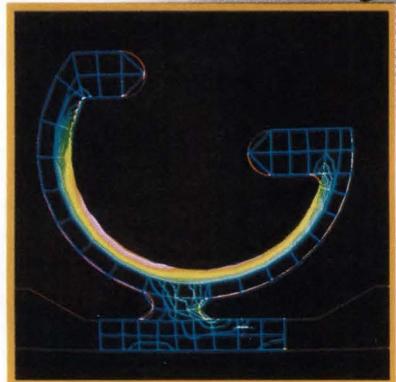
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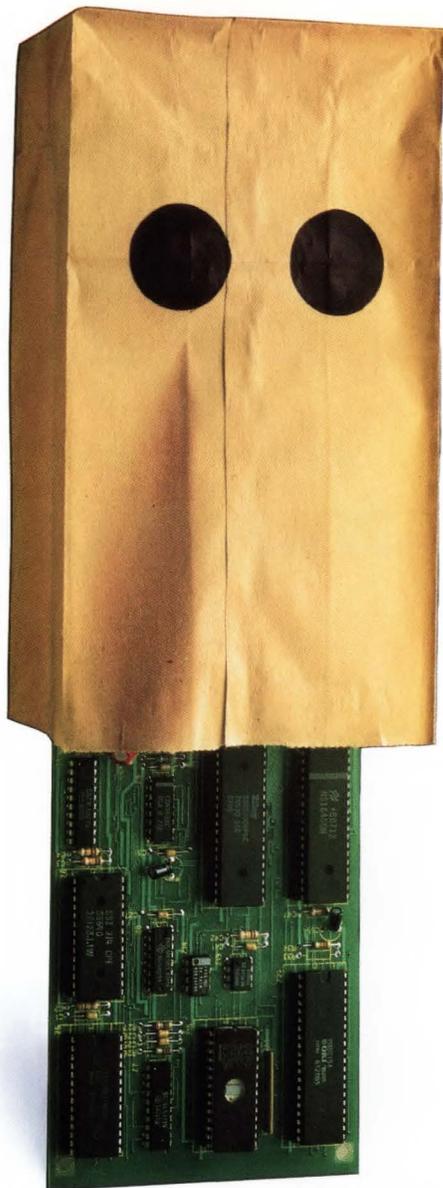
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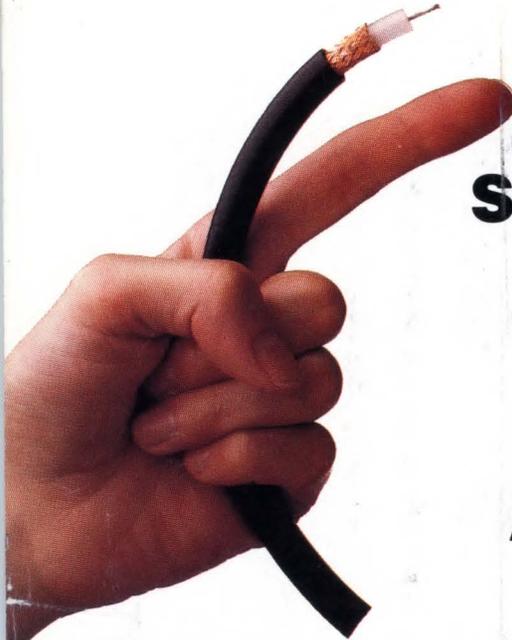


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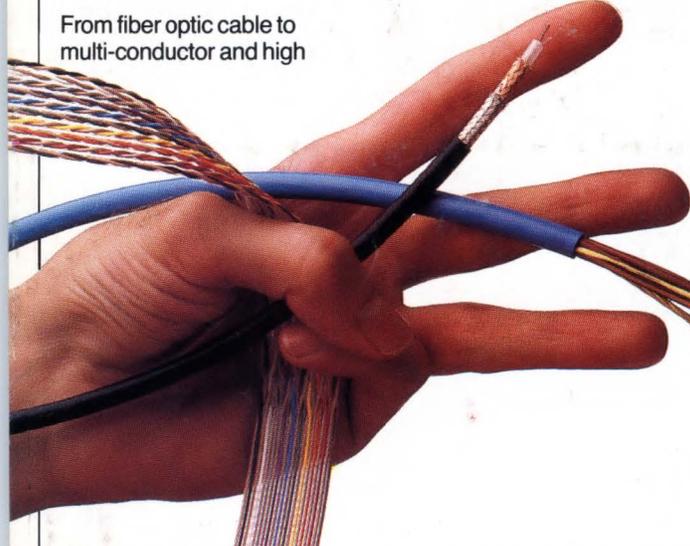
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