

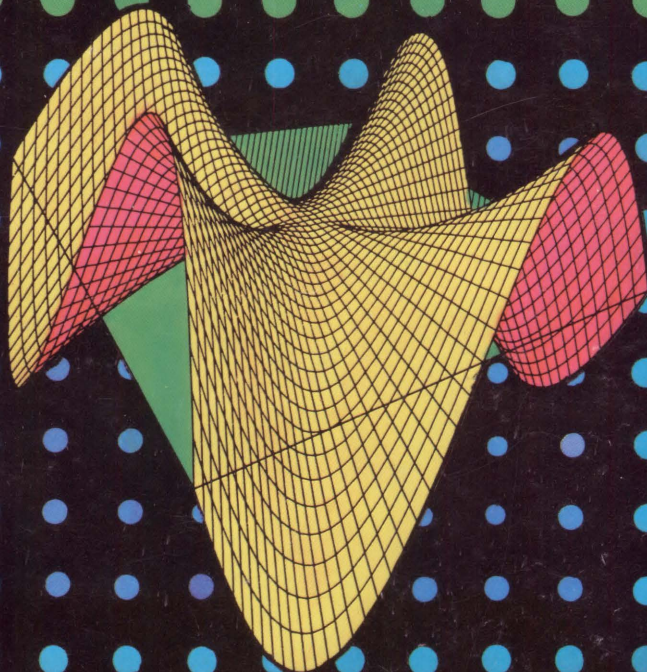
A PENNELL PUBLICATION

NOVEMBER 1980

COMPUTER DESIGN

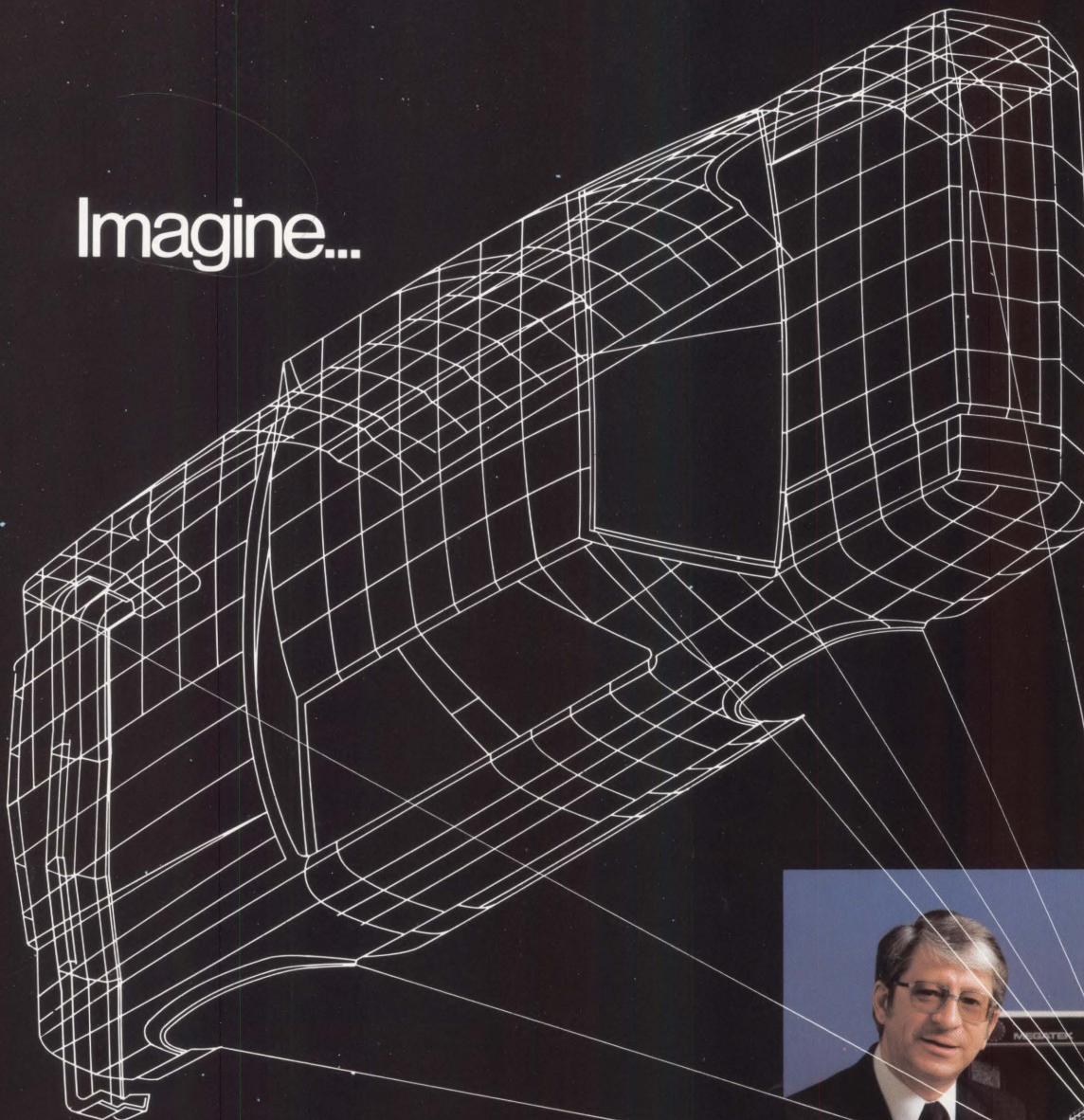
THE MAGAZINE OF
COMPUTER BASED **SYSTEMS**

ADVANCES IN INTERACTIVE GRAPHICS SYSTEMS ARCHITECTURE
LSI DEVICES SUPPORT BUBBLE MEMORY SYSTEM DESIGN
CD DATACOMM



See Special Section on Data Communications

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"Megatek's refresh display is an extremely powerful tool for visualizing, manipulating, experimenting and altering design parameters.

"Megatek systems interface easily to a broad range of computers and enhance the engineer's feeling of direct interaction with his design."

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"Customers for our software package can select any graphics terminal they want. A large percentage choose Megatek. Price/performance is the reason why. If I were going to put down dollars for a production refresh terminal, I'd put my money on Megatek."

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Model 6809 has been designed and built with all the innovative features and reliability that Kennedy products are

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DEPARTMENTS

11 CALENDAR

102 TECHNOLOGY REVIEW

Large scale data processing system, structured in a multilevel function concept, offers high system productivity because workload is shared among largely autonomous processors

130 DIGITAL CONTROL AND
AUTOMATION SYSTEMS

Minicomputer locates and tracks finished products from assembly line to shipping department

194 TECH BRIEFS

207 MICRO DATA STACK/COMPUTERS,
ELEMENTS, AND SYSTEMS

Using high level languages with microprocessors involves considerations different from those of larger computers, but many advantages overcome the few burdens

232 AROUND THE IC LOOP

Loss of data in the event of a power outage can be prevented by replacing CMOS devices with non-volatile logic devices produced using an MNOS process

250 PRODUCTS

294 LITERATURE

297 ADVERTISERS' INDEX

Reader Service Cards
pages 299-302

Number of copies printed this issue—89,500.

SPECIAL SECTION

DATA COMMUNICATIONS 23

FEATURES

ADVANCES IN INTERACTIVE GRAPHICS
SYSTEMS ARCHITECTURE 147

by Walter M. Anderson

Spurred by advances in electronics technology, interactive graphics system designs evolved through several generations before returning to an early, established architecture that has finally become cost effective for widespread use

LSI DEVICES SUPPORT BUBBLE MEMORY SYSTEM DESIGN 159

by Sam Joseph Nicolino, Jr

Family of LSI support devices aids in design of customized bubble memory systems by handling all of the interfacing details and timing sequences required when connecting up to 8M bits of bubble memory to a single controller

MAKING PL/M PROGRAMS MORE UNDERSTANDABLE 169

by Douglas L. Abbott

Self-documentation in PL/M programs can be extended through use of compiler directives to make program statements more similar to an English language description of their primary function. The same technique also allows simple extensions of the language

MASK AND MENU FILE SYSTEM
EASES OPERATOR HANDLING 178

by K. Buchmann

Microprocessor based file system offers fast, convenient access to stored data through masks and menus that assist operators without impacting throughput



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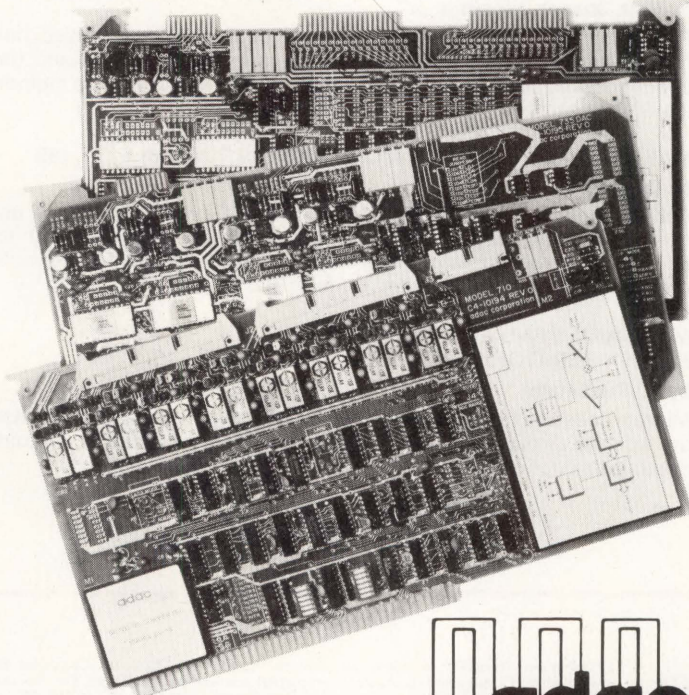
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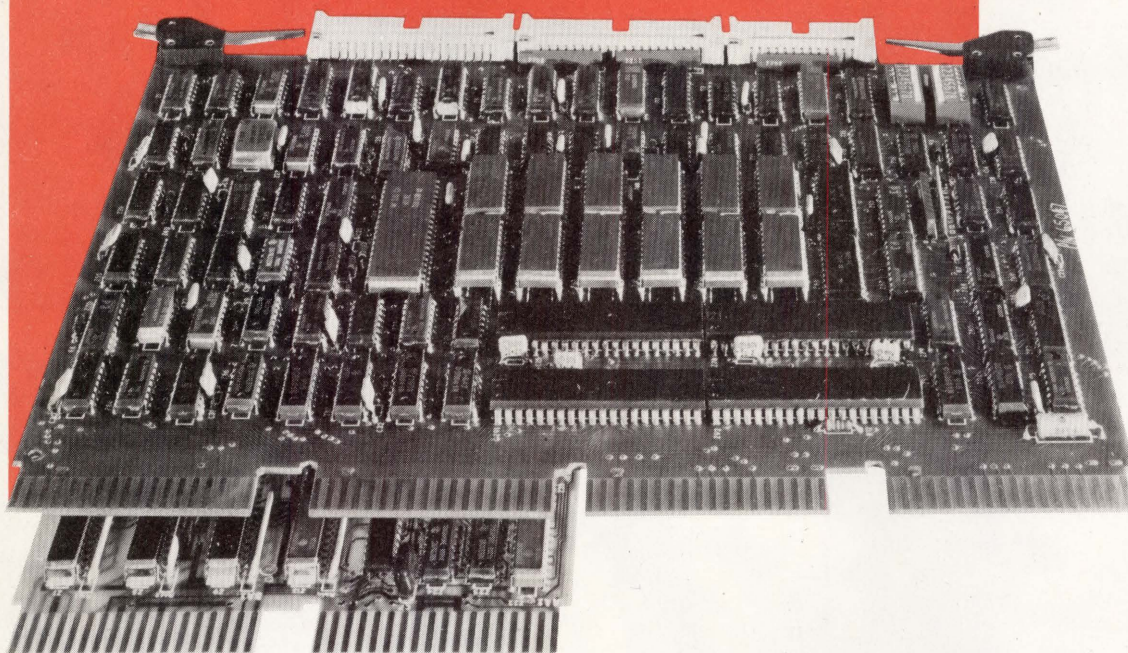
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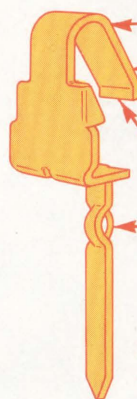
You know the secret of gas tight reliability in a low profile DIP socket. It is the "squeeze" or force the contact exerts on your IC lead. RN single leaf high compression contacts exert a "normal force"* that is 4 to 5 times greater than conventional dual leaf contacts. Result? RN low profile ICL series sockets are MIL-SPEC qualified (MIL-S-83734) to meet the toughest gas tight performance standards in the world. You can't buy a more gas tight low profile socket — anywhere! And, our prices compare very favorably with any comparable socket.

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Test	Procedure	Results
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Corrosive Atmosphere	MIL-S-83734 Paragraph 4.7.16 10-25 ppm $(\text{NH}_4)_2\text{S}$, 4 hours	$R_C = 8.5\text{m}\Omega$ average
Moisture Resistance	MIL-S-83734 Paragraph 4.7.14	$R_i \geq 10^{12}\Omega$
Thermal Shock	MIL-S-83734 Paragraph 4.7.13	No Damage
Mechanical Shock	MIL-S-83734 Paragraph 4.7.11	No Discontinuity
Vibration	MIL-S-83734 Paragraph 4.7.1	No Failures $R_C = 7.0\text{m}\Omega$ average (final)
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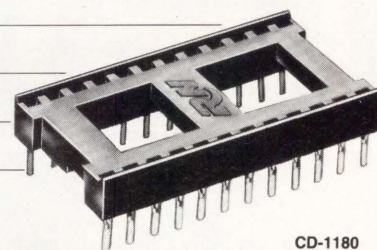
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Operating at 0 to 10 MHz, both units give you 32 channels of data domain information. But the K100-D's memory is 8 times as deep as the 1610B's—512 words versus 64. The 1610B's 7 levels of triggering exceed the needs of most users, and those who do need this capability can generally get it from their development system. With the K100-D, you don't sacrifice vital timing information for data domain capabilities you don't need.

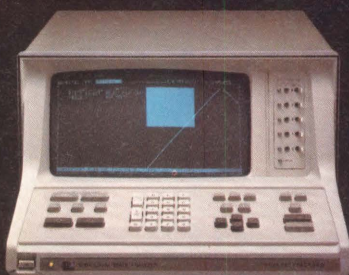
The final analysis.

To help you evaluate your needs before you buy, we've prepared a point-by-point competitive comparison of the Biomation K100-D and the H-P 1610B. (Incidentally, it also shows how the K100-D beats H-P's general purpose 1615A

hands down.) To get your free copy, just use the reader service number or write Gould Inc., Instrument Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.

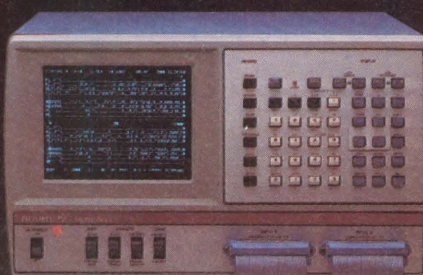


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A sophisticated data-domain-only
logic analyzer



Analysis: Software
Speed: to 10 MHz
Channels: 32 data
Memory: 64 words

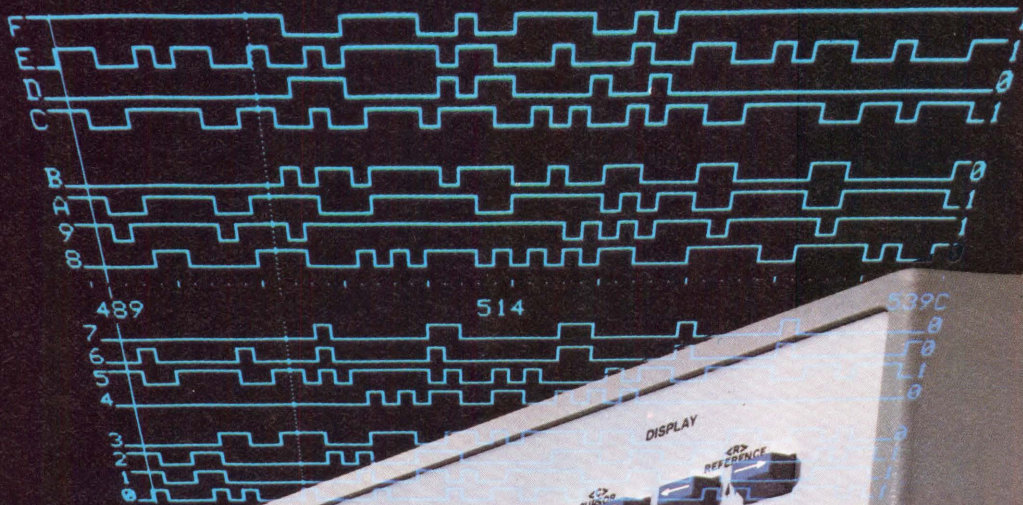
Biomation K100-D
The industry's finest data/timing
logic analyzer



Analysis: Software & Hardware
Speed: to 70 MHz data domain
to 100 MHz time domain
Channels: 32 data to 12 MHz,
16 data to 70 MHz
16 timing to 100 MHz
Memory: 1024 words @ 16 channels
512 words @ 32 channels

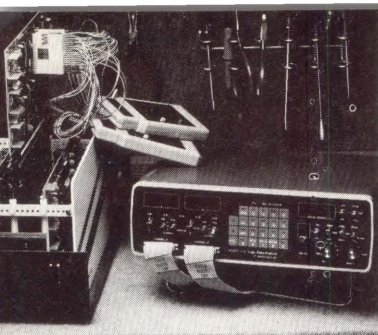
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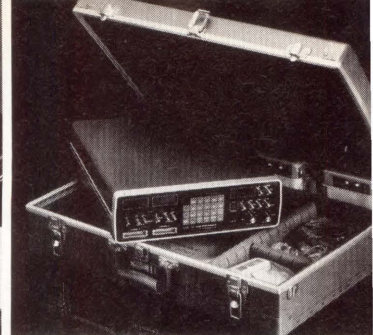
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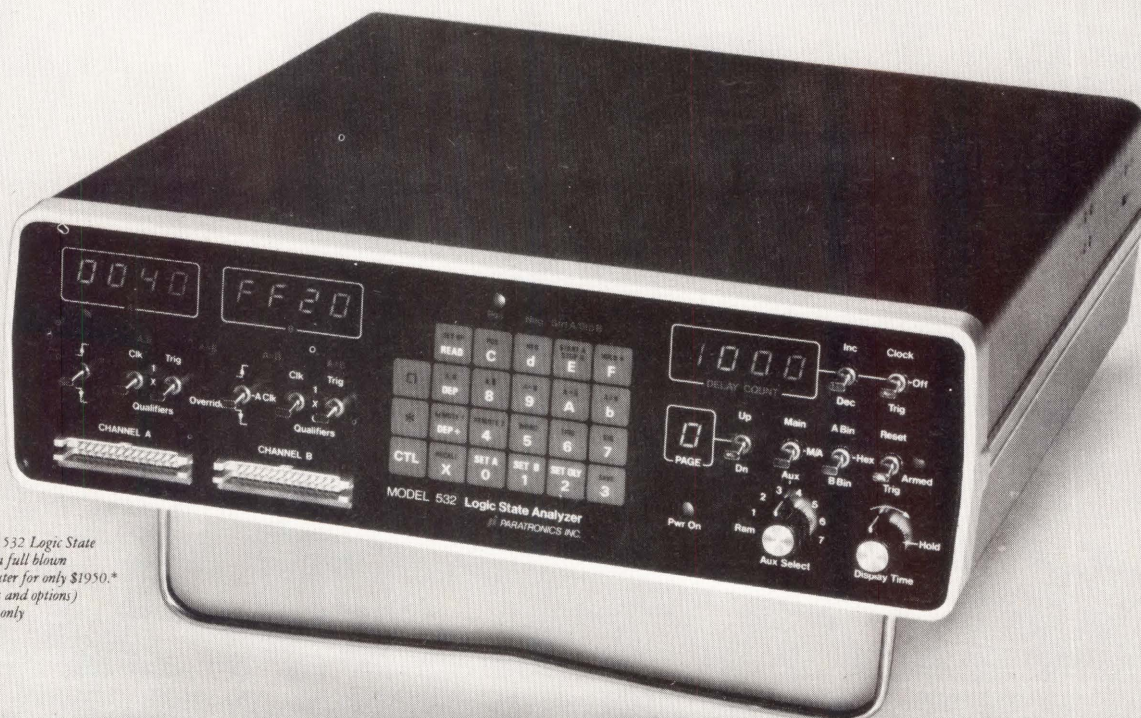
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CALENDAR

CONFERENCES

DEC 1-4—Internat'l Conf on Pattern Recognition, Konover Hotel, Miami Beach, Fla. INFORMATION: Harry Hayman, 5th Pattern Recognition, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

DEC 1-5—Symposium on Distributed Data Acquisition and Control, Miami Beach, Fla. INFORMATION: Dr Earl Swartzlander, Jr, TRW R3/2044, One Space Park, Redondo Beach, CA 90278

DEC 2-5—CMG XI (11th Internat'l Conf of the Computer Measurement Group), Sheraton-Boston Hotel, Boston, Mass. INFORMATION: Judith G. Abilock, Price Waterhouse and Co, Office of Government Services, 1801 K St, NW, Washington, DC 20006. Tel: 202/296-0800

DEC 4—California Computer Show, Hyatt-Palo Alto, Palo Alto, Calif. INFORMATION: Norm De Nardi, Norm De Nardi Enterprises, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

DEC 8-10—Internat'l Electron Devices Meeting, Washington Hilton, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Associates, 1629 K St, Washington, DC 20006. Tel: 202/296-8100

DEC 10-11—Computer Networking Symposium, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

JAN 13—Invitational Computer Conf, South Coast Plaza Hotel, Costa Mesa, Calif. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

JAN 13-15—Communication Networks Conf and Expo, Albert Thomas Convention Ctr, Houston, Tex. INFORMATION: Terri Hamilton, The Conference Co, 60 Austin St, Newton, MA 02160. Tel: 617/964-4550

JAN 19-22—ATE Seminar/Exhibit, Pasadena Center, Pasadena, Calif. INFORMATION: Jennifer Garlid, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

FEB 9-12—Internat'l Symposium on Information Theory, Santa Monica, Calif. INFORMATION: Profs Izhak Rubin or Kung Yao, System Science Dept, 4531 Boelter Hall, U of Southern California, Los Angeles, CA 90024. Tel: 231/825-2240

FEB 18-20—Internat'l Solid State Circuits Conf, Hyatt Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 21-26—Compcon Spring '81, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 16-18—Industrial and Control Applications of Microprocessors (IECI), Sheraton Hotel, Philadelphia, Pa. INFORMATION: H. Roy Nagle, Dept of Electrical Engineering, Auburn U, Auburn, AL 36830

MAR 23-25—Office Automation Conference, Albert Thomas Convention Ctr, Houston, Tex. INFORMATION: Carol Sturgeon, Office Automation Conference, PO Box 9659, Arlington, VA 22209. Tel: 703/558-3617

MAR 23-26—5th International Conference on Digital Communications, Congress Bldg, International Fair of Genoa, Genoa, Italy. INFORMATION: Manager, Rome Branch of Administrative Office 5th ICDSC, Telespazio SpA, Corso d'Italia 43, 00198 Rome, Italy

MAR 24-26—FOC '81 East Fiber Optics Conference and Exhibition, Hyatt Regency, Cambridge, Mass. INFORMATION: Ellen M. Bond, Information Gatekeepers, Inc, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022, or Hawley Russell, 5 rue Davioud, Paris 75016, France

SEMINARS

DEC 1980-FEB 1981—Data Communications for Minicomputer Users, various U.S. cities. INFORMATION: Margaret Harveston, MICOM Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311. Tel: 213/882-6890

DEC—Special Curricula on Data and Voice Technology, various dates and locations. INFORMATION: Systems Technology Forum, Inc, 8991 Cotswold Dr, Burke, VA 22015. Tel: 703/425-9441

DEC—Data Communications: Introduction to Concepts and Systems; Advanced Concepts and Systems; and Effective Network Design, various dates and sites. INFORMATION: Joe Menendez, Datapro Research Corp, Delran, NJ 08075. Tel: 609/764-0100

DEC 2-4—Networking: Design and Implementation of Computer Communications Networks, Ramada Inn, Lanham Md. INFORMATION: Registrar, Digital Equipment Corp Seminar Programs, 29 Hudson Rd, Sudbury, MA 01776. Tel: 617/493-2858

Microprocessor Application Design, Various locations and dates. INFORMATION: Ann Verdi, Advanced Micro Devices, Customer Education Center, 490-A Lakeside Dr, PO Box 453, Sunnyvale, CA 94086. Tel: 408/732-2400; outside Calif, 800/538-8450

SHORT COURSES

DEC 1980-JAN 1981—Microprocessors: A General Introduction; Data Communications Concepts; and MCZ-2 Systems, various dates and locations. INFORMATION: Steve Blank, Zilog, 10340 Bubb Rd, Cupertino, CA 95014. Tel: 408/446-4666

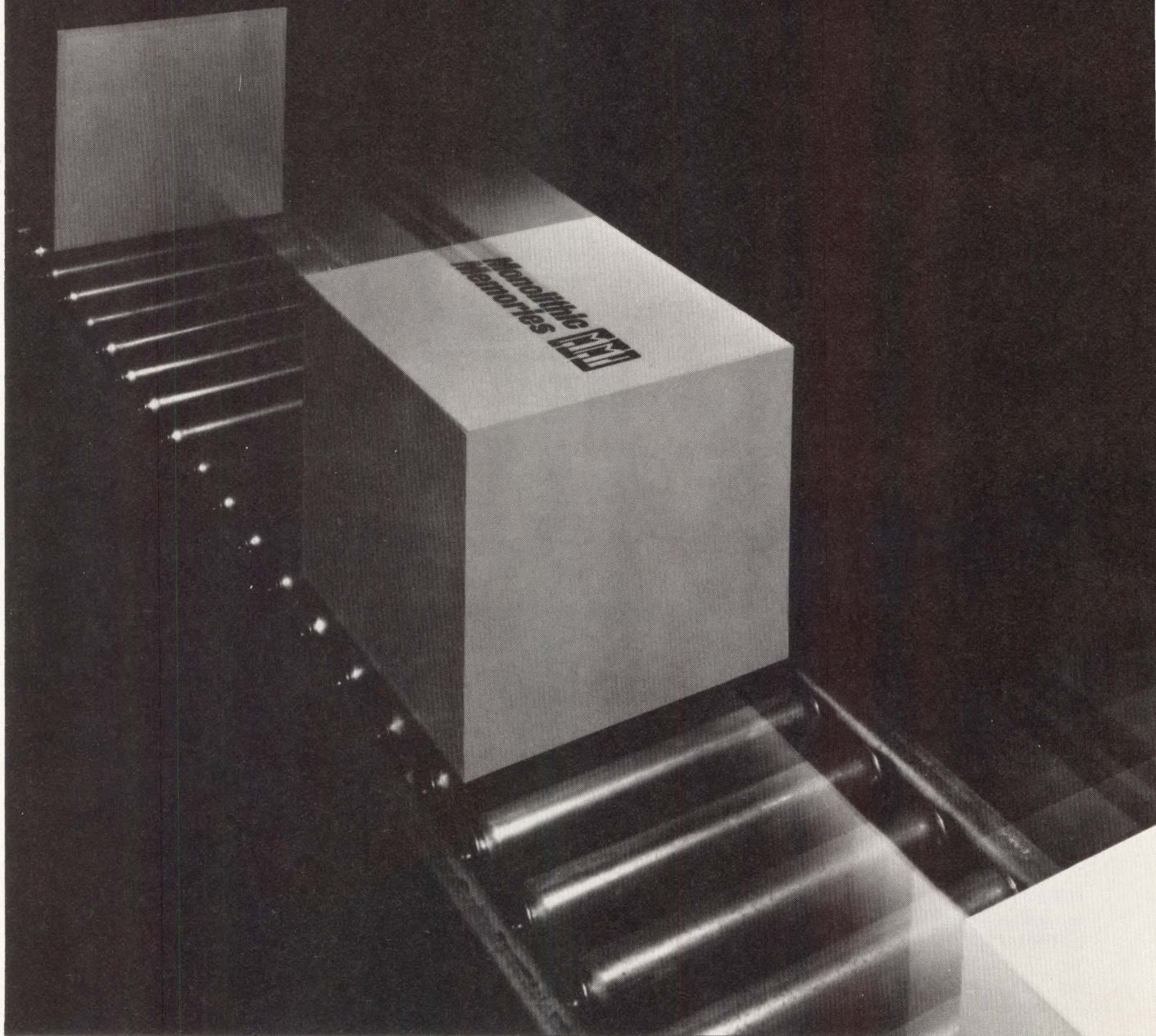
DEC 1-3—Software Design for Data Communications Systems; DEC 8-10—Packet Switching Networks for Data Communications; DEC 2-5—Computer Graphic Systems: Designs and Applications; DEC 15-19—Structured Analysis, Design, and Testing of Computer Systems; DEC 17-19—Design of Digital Control Systems, George Washington U, Washington, DC. INFORMATION: Director Continuing Education Program, George Washington U, Washington, DC 20052. Tel: 202/676-6106

DEC 9-12—Computerized Robots, Los Angeles, Calif. **JAN 13-16 and JAN 20-23—Programming in ADA, The Modular Language for Concurrent and Real-Time Applications**, Los Angeles, Calif, and Washington, DC. INFORMATION: Ruth Dordick, Integrated Computer Systems, Inc, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: 213/450-2060

JAN 12-15, 1981—Principles and Applications of VLSI Technology, Sheraton Palace Hotel, San Francisco, Calif. INFORMATION: Leonard Klein, Palisades Institute, 201 Varick St, New York, NY 10014. Tel: 212/620-3377

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Monolithic Memories

Your design want to use How do you

Ask the leader in gate arrays, International Microcircuits Incorporated.

Gate arrays are now being used for a wide variety of LSI applications. If your designers want to take advantage of gate arrays, here are the questions and answers that will help you decide.



Frank Deverse, President

Just what is a gate array?

A gate array is the fastest way to get to a unique digital LSI device at low cost. We take a pre-designed, preprocessed matrix of transistors and interconnect them uniquely for each customer. The result is a **proprietary silicon solution** to your logic needs.

Why should I consider gate arrays?

Quick access to LSI, low development costs, and the opportunity to leapfrog

the competition and get your product to market faster. Like IBM did with the 4300.

Are gate arrays just another niche product?

We believe gate arrays are a mainstream technology because they solve the new set of problems resulting from the push toward VLSI. High density silicon helps solve the problems of reliability, parts count, power dissipation and testing. Gate arrays solve the key problems of this density: design time and talent. They give you economical access to the benefits of LSI. The issues are universal. The gate array solution is very attractive.



Joe Kroeger, Director of Marketing

There must be some tradeoffs involved.

Sure. With gate arrays you will considerably shorten your development time and cost—translate a superior design into an IC quickly—but you may not use your chip space as

efficiently as with fully custom logic. (But ask us again next year; even that difference is going away.) Corporately, this means that if you need to get your product to market quickly in moderate volume, you need gate arrays. If you have several million units that you have to shave every cent of cost from, you need custom logic.

What do the costs look like?

Since many customers make use of common background chips, the bulk of the tooling and design costs have already been amortized. To get to your proprietary circuit takes—ballpark—\$10K, 7 weeks, and we do the layout. I'll give you a firm quote when we see your logic problem.

Who's using gate arrays now?

You already know about IBM. The customers who've been coming to us since 1974 are all over the industry, but they're each at the leading edge of their business. They're using gate arrays for their leapfrog generation of products.

And we now see new gate array suppliers entering the market in droves.

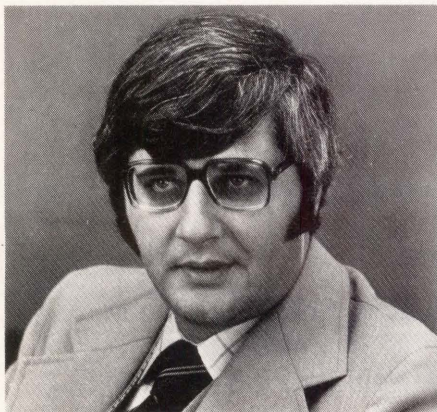
Sounds like a booming business. Why?

Three converging forces are making gate arrays more widely applicable. As standard logic becomes more dense and therefore more specialized, volumes are declining and part numbers are proliferating. Today's complexity of circuits is lengthening standard product development times. And gate arrays

engineers gate arrays. decide?

themselves are far faster and more versatile than they were a few years ago. We're delivering 2,000 gate-cells per chip now, looking at about 4,000 soon and forecasting nearly 10,000 in '82. Three years ago we were offering less than 500 gate-cells per chip.

It's not a sudden boom. It has been building for several years and we have done more than 400 circuits during that time.



Orhan Tozun, Director of Engineering

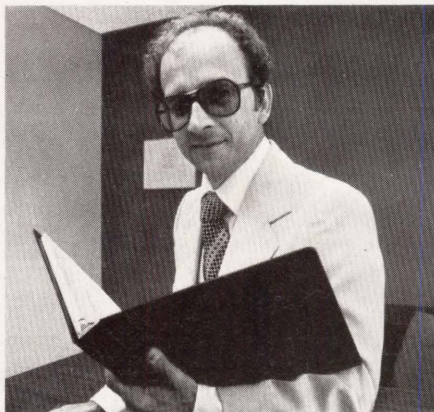
How do we interface with you? How do we get started?

Our engineering department talks with your designer and evaluates your logic to make sure it's do-able on one of our many gate arrays. The next step is a firm quote to let you evaluate the economics of our solution. That includes both development and production costs. We can do it because our CAD

system gives us consistency and our years of experience provide projectable yield information that lets us cost your job accurately in advance.

Then we send you our logic, right?

Right. We take it through a logic restructuring and minimization, block out the functions from our CAD library and lay out the interconnections between logic blocks. Then we check it. And re-check it. Only then do we commit to fabrication.



Rick Picard, Director of Operations

How do we minimize risk with gate arrays?

Let's look at each of the risk elements that apply to any development work, and see how vulnerable you are by using gate arrays.

1. Reliability. Gate arrays are no more subject to reliability failures than any IC; actually, the regularity and repetition inherent in gate arrays improves their

reliability. We use all the time-tested QC technology. Standard processing is used throughout.

2. Functionality. We use CAD to convert your logic into silicon. And we have only one layer to get right. Everything else is proven. We spot any problems fast. **It will work.**

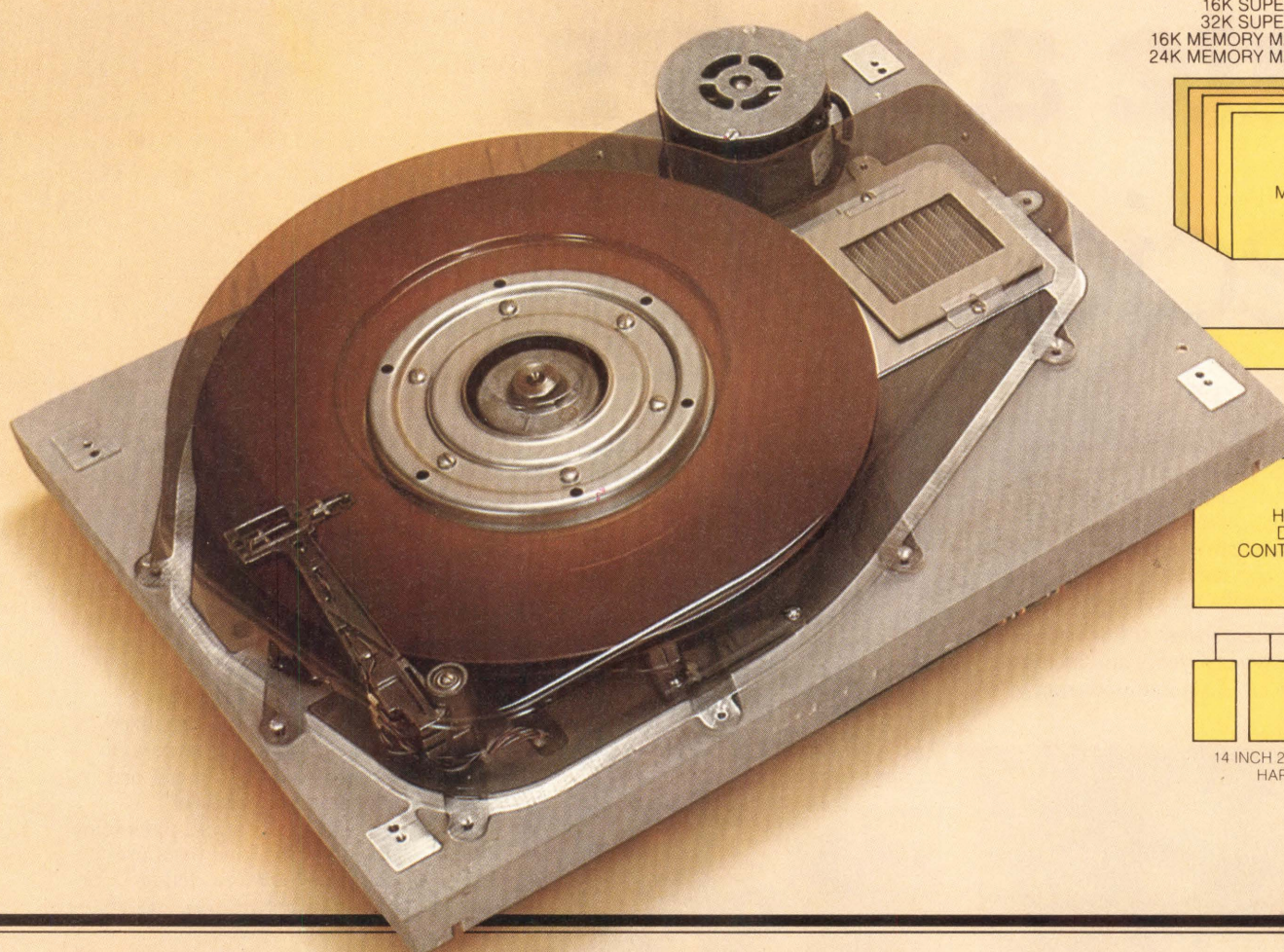
3. Reliability of supply. Gate array technology lets us inventory pre-processed, ready-to-be-personalized wafers. We keep plenty of wafers on hand to support our customers' orders both for development and for production. Personalization, packaging and test are all performed in-house. We can promise 4-6 week delivery for production quantities. And costs of \$.02 a gate or even lower.

Interested? TWX us! We'll TWX you complete information right away. Or write us at 3350 Scott Blvd., Building #37, Santa Clara, CA 95051. Tel. (408) 727-2280.

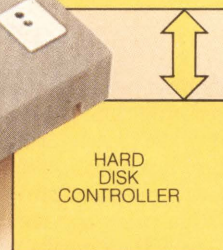
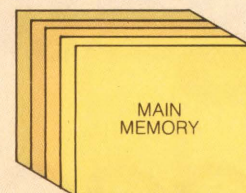
TWX: 910-338-2032

**INTERNATIONAL
MICROCIRCUITS
INCORPORATED**
Gate Array Leadership

While they were thinking hardware and software, we were thinking



16K SUPER RAM
32K SUPER RAM
16K MEMORY MASTER
24K MEMORY MASTER



14 INCH 26 MEGABYTE
HARD DISK

S-100 SYSTEMS. From add-in memory boards to add-on hard disk. High performance S-100 busboards. Single, dual and quad-density disk systems with up to 1.2 megabytes on a single floppy disk drive. I/O boards. All, with the Morrow Designs systems approach to hardware and software.

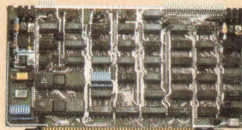
COST EFFECTIVE SYSTEMS.

Morrow Designs Discus M26 offers 26 usable megabytes of memory for just \$4,995. About \$192 per megabyte. And, it's a complete system, including a Shugart SA4008 Winchester-type sealed-media hard disk, power supply, cables, and cabinet with fan. The single board controller supervises all data transfers, communicating

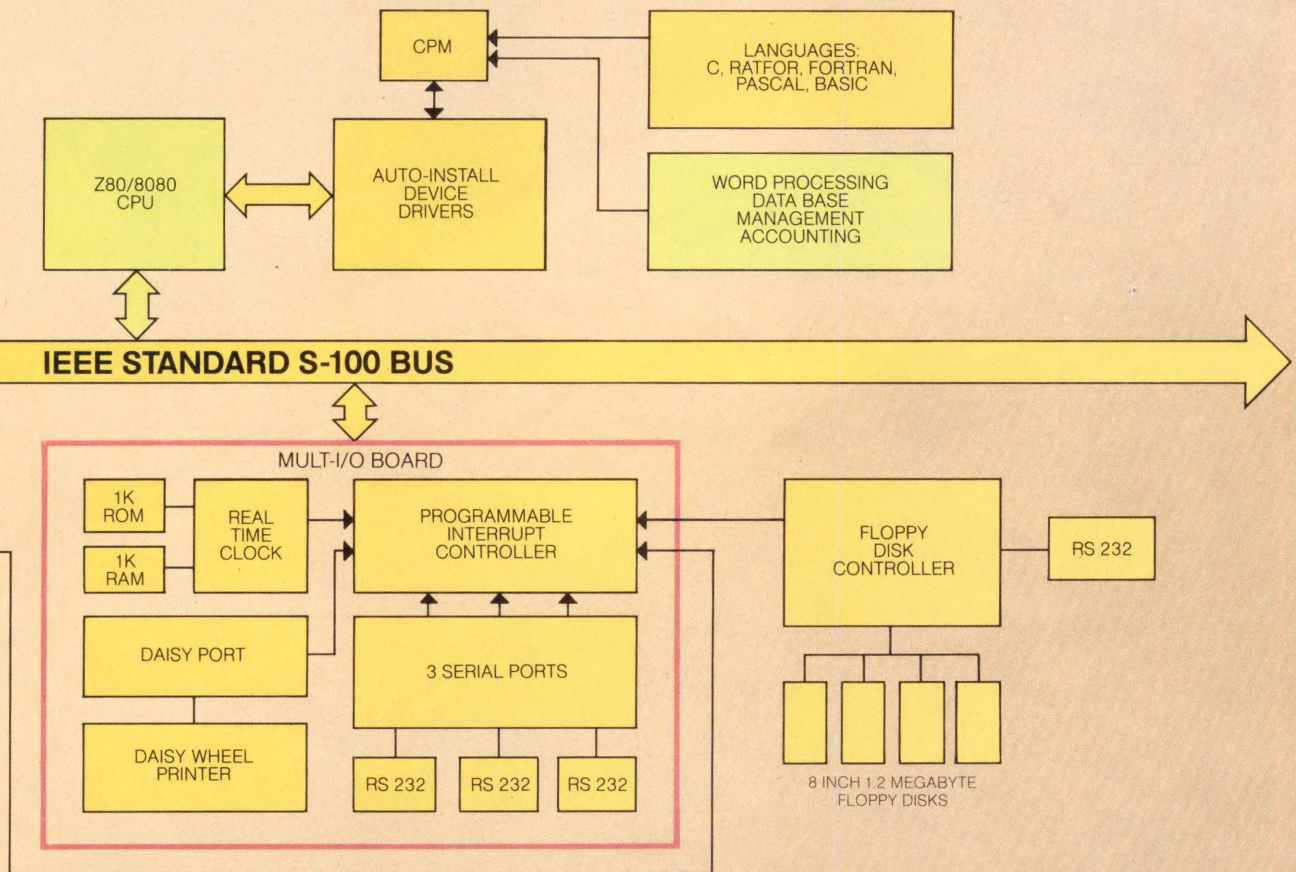
with the CPU through 3 I/O ports (command, status, data). The controller can generate interrupts at the completion of each command. A 512-byte sector buffer is on-board. And the system is available for S-100 mainframes.

SYSTEMS FOR SYSTEMS. Whether you're building systems or trying to expand your present system at reasonable costs, Morrow Designs offers complete, cost-effective subsystems. Modular systems that allow you to build your system your way.

SOFTWARE FOR SYSTEMS. Morrow Designs backs each subsystem with high-quality, fully-tested software. INSTALL software allows you to attach



systems.

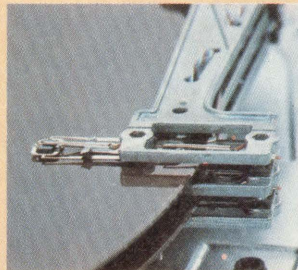


any Morrow disk system to any system operating under 2.+ CP/M. Morrow CPM/CDOS software allows you to attach any Morrow disk drive to Cromemco Systems. In fact, if software runs under CP/M, it will run on any Morrow Designs hardware.

COMPARE PERFORMANCE.

Hardware performance. Software performance. System performance. Any Morrow Designs disk drives, hard or floppy, can be mixed and matched through Morrow Designs standard software. And all necessary hardware, software and firmware is included with each system.

NOW, COMPARE PRICE. Morrow Designs products offer maximum efficiency at minimum cost. But we don't cut corners. What that means



to you is reliable system efficiency at cost effective prices.

Better systems for less. See Morrow Designs full line of memory and I/O, plus floppy disk and the M26 hard disk system at your computer supplier. Or, send in the coupon for our full line catalog. Can't wait: Call us at (415) 524-2101.

MORROW DESIGNS

5221 Central Ave. Richmond, CA 94804

Gentlemen, Please send me your complete OEM hardware and software specifications. Plus the name of my nearest distributor.

Name

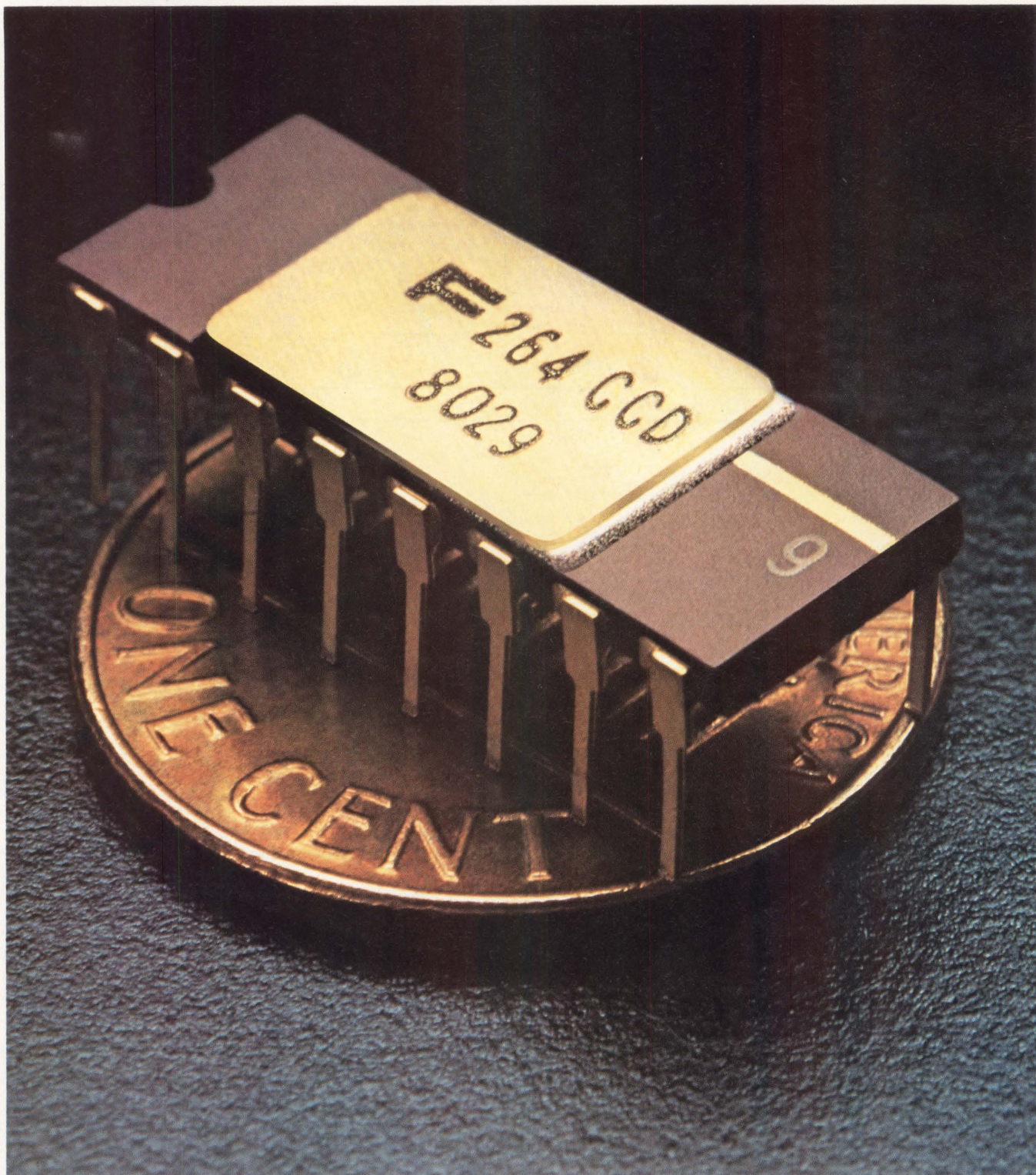
Company

Address

City State Zip

FAIRCHILD

A Schlumberger Company



The best way in memory to

Our 64K solid-state CCD memory is easier to interface with your large memory applications.

If you've been using 16K DRAMs for swapping stores, disc enhancement or digital delay, get ready for a much more cost-effective solution. The new 64K F264 CCD from Fairchild.

Using conventional n-channel Isoplanar™ silicon gate MOS technology, we've produced a CCD solid-state serial memory that can really save you time and money.

Specs that defy comparison.

The F264 is organized 16 x 4K x 1 and offers data rates

ranging from 1-5 MHz. It has TTL-compatible inputs and outputs. And, power dissipation is extremely low, too. Typically 220 mW at 5 MHz and 65 mW during standby at 1 MHz.

It's packaged in a standard 16-pin DIP and requires only two high-frequency clock inputs for easier interfacing with other solid-state circuits.

Do a lot more for a lot less.

The new F264 memory is about half the cost per bit of DRAMs. It's also cost-competitive in fixed-head disc and drum replacement applications. More importantly, there are no trade-offs between price and performance. Fairchild gives you the best of both, and more.

In addition, our

CCD memory is extremely easy and low cost to test. Compared to DRAMs, it requires 1/4 the test time per bit and can be tested on your standard memory test systems.

We also make a 32K CCD serial memory, the F232, with cost-efficient characteristics similar to those of the F264. It has a data rate range of 1-4 MHz, and is also packaged in a 16-pin DIP.

Our experience as a pioneer in CCD imaging has helped us produce the most cost-efficient devices in memory. For delivery information on our F264 or F232 CCD memories, call or write MOS Products at Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, CA 94042.
Tel: (408) 224-7334.
TWX: 910-338-2028.

Fairchild Camera and Instrument Corp.

save more cents per bit.

CIRCLE 12 ON INQUIRY CARD

ITTM is the difference between too smart and too dumb.

SALES ORDER ENTRY		P.O. # <u>0 475662-0</u>		S.O. # <u>01709-56</u>	
CUSTOMER: LEAR SIEGLER DATA PRODUCTS DIV. 714 N. BROOKHURST STREET ANN ARBOR, MI. 48103 PHONE: (714) 774-1810 TELEX: 65-5444 TNR: 910-591-1157				DATE: <u>08/25/80</u>	
				SHIP VIA: <u>AIR EXPRESS</u>	
				DELIVER TO: <u>ENGINEERING DEPT.</u>	
ITEM #	DESCRIPTION	QUAN.	PRICE		
1					
2					
3					
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REMARKS:		TOTAL			

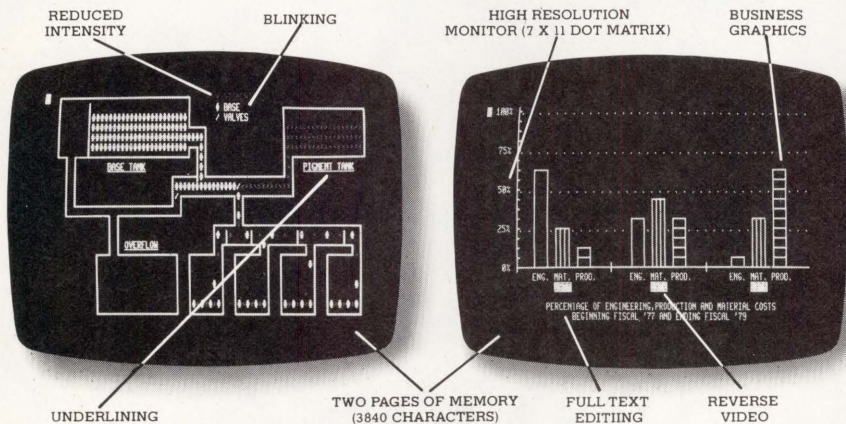
IT
Intermediate Terminal

Just when you thought you were totally confused by the incredible variety of "smart" computer terminals on the market, Lear Siegler brings you exactly what you need. It is IT, the Intermediate Terminal™ video display.

IT banishes all the confusing claims being made in the computer marketplace by compressing the broad spectrum of "smart" termi-

could go on all afternoon. Outstanding among them are the two pages of display that are standard with IT. Use them both and get up to 3840 characters of display potential. Or, allocate the second as a print buffer and be sending data on page two while entering data on page one.

Each page has the following independent page characteristics:



nals into ITself. Now, when you're looking for a terminal that isn't too smart but isn't too dumb either, IT is perfect for the job. And instead of having to weave your way through the confusing forest of "smart" terminals, just look for IT. Because IT is enough.

IT brings you the same high standards and solid workmanship that made its cousin, the Dumb Terminal® video display, a legend in its own time. IT may be of average intelligence, but there's nothing average about IT's consistent, quality performance and sensible features.

IT is completely self-contained, with full editing, formatting and protected field capabilities. Not to mention a microprocessor which increases reliability and ease of use.

TWO PAGES ARE BETTER THAN ONE.

The list of IT's special features

protect, program mode and cursor retention. And when you change from one page to another, these characteristics are stored in memory to be recalled at another time, letter perfect.

IT™ HAS QUITE A DISPLAY.

With IT, specific areas are designated as protected fields. They can't be typed over unless you remove the terminal from the protected mode. Even your remote computer can't overwrite the protected fields until IT is removed from the protected mode. Background (protected data) can be displayed at a lower intensity, while foreground is displayed at normal intensity and may be modified. You can even tab the cursor forward and backward to the start of each unprotected field.

And when you depress IT's special function key, a special function sequence is transmitted. The

remote computer is then in full control. And all control functions that can be initiated from the keyboard can also be executed from the remote computer.

Also on IT, full or half duplex operation is switch and keyboard selectable. You can also choose from conversation or block transmission, which can be initiated by you or the computer. In block mode, a line, a message or a page can be transmitted in its entirety.

IT™ IS NOT JUST ANOTHER PRETTY FACE.

IT's editing capabilities allow you to clear the screen, or use the cursor for a character change. In addition, IT comes complete with character insert and delete, line insert and delete, erase to end of line/field/screen, and tab and back tab. IT's full controls also allow you to skip protected fields, backspace, forespace, move up, down, return, home, and new line.

And when it comes to behavior modification, IT has few peers. Because IT comes with a factory installed personality for selected parameters. Such as an alternate ESCape sequence lead-in, in addition to the standard ESCape. A different End Block character. A different New Line character sequence. A different field separator. And a function sequence preamble.

FIND OUT THE WHOLE STORY ABOUT IT™.

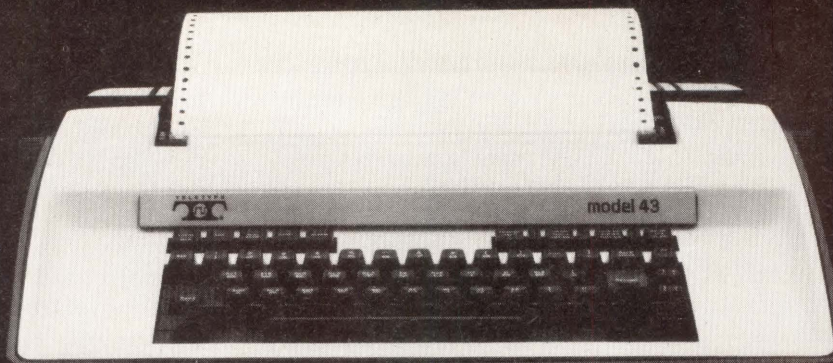
The people at Lear Siegler would be more than happy to fill you in on all the details about IT. Just drop us a line or call. Because IT is worth it.



LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

IT™, the Intermediate Terminal from Lear Siegler.

Lear Siegler, Inc./Data Products Division, 714 North Brookhurst Street, Anaheim, CA 92803 800/854-3805. In California 714/774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices: • San Francisco 408/263-0506 • Los Angeles 213/454-9941 • Chicago 312/279-5250 • Houston 713/780-2585 • Philadelphia 215/245-1520 • New York 212/594-6762 • Boston 617/423-1510 • Washington, D.C. 301/459-1826 • England (04867) 80666.



IT'S HARD TO KEEP A GOOD MACHINE DOWN.

At least that's what our customers tell us.

They report that the Teletype* model 43 printer is the most reliable machine they've ever bought. And that downtime is practically nil.

For example, Mr. Albert Brooks of NCE Terminals writes us to say that, "our records show the Teletype model 43 has the highest reliability and mean time between failure rates of any terminal we presently distribute and service."

Thanks, Mr. Brooks.

And Mr. Robert Jones of Leasametric, a company that currently rents out over 1000 of the model 43 teleprinters, reports that

"according to our records, the failure rate ranges between 1½% and 2%."

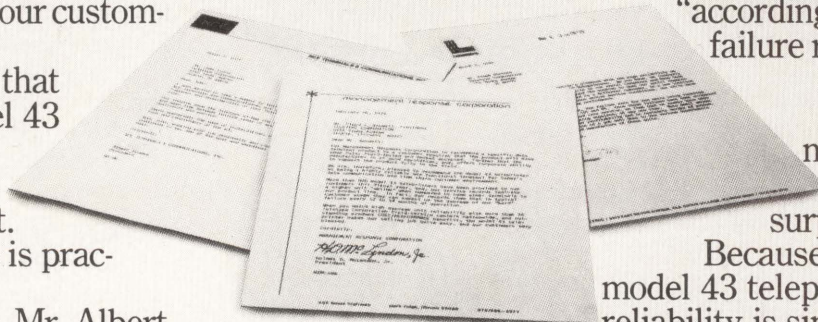
And while that may surprise some people, it's no surprise to us.

Because the reason for the model 43 teleprinter's amazing reliability is simple: simplicity.

Now LSI (Large Scale Integration) circuitry performs almost all of the functions that used to be done mechanically. So less moving parts means less chance of downtime.

And less downtime means less aggravation. And isn't that the kind of printer you want working for you?

The Teletype model 43 printer. It's the kind of machine that gets fan mail.



Teletype Corporation
5555 Touhy Avenue, Dept. 3185
Skokie, IL 60077
Telephone (312) 982-2000

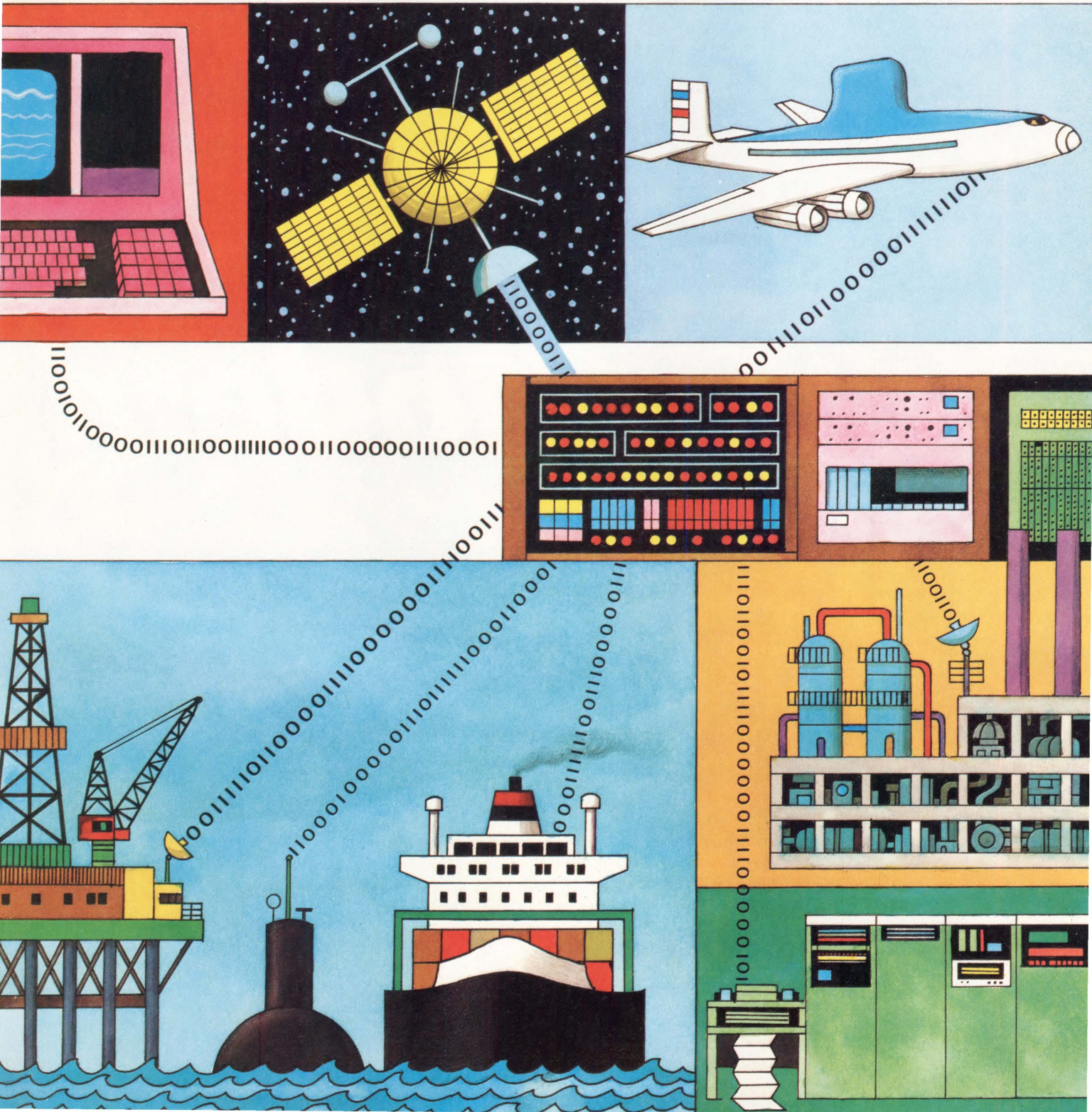
*Teletype is a trademark and service mark of the Teletype Corporation.

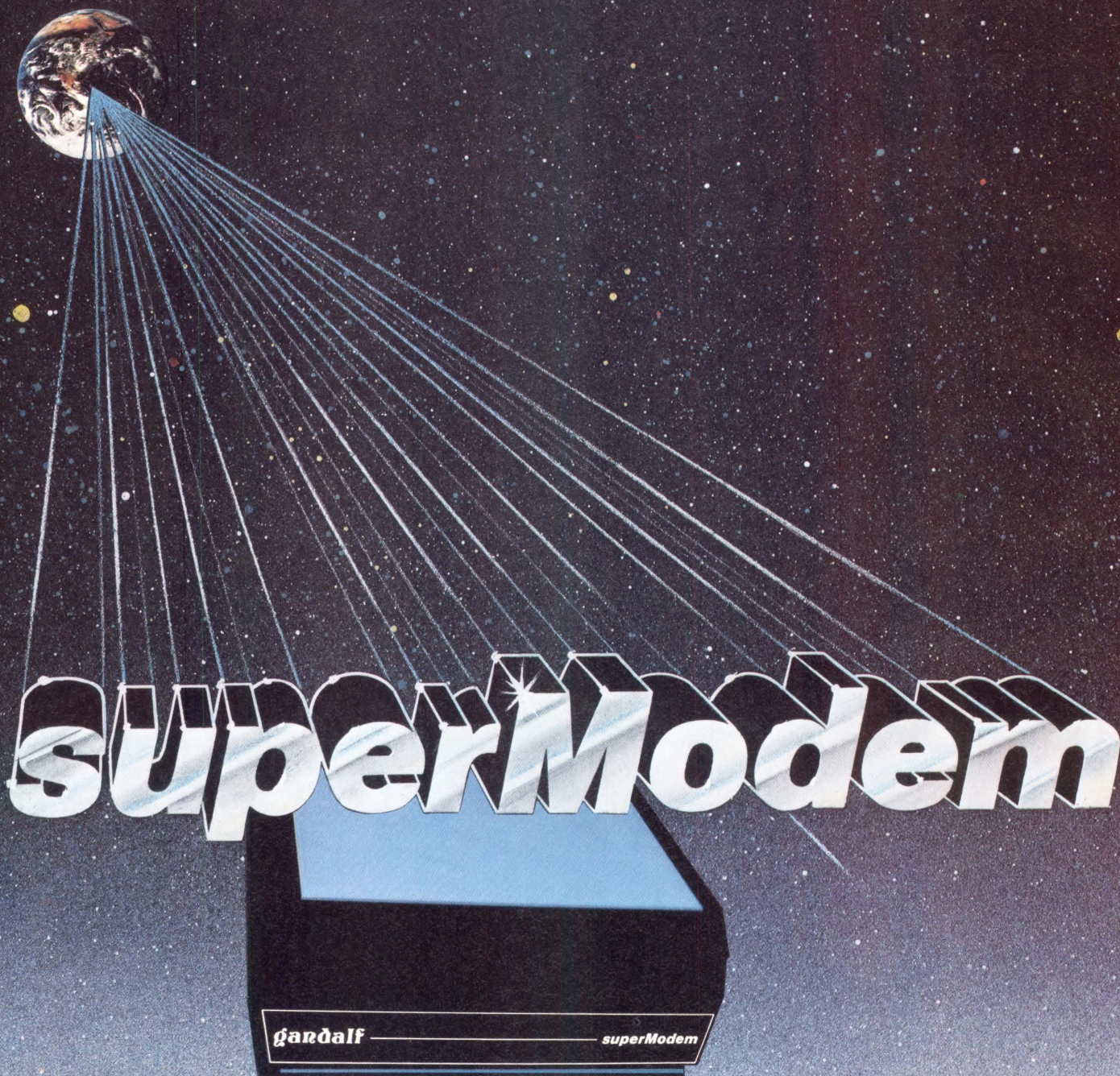
CIRCLE 14 ON INQUIRY CARD

COMPUTER DESIGN

NOVEMBER 1980

SPECIAL SECTION: DATA COMMUNICATIONS



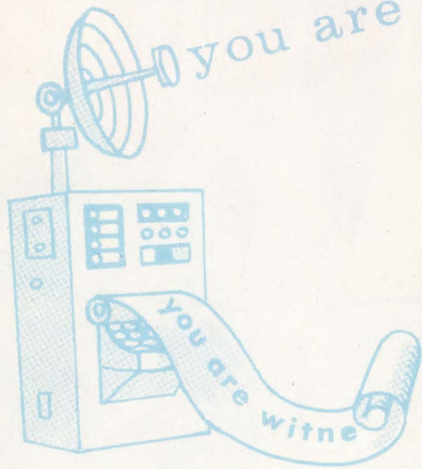


FEATURES

- 9600 bps long distance transmission over unconditioned 3002 lines.
- A patented modulation technology that eliminates the need for conventional equalization.
- Data recovery using discrete Fourier Transform signal analysis by a proprietary ultra-fast digital processor.
- Inherent immunity to 9 out of 10 random noise hits that affect conventional modems.
- Quadraplex channel option.
- 9600 bps dial back-up.

gandalf

Gandalf Data, Inc., 1019 S. Noel, Wheeling, Illinois 60090 (312) 541-6060
Gandalf Data Communications LTD., Gandalf Plaza, 9 Slack Road, Ottawa,
Ontario, Canada K2G 0B7 (613) 225-0565
Gandalf Digital Communications LTD., 4 Cranford Court, Hardwick Grange,
Warrington, Cheshire, England



You are witnessing the first public demonstration of the transmission of data from a computer into outer space for relay via a communications satellite

COMPUTER "TALKS" TO TELSTAR

A Prelude to World Data Network

"You are witnessing the first public demonstration of the transmission of data from a computer into outer space for relay via a communications satellite"—these are the first words printed out by the Honeywell 800

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to Telstar

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signs of continued healthy growth.

These developments, he said, "will

create a tremendous demand for fast

data communications that can only be

met by sophisticated data processing

and communications networks."

"The capability of computers to process huge quantities of business data is well known. The ability of existing communications networks to handle transmission of data from computer-to-computer is also an accom-

one to control data transmission, the other to control data reception. The transmitting program guided data from the computer through the communications network and back. The receiving program accepted the data,

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EDITORIAL

"Prelude to World Data Network."

It sounds like 1980, but it goes back 18 years. AFIPS was sponsoring its third Joint Computer Conference in Philadelphia (December 4 to 6, 1962) when *Computer Design* published the first number of its first volume.

Within that premier issue, "Computer Talks to Telstar—A Prelude to World Data Network" (p 7) recounted news of the Honeywell 800's transmission of data signals through telephone circuits to Andover, Maine. From there data went by microwave to Telstar, and then traveled back over the same route to the 800 in Newton, Massachusetts.

On page 13, the Wednesday afternoon session of the Philadelphia Joint Computer Conference was recommended to our readers (Does anyone remember?) because it was all on data communications systems. A feature article (p 38) about General Electric's data transmission control system designed with a Datanet-15 and the GE-225 computer heralded "high speed transmission to and from computers..." as a powerful management tool.

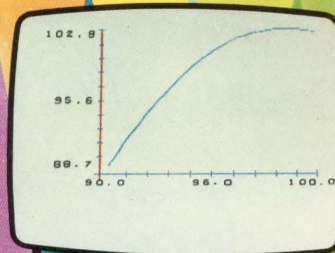
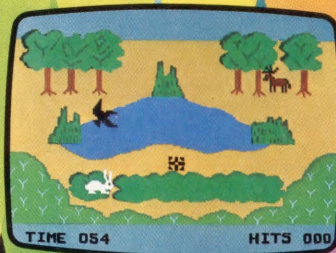
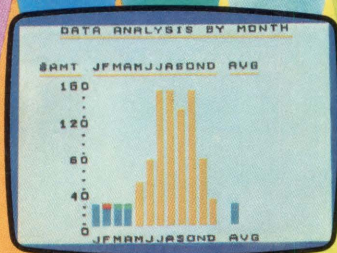
Since its inception in those early years of data communications technology, *Computer Design* has published hundreds of articles for those of you designing systems to move digital data from one location to another. In the early 60s few trade publications other than *Computer Design* had made that editorial commitment—and we made it because good system to system interface demanded it. Later, 11 years ago exactly, *Computer Design* inaugurated its "Communication Channel" department covering all phases involving data communications. In the 70s (and now in the 80s) other publications serving the industry have made similar commitments as is evidenced by the number of communications oriented magazines now being printed.

In this issue of *Computer Design* we are celebrating our 18th anniversary of communicating information important to your responsibilities in computer based systems design. This special communications issue has been compiled as a symbol of *CD's* birthday month. We feel it meets and serves your needs. Your comments—pro or con—will be welcome and appreciated.

be handled by international computer networks and satellites when they pass from the development to the commercial stage.

Two special computer programs were used during the demonstration,

also made test transmissions to the satellite. Other manufacturers will also demonstrate computer-to-computer transmission via Telstar, utilizing existing AT&T data communications facilities.



DISPLAY PAGE	
PAGE 27	1
1 COMPANY	XYZ CO
2 SHARES	100
3 CERT. NO.	XC342346C
4 TOT. BASIS	89.80
5 PUR. DATE	78.0215
6 NEW QUOTE	92.0000
7 Q. DATE	80.0526
8 MKT. VALUE	9200.00
9 GAIN/LOSS	310.00
10 LOCATION	FIRST BANK
11 COMMENT	SON'S ACCT

PRESS AID TO SEARCH
PRESS PROCD TO PREVIEW PAGES
PRESS PROCD TO PRINT SCREEN
PRESS BACK WHEN FINISHED

Color it TMS9918A. New video display processor. From Texas Instruments.

TMS9918A. For color applications never before possible with a single chip.

TMS9918A. For graphics terminals. Video games. Arcade games. Home computers. Industrial process monitoring. Drafting, animation and education systems.

TMS9918A. For generating excitement in sixteen distinct colors.

This 40-pin plastic DIP generates a standard National Television Systems Committee (NTSC) composite video signal to drive a color or black/white monitor — you can tie it to an ordinary home TV antenna — simply by using a suitable RF modulator. The low-power TMS9918A requires only a 5-V supply.

Another leadership peripheral circuit in TI's 16-bit 9900 Family, the TMS9918A is designed with a general 8-bit data bus, allowing interface to virtually any CPU.

3-D capability

TMS9918A allows 3-dimensional simulation through thirty-five prioritized display planes. This unique feature

TMS9927 Video/Timer Controller

For high-resolution CRT terminal applications, TI offers the industry standard. A direct second source of SMC's CRT5027, the TMS9927 provides programmable timing and display for standard and non-standard CRT monitors, in both interlaced and non-interlaced formats. TMS9927 and TMS9918A — a powerful combination for full video capability — from Texas Instruments.

allows objects on the screen to pass in front of one another, just like they were on different planes.

An external video input pin lets you input a standard broadcast signal, have the TMS9918A overlay text/graphics, and output the resultant mix to a color display.

Imagine the possibilities this feature offers: subtitles, interactive broadcasting — and more.

Do-it-yourself flexibility

With the patterns defined in RAM, TMS9918A allows quick, easy alternate pattern set implementation. A powerful graphics mode allows complex graphics presentations, utilizing all 16 colors.

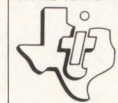
Thirty-two pattern objects can be moved smoothly across the screen to a positional resolution of one picture element. For textual applications, a flexible text mode provides resolution of 24 lines of 40 characters.

A typical video subsystem consists of a TMS9918A, eight dynamic RAMs and two TTL devices to generate CPU-9918A select signals.

The TMS9918A is available right now at your nearest authorized TI distributor.

For more information, write to Texas Instruments Incorporated, P.O. Box 1443, M/S 6404, Houston, Texas 77001.

Fifty Years
of
Innovation

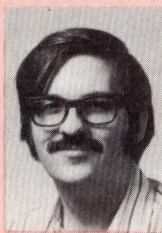


TEXAS INSTRUMENTS
INCORPORATED

CIRCLE 16 ON INQUIRY CARD



V. Godbole



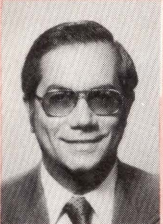
D. Bennett



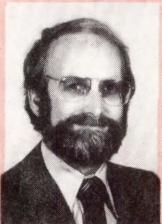
W. L. Schumacher



G. H. B. Yancy



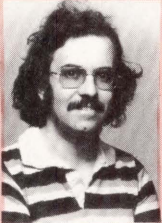
J. Jurenko



C. A. Cox



R. M. Groenke



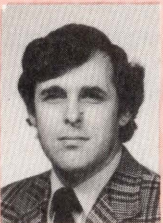
J. Forecast



C. M. Johnson



J. L. Jackson



W. Damm



J. Schriesheim



D. B. Kirby

CD DATACOMM

INTRODUCTION	25
PARTITIONING OF SYSTEM TASKS SIMPLIFIES DIGITAL SIGNAL PROCESSING	29
by Victor Godbole	
MULTIPURPOSE CONNECTOR MIXES ELECTRICAL AND OPTICAL SIGNALS	39
by W. L. Schumacher	
GETTING THE MOST MODEM FOR THE LEAST MONEY	45
by John Jurenko	
THE INCREASED ROLE OF REMOTE CONCENTRATORS IN DATA COMMUNICATIONS NETWORKS	51
by Ronald M. Groenke and Craig M. Johnson	
PLUG-IN ROM CUSTOMIZES NETWORK TESTER TO SPECIFIC INSTALLATION	55
by Wendell Damm and David Bennett	
FIBER OPTIC CABLES INCREASE EFFICIENCY OF DIGITAL TRANSMISSION SYSTEMS	59
by Gayton H. B. Yancy	
DUAL-SPEED ALTERNATE VOICE/DATA MODEM REDUCES SUPPORT REQUIREMENTS	67
by Christopher A. Cox	
COMMUNICATIONS EXECUTIVE IMPLEMENTS COMPUTER NETWORKS	71
by John Forecast, James L. Jackson, and Jeffrey Schriesheim	
PERFORMANCE MEASUREMENT IN DATA COMMUNICATIONS NETWORKS	77
by David B. Kirby	
DATACOMM ITEMS	82
DATACOMM PRODUCTS	92
DATACOMM Reader Service Card	80a

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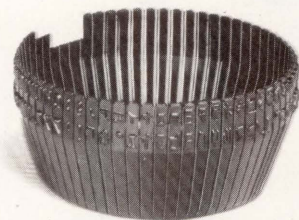
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PARTITIONING OF SYSTEM TASKS SIMPLIFIES DIGITAL SIGNAL PROCESSING

By utilizing a conventional microprocessor for data handling, I/O, and decision making, an intelligent peripheral device is freed to handle complex signal processing tasks in real time

Victor Godbole

American Microsystems, Incorporated
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The complexity of signal processing in voiceband data communications varies with the nature of the application. Low speed modems using frequency shift keying techniques can perform entirely in the analog domain. On the other hand, in higher speed modems the use of multilevel data encoding schemes results in a significantly higher level of complexity. It is difficult to achieve high precision and stability when using analog techniques to implement the large amounts of filtering and adaptive equalization schemes employed in high speed modems.

By contrast, digital signal processing techniques are better suited to high speed modem applications and offer several distinct advantages. Performance is stable and repeatable from unit to unit. High precision can be achieved and is limited only by the number of bits that the signal processor can handle. Greater flexibility is also obtainable because it is easier to modify response by simply varying the proper arithmetical coefficients. Moreover, major building blocks of the arithmetic unit (adder and subtractor, multiplier, etc), can be timeshared, allowing complex tasks to be broken down into several repeatable fundamental tasks.

Suitable hardware in large scale integration (LSI) form is now becoming available to reduce component count and the cost of hardware implementation in applications that require digital signal processing techniques. Conventional microprocessors, since they lack needed arithmetic power and speed, are not well suited to the requirements of complex digital signal processing. Algorithms used in such processing are highly multiplication intensive. Even for only a single, second order, digital filter section, the processor must perform four multiplications, four additions, and two store operations. Conventional microprocessors cannot perform 8- or 16-bit manipulations fast enough to process a significant number of these filter sections within the typical 125- μ s sampling interval corresponding to the 8-kHz sampling rate used in voiceband data communications systems.

The necessary ingredients of a digital signal processor are a specialized architecture and an instruction set tailored to provide computational efficiency. A specialized digital signal processor, configured as an intelligent peripheral to operate in conjunction with a conventional microprocessor, allows efficient partitioning

of system tasks. The microprocessor then becomes a controller for managing data flow, including input/output (I/O), and for calling out the application-specific routines stored in the signal processing peripheral. In turn, the peripheral actually performs the hard work associated with a specific signal processing task.

Architectural Functions

For optimum architecture, the general requirements of digital signal processing algorithms, as well as specific application details, must be considered. Filtering is a basic requirement in most voiceband communications systems. Both recursive (filters using feedback) and nonrecursive (transversal filters) are widely used. Because they provide minimum delay distortion, transversal filters are most suitable when a linear phase characteristic is required. Recursive filters are generally used when a steep filter response is desired with minimum computation. However, recursive filters exhibit a nonlinear phase characteristic that results in higher delay distortion.

A basic second order filter section can be used as a building block for higher order filters. In the equation for a second order recursive filter section

$$W_n = X_n + a_1 W_{(n-1)} + a_2 W_{(n-2)}$$

$$Y_n = W_n + b_1 W_{(n-1)} + b_2 W_{(n-2)}$$

a_1 , a_2 , b_1 , and b_2 are fixed coefficients.¹ X_n and Y_n represent input and output samples respectively, and W_n , $W_{(n-1)}$ and $W_{(n-2)}$ are intermediate computed results for present and past sampling instants. Clearly, some provision must be made for storing signal and coefficient data. Examination of the equations points out that half the data memory in a system can be read only memory (ROM) while the other half must be random access memory (RAM) holding variable signal data. This half ROM, half RAM division of data memory should achieve a considerable reduction in the overall size of data memory. To improve throughput, one must also make provision for accessing the coefficient data word simultaneously with the signal data word for multiplication. This calls for a dual output port memory structure. Use of a pipelined multiplier achieves still further improvement in throughput.

When the multiplier delay equals one instruction cycle, a product becomes available from the multiplier during the instruction immediately following the instruction in which data were entered into the multiplier. An instruction structure can then be realized to read two words from data memory, perform an arithmetic operation on them, and store the result back into data memory, all in only one cycle. This sort of dual operator instruction format for simultaneous arithmetic and data transfer operation is vital for realizing computational efficiency. The equations also show that digital signal

Instruction Repertory Promotes Efficiency

Special instructions implemented by the S2811 demonstrate the impact of instruction set design on digital signal processing efficiency.^{5,6} For example, signal processing algorithms such as that for the second order recursive filter operate extensively on delayed samples. By using a special instruction that transfers the V-port input register content to RAM (TVPV), the previous value read from the V-port passes directly to a memory location designated in the current instruction, implementing digital filter Z^{-1} delays with minimum software overhead.

A set overload protect (SOP) control mode allows the accumulator output to saturate to the maximum or minimum signed value, depending on the direction of overflow, whenever an overflow occurs. This feature is invaluable for implementing recursive filters, where oscillations might be caused by feedback after accumulator overflow.

First level loop nesting normally involves a great deal of software overhead. To avoid this, the S2811 includes a hardware loop counter allowing up to 32 iterations. Jump instructions such as jump conditional direct (JMCD) and jump conditional direct and increment (JCIDI) test the loop counter for a zero condition before performing the program step, providing iteration test and loop control without adding program instructions.

Efficiency increases in digital signal processing when several tasks are performed in parallel. Complex (multifunction) instructions simplify parallel task implementation. Some signal processing tasks must fetch data words that are separated by a fixed offset in memory. An instruction that interchanges the roles of the base and index registers (SWAP) allows the base and index registers to work together and achieves a dual base addressing scheme. For example, the jump conditionally dual tracking (JCDDT) instruction increments the base and index registers. It then tests to determine whether the loop counter is zero, and, if it is not zero, branches to the specified address. The loop counter is decremented after the test.

This approach saves several steps when programming iteration loops that fetch and process data words separated by fixed memory offsets, thereby reducing execution time in, for example, Fast Fourier Transform processing.

processing algorithms, such as recursive filter algorithms, operate extensively on delayed samples. A register must temporarily hold a value that was read from a location in data memory during one instruction until it is transferred to another data memory location during the next instruction. This implements digital filter Z^{-1} delays with minimal software overhead.

To provide sufficient dynamic range, an appropriate word length should be chosen to represent signal and coefficient values. In most applications, a 70-dB dynamic range is adequate, indicating that a 12-bit word is acceptable. Also, as pointed out earlier, higher order filters can be implemented by using a second order filter section as a building block. When permitting higher order computations to use the same set of instructions or subroutines designed for the basic second order filter, some facility must be provided for multiple iterations and iteration testing.

These and other considerations suggest an architecture that is specialized toward efficient implementation of digital signal processing algorithms. Once the basic building blocks are identified, the next task places a quantitative judgment on the sizes of the various blocks. How much data memory is required? How large an instruction ROM? How many different instructions? A careful study of various applications, cost vs size tradeoffs, and the level of design complexity provided answers to these questions.

Application Examples

The specialized architecture selected for use in the AMI S2811 signal processing peripheral (SPP) is shown in Fig 1. Although specialized for voiceband data communications requirements, this architecture also supports any algorithms or numerical computations that are multiplication intensive, that use delay elements, and that are suitable for easy implementation of in-place computations. Filtering is one of the basic signal processing tasks encountered in voiceband data communications systems. Among these tasks are to limit bandwidth, smooth a demodulated signal, smooth a rec-

tified waveform for averaging, and provide equalization. Both recursive and transversal filter types are widely used.

Transversal Filter

A typical application for a transversal filter is in the modem's receiving circuit, where it is used to remove the high frequency components from the demodulated signal. The equation for an N-stage (N-tap) transversal filter (Fig 2) can be written as

$$X(k) = C_0x(k) + \sum_{n=1}^N C_nx(k-n)$$

Here C_1 to C_n are respective tap weights and $x(k)$ and $X(k)$ represent, respectively, the input and output sample values at the k th sampling instant. The equation shows that computation of $X(k)$ involves a "sum of products" type operation. It is convenient to carry out the computation sequentially.

Operations to be performed at any given tap can be summarized as follows: accumulate product from previous tap; start multiplication for current tap; update the signal value associated with the current tap by shifting in the signal sample from the previous tap; and decrement the iteration counter. If the iteration count is zero, accumulate a final product, store it in the memory location designated for the output sample, and

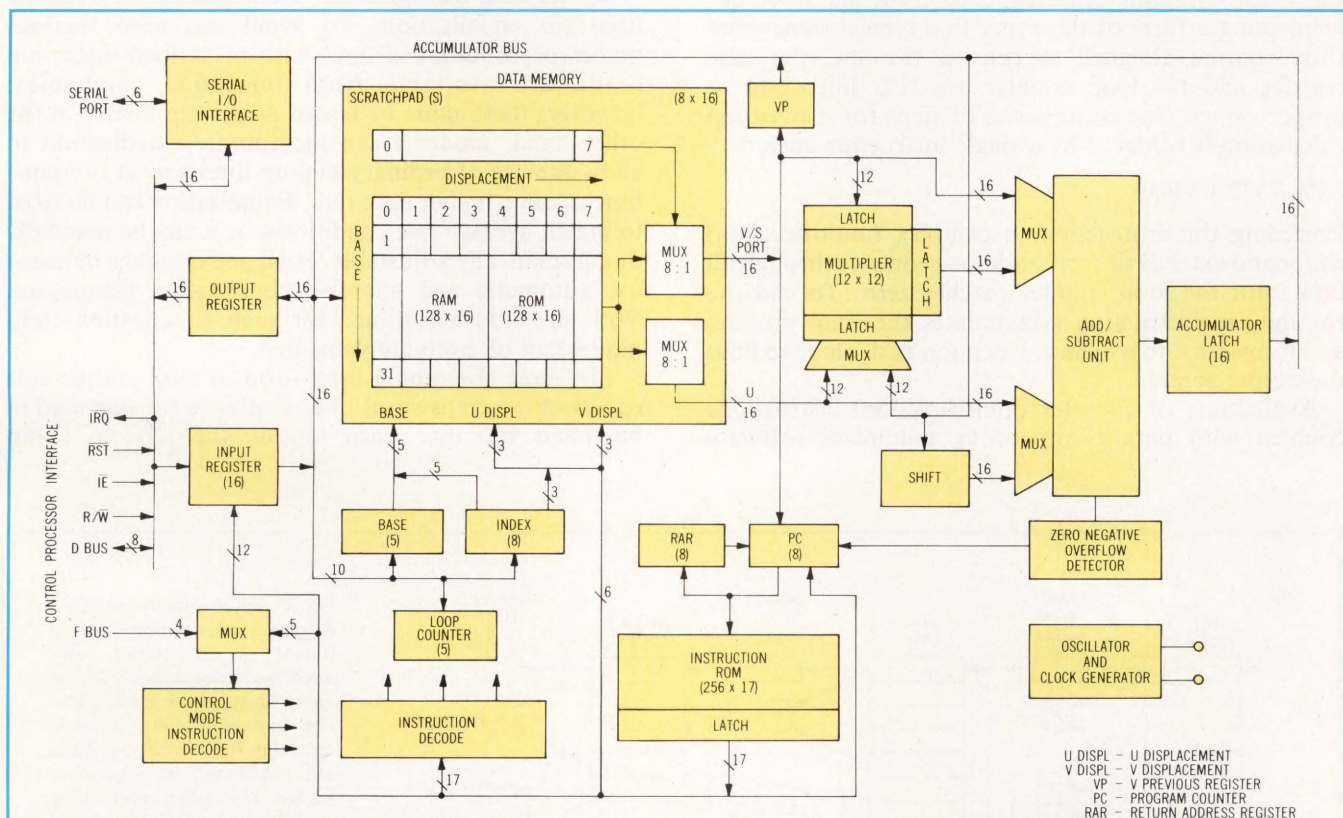


Fig 1 Specialized signal processing architecture. Arithmetic unit consists of high speed parallel multiplier and addition/subtraction unit (ASU). Dual port data memory is organized as half RAM, half ROM, for storing signal and coefficient

data, respectively. Instruction ROM holds signal processing routines. Serial and parallel I/O ports provide signal and control interface

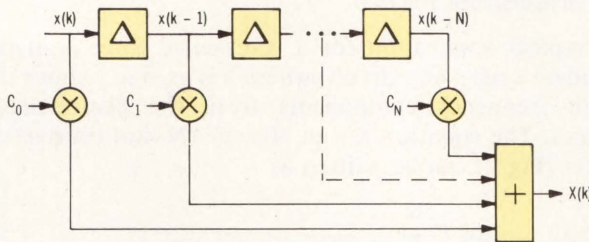


Fig 2 Transversal filter. Output $X(k)$ at a given sampling instant is a function of present and past values of input $x(k)$ only. No recursion of output occurs. Signal value at each tap is multiplied by its tap weight. Products from all taps are accumulated to produce output

terminate the computation sequence. If the iteration count is nonzero, proceed to the next tap.

Implementing the Filter

An SPP can implement the filter by storing a sequence of instructions in the form of a program or subroutine within the instruction ROM and by creating a memory map for accessing signal and coefficient data. Fig 3 shows the computational sequence in the SPP when implementing a filter of this type. In a typical transversal filter routine designed to run on the SPP, the base register and the loop counter are first initialized to proper values. The entire series of steps for a given tap calculation is achieved by a single instruction such as

APA TVIB UV(4,0)

Preceding this instruction, a complex (multifunction) command extends the computation sequence through all taps until the loop counter reaches zero. To end the routine, an instruction accumulates the final product and transfers it to a memory location designated to hold the output sample.

Availability of complex (multifunction) instructions coupled with parallel processing minimizes software

overhead. To implement an N -tap transversal filter, for example, six source statements, six machine instructions, and a total processing time of $N + 5$ instruction cycles are required. With a 300-ns instruction cycle time, this corresponds to an execution time of about $5 \mu s$ for a 12-tap filter. The typical 8-kHz sampling rate in voiceband data communications systems allows $125 \mu s$ for all the different signal processing tasks that must be performed, so it is important to minimize individual task computation times. This permits one signal processing device to perform all of the tasks that most applications require.

Equalization

Voiceband data communications channels are nothing more than voice grade telephone lines, and these introduce both amplitude and delay distortion into the transmitted signal. Amplitude distortion is caused by variations in gain as a function of frequency within the passband. Delay distortion is caused by the nonlinear relationship between the signal's phase shift and its frequency characteristic. Both types of distortion result from channel characteristics. Delay distortion causes interference between adjacent transmitted information samples; it is also known as intersymbol interference (ISI).

As the data transmission rate increases, so does the need for equalization. To avoid this need, various grades of conditioned lines with prescribed distortion limits are available from telephone companies; however, these must be leased as private lines. On the other hand, modems can incorporate equalization to allow the use of ordinary dial-up lines and at the same time attain a higher data rate. Equalization can be fixed to match average line conditions, or it can be manually or automatically adjustable. High performance modems use automatic and adaptive equalization techniques. With the SPP, algorithms for such equalization techniques can be easily implemented.

The most commonly used form of easily adjustable equalizer is a transversal filter similar to the one used in baseband filtering. Each tap on the $(2N + 1)$ -tap

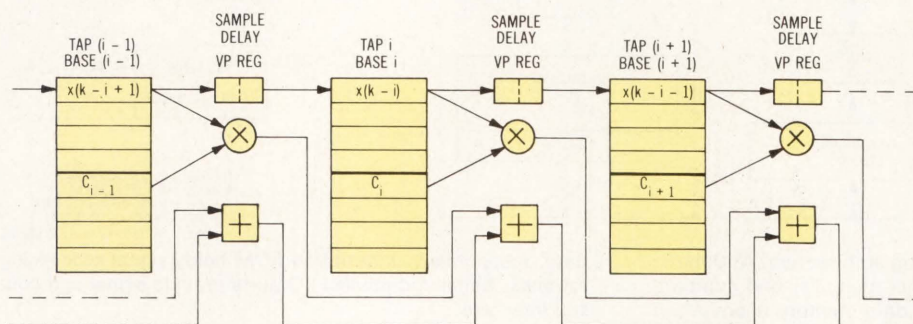


Fig 3 Filter implementation. A group of memory words (base) is associated with each tap. In each base, signal value is stored in RAM location and coefficient value is stored in ROM location. Taps are processed in sequence. Adder, multiplier, and delay register blocks are used repeatedly, under program control, until all taps have been processed

transversal equalizer is connected to a summing amplifier through a variable gain device. The equation for the equalizer can be written as

$$X(k) = \sum_{n=-N}^N C_n x[k - (N + n)]$$

where $x(k)$ are input samples to the equalizer and $X(k)$ are equalizer outputs.

Consider first the use of an equalizer in a baseband pulse amplitude modulation (PAM) system where the equalizing filter is inserted between the receiving filter and an analog to digital converter (ADC).² Ideally, if the received pulse has a peak at $t = 0$ and ISI on both sides, one would like to have

$$X(k) = \begin{cases} 1, & \text{for } k = 0 \\ 0, & \text{for } k = \pm 1, \pm 2, \dots, \pm N \end{cases}$$

This condition cannot always be realized because there are only $2N + 1$ tap gains available. For example, a 3-tap equalizer can be designed for zero ISI in the equalized pulse on either side of $t = 0$, but with a small ISI at points further out from $t = 0$ where the unequalized pulse had zero ISI (Fig 4).

Complex Valued Adaptive Equalizer

Equalizers used in high performance modems extend the basic transversal equalizer just described. In a typical configuration for a 4800-bit/s modem conforming to CCITT V.27 specifications³, the equalizer is inserted between the baseband filter and the quadrature phase shift keying (QPSK) detector. The baseband filter actually consists of two transversal filters that smooth the in-phase and quadrature phase components of the demodulated signal. The inphase and quadrature phase components can be considered as forming a complex number $x + jy$ as input to the equalizer. For an adaptive equalizer, the tap gains given by complex value $a_n + jb_n$ are updated from computations performed on error signals e_x and e_y supplied by the QPSK detector.

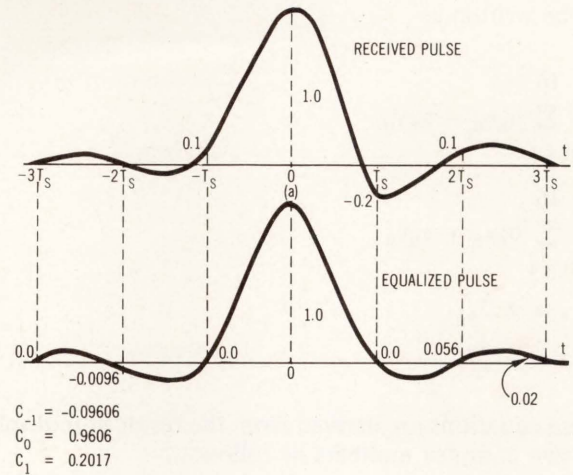


Fig 4 Three-tap equalizer input/output. Received pulse has peak at $t = 0$ and ISI on both sides of $t = 0$. Three-tap equalizer can be designed for zero ISI on either side of $t = 0$, but with small ISI at points well removed from $t = 0$ where received pulse may have had zero ISI

In a typical application, the baseband filters are sampled at 8 kHz, and the equalizer is sampled at 1.6 kHz or at the baud rate. It is necessary to sample baseband filters at the higher sampling rate in order to remove higher frequencies contained in the signal after demodulation. Thus, four out of five filter samples are simply discarded, and the equalizer processes one out of every five samples supplied by the filters. Equalizer output is a complex number that is processed to decode the received symbol. An error signal can be computed on the basis of the actual received symbol and the equalizer output. Equalizer tap gains are updated at a baud rate based on this error signal.

Typically, the equalizer may consist of 8 to 16 taps. Fig 5 shows the signal flow graph for a 16-tap equalizer.

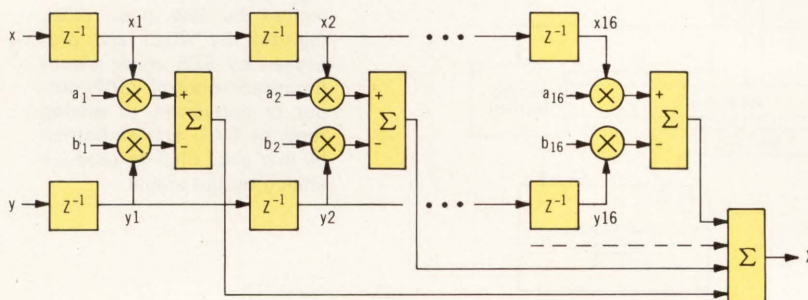


Fig 5 Equalizer implementation. In-phase and quadrature phase components are multiplied by their respective tap weights. Resulting quadrature phase data is subtracted from inphase data. Results from all taps are summed to produce real (inphase) component of equalizer output. Imaginary (quadrature phase) component of output is produced separately in similar manner

The equations for the 16-tap complex valued equalizer can be written as

$$X = \sum_{n=1}^{16} a_n x_n - b_n y_n$$

$$Y = \sum_{n=1}^{16} b_n x_n + a_n y_n$$

$$x_{n+1} = Z^{-1}x_n$$

$$y_{n+1} = Z^{-1}y_n$$

These equations are derived from the result of multiplying two complex numbers as follows:

$$(x_n + jy_n)(a_n + jb_n) = (a_n x_n - b_n y_n) + j(b_n x_n + a_n y_n)$$

Here, X and Y represent, respectively, the real and imaginary (inphase and quadrature phase) components of the equalizer output.

The complex valued equalizer can be implemented in a manner similar to that of a transversal filter on the SPP. However, there are some important differences. Coefficient values are not fixed; therefore, they must be stored in RAM. Equalizer computation involves complex numbers; hence, both x and y input data values are stored in adjacent RAM locations. Equalizer output also is a complex number whose real and imaginary components are computed in separate passes.

Other common signal processing tasks such as carrier generation, modulation and demodulation, and averaging can be handled in much the same fashion after programming appropriate algorithms for their implementation.

Building A Signal Processing System

Once the SPP has been programmed with application-specific routines, its use in the system proceeds completely under microprocessor software control. Hardware interfacing of the SPP is straightforward because it is handled like any other memory mapped peripheral. In a general purpose signal processing system configuration (Fig 6), serial I/O ports are used directly with ADCs and digital to analog converters (DACs) to provide a signal interface. A parallel port implements the control interface to the microprocessor.

To prevent aliasing of out-of-band signal and noise frequency components caused by the sampling process, the input analog signal must be bandwidth limited before it can be digitized and processed in the SPP. For providing bandwidth limiting to 3.4 kHz, standard D3 channelbank⁴ filters commonly used in pulse code modulation (PCM) telecommunications are ideally suited to perform the antialiasing filter function in the signal processing system. D3 channelbank filters are now available as monolithic integrated circuits, further simplifying system design. On the output side, a similar low pass smoothing filter should be used after the DAC, limiting the signal spectrum to around 3.4 kHz as required in voice grade telephone channels.

In a system, the microprocessor typically sets up the initial conditions and parameters, then begins execution of a signal processing task by calling out an application-specific routine stored in the SPP. Depending on the application, processing may continue until the SPP is interrupted by the microprocessor, perhaps to select a different algorithm or for periodic updating of adaptive algorithm coefficients. Or, the SPP may interrupt the processor for intermediate I/O conditions or to signal the end of a processing task. Thus, either an open ended or an interactive mode of signal processing can be selected for maximum flexibility.

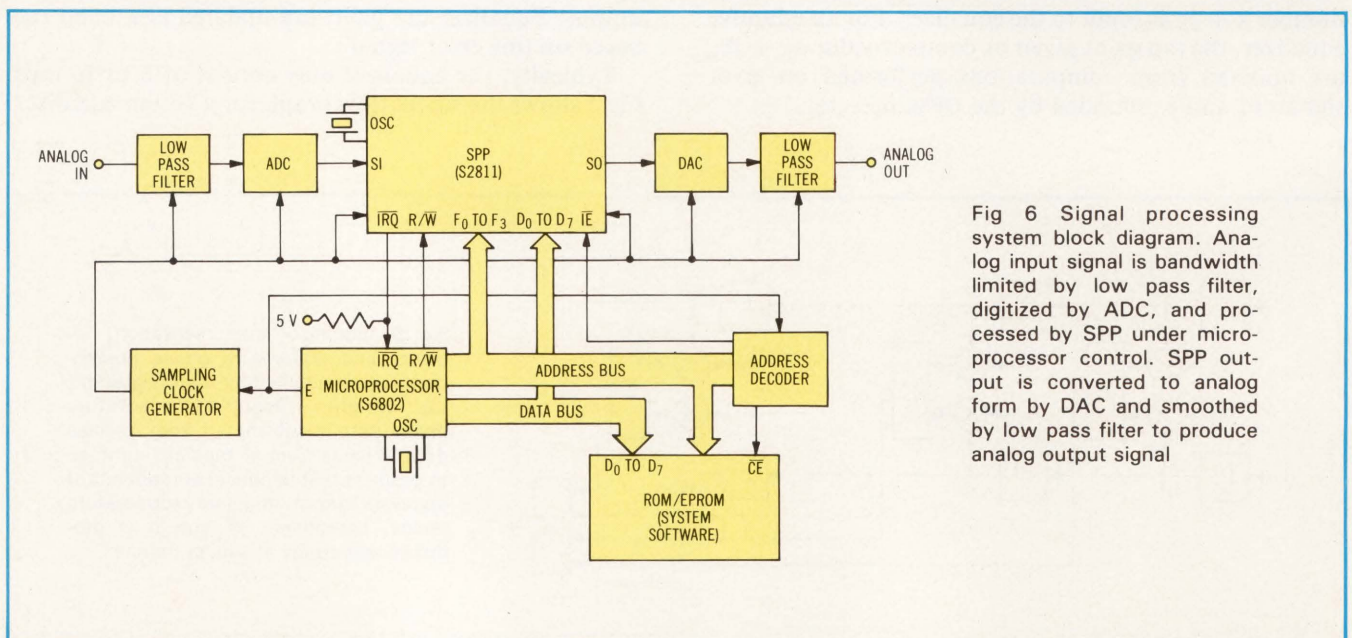


Fig 6 Signal processing system block diagram. Analog input signal is bandwidth limited by low pass filter, digitized by ADC, and processed by SPP under microprocessor control. SPP output is converted to analog form by DAC and smoothed by low pass filter to produce analog output signal

Conclusion

Designers of high performance voiceband data communications systems can simplify most commonly encountered digital signal processing tasks by selecting devices with architectures optimized for signal processing. Such devices use parallel processing to implement highly multiplication intensive sum-of-products type algorithms most efficiently. Careful consideration must be given to partitioning of system tasks. It is best to have normal data handling, I/O, and decision making tasks handled by a conventional microprocessor, while leaving the complex tasks of signal processing to a specialized device organized as an intelligent peripheral that operates in parallel with the microprocessor.

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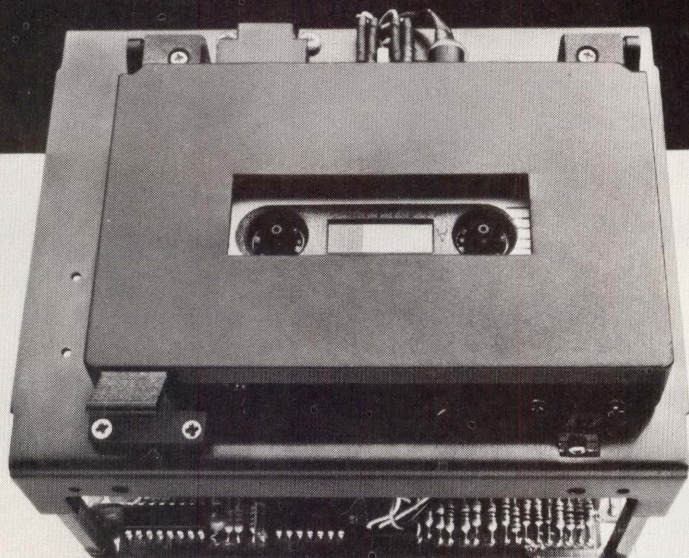
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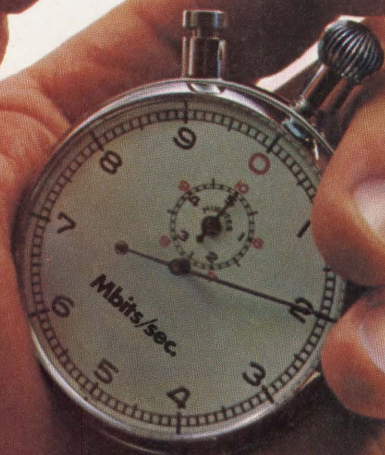
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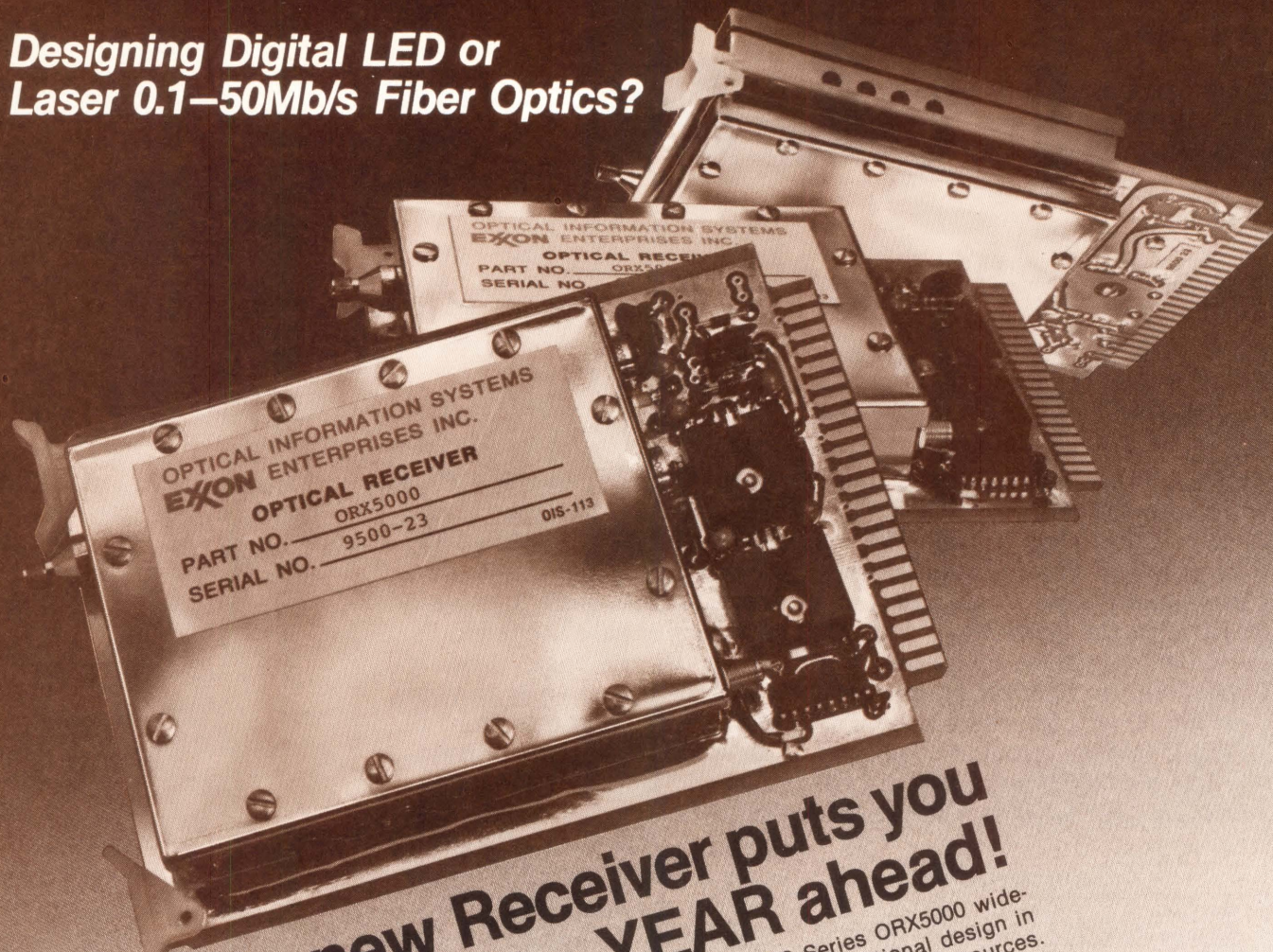
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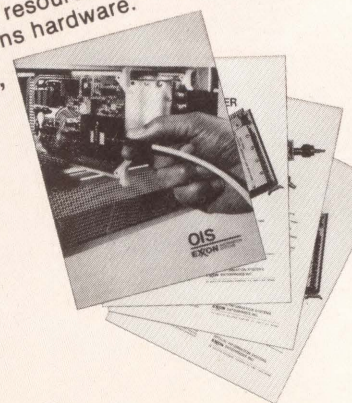
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MULTIPURPOSE CONNECTOR MIXES ELECTRICAL AND OPTICAL SIGNALS

Fiber optic cable connector mixes coaxial, power, signal, and optical cables in a single housing that rivals standard electrical connectors in economy and ease of use

W.L. Schumacher

AMP, Incorporated
Harrisburg, PA 17105

For more than two decades, designers have been intrigued by the potentials of fiber optic technology and its ability to transmit information through thin strands of transparent glass or plastic. Compared to conventional coaxial cable or twisted wire pairs, fiber optic links permit tremendous reductions in size and weight of computer related systems. In one weight-critical airborne installation, for instance, 302 copper cables, with a total length of 4832 ft (1.473 km) and weight of 87 lb (1.2 kg), were replaced by 13 optical fibers with a total length of 250 ft (76 m) and weight of 3.6 lb (0.05 kg), approximately a 20 to 1 length and a 24 to 1 weight reduction.

In addition, the data security/noise immunity benefits of fiber optics are proven. Fiber optic systems' immunity to radio frequency or electromagnetic interference is an important consideration, particularly when cables are strung through factories or under the street conduits where relays, motors, or other noise generating units are operating. With ever more attention

being paid to computer security, the fact that fiber optic systems are virtually immune to unauthorized tapping is also of special interest.

Critical Cost Considerations

Although some computer designers have made excellent use of fiber optics, others have held back, usually, it seems, because they could not justify the high perceived cost. And some costs were very high indeed. Now, however, many costs are dropping. The price of fiber optic cable itself is declining in early 1980 to as low as \$1.00/m. Simultaneously, cable attenuation (and therefore system performance) is improving. Attenuation of 10 dB/km at 820 to 900 nm is common.

Cost of emitters, such as LEDs used in optical transmitters and photodetectors used in receivers, are declining too. Critical components in any data link, the connectors have also been keeping pace in performance,

availability, and price. Dozens of specific connector designs are solving individual designer problems, and new connector concepts have advanced the state of the art.

Connector Economies Keep Pace

One of the newest and most significant developments in fiber optics connectors is the multipurpose connector—a device that can incorporate coaxial, power, signal, and optical cables in a single, familiar connector housing. (See Fig 1.) Although the mix or match concept of incorporating various types of fiber optic connections into a standard connector is relatively new, the connectors themselves are not. Rather, the connectors are the same familiar multiple pin designs that have been on the market for over 20 years.

Today's standard multipurpose connectors can accommodate fiber optic circuits because contacts (insertion mechanisms) have been developed that are easily affixed to any fiber optic cable, single-strand or bundled. These ferrule type contacts may simply be substituted for any one or more pins in the multipin connectors to convey optical instead of conventional electrical signals. The connector housings, therefore, remain unchanged—standard design, mass produced, easily handled, proven service, low in cost. This low cost

concept is a distinct departure from the conventional approach to fiber optic connectors, which often emphasizes custom design, precision manufacture, expensive materials, and, therefore, higher overall cost.

Essentially, the function of a fiber optic connector is to bring pairs of optical cables as close together as possible without having them actually touch. In addition, the fibers, which may comprise either single-strands or bundles, must be very precisely oriented in relation to each other. If ends of optical cables are improperly positioned and consequently come into contact with each other, the surfaces are subject to abrasion and damage. If the fibers are not well aligned axially, excessive attenuation of signal strength can occur. Either situation can lead to signal losses greater than the generally acceptable range of 2 dB.

Traditionally, fiber optic connectors achieve precise positioning through precision manufacture of the connector itself. Very close tolerances are called for in the range of $\pm 0.00025"$ (± 0.00635 mm). Metals from which such connectors are machined often are expensive. Methods of attaching fibers to connectors can be complex, exacting, time consuming, and can require highly trained personnel. Designers have found that such hard precision connectors have two main drawbacks: they are expensive to manufacture, assemble, handle, and install; and although the connectors are precision fashioned, many of the optical fibers they hold are not. Whether the fiber is of glass, of plastic, or of some combination, diameters may deviate from nominal by up to $\pm 5\%$ and may be out of round.

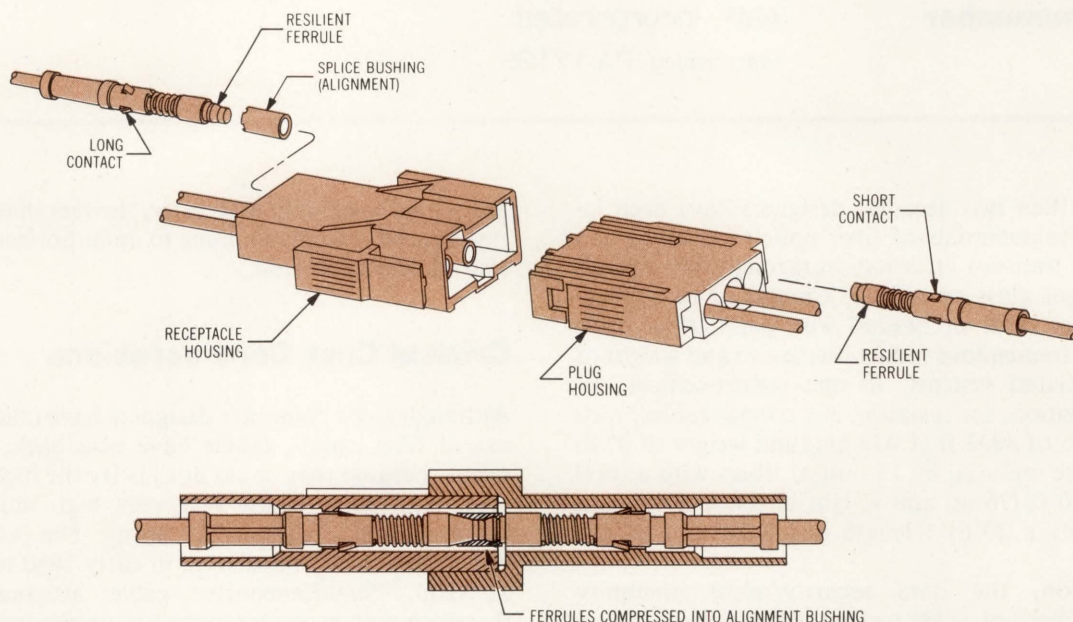


Fig 1 Multipurpose connector. Using familiar multiple pin design, connector allows substitution of elastomeric plastic ferrule contact for any one or more electrical signal pins

Clearly, these factors make it very difficult to ensure the required positioning and alignment, even when employing precisely dimensioned hard connectors.

Alternative Design

An alternative to precision machining is a connector system that positions the fiber within the connector each time they are assembled, and automatically makes allowances for dimensional deviations in the fiber. Ideally, the joining process should precisely position the fiber every time, regardless of a fiber's possible deviations from nominal diameter or from perfect roundness. This ideal is now achievable through use of a ferrule type connector terminal made of elastomeric plastic. When a fiber is passed through a hole in the axial center of such a ferrule and the ferrule is compressed, the fiber is automatically centered even if it deviates from nominal standards.

Ferrule is the Key

At the heart of the multipurpose connector system is the elastomeric ferrule mentioned above. (See Fig 2.) One standard ferrule design is the basis of both male and

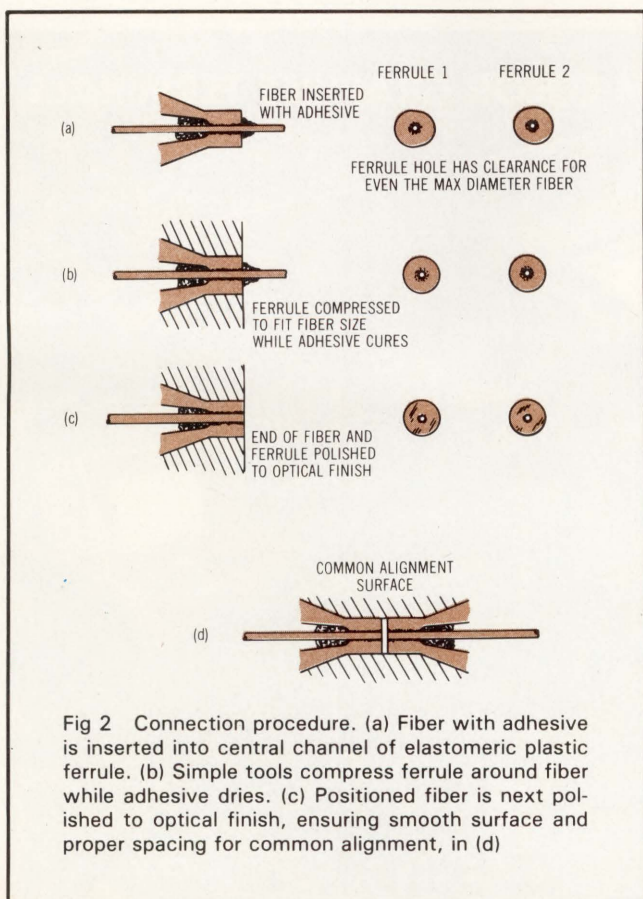


Fig 2 Connection procedure. (a) Fiber with adhesive is inserted into central channel of elastomeric plastic ferrule. (b) Simple tools compress ferrule around fiber while adhesive dries. (c) Positioned fiber is next polished to optical finish, ensuring smooth surface and proper spacing for common alignment, in (d)

female connectors. To ensure proper mating, a simple plastic alignment bushing or sleeve is added to one of the ferrules in each pair to create a female configuration. Manufacturing techniques for these ferrules require careful quality control but no exotic techniques. The ferrule body with an axial channel to accept optical fibers is molded of resilient thermoplastic, then inserted into a brass retention sleeve. Retention springs of stainless steel are added, followed by cadmium plated compression springs. Each of the ferrule sizes is designed to fit a specific, standard connector cavity. All will accommodate single optical fibers 250 to 600 μm in diameter [up to a maximum of 45 mils (1.14 mm) in diameter for bundle fibers]. To link two optical fibers, the fiber is placed inside the resilient ferrule and compressive forces are applied via a compression ring. These forces uniformly compress the thermoplastic, reducing the inside diameter of the ferrule. This process, of course, ensures a tight grip on each fiber, of even the smallest diameter. In addition, it optimizes centering of the fiber within the ferrule and therefore within the connector cavity.

Thus, optical fibers can be connected with each other in a simple 5-step process:

1. Insert fiber into central channel of elastomeric ferrule. Although care should be exercised, no special skills are required.

2. With simple hand tools, tighten compression ring around ferrule, locking the fiber in place and positioning it centrally.

3. Polish the positioned fiber to appropriate length to ensure smooth surface and proper spacing between fiber ends. (This process is simple.)

4. Insert paired ferruled cables in appropriate cavities of the multipurpose connector housing. (Other cavities can contain copper wires.)

5. Mate the housings in conventional manner.

Growing Applications

The ferrules can be used with either glass or plastic fibers, although glass may call for a supplementary drop of epoxy adhesive to ensure a good bond to the thermoplastic ferrule material. The ability of designers to cluster all cables, optical or electrical, in a single convenient connector is having an impact on their thinking about fiber optics in such applications as machine control, process control remote monitoring, and remote terminals. The advantages are:

1. Unwanted effects of dimensional variations in optical fibers are minimized or eliminated by use of resilient plastic. This same resilience helps cushion sometimes delicate fibers against vibration and other mechanical problems.

2. Good signal transmission can be expected because fibers are accurately positioned and aligned. Insertion losses can be held to the range of 2 to 3 dB, considered acceptable in computer applications.

3. Overall cost is low, traceable to modest cost of ferrules, simple assembly techniques, and standard, mass produced connector housings. Total installed cost

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per fiber optic cable is likely to be one-third, or less, of previously available optical links.

4. Connections are easy to disconnect/reconnect. Rugged connector housings may be connected and reconnected for an indefinite number of cycles. Individual contacts may be removed from their cavities and reinserted, if desired.

5. Inventory of connectors is minimal since no special housings are required for optical connections.

6. Assembly (or disassembly) is simplified, since all connections are made in one step—rather than requiring separate steps for power, coaxial, and optical connections, for example. Circuit integrity is also improved.

7. Weight and space requirements are kept at a minimum.

A Boost for Fiber Optics

This apparently simple connector technology, based on the ability of elastomeric plastic to automatically position optical cables when the plastic is compressed, is already having a significant impact on computer technology. With connector costs down, interest in fiber optics is up. Laboratory and field experience are demonstrating reliability; application bugs are being worked out. Manufacturing and service technicians find

familiar connector configurations easy to work with. With no need to stock exotic connectors or special hardware, inventory costs are low. Only a few sizes of ferrules to accommodate most cable sizes must be added to inventory; all other tools and hardware are standard for all sizes of ferrules and/or for standard connector housings.

Designers are now moving ahead, with the aid of experimental kits, to explore and utilize fiber optics in their systems design. Once prototype circuits have been proven feasible, the availability of multipurpose connectors will further the adaptability and economy of the fiber optic/computer system design. **CD**

W. L. Schumacher, principal development engineer with AMP, Incorporated, holds patents in the areas of high voltage connectors, basic crimp configurations, coaxial connectors, coaxial cable construction, mass termination connectors and tooling, and fiber optic connectors. An electrical engineering graduate of the University of Missouri at Columbia, and a member of the Faculty of the Center for Professional Advancement, East Brunswick, NJ, he is reported to be in the top 1% of the half million U.S. inventors.

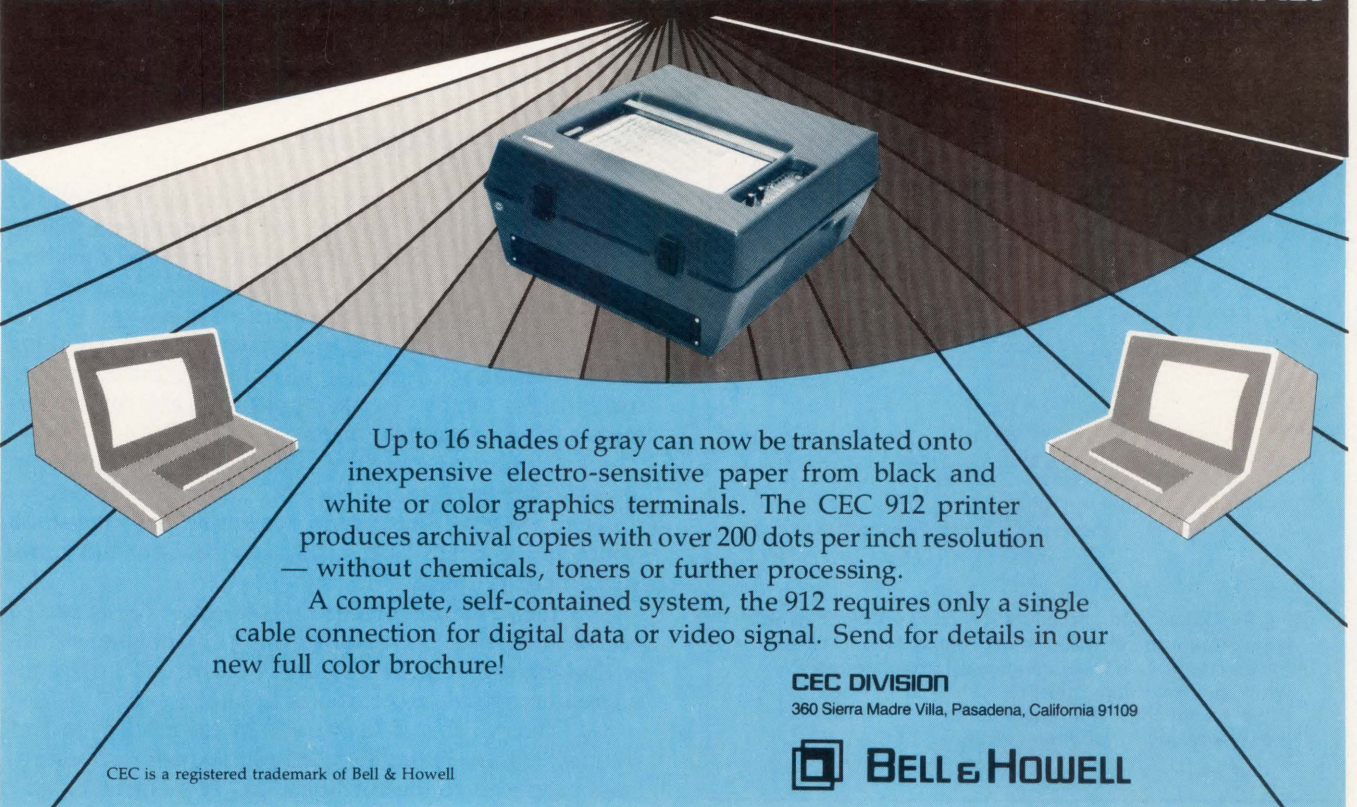
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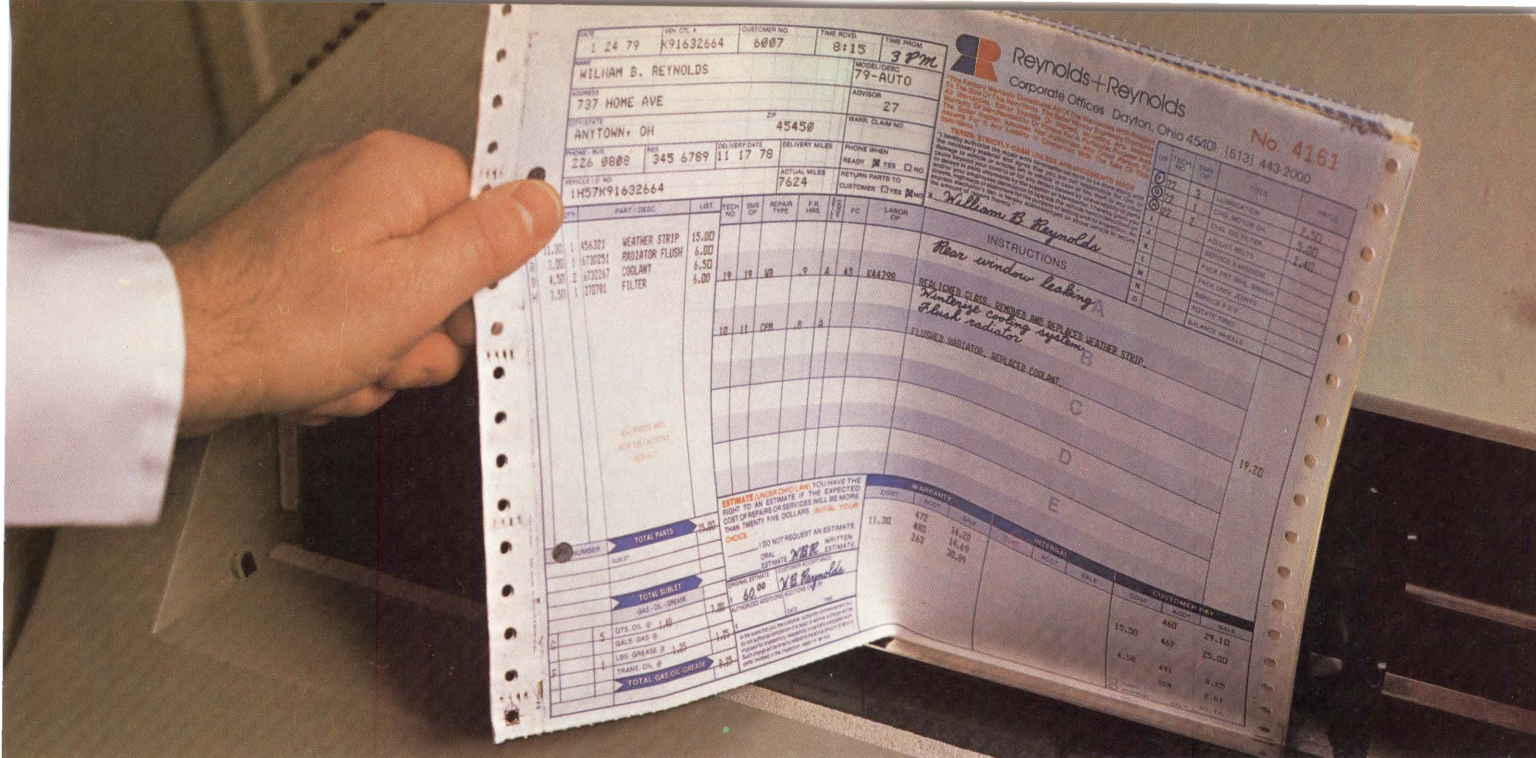
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GETTING THE MOST MODEM FOR THE LEAST MONEY

Today's relatively low modem costs can be cut further by defining specific data communications requirements and matching them to available modems, thus reducing the need for custom design.

John Jurenko

Universal Data Systems, Incorporated
5000 Bradford Dr. Huntsville, AL 35805

Compared to the cost of central processing units and most peripheral devices, modems are relatively inexpensive. As distributed data processing grows in importance, however, systems engineers become increasingly sensitive to the cost of dozens or even hundreds of modems within a single system. One of the best ways to control modem cost is by stripping away everything that is not absolutely essential. Making the modem an integral part of a terminal, for example, eliminates the expensive housings, power supplies, controls, and switches that are required in a self-contained modem. The original equipment manufacturer modem, a board that can be plugged into a slot within the cabinet of a terminal or other system component, reduces this essential subsystem to its least costly configuration.

Modems are such a highly specialized part of a data communications system that many original equipment manufacturers (OEMs) purchase these subsystem elements from outside vendors. The technologies employed in modem design and manufacturing span a great many disciplines. Within the deceptively simple appearing boards, high speed streams of digital data are

converted into audio signals; waveforms are precisely shaped, clipped, and buffered; the whole conversion process is performed in the opposite direction; and an immense variety of control and housekeeping functions are handled through a combination of hardwired and software techniques.

Signal handling is only part of a modem's job. Many systems also require the modem to handle diagnostic and testing chores and to give detailed indications of existing conditions within the modem itself, the associated terminal, the interconnecting network, and even the modem and terminal at the other end of the communication path. For high speed operation, modems incorporate automatic adaptive equalization that changes the filter characteristics with time as the transmission lines change. Finally, because they span the gap between a data processing system, with all of its peculiarities, and an interconnecting network, with its own rigid set of rules and peculiarities, modems can be viewed as devices that perform a combination of electronic, mechanical, and government agency mandated isolation functions.

Considering all of the factors just mentioned, it is tempting to compile a very detailed list of specifications when seeking bids from modem vendors. In many cases, the tendency toward overspecification can lead to a much more expensive modem than the system actually requires. Temperature tolerances, for example, can be overstated to the point where an otherwise suitable off the shelf modem must be passed by in favor of a custom designed unit that uses specially selected components, incorporates additional circuitry, and requires expensive qualification testing. The cost of all this special work is worthwhile, of course, provided that the system truly

needs the extra performance. However, most systems do not require much more than generally accepted performance within industry standard temperature ranges.

Throughout the modem industry, manufacturers suggest a high degree of vendor participation when it comes to specifying a custom modem for an OEM application. Their advice is to arrive at a general characterization of the modem performance level required and then to submit this outline information to selected vendors. Detailed specifications should be drawn up jointly with the vendors. This approach offers many benefits. There is a good chance of obtaining a recommendation for an off the shelf product that would cost less than a custom design. The final specification will be more meaningful than a specification generated by engineers who have limited modem experience. Costly overspecification can be avoided. Necessary details will be included that might

Modem Specification Outline

(Check Appropriate Boxes)

1. General System Information

- ☐ Dial-up telephone network
- ☐ Dedicated private line network
 - ☐ 2-wire
 - ☐ 4-wire
 - ☐ Point to point
 - ☐ Multidrop
- ☐ Approvals and standards
 - ☐ FCC Part 68
 - ☐ Underwriters' Lab
 - ☐ CSA
 - ☐ PTT
 - ☐ Other _____

2. Data Flow Information

- Speed is _____ bits/s
- ☐ Synchronous
- ☐ Asynchronous
- ☐ Full-duplex
- ☐ Half-duplex
- ☐ Simplex
- ☐ Extreme data accuracy required

3. System Interface Information

- ☐ Direct logic interface
 - ☐ TTL
 - ☐ CMOS
 - ☐ Other _____
- ☐ RS-232
- ☐ MIL-188
- ☐ EIA-449
- ☐ IEEE-488
- ☐ CCITT V.24
- ☐ Other _____

4. Terminal Power Available

- ☐ OK to tap terminal
 - \pm _____ Vdc
 - _____ mA
- ☐ Dc to dc converter required
 - Modem must have independent power supply.
 - Power mains provide _____ V at _____ Hz.

5. Modem Circuit Board Requirements

- \pm _____ in long
- \pm _____ in wide
- _____ (max) in between cards (standard = 0.5 in)
- operating temperature max (standard 50 °C)

6. Features and Options Desired

- ☐ Analog loop test
- ☐ Digital loop test
- ☐ CCITT pseudorandom code generator
- ☐ Error detect and display
- ☐ Squelch
- ☐ Multiple RTS/CTS delays
- ☐ Auto dial
- ☐ Auto answer
- ☐ 2-wire/4-wire select
- ☐ Originate only
- ☐ Answer only
- ☐ Manual originate/answer select
- ☐ Automatic originate/answer select
- ☐ External clock input
- ☐ Output level select
- ☐ Reverse channel
 - ☐ 5 bits/s
 - ☐ 75 bits/s
 - ☐ 150 bits/s
- ☐ Disconnect options
 - ☐ a. 12-s absence of carrier
 - ☐ b. Loss of carrier
 - ☐ c. Loss of line current
 - ☐ d. Receive Long Space
 - ☐ e. Send Long Space
- ☐ Busy out
- ☐ Constant carrier
- ☐ Carrier detect level

7. Purchasing Information

- Need _____ units this year
- Need _____ units next year
- Need quote by _____ (Date)
- Need evaluation prototype by _____ (Date)
- Need _____ units per _____

otherwise be overlooked, especially in the area of telephone network interfacing. Helpful suggestions may result in testing and diagnostic features that cost less when incorporated into the modem subsystem than when included elsewhere in the overall product design. Finally, a written test procedure may be supplied if requested.

There are basic facts that any modem manufacturer must know in order to respond to a request for an OEM modem to be used in a product or system. If OEM modem customers would begin the purchasing process by preparing these facts, the entire relationship with vendors would be smoother, the process leading to a firm quotation would be easier, and far fewer problems would occur in the long run.

General System Application Information

Vendors need to know whether the system will be interconnected through the regular dial-up telephone network or through some type of leased line network. If the dial-up telephone network will be used, they must know whether this will involve Federal Communications Commission (FCC) registered, direct connect interfacing. Is the system (or any portion of it) destined for use in a foreign country? If so, which one? What sort of governmental agency approval might be required? (The FCC, Underwriters' Laboratories, CSA, and PTT, among others, should be considered.) If the system will be interconnected through a leased line network, is it a 2-wire system or a 4-wire system? Is it a point to point system, or is it a multidrop system with one transmission line connected to more than two stations? Are there any special engineering features that the modem vendor should know about? Will the system use any unusual data links, such as satellites or other long path carriers?

Specific Data Flow Information

Vendors also must know the required bit rate for digital data transmission. Modems are available to handle data speeds from fewer than 300 to 9600 bits/s. Special purpose modems can handle data at far higher rates; however, they are not compatible with the constraints encountered on conventional voice grade telephone lines. Will the system handle synchronous or asynchronous data? Will the terminals require full-duplex operation, or will half-duplex operation suffice? The required level of accuracy is another important data transmission parameter. For example, facsimile systems may be rather undemanding, while banking systems involving electronic transfer of funds cannot tolerate errors.

System Interfacing Information

What kind of interface is required? Available modems provide interface capability for use with several types of integrated circuits including transistor-transistor logic and complementary metal oxide semiconductor logic. Also available are so-called standard interfaces, such as EIA RS-232-C, MIL STD-188, IEEE-488, EIA RS-449, and CCITT V.24 and, if required, custom designed, bus oriented interfaces. In addition, another important piece of system information, the connector requirements, should be determined. How will other system elements connect to the modem? How will the modem plug into the network interconnection wiring?

Power Availability and Form Factor

Must the modem contain an independent power supply, or can operating voltages be taken from the associated terminal? If terminal power can be used, the available voltages and currents must be determined. How much space has been allotted to the modem? What are the dimensions of the cards used in the system? What is the separation between card slots? Where are the card connectors located, and what type of connector is being used? Must the modem occupy only a single card slot, or can it take up two or more slots? During actual system operation, will the modem card be in a vertical position or in a horizontal position? This last consideration can affect heat transfer and component cooling. Vendors also should know about any special environmental qualification that would require the modem to be constructed using a special printed circuit board material or specially qualified components.

Special Features and Options

Special features rank among the most difficult portions of the specification to anticipate. However, in this area, one can expect a great deal of prompting and assistance from the modem manufacturer. Are there any special testing needs? For example, analog or digital loop testing, built-in signal generators, and CCITT pseudorandom noise generators all are available, along with an almost infinite lineup of other diagnostic capabilities including automatic remote diagnosis, error detectors, quality monitoring subsystems, and so on. Additionally, such items as light emitting diodes that indicate functions generally used for testing (but not for signal handling) also can be specified. An example is a simple indicator that shows the presence of a carrier signal, a transmitted data signal, a received data signal, or any number of modem and terminal interface functions.

Options such as those described in some of the Bell standards should be considered. Does the modem require a squelch feature? Will the system employ only one delay between a request to send and a clear to send, or might several delay intervals be required? The list of possibilities in this category is a long one.

Environmental Considerations

Normal environmental specifications for industry allow the equipment to operate within a temperature range of 0 to 50 °C. Relative humidity can be as high as 95% (without condensation). If the system must tolerate more extreme environments, the special component, construction, and testing requirements will have an especially significant impact on cost.

Purchasing Information

Of necessity, vendors require the best forecast of quantities needed and as much information as possible about the timing of deliveries. How closely can needs be synchronized with the modem vendor's normal cycle of product development, prototype testing, manufacturing release, volume production, and delivery? The earlier an agreement on these questions is reached, the more accurately actual costs will match initial cost estimates.

Proprietary Agreements

Assuming the required modem will be a custom designed product, the vendor should know whether a long

term proprietary agreement will limit wider distribution or, alternatively, whether the design can be offered to other potential customers.

Custom Design Cost Considerations

Past relationships with other OEM subsystem vendors are a good guide in dealing with a modem manufacturer. Obviously, off the shelf, standard products are the least expensive to purchase, and this cost advantage remains valid when relatively minor modifications must be made to existing standard products. Using existing products to satisfy needs is a good business practice that benefits both parties.

If the product does call for custom design engineering, there will of course be a charge for the development effort involved. Typically, these charges are nominal and significantly lower than charges encountered in certain other segments of the electronics industry.

How to Get Started

Perhaps the best way to get started is by attempting to answer the questions presented here and in the Modem Specification Outline. Then, after organizing the data in some fashion, one or more modem manufacturers can be contacted by telephone. Allow the manufacturer to help decide whether an informal discussion among engineers might be of use before the specification is sent out for bids. An honest and helpful reply can be expected because the business advantages of volume production encourage modem manufacturers to exhaust all possibilities involving standard products before initiating a custom design project. **CD**

Note: To obtain a better understanding of modems, modem technology, and some of the technical concepts mentioned in this article, request a free copy of the booklet *All About Modems* from the author.

John Jurenko joined Universal Data Systems in 1975 as National Sales Manager, participating in the development of sales representatives and distributor programs, and was named Vice President of Sales in 1979. He has earned his BS and MS in electrical engineering.

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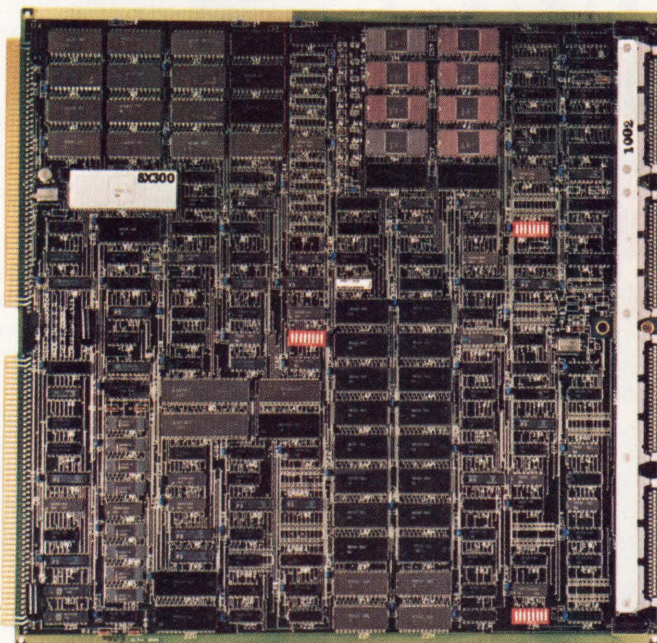
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THE INCREASED ROLE OF REMOTE CONCENTRATORS IN DATA COMMUNICATIONS NETWORKS

As data network complexity grows, so does the need for sophisticated remote concentrators. Special functions enable available devices to cost-effectively match those requirements

Ronald M. Groenke
Craig M. Johnson

NCR Comten, Inc
2700 Snelling Ave North, St Paul, MN 55113

In their early days, remote concentrators played a fairly simple role in a data communications network. They concentrated data received at a remote site from multiple lower speed lines for transmission over one or more high capacity lines, reducing communications line costs.

As data communications networks grew increasingly complex with the advent of satellite communications, public data networks, and a variety of common carrier offerings, remote concentrators had to become increasingly sophisticated. While the concentrator's basic function remains the same—the concentration of data for transmission over high speed lines—accomplishing that function, along with providing added features, has required significant advances in the equipment's system software capabilities. This evolution in remote concentrator technology must be viewed in conjunction with the evolution in data communications networks.

Today, as in the past, the purpose of a data communications network is to provide optimum communication between users—between two or more people, between a person and an application, or between two applications. Two fundamental capabilities of an effective communications network, connectivity and networking, derive from this purpose.

Connectivity allows a user to access the network and perform meaningful communication with the desired destination. This is usually accomplished by sets of formats and protocols for both node to node and end to

end communications. In today's environment, however, most users must achieve this connectivity not only with IBM compatible systems network architecture (SNA) and pre-SNA, but also with other unique or special purpose equipment. As new products and service offerings become available, designers must support international standards such as CCITT Recommendations X.25 and X.21.

Networking provides a transparent channel for the orderly flow of information between end points. Users now achieve this networking through various levels of communications service and a variety of common carrier offerings.

The user can optimize a network by selecting the proper level of communications service to provide adequate throughput and performance at an acceptable cost. For high throughput or performance oriented applications, a user may configure a dedicated path through the network, as in a circuit switched link. For other applications, the user may select a multiplexed or store and forward channel in which data are generally divided into packets and forwarded to the destination as bandwidth is available. Most users require the capability to support combinations of these levels of service within their network.

Support for the variety of common carrier offerings available, such as leased and dial-up circuits, satellites, and public data networks, is also necessary. Despite all

of these variables, in order to be feasible the channel between end users of the network must be transparent to the operators and independent of the level of service selected, the common carrier offering used, the number of intermediate nodes, and the formats and protocols employed.

It is in these increasingly complex data communications networks that today's remote concentrators must operate. As in the past, the remote concentrator receives data at a site distant from multiple lower speed lines and concentrates the data for transmission over one or more high capacity lines without imposing any changes in the terminal operator's or host processor's executing procedures or software. Although the concentrator's fundamental function has remained the same, performing that function calls for increasingly sophisticated system software.

Users continue to demand more efficient and effective usage of their complex and dynamic data communications networks. Providing a transparent trunking facility between interconnected communications processors, the communications networking system (CNS) presents a cogent example of this increasing software sophistication. Rather than using many individual lines between terminals and a frontend processor, a CNS concentrator adaptively multiplexes data from many terminals—both synchronous and asynchronous—for transmission over a high speed trunk facility. Any terminal attached to a CNS network can access a host application anywhere in the network, once the correct connection sequence and access codes have been entered (Fig 1).

To optimize network throughput during data communications, CNS software assigns trunk bandwidth only when data need to be transmitted. At other times,

such as when entering data from the keyboard or waiting for a response, the trunk bandwidth is available and dynamically assigned to other terminal connections.

To ensure high network reliability, CNS allows multiple circuits running at the same or different speeds to establish a trunk between any two nodes. The resultant trunk bandwidth is the sum of the speeds of the individual circuits. In the event of one circuit failure, communications continue in the remaining circuits, and data in transit on a failed circuit are automatically retransmitted on a good circuit. Data from both asynchronous and binary synchronous terminals are put into a unique buffer and format. Transmissions between nodes are acknowledged and retransmitted if errors occur, and a record of the number of buffers and blocks sent and received is maintained. Order of block sequence from terminal to host and host to terminal is guaranteed.

Finally, to enhance network flexibility, CNS can co-exist not only with pre-SNA, but also with compatible SNA support, thereby providing an orderly migration to the newer terminals and bit oriented communications procedures. Satellite links can also be used for CNS trunk circuits, and in certain configurations the propagation delays inherent in satellite communication are masked out to allow terminals to operate at rated speeds—avoiding the severely degraded mode normally expected with long delay links.

Other features permitting terminals to access multiple applications include terminal switching, line switching, and alternate pathing. But the significance of these developments resides more in the increasing sophistication of system software for remote concentration than in the existence of CNS per se. Users now have available extended dimensions of networking configurability and new plateaus of increased resource utilization.

Not all users, however, require or can economically justify the extensive functions and performance of a separate remote multiplexer system. More will be

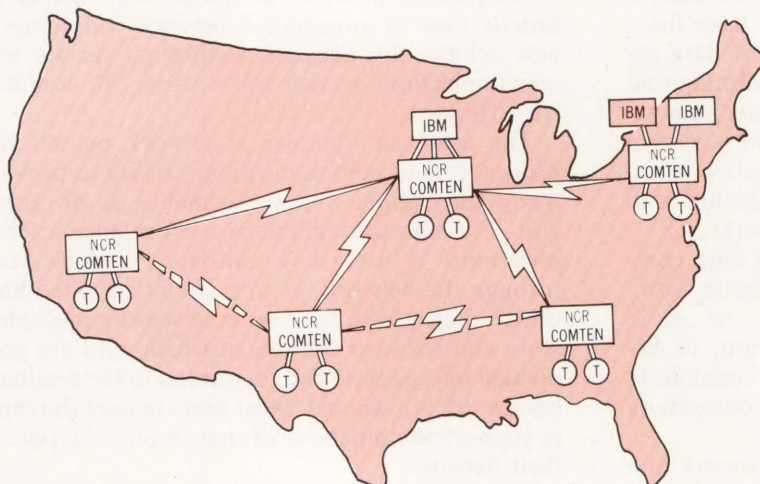


Fig 1 Role of concentrator in network. Software assigns trunk bandwidth only when needed, optimizing throughput. Terminals (T) can access host application software anywhere in network. Broken lines indicate switched circuits

joining their ranks as declining hardware costs, growing software sophistication, and increasing availability of telecommunications facilities stimulate the growth of data communications networks.

Less expensive remote concentrators have emerged to satisfy this user base, reducing communications cost while offering sophisticated features. One example is the 3400 link processor system (LPS), which offers remote concentration functions. The system consists of a link controller (3401 LC) and one or more 3410 link processors (LPs). The 3401 LC co-resides with the 3600 communications system, and presents data received from 3410 LPs to the 3600 system software in a transparent manner. Because the 3401 LC is integrated with the 3600 communications system, it requires less hardware than a separate multiplexer system. Residing at a remote location, the 3410 LP gathers data together from terminals and clusters to transmit to the 3401 LC (Fig 2). The 3410 can support up to 31 lines.

Despite the decreased cost, users of lower end systems such as the 3400 LPS still benefit from most of the functions and capabilities offered by remote concentration software, such as CNS. The 3400 LPS, for example, significantly reduces users' communication costs by multiplexing data from remote clusters and terminals over shared trunk facilities to the 3600 communications system, and by compressing data on the trunks to reduce the number of characters that are transmitted. In addition, the use of bit oriented protocols on the 3400 LPS trunks provides increased reliability and error correction, particularly for start/stop or binary synchronous terminals.

The 3400 LPS supports start/stop, binary synchronous, and synchronous data link control (SDLC) communications protocols on both switched and leased facilities. For switched circuits, the 3400 LPS supports remote auto dial and auto answer. For remote auto dial, each autodial line requires a standard automatic calling unit (ACU), but the autocall adapter function is performed within 3410 software. For start/stop terminals, automatic baud rate detection allows multiple terminal types and speeds to share the same access ports.

With the increasing prevalence of distributed data processing and growing complexity of data communications networks, remote concentrators have become more sophisticated. Not only large system users, but also a growing number of smaller system users who implement data communications networks will profit from this sophistication.

Although the high cost of communications networks once restricted their critical applications to a limited number of users, communications networks, like home computers, now appear in growing numbers, and are employed in a variety of applications. Also increasing is the number of common carrier facilities and the proliferation of terminals and terminal types. All of these factors contribute to the demand for remote concentration.

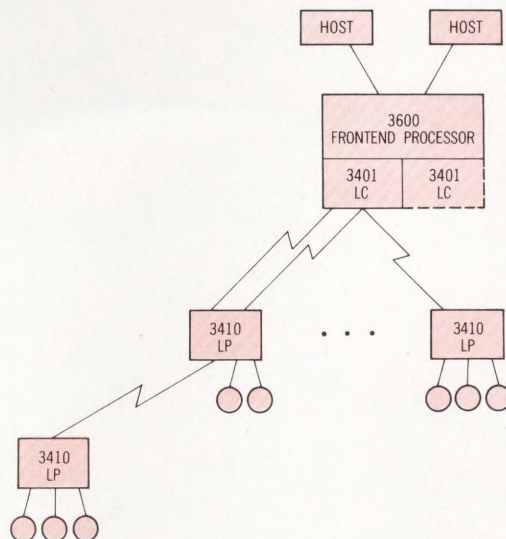


Fig 2 Typical link processor configuration. Integrated within 3600 communications system, link controller (LC) connects one or more link processors with frontend processor. Link processor (LP) at remote location gathers data from terminals and clusters

The challenge, therefore, is not simply to meet a growing demand and produce an adequate supply of remote concentrators. The challenge is to provide concentrators that are sophisticated yet cost-effective enough to meet the users' needs in the increasingly complex world of data communications. **CD**

Ronald M. Groenke, as NCR Comten vice president of systems development, defines long term product strategies and concepts. Previously responsible for communications networking system hardware and software development, Mr Groenke holds a BS in mathematics from the University of Minnesota. His interests include software design, simulation modeling, optimum data communications techniques, and the integration of voice, data image, and text.

Director of communications architecture at NCR Comten, Craig M. Johnson defines and maintains communications network architecture (CNA) as the management and technical communications plan for NCR products. Mr Johnson holds a BS in mathematics from the University of Minnesota. Data communications, particularly distributed data processing, is his major field of interest.

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PLUG-IN ROM CUSTOMIZES NETWORK TESTER TO SPECIFIC INSTALLATION

A ROM pack that tailors a system to a particular data communications network reduces the need for intricate setup procedures, complex data displays, or complicated operating procedures

Wendell Damm
David Bennett

Tektronix, Incorporated
PO Box 1700, Beaverton, OR 97077

Within the next five years, as devices are supplied by hundreds of different vendors and appear in data communications networks, the installed base for these devices could grow from a few million to more than 10 million. Coupled with the growth of multivendor networks, this nearly threefold increase in the installed base of equipment will create network maintenance problems that current service policies do not adequately address. Network service managers and network equipment suppliers will require test equipment specifically designed for use in data communications networks, equipment that can be tailored to the characteristics of individual networks and of specific equipment within networks. A primary task for this test equipment will be to isolate the faulty equipment in a network that is down. The test equipment's sophisticated analysis of network operation and interpretation of test results must be automated to eliminate the need for extensive technician training involving complex operating procedures, front panel display formats, and instrument readouts.

Suppose that on a typical morning, the service manager for a data communications network answers the telephone to learn that a terminal operator has encountered a problem. The terminal is acting peculiarly and seemingly needs to be repaired. After asking the appropriate questions and obtaining as much information pertaining to the failure as possible, the service manager must make an educated guess as to how to proceed. Symptomatically, this particular terminal operates

properly for a period of time, then requires several minutes for a screen update. Checking with other terminal operators, it is determined that other terminals in the area have experienced similar problems, but the operators either have not been inconvenienced to the point of reporting the difficulty or have not known whom to call.

The service manager consults a network map to identify equipment that might be involved in the failure (Fig 1). This particular site has a multiterminal cluster, and the problem appears to have affected all of the terminals in the cluster. A 9600-baud leased telephone line connects the cluster to a mainframe computer. The terminals are compatible with the computer although they were manufactured by a different company. The modems, advertised as being fully compatible, are manufactured by yet another company. Because it seems highly unlikely that all terminals in the cluster would experience identical hardware problems at the same time, it seems obvious that the problem lies with one or more pieces of the shared communications equipment.

Being relatively certain that the problem involves equipment supplied by one of the vendors, the service manager must now convince the vendor that the problem involves his equipment. A test device tailored to this particular network configuration would be useful for providing a third party determination of which equipment is at fault, test equipment that would allow

the service manager to contact the appropriate vendor on his first call and lend credibility to the report of trouble.

Without test equipment tailored to the particular network configuration, a classic example of circular finger pointing will most likely occur. A few telephone calls establish that each of the vendors agrees to the existence of a problem. However, the mainframe company categorically denies making recent software changes that could affect terminal operation. The telephone company assures the service manager that the line was perfectly good yesterday and is therefore still good today. According to the modem vendor, appropriate lights are lit to indicate that the modems are operating properly. The network service manager, whose main concern is getting the network back into service, must request that a service technician from each of the vendors involved visit the site to determine if that company's equipment is the cause of the problem. Without suitable test equipment, he can only guess which vendor to call first. If he is lucky, he may contact the correct company the first time; more likely, one or more unnecessary service calls will be made before the correct company is ascertained.

Further complicating this typical present day problem are several factors that will require the evaluation and possible change of service philosophy over the next few years. These factors include the rising cost of downtime, the increase in software and hardware interaction, the expansion of the product base, and the

problem of building the technicians' skill level as rapidly as the growth in complexity of the products.

Equipment downtime can be extremely expensive and frustrating for those who depend on data communications networks. A failure in a critical portion of the system can dramatically upset day to day operations, idling expensive equipment and personnel. The service manager must react quickly and positively to a failure report. Increasing hardware and software interaction further complicates the service strategy. A seemingly minor software change can propagate through an entire system, eventually affecting data communications. Moreover, the new software might run for weeks or months before an error propagates to the point that a problem becomes apparent. This time lapse further obscures its true cause, frustrating repair efforts. With the number of terminals and sites likely to double over the next two years, and adequate support of systems presently straining every service manager's resources, the primary concern over support for new data communications requirements is people. Skilled technicians are seemingly being trained as rapidly as possible and yet are still in short supply. A much larger equipment base will be correspondingly more difficult to support in just a few years.

Although traditional test equipment will not be able to solve these problems by the end of this century, when there could be as many terminals as workers in the United States, test equipment is presently evolving to permit the isolation of the faulty network components by technicians who have not had to learn complicated instrument setup and operating routines and who need not be able to interpret complex displays of data.

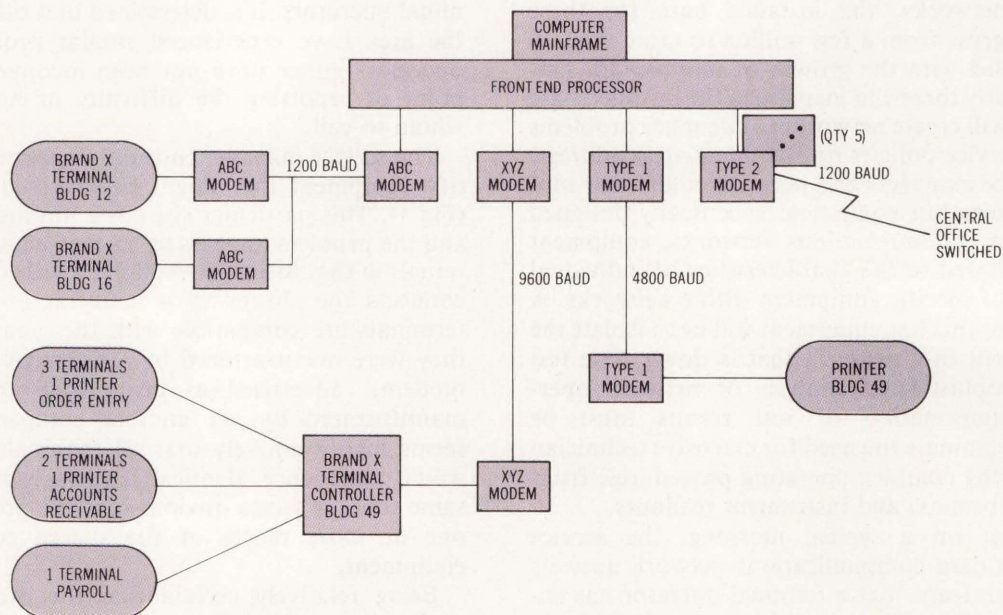


Fig 1 Partial network map. Clusters of terminals manufactured by one vendor connect to mainframe from second vendor through modems supplied by one or more additional

vendors. Service manager consults network map to determine which equipment might be involved in failure

CD DATACOMM

Designed for use in data communications networks, this new test equipment could increase the productivity of maintenance personnel. It must include monitoring capabilities to diagnose software and protocol problems, bit error rate testing to isolate communications link problems, and simulation capabilities to exercise terminals and other peripherals offline (Fig 2). Moreover, this test equipment must be lightweight and portable enough so that technicians will be able to carry it to the site, and it should be priced reasonably enough to make broad distribution economical.

With access to one such piece of test equipment currently available, the Tektronix 834 Programmable Data Communications Tester, our service manager would be able to send a service technician to the problem site to identify the faulty equipment. Once at the site, the technician would begin by monitoring the data link. The tester would first be connected to monitor activity on the line, to capture data without affecting data transmission. Examining the data for polls and selects addressed to the controller, the technician would determine that the controller is being polled at a reasonable rate and is being selected, and that the data are being transferred. Using the tester to verify the block check characters in the data would reveal that the data blocks do not contain errors at this point in the network. The technician would also be able to observe that there are periods in which bursts of negative acknowledgment characters originate in the host.

Next, the common control equipment for the terminals would be exercised by simulating the mainframe in normal operation. Before disconnecting any equipment, the technician would inform site management and the computer operator. Then, disconnecting the terminal cluster controller from the modem, the technician would connect the tester to simulate the modem. The terminals would be exercised with polls and data transfers using a simulation routine in the tester that would be customized for the installation. The simulation exercise would include polling and selecting each terminal, setting up various displays, and verifying that the cluster controller and all terminals are operating correctly. It could also include normal operational tests as well as tests to verify the proper response to abnormal conditions.

Once this phase of testing demonstrated that the terminal equipment is operating properly, the technician would prepare to test the data link by connecting the mainframe end modem in a digital loopback configuration. The bit error rate test used to exercise the link is a repetitive pseudorandom pattern that runs either for a specified number of bits or for a specified duration. The number of bit errors and 1000-bit blocks that have errors would be recorded in the tester. As bit rate error tests have become standardized, modem manufacturers and telephone companies will accept their results as evidence of the condition of modems or data lines. A high ratio of bit errors to block errors would indicate an intermittent problem with the data link that would affect several blocks of data.

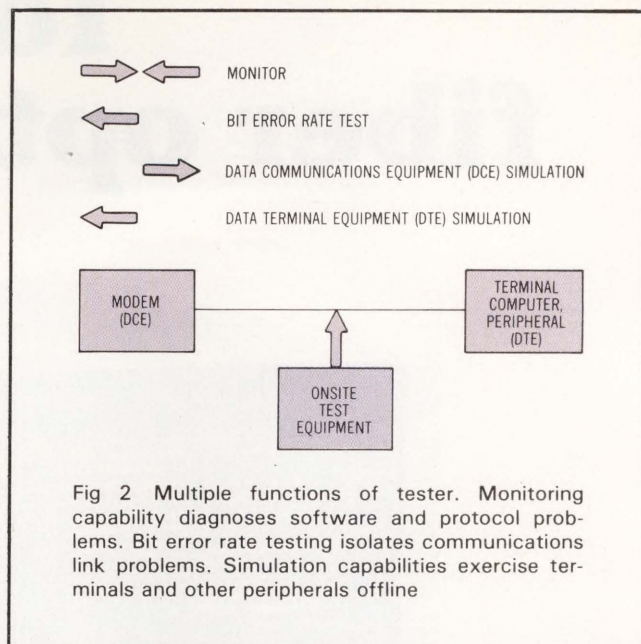


Fig 2 Multiple functions of tester. Monitoring capability diagnoses software and protocol problems. Bit error rate testing isolates communications link problems. Simulation capabilities exercise terminals and other peripherals offline

The technician would next connect the mainframe end modem in analog loopback configuration and repeat the bit error rate test. If no errors are detected, the problem would be isolated to the host modem. When the host modem is replaced, the link would return to normal operation and the terminals would operate properly.

All instrument setup procedures and test program functions just described and customized for a specific network installation can be stored in a plug-in read only memory pack that can be inserted easily into the back of the tester. This read only memory pack will tailor the tester to the service technician's particular tasks. Because only a few buttons need to be operated before the instrument can analyze the network, determine which is the faulty element, and display these test results, technicians will require relatively little training on test instrument operation or on the network configuration before they can isolate faulty network elements.

CD

For the past two years, Wendell Damm has been project manager for the Tektronix 834 Programmable Data Communications Tester and the 833 Data Comm Tester. Prior to that, he held several different engineering design and management positions. Wendell received his BSEE from the University of Nebraska.

David Bennett is a software designer in the Service Instruments Division at Tektronix, Inc. Having recently completed the realtime data acquisition and simulation software for the 834 Programmable Data Communications Tester, he is currently developing application ROM packs for specific protocols which will expand the 834's capabilities. He holds a BSEE from Oregon State University.

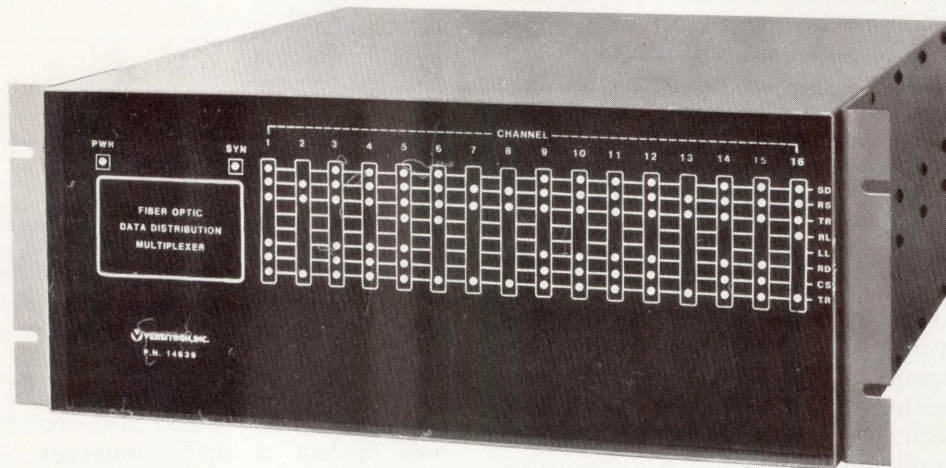
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Total fiber optic system



Versitron's new fiber optic data distribution system provides all of the features of fiber optic transmission while maintaining a cost effective edge over a conventional hardwire unit. The system provides a direct full duplex link to the CPU port for 16 terminals from several different locations — all over a single fiber optic cable pair!

Multi-Drop Multiplexers The heart of the system is Versitron's new multi-drop multiplexer. This equipment consists of a central unit, located at the CPU, and several remote units located throughout the local distribution network. The central unit operates as a conventional time division multiplexer; providing an aggregate (16 channel) interface to the local distribution network over a fiber optic cable pair, and 16 EIA interface parallel data channels to the CPU. Each of the remote units is assigned a number of channels. Each unit continuously adds its assigned channels into the proper time slots on the transmit aggregate signal and withdraws the channel data from the receive aggregate signal. Once the parallel data is recovered it may be brought through an EIA

handles
16
channels
of
local
distribution
data

connector directly to the terminal; or, for terminals located some distance away, through a separate parallel data fiber optic link.

Flexible Configuration The exact system configuration — the number of remote units and the number of channels/unit — is totally dependent on the individual site requirements. Additionally, the system configuration may be changed at any time simply by swapping circuit cards.

The system is designed to operate with any combination of synchronous or asynchronous terminals up to a maximum of 19.2 kbps for synchronous or 9600 baud for asynchronous. The built-in diagnostics include the ability of the central unit to command a remote channel loop-back without affecting traffic on the remaining channels and a complete front panel status display.

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Gayton H. B. Yancy

Raytheon Data Systems Company

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Transmission equipment connects the telephone switching equipment interfaces located in geographically dispersed central offices, establishing transmission paths called trunks between these offices. Signals traversing the trunks are derived from local connections to end user telephone voice circuits [Fig 1(a)]. Efficient, high quality digital transmission of analog voice circuit signals requires implementation of two distinct processes at the ends of the trunk. One process converts the analog voice signal into a digital pulse stream at the trunk transmitting end and then converts the pulse stream back to its original analog representation at the receiving end. Superimposed upon this process, another process multiplexes parallel digitized voice data streams into higher bit rate serialized pulse trains before transmission along the trunk and demultiplexes the serial pulse trains back to the original parallel streams after reception at the end of the transmission path.

When implemented for commercial telephone service in North America, these processes must conform to a data rate hierarchy and a set of encoding techniques established by the Bell System. Data rates required for compatibility with Bell System digital transmission networks are

DS1	1.544M bits/s
DS1C	3.152M bits/s
DS2	6.312M bits/s
DS3	44.736M bits/s
DS4	274.176M bits/s

The DS1 rate of 1.544M bits/s contains 24 interleaved digitized voice circuits in addition to overhead bits that aid in demultiplexing. DS1 and DS1C (3.152M bits/s with 48 voice circuits) are the first levels in the Bell System data rate hierarchy and are used for low, medium, and high density trunking applications. Of the remaining three levels in this hierarchy, only the fourth level, DS3, at 44.736M bits/s and a voice circuit capacity of 672 is used extensively. DS2 (6.312M bits/s with 96 voice circuits) and DS4 (274M bits/s with 4032 voice circuits), the third and fifth levels respectively, are infrequently used and will not be discussed further here.

Equipment used to achieve the transformation from analog voice signals to the DS1 and DS3 levels (and back) include the T1 channel bank and the M13 multiplexer. Circuitry in the channel bank samples the amplitude of each 4-kHz bandwidth voice circuit at an 8-kHz rate and encodes each sample with eight pulses. This sampling and encoding results in a 64k-bit/s data stream for each digitized voice circuit. Multiplexer circuitry in the channel bank serializes 24 of the digitized voice outputs into a 1.544M-bit/s DS1 signal. The M13 multiplexer serializes a maximum of 28 DS1 signals into a 44.736M-bit/s DS3 signal. (The output rate and format of this multiplexer remain unchanged if fewer than 28 DS1 signals are supplied as input.) DS1 and DS3 signal formats contain specific overhead framing bits to permit demultiplexing from DS3 to DS1 and from DS1 to 64k bits/s at the trunk receiving end. Transmission facilities operating at the

DS1, DS1C, and DS3 signal rates are designated as T1, T1C, and T3 transmission systems, respectively. In addition to the transmission facilities mentioned previously, T3C systems which operate at 90M bits/s and provide two standard DS3 signal interfaces are used to provide higher voice circuit capacity (1344) at lower cost.

Alternate Technology for Digital Telephone Transmission

High density digital trunks can often accommodate more than 1000 simultaneous conversations and are

now implemented with copper wire cable span line systems [Fig 1(b)] and microwave radio systems. Digital microwave radio systems are often used in locations with sufficient carrier frequencies to service the required traffic, particularly in rural and suburban areas where central offices are separated by ten miles or more and the terrain traversed by the trunk is rocky or otherwise unsuitable for cable installation. Copper wire cable span line systems have been used extensively in densely populated metropolitan areas to interconnect central offices that are typically less than four miles apart. In addition, these systems have been used in digital microwave radio trunking applications as entrance links that connect central offices in their downtown locations to a remote radio site. In many entrance link applications, fiber optic cable systems are now less costly than

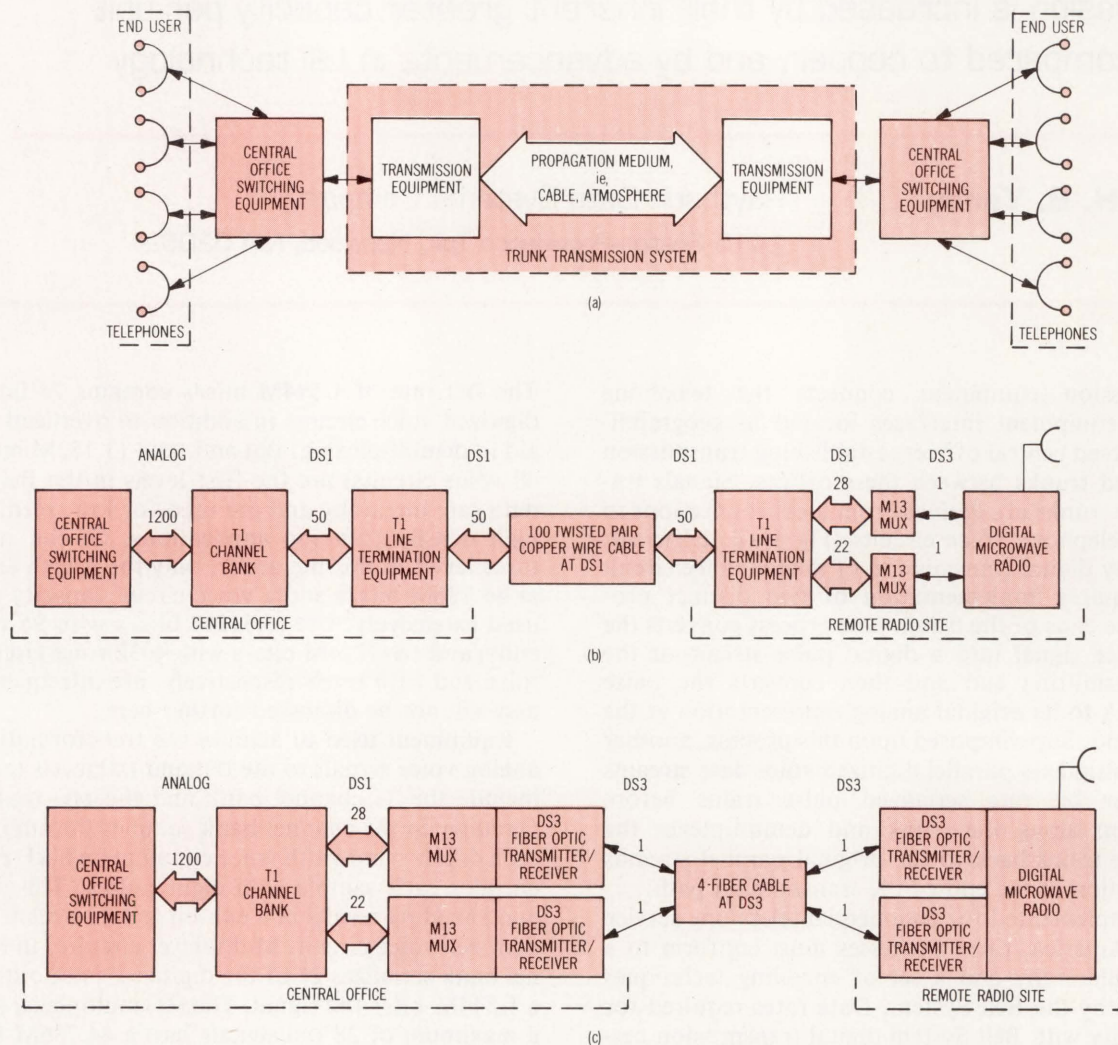


Fig 1 Telephone digital trunk architecture. In (a), conventional transmission system connects central offices via copper cable or microwave; in (b), copper cable entrance link to microwave facility handles

1200 voice channels; and in (c), similar entrance link can multiplex 1200 voice channels in two stages using only four fiber optic cables

copper wire cable span line systems [Fig 1(c)]. Since the amount of duct space required by a fiber optic cable is considerably less than that required by a copper wire cable of equivalent transmission capability, fiber optic systems also provide a cost-effective means of expanding trunk capacity in metropolitan areas with limited cable duct space. In time, as fiber optic cable and component costs decrease, this technology will cost less than copper wire cable span lines in most if not all applications.

All telephone digital transmission systems contain transmitting electronics, a propagation medium, receiving electronics, time division multiplexing electronics, protection switching electronics, and maintenance electronics. Each of these subsystems is characterized by span lengths that are determined by (a) the system gain and bandwidth achieved by the transmitting and receiving electronics, and (b) the attenuation and bandwidth properties of the propagation medium. In those instances where trunk span lengths exceed the maximum span length for the selected transmission system, regenerative repeater circuitry used at transmission system span intervals achieves end to end transmission. The table compares alternate technology high density trunking system performance characteristics.

Apart from mandated performance requirements, transmission facilities are often required to have path availabilities exceeding 99.9999% (path downtime of less than 32 seconds per year). To meet these availability criteria, transmission equipment configurations contain 1:1 and 1:N automatic protection switching equipment and redundant transmission electronics (Fig 2). Since maintaining a ratio of 1:1 between transmission and protection electronics is expensive in terms of initial price and manpower required to maintain both sets of electronics, 1:N configurations are used to reduce redundant circuitry quantity and therefore to provide the required transmission system availability at reasonable cost.

Mean time to restore requirements of ten minutes for transmission facility standalone equipment dictates extensive built-in test, self-monitoring, and diagnostic capabilities that must be designed into trunk hardware. As a result, terminals have maintenance panels and local alarm lights for plug-in assemblies. To minimize the

mean time to repair these systems, each terminal includes a remote fault alarm interface. In some DS3 fiber optic systems, these interfaces permit remoting terminal operation status and fault status to a centralized maintenance location by means of copper wire pairs which, in some instances, are incorporated into the fiber optic cable. In other systems such as the 90M-bit/s equipment, overhead service channel bits in the transmitted signal carry remote fault alarm and maintenance voice circuit information. In each of these examples, excess travel time for the repair of system malfunctions is reduced, since the remoting of the alarms provides a means of determining the most probable site at which the fault has occurred.

Basic Elements of a Fiber Optic Transmission System

Basic elements that constitute a fiber optic transmission system are a fiber optic cable, a fiber optic transmitter, a fiber optic receiver, transmission rate multiplexing electronics, protection switching electronics, and maintenance electronics. Fiber optic cables allow duct, aerial, and buried installation. The two basic fiber (light waveguide) constructions permit either single-mode propagation or multimode propagation. Single-mode light waveguide has an extremely small fiber diameter which approximates the light wavelength and permits only one mode of propagation. This presents difficulties in coupling light into the fiber and in performing splicing operations, a consideration that precludes the use of single-mode fiber optic cable in most applications, despite its superior bandwidth characteristics. Multimode light waveguide has a larger fiber diameter and permits propagation not only of a fundamental mode, which travels down the center of the fiber, but also of additional modes resulting from internal reflection paths. Since the transit times for these modes will differ, pulse spreading occurs as the light travels along the optical guide.

To minimize modal dispersion, fibers are constructed with a controlled, parabolically shaped index of refraction cross-sectional contour. Such graded index fibers allow the light ray propagation velocity to increase as the length of the internal reflection transmission path increases. Fig 3 depicts multimode propagation and the parabolically shaped index of refraction contour that tends to equalize mode transit times. Fig 4 shows a

High Density Digital Trunking Alternate Technology
Performance Comparison

Technology Description	Facility Designation	Data Rate	Propagation Medium	Span Length
Copper span line	T1	1.544M bits/s	Copper wire	2 km
Fiber optic system	T3C	90.148M bits/s	Glass fiber	10 km
Microwave radio	T3C	90.148M bits/s	Atmosphere	30 km

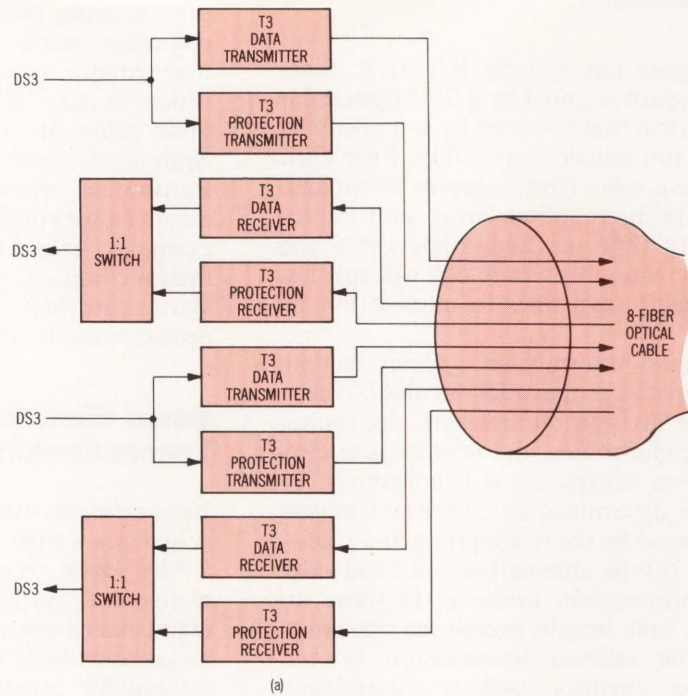
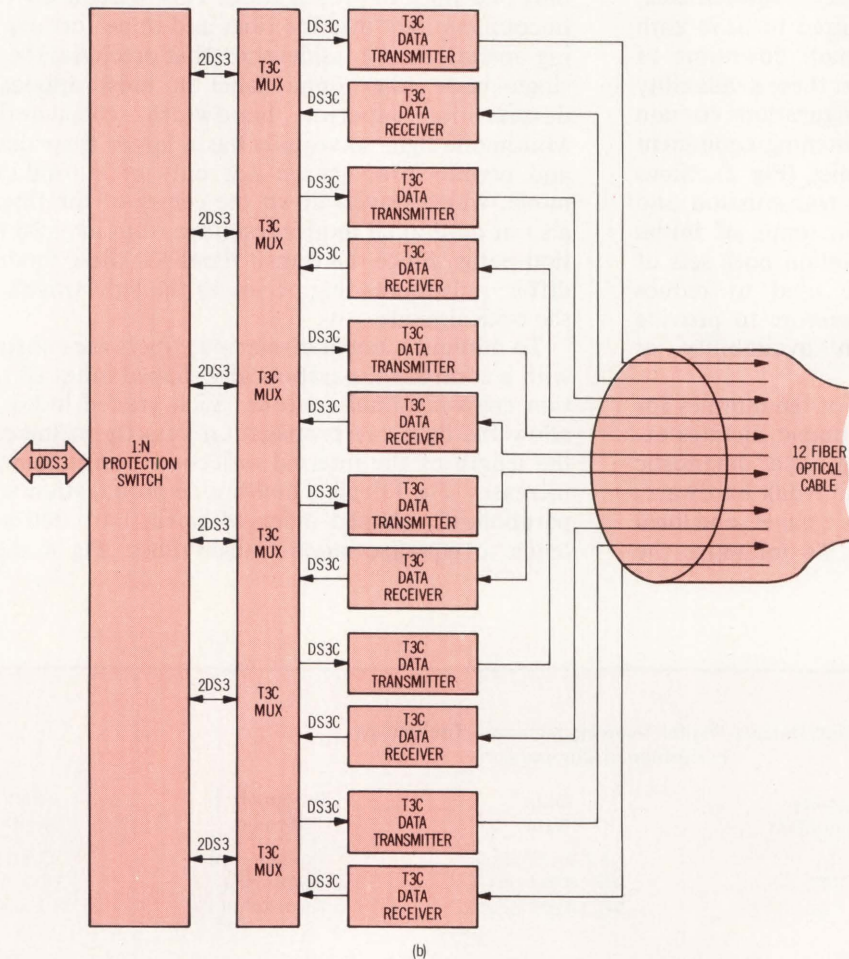


Fig 2 Automatic protection switching equipment. In (a), fully redundant transmission electronics help meet 99.9999% availability requirement. To reduce initial price and ongoing maintenance costs, configuration in (b) relies on automatic protection switching to provide comparable system availability using 1:N redundancy



typical general purpose multimode cable that features a buffered steel core member for strength and six fibers in loose fitting halar buffer jackets. Wrapped around the buffer jackets are a binding material, a layer of kevlar for crush resistance, and a polyurethane outer jacket. Commonly employed options and additions to this construction are dielectric core strength members, armor for rodent proofing, and a polyurethane gel to fill in the fiber buffer jackets. The last option is important in installations that are subject to freezing temperatures because the gel filling excludes moisture and the formation of ice, which would mechanically stress the fiber and alter its transmission characteristics.

Fiber optic transmitters use injection laser and light emitting diodes as light sources. For high performance digital telecommunications systems operating at the DS3 rate and above, the injection laser diode is preferred because it makes superior use of fiber optic cable transmission properties and provides a more concentrated light output, hence higher transmission coupling efficiency to the fiber. Moreover, an injection laser diode has a high degree of spectral purity, minimizing the effect of waveform spreading caused by material dispersion in the fiber on data recovery.

Fiber optic transmitters also contain emitter coupled logic drive circuitry for high speed modulation of the laser source, monitoring and control circuitry to maintain the proper relationship between laser drive current and optical power output, and randomization circuitry to ensure clock recovery at the receive end of the fiber span. Fiber optic receivers use either PIN or avalanche photodiodes as light detectors. Avalanche photodiodes offer threshold levels up to 20 dB better than PIN photodiodes and are therefore used in high performance systems. Transimpedance amplifier circuitry is used to raise the photodiode current output to voltage levels required by the emitter coupled logic hardware, whereas clock recovery and derandomization circuitry are used to provide the final received data output. Both injection laser diodes and avalanche photodiodes are commercially available from multiple sources.

Performance of Current Fiber Optic Systems

Data rates of 400M bits/s (Japan) and 322M bits/s (Canada) have been achieved in systems that have been installed and are operational. Since the required cable bandwidth is proportional to the system data rate span length product, higher data rates require higher cable bandwidths for equal span lengths. At data rates above 100M bits/s, achievable cable bandwidths dominate system design constraints since, at these data rates, systems are more limited by dispersion than they are by attenuation. For systems using data rates below 100M bits/s, cable attenuation is the most significant parameter limiting span length. Attenuation is specified in terms of decibels per kilometer and varies linearly

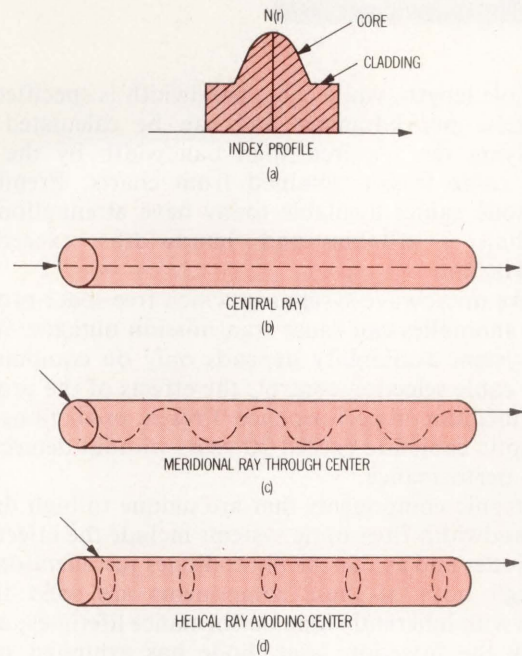


Fig 3 Multimode propagation paths. Parabolic index of refraction profile equalizes transit times to prevent dispersion and allows alternate internal reflection paths

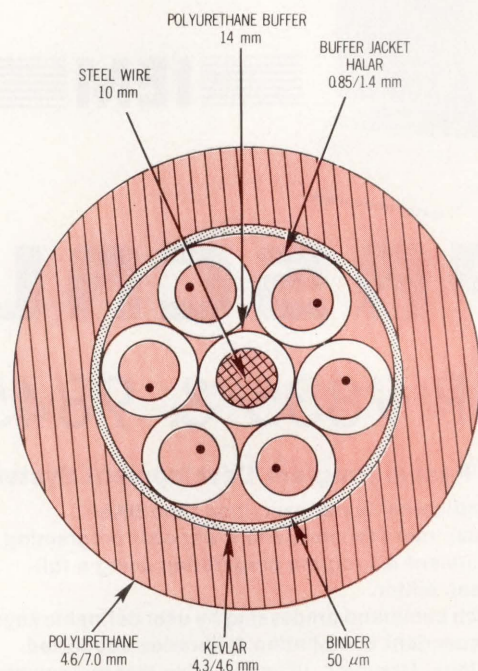


Fig 4 Typical fiber optic cable. Cross section of general purpose cable shows six jacketed optic fibers with other protecting and binding materials that resist crushing, icing, and mechanical damage

with cable length, while cable bandwidth is specified in megaHertz per kilometer and can be calculated by multiplying the required span bandwidth by the effective cable length obtained from charts. Premium multimode cables available today have attenuation of less than 3 dB/km and bandwidths exceeding 800 MHz/km.

Unlike microwave systems in which free space propagation anomalies can cause transmission outages, fiber optic system availability depends only on equipment; proper cable selection controls the effects of the propagation medium on performance. Present predictions for fiber optic cable life exceed 20 years without deterioration in performance.

Electronic components that are unique to high data, high bandwidth fiber optic systems include the injection laser diodes and avalanche photodiodes just mentioned. Although both of these components are solid state devices with inherently long performance lifetimes, until recently the injection laser diode has exhibited poor lifetime performance due to poor heat dissipation. Present measured lifetimes on individual devices are in the tens of thousands of hours with predictions (based on accelerated lifetime tests in the laboratory) of hundreds of thousands of hours. Conservative designs use ther-

moelectric cooling devices to control injection laser diode junction temperatures; however, increased availability can be obtained by incorporating automatically switched redundant protection circuitry into the system design.

System transmission quality standards are expressed in terms of bit error rate. The Bell System has established a fiber optic system bit error rate standard of 10^{-10} (ie, a maximum of 1 bit error for every 10G bits transmitted). Such performance is determined by the transmitter optical power coupled into the fiber, the optical detector receiver threshold, the cable attenuation, and the cable bandwidth.

Conclusions

The future of fiber optic systems in high density digital telephone trunks is quite bright. All new and replacement high density digital transmission cable systems may eventually be implemented using fiber optic technology because of the greater capacity in less physical space at a potentially lower cost. When this lower cost potential will be fully realized is a matter of conjecture, but there are encouraging trends. Unlike that of copper cable, the price of fiber optic cable is declining. Similarly, as large scale integration technology matures, the cost of the multiplexing electronics required to take full advantage of fiber optic transmission will also decline. Fiber optic technology is not simply a fad but is in fact a revolutionary advancement in data processing and communications electronics. Practical, economically viable systems exist today for many high density digital trunking applications. In the future, this technology will not only meet presently conceived applications but will undoubtedly stimulate the generation of additional applications and application concepts. **CD**

This article is based on an earlier article entitled "Fiber Optic Digital Telecommunications Systems," which appeared in the Raytheon publication *Electronic Progress*, vol xxii, no 1, Spring 1980.

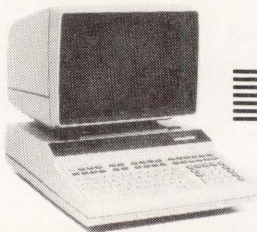
Since 1977, Gayton H. B. Yancy has worked for the telecommunications product line at Raytheon Data Systems as wideband digital systems program manager, government marketing manager, and fiber optic product manager. He received a BS and a BA in physics from Brown University and is a graduate of the Raytheon Engineering Management Program.

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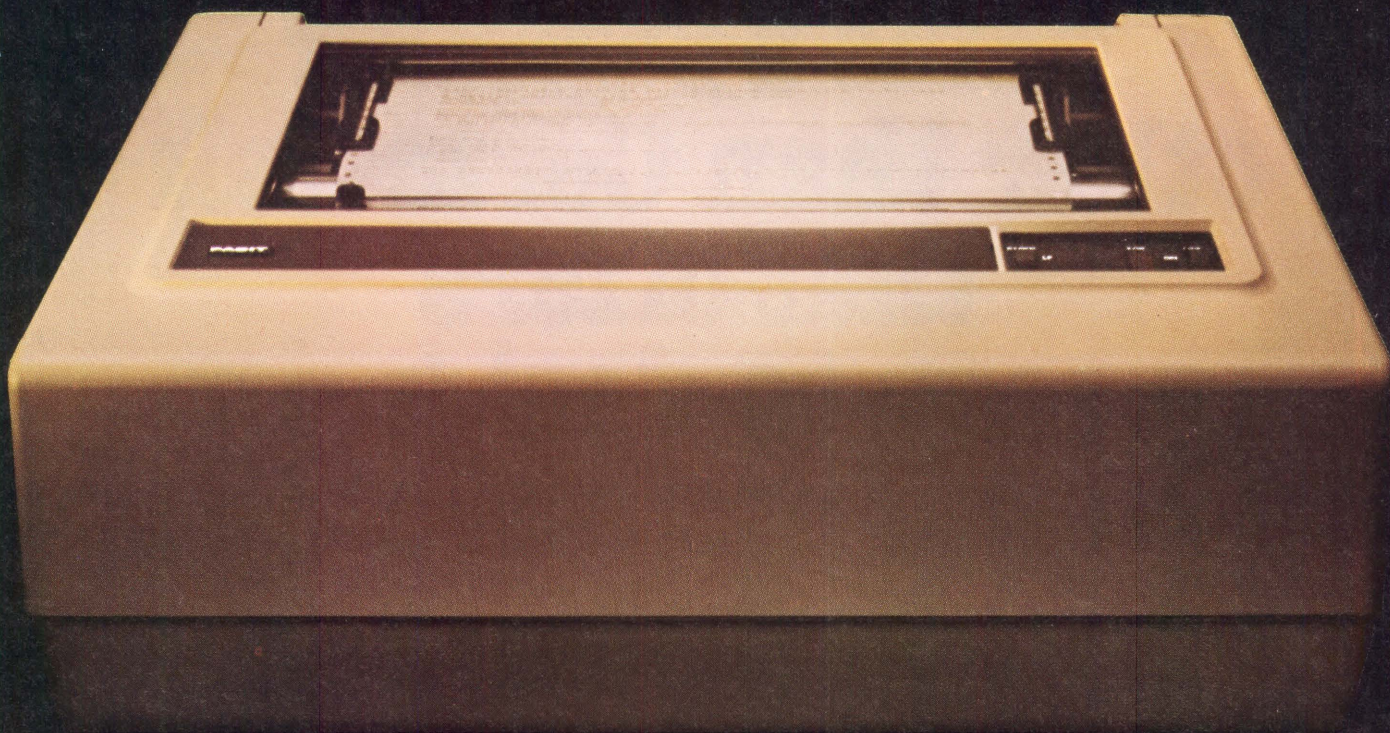
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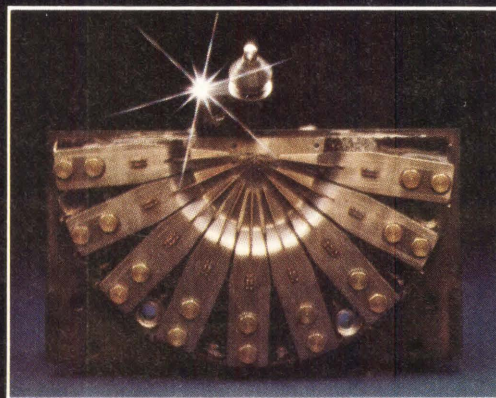
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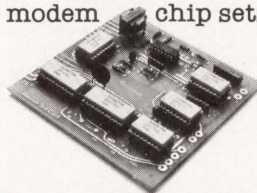
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DUAL-SPEED ALTERNATE VOICE/DATA MODEM REDUCES SUPPORT REQUIREMENTS

Fulfillment of unusual transmission requirements through use of dual-speed alternate voice/data modem achieves a remote diagnosis and support capability and reduces the number of service calls

Christopher A. Cox

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6 Shattuck Rd, Andover, MA 01810

As minicomputers and small business systems decline in cost and become easier to use, they are being installed by companies that have never before owned computers. Once these entry level users become familiar with their equipment, they often add a communications capability to exchange data with other locations. Of course, as with larger mainframes, small systems require support in such areas as maintenance, diagnostics, and software. Original equipment manufacturers and systems houses, who usually sell and support these small systems, often have only a limited staff for onsite customer support; therefore, onsite help for end users is often spotty, despite the fact that entry level customers need extensive help in the period immediately following installation of new equipment as well as when system malfunctions occur. To provide this support, systems houses require a means to serve their customers while operating within limited budgets. Because extensive site visits by field support representatives are cost-prohibitive, an attractive alternative incorporates the communications capabilities frequently added to entry level systems, by using the automatic voice/data FCC registered, dial line modems to link a central support site to the remote

users. In addition, these modems are used to debug and quickly update application software. User software is analyzed and corrected by centrally based experts. And, although relatively slow, complete programs can be downline loaded for less than the cost of an onsite visit.

Use of a communications link for customer support presents unusual transmission requirements. Relatively small amounts of data, consisting primarily of requests for system status information or detailed operating statistics, pass from the diagnostic site to the user location. Most data transmitted from the support center to the equipment site, however limited in volume, elicit a much larger and more detailed reply that must be transmitted in the opposite direction, from the user site back to the support center.

Since video terminals are common features at both central support sites and remote user locations, they are used to handle the diagnostic probes and resulting data replies. Because they display the test data, the transmission speed inbound to the diagnostic center must be fast enough to move a significant volume of information in a short time. Furthermore, the diagnostic center must service multiple users; therefore, individual customer

sessions must be of limited duration. Setting the higher, inbound data speed at 2400 bits/s represents the optimum tradeoff between data transmission rate and modem hardware cost (Fig 1).

At 150 bits/s, the lower outbound transmission speed is sufficient to handle keyboard entries from the diagnostic center and reflects an established rate in existing split speed modems that use the slower reverse channel capability for testing. Use of established designs reduces engineering costs, and the 150-bit/s rate suffices to transmit the relatively short test commands and data requests outward from the diagnostic center.

Apart from split speed operation, voice coordination before and after the transmission of system data is always desirable. A voice interchange can initiate communication for purposes such as defining a system problem and requesting user assistance, troubleshooting, or downline loading of software upgrades. With voice interchange, calls are typically initiated via conventional dial-up and voice procedures. The interchange that initiates the call is then interrupted for periods of data transmission, and after each of these, voice mode is again established.

Only at infrequent intervals is it necessary to establish communication between an equipment site and the diagnostic center. For this reason, and because the support center must service a maximum number of user sites, privately leased telephone lines and the computer data ports they tie up would prove far too costly. This leaves dial-up telephone lines as the best communications option. Also, because entry level users tend to have a limited number of dial-up lines, alternating voice and data mode within a single interchange avoids the need for two separate communications links (Fig 2). An FCC registered modem with telephone company jacks makes user installation easy and eliminates direct access arrangements.

Alternate voice/data capability has been implemented before in modems, but the earlier versions included only manual switches that simultaneously had to be set to the

required mode by operators at each end of the link. Automatic switching from voice mode to data mode and back introduces some unusual features into the unit. Once a call is initiated, the modem pair operates in its normal, voice mode. Then, when an operator at one end of a link keys a command into the terminal, signals transmitted to the distant modem effect the switch to data mode before the digital signals are received. Once a data transmission is complete, the sending modem generates a soft carrier tone to prevent extraneous characters from being received at the remote end, ensuring an error free transition from data mode back to voice mode. This automatic switching provides easy to use and reliable alternate voice and data transmissions.

As with other modems, the alternate voice/data units must be used in pairs; however, because of the dual-speed capability, only complementary units can operate together. In other words, a 2400-bit/s transmitter and a 150-bit/s receiver can operate only with a 2400-bit/s receiver and a 150-bit/s transmitter at the other end of the data link. The higher speed transmission uses serial synchronous mode, while the lower speed transmission uses serial asynchronous mode. In effect, two complete modem pairs are operating over a single link with full-duplex capability.

Since conventional loopback testing is not possible because of the different data speeds being used, the unit includes manual test sequences during which either transmit or receive mode can be monitored by the introduction of separate test patterns. Both data sets in an operating pair have a 7-position audio monitor switch for testing. This switch is used to select the source to be monitored by telephone.

Although designed for the specific dial-up diagnostic application, features of the alternate voice/data modem suggest that it can be adapted for other uses with relatively minor modifications. From a design standpoint, the dual data speeds could be changed to other data rates without significant problems. Moreover, the device could be adapted for use on private lines where alternate voice/data mode is indicated. Split speed communications links should also grow in importance as designers explore ways to get more efficient use out of existing facilities. Certain applications have operating

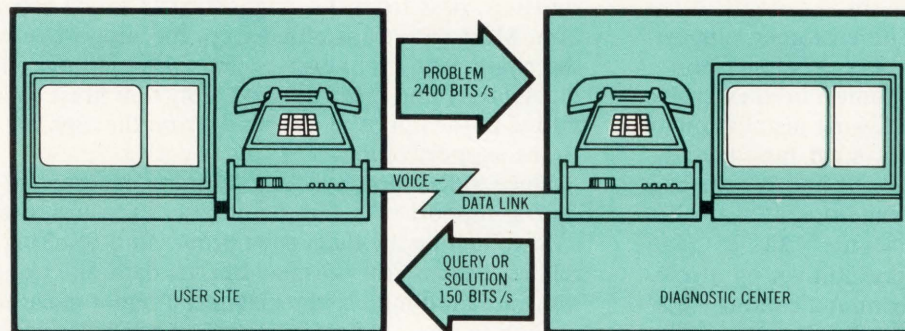


Fig 1 Split speed operation aids diagnosis. Only small quantities of data originate at diagnostic center; however, these can be inquiries that typically require much larger transmissions in response

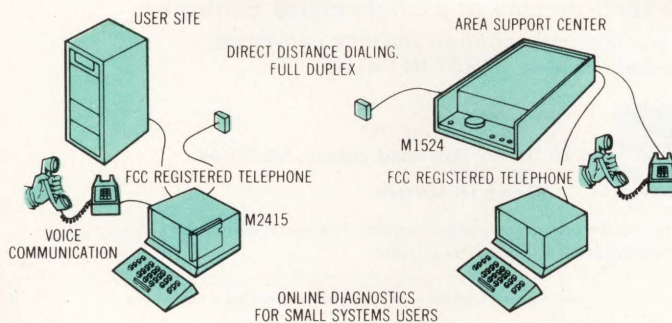


Fig 2 Alternate voice/data operation simplifies interaction. Used in complementary pairs, 2400-bit/s transmitter and 150-bit/s receiver communicate with 2400-bit/s receiver and 150-bit/s transmitter, achieving two complete modems in full-duplex operation

patterns that lend themselves to dual-speed operation, some of which are in emerging telecommunications areas where the capabilities of the alternate voice/data modem may help to accelerate user acceptance.

Among the more promising applications is the Viewdata type of service providing low cost, inhome access to an extensive, consumer oriented data base, currently undergoing tests in Europe, Canada, the United States, and elsewhere. When used in residential environments, this consumer service exhibits many of the characteristics that require a dual-speed alternate voice/data modem, such as inquiries that can be established via conventional dial-up telephone links in voice mode and interactive sessions involving short, low speed data transmissions from the home to the data base, and longer, higher speed transmissions from the data base to the home television set. Many of the tests are now conducted exclusively in data mode through use of special terminals and split speed modems. A device such as the alternate voice/data modem would allow consumers to interact with the service providers in voice mode for special or nonstandard inquiries.

Electronic mail applications in office automation systems typically use only data mode and exhibit short inquiry, longer response sequences suitable for split speed operation. With voice mail applications at the threshold of widespread usage as an addition to conventional electronic mail, it is possible that an alternate voice/data capability could spur voice/electronic mail applications because certain types of messages are more effective when delivered orally.

The dual-speed, voice/data features are also seen as an adjunct to certain forms of teleconferencing. Full motion video teleconference links using wideband communications facilities are still cost prohibitive for many companies. Among the alternatives are public teleconference facilities such as those being researched by large motel chains. Some of these systems will offer one way video with dial-up telephone links used for the return communication path. With voice/data modems, the dial-up links could support both voice and data.

Another form of teleconferencing involves voice only meetings and relies on dial-up facilities for an expanded version of the conference call. The introduction of voice/data modems with dual-speed operation might facilitate the addition of facsimile or other data devices to such calls at relatively small additional cost. Other applications such as credit verification, timesharing, and inquiry/response systems suggest that the alternate voice/data modem may have spawned a new generation of more efficient modem designs. In fact, the diagnostic systems house applications for which the device was designed may be only the first of many uses to which it can be adapted. **CD**

Christopher A. Cox is the technical specialist for Intertel's OEM Marketing and Sales groups. A graduate of the Kingston College of Technology in Surrey, England, where he received Associate Membership in the Institute of Electrical Engineers, United Kingdom, he is responsible for new product planning for standard and custom modems, and OEM product marketing.

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	Height	8.5"	8.2"	8.5"



COMMUNICATIONS EXECUTIVE IMPLEMENTS COMPUTER NETWORKS

Portable software subsystem creates a self-contained data communications environment that handles a range of equipment under most realtime operating systems and layered network protocols

John Forecast
James L. Jackson
Jeffrey Schriesheim

Digital Equipment Corporation
146 Main St., Maynard, MA 01754

More and more computers of all sizes and types today are expected to participate in computer networks to some degree. Network participation requires a number of communications functions that enable user programs on any one computer to exchange data with user programs on any other computer in a network. However, many of the operating systems currently installed on various computers lack a network communications capability. Collectively called the Communications Executive, a group of software modules creates an environment within which data communications software can execute in cooperation with an operating system. Tailored to the needs of the communications software, the special environment shields data communications programs from involvement with internal mechanisms of the host operating system. Just as the operating system supervises execution of user programs on the computer, so the Communications Executive supervises execution of data communications software. Together with the software it manages, the Communications Executive can be considered a dedicated communications subsystem.

Development of the Communications Executive (CommExec) addressed several objectives intended to ensure its broad applicability in meeting both present and future needs. Major hardware oriented objectives included applicability to the entire PDP-11 computer family, potential for extension to other computer architectures, operation on either small host computers or frontend processors within larger computer systems, and the ability to handle a full range of communications

equipment from simple character interrupt devices to microprocessor controllers. Software objectives included compatibility—at least in concept—with any current DEC operating system and with any layered communications protocol, regardless of hardware environment. To make effective use of computer resources, the CommExec was also optimized for fast execution, efficient use of central processing unit (CPU) time, and minimum use of physical memory space. In the long run, it was designed as a flexible, modular system that would accommodate changing hardware and software tradeoffs.

First implemented under the RSX-11 family of realtime operating systems, the CommExec supports operation of the DECnet implementation of digital network architecture (DNA) as well as other hierarchical layered network software such as CCITT Recommendation X.25. Although specifically applicable to DNA, the relationships between the various protocol layers are representative of virtually any hierarchical network software (Fig 1). The highest layer contains the user programs through which access to the computer network is obtained. A network management layer includes all software modules used to monitor and manage the network. Next, the network application layer contains software modules supplied by a vendor to provide network application functions such as remote file access and file transfer. Between the three user oriented layers just described and the four system oriented or kernel layers below, a session control layer includes all operating system dependent functions that are involved in net-

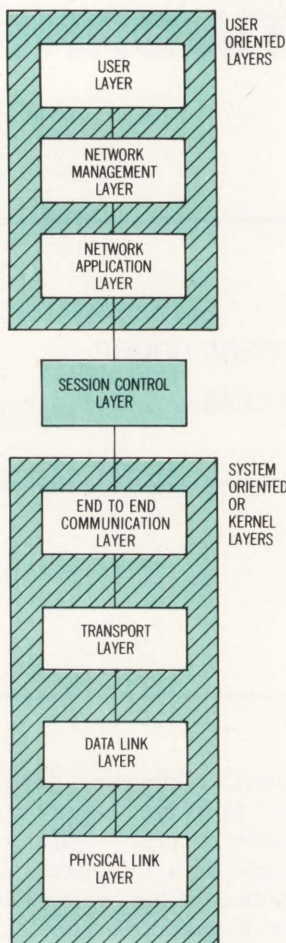


Fig 1 Digital network architecture. Hierarchical, layered configuration includes three user layers (at top), supervisory layer, and four system or kernel layers (at bottom). Although specifically applicable to DNA, relationships between protocol layers could represent virtually any hierarchical network protocol

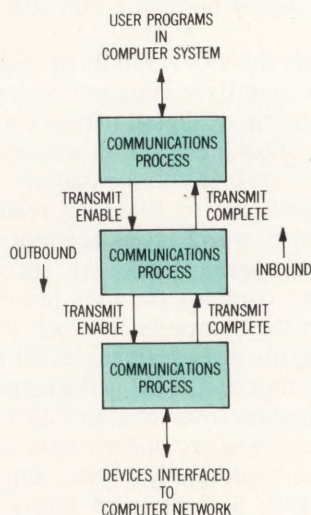


Fig 2 Typical generic functions. Common to all communications processes in layered hierarchy, generic functions such as transmit enable and transmit complete permit processes to cooperate when handling inbound or outbound data

work activity. Software for handling network input/output (I/O) requests, controlling access, and initiating network tasks in response to received connects resides in the session control layer.

Supervising interprogram communication between computers in the network, an end to end communications layer creates, manages, and erases logical links that form virtual communications paths between cooperating programs running on different computers. The next kernel layer, the transport layer, moves message packets between source and destination computers within a network. A data link layer ensures error free transmission of message packets across the communications medium, and a physical link layer contains software that performs the actual message transmission and receipt.

Communications Processes

In any architecture such as DNA, network software comprises a number of communications processes that function identically in the communications subsystems of computers at all nodes in the network (Fig 2). A communications process is simply a collection of software modules that share a common identity. All of the modules are scheduled together; when necessary, their context is saved and they are suspended together. When running, a particular communications process executes at a particular priority relative to other processes within the communications subsystem. Processes remain unaware of the priority at which they or other processes execute. In fact, although it is never called upon to preempt itself and so need not be reentrant, a process can run with different priorities at different times.

A communications process is sequentially queue driven, beginning execution of requests in the order in which the requests were received. Although an interrupt driven approach might at first seem more natural, the queue driven approach is most consistent with a modular implementation strategy and allows tighter control of interfaces between the layers. Interrupts originate only in interface devices driving physical lines, where they are required to avoid loss of data inbound from the network.

In addition to being sequentially queue driven, a communications process is channel oriented. It deals with one or more channels, each associated with a physical or virtual communications path within the network. A communications process is always scheduled to perform services for one channel at a time; within a communications process, unique but identically formatted data bases define each channel.

Whatever specific operations the hierarchical structure of Fig 2 performs in each communications process, a set of generic functions common to all communications processes permits them to cooperate when handling message traffic. Moving from top to bottom within the hierarchy, these generic functions are control enable, receive enable, transmit enable, and exceptions. Moving upward from the lower level communications

processes, the generic functions are, as one would expect, control complete, receive complete, transmit complete, and exceptions complete.

Generic functions implement the conceptual model that defines the communications subsystem. In the model, a process (either a communications process or a user program) represents either a source or a sink for a stream of data associated with a particular channel at any particular moment. Similarly, the model assumes that the computer is linked to a network that directs data from a source communications process to a sink communications process. Messages en route from a source to the network are outbound data, and messages en route from the network to a sink, inbound data. Owing to the hierarchical relationship among communications processes, both outbound and inbound data will be handled by more than one process.

For outbound data, a transmit enable request is passed from one communications process to another until, typically, the data pass through a device handling process. Once the data have been transmitted out of the node and into the network, the device handling process returns a transmit complete request to the communications process above it in the hierarchy. The sequence of communications process interaction is then reversed, and the user program is finally informed. At each layer, protocol characteristics determine when completion will be propagated up to the next layer. Similarly, control function requests can be issued downward through the hierarchy, and control complete acknowledgments propagate back up to the requesting user program.

Data are handled differently in the inbound direction. Device handling processes know nothing about either the length of messages they will next receive or their exact time of arrival. To maintain communication with the network, therefore, the communications process must continuously attempt to receive messages, provided only that it has adequate buffer space. Except when servicing interrupts, a device handling process always runs at the hardware priority of the device it is handling.

In the RSX-11M implementation, the three lowest layers of the communications hierarchy include three classes of communications processes, usually with more than one process in each layer (Fig 3). A device driver module (DDM) controls a particular type of line interface device, such as a multiplexer or a single line interface. The device can be synchronous or asynchronous, serial or parallel. Channels handled by a DDM are the one or more communications lines controlled by the interface device. A DDM executes as a result of either a device interrupt or a scheduling request from a data link control module.

Second among the three classes of communications processes within the kernel levels, a data link control module (DLC) implements a particular data link protocol. Channels handled by a DLC are the communications lines on which the protocol is implemented. A DLC

communicates with a DDM on one side and a logical link control module on the other. Both DLCs and DDMs have data bases (line tables) used to manage each of their associated communications lines.

A logical link control module (LLC) implements the packet level protocol used on a particular channel, which at this level is a virtual communications path. Each LLC communicates with a DLC on one side of the communications path and with a user program on the other side.

Since communications processes provide the required generic functions, the communications hierarchy is entirely modular; any process within any of the three lower layers can be replaced by another module that performs an equivalent function in a different way. For example, a process that implements the digital data communications message protocol (DDCMP) can replace a process that implements the synchronous data link control (SDLC) protocol. Or, both DLC and DDMs can be replaced by a DMC11, an intelligent hardware interface that performs both functions.

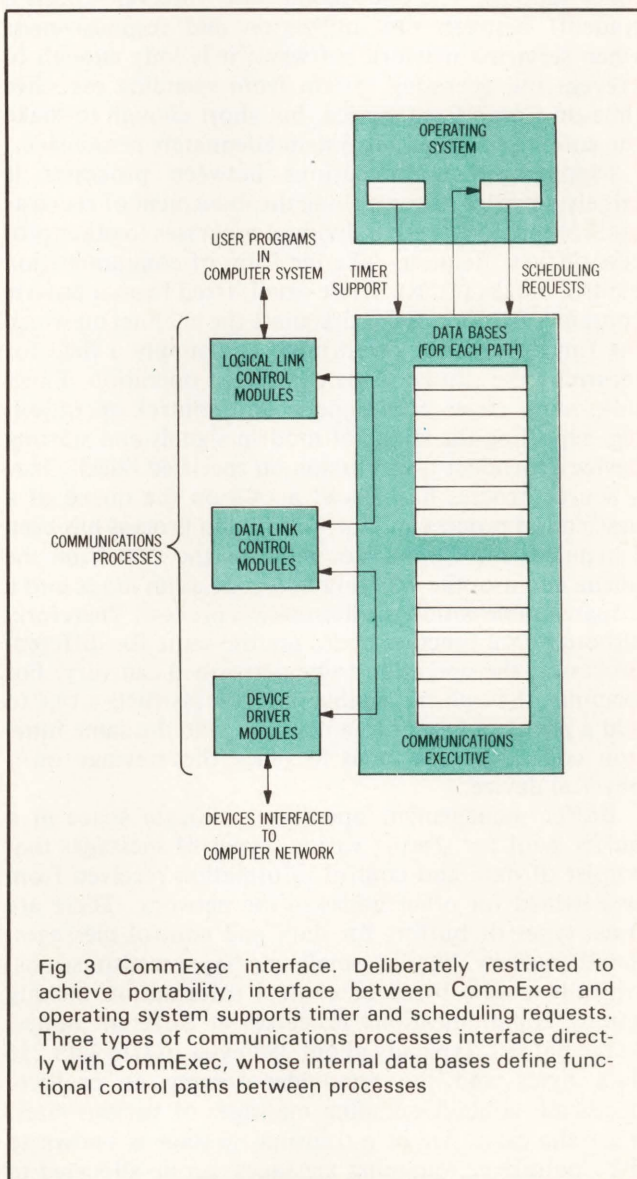


Fig 3 CommExec interface. Deliberately restricted to achieve portability, interface between CommExec and operating system supports timer and scheduling requests. Three types of communications processes interface directly with CommExec, whose internal data bases define functional control paths between processes

CommExec Functions

CommExec interfaces communications processes with the operating system, supervises communication between processes, and manages the process buffers. It also provides a set of utility subroutines that perform such operations as cyclic redundancy checking. No data pass between the CommExec and the operating system; instead, the interface consists of only two specific control functions, request scheduling and timer support, both of which require the CommExec to initiate action among communications processes. Whenever one communications process queues a request to another, the operating system signals the CommExec by means of a scheduling request so that it may process all requests in the communications process queues. The timer provides a signal for action once every second, and that signal is passed on to all communications processes requesting timer support. The one-second timer interval reflects a tradeoff between CPU utilization and responsiveness when servicing network software; it is long enough to prevent the operating system from spending excessive time on CommExec service, but short enough to make the communications subsystem adequately responsive.

Managing communications between processes is largely a matter of controlling the movement of requests and completions from individual processes to other process queues. Requests take the form of communication control blocks (CCBs). These small, fixed format buffers contain a function field, designate the channel on which the function will be performed, and supply a field for returning the status of the completed operation. Function codes cover both generic and control operations (eg, reporting the status of modem signals and starting device dependent transmission on specified lines). Once a source process has placed a CCB on the queue of a destination process and the destination process has been scheduled, the CommExec removes the CCB from the queue and uses the CCB function code as an index into a dispatch table within the destination process. Therefore, although CCB function codes are the same for different processes, the operation to be performed can vary. For example, the transmit enable function instructs a DLC to add a protocol header to a message, and the same function code directs a DDM to place the message on a physical device.

Buffer management operations allocate space in a buffer pool for storing various types of messages that consist of data and control information received from or destined for other nodes in the network. There are three types of buffers for data and control messages. Small buffers handle small message transmissions, typically a few bytes of control information passing among communications processes at different nodes. Large buffers, typically about 280 bytes in size with 256 data bytes and the remainder serving as protocol overhead, contain outgoing messages of various sizes. Since the exact size of a transmit message is known to the CommExec, outgoing messages can be allocated to

either small buffers or large buffers, using available memory most efficiently. Because the size of large buffers is user defined, network managers can trade the protocol efficiency of large buffers for the reduced error rate of small buffers. The third buffer type, a receive buffer, accommodates variable length messages received from a physical line. A device handling process must buffer incoming data in the largest available buffer. Receive buffers are therefore the same size as large buffers.

Included in the CommExec, a number of data bases functionally describe the control paths of data between communications processes. Data bases maintained for any particular process relate to the type of channel that the process serves: physical devices for DDMS, data links for DLCs, and logical links for LLCs. DDM data bases include error counters for devices, and DLC data bases include protocol error counters, definitions of stations on multidrop lines, and polling parameters. For LLCs, data bases include logical link states, numbers of messages outstanding, and the number of the next message expected.

The restricted interface between the CommExec and the operating system permits the CommExec to operate under virtually any operating system without substantial modification. Timer and scheduling request signals that initiate CommExec action are basic elements of most operating systems, and the CommExec requires no other functions. Process context handling further demonstrates the value of a narrow interface between the operating system and the CommExec. Since a communications process cannot be reentered and its execution cannot be interrupted by another process, context handling within a process is greatly simplified and therefore significantly faster than context switching for user programs. Moreover, the CommExec manages communications process context independently of the scheduler in the operating system. Had the communications subsystem instead been implemented using only context switching support provided by the operating system, far more overhead would have been incurred.

Communications Tasks

Interaction between a task and the communications subsystem determines how a user program obtains access to communications services and is almost as important as the relationship between the operating system, the CommExec, and the communications processes. To allow easy communication between user programs and other network programs, the program interface for obtaining network services is consistent with the interface to local devices. Under RSX-11M, for example, the interface between programs and the communications subsystem uses the standard queue input/output (QIO) mechanism that allows device specific functions. Thus, a printer device can write a record; a disc can read or write a block; and a network can connect to a specified program, transmit or receive data, and disconnect from the program. Through use of the QIO mechanism, the entire communications subsystem appears to user programs as a single device.

When a QIO is issued (Fig 4), some initial validation is performed by the operating system and the network user interface. The LLC is notified of each valid request. It interprets each request and, in general, issues one or more CCBs to the DLC layer. Some time later, when the request has been satisfied, the user task receives details of request completion. For example, to receive data, a QIO may indicate completion with 256 bytes received, or it may indicate failure because the logical link was destroyed.

Suppose that a user program issues a request for the communications subsystem to obtain a quantity of data—some number of messages or packets—from a computer at another node in the network. Assume, also, that connect and accept messages have been exchanged with the other node, and that a number of transmit and receive operations will occur until the task is completed and a disconnect is accomplished. Necessarily omitting many details, the sequence of operations begins when the user program issues an operating system request to transmit a block of data. The user interface translates this request into a CCB, which it passes on to the LLC for processing. After adding its own protocol to the data, the LLC places the CCB on the DLCs queue with a transmit enable function code. In turn, the DLC appends its own level of protocol to the data and queues the buffer to the DDM, which accepts the transmit enable CCB and places the data on the communications channel.

When the data packet arrives at the receiving computer, the DDM places the message in a receive buffer and queues it to the DLC with a receive complete function code. The DLC strips off its own level of protocol and queues the message to the LLC. The LLC removes its layer of protocol and matches the message with a receive request previously issued by the user program running on the receiving computer. This I/O request specifies the final location of the data message, which will be copied before the user program on the sending computer is notified of successful I/O completion.

Summary

Most operating systems lack a built-in communications capability and therefore cannot perform the basic functions required by a user program to exchange data with other programs running on other computers in a network. Designed as a general purpose communications subsystem, the CommExec structural model creates a data communications environment in cooperation with virtually any operating system using any hierarchically layered protocol. A current implementation runs on any member of the PDP-11 family and is extensible to other architectures, either in small host processors or frontend processors on larger machines. Its ability to handle the full range of communications devices combines with a deliberately restricted operating system interface to achieve a flexible, modular network communications capability. **CD**

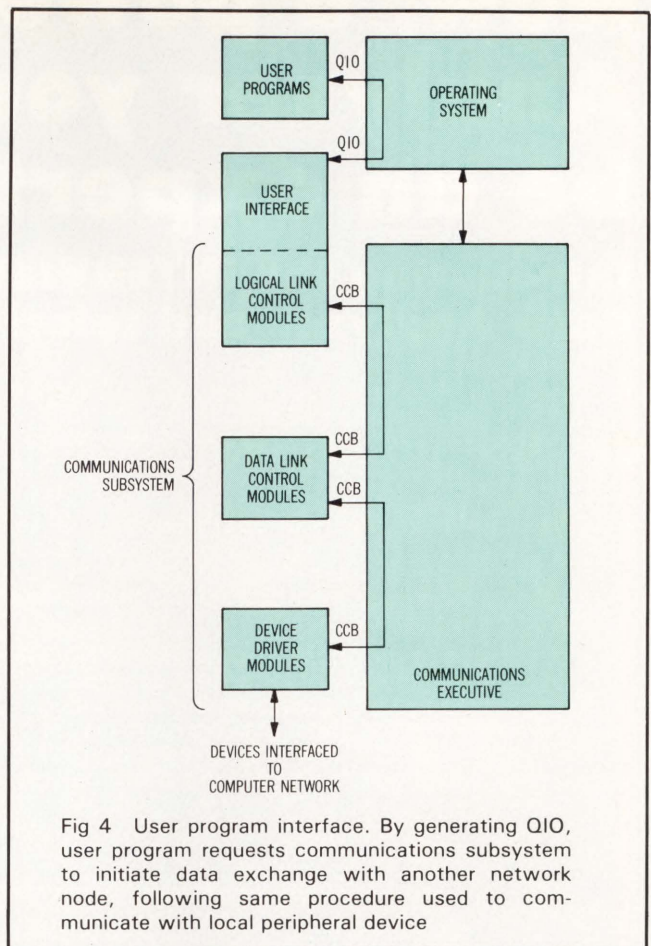


Fig 4 User program interface. By generating QIO, user program requests communications subsystem to initiate data exchange with another network node, following same procedure used to communicate with local peripheral device

A principal software engineer at Digital Equipment Corporation, John Forecast joined the company in England in 1974. Transferred to the United States in 1977, Mr Forecast became technical consultant to the distributed and mid-range systems group at DEC. He holds the BA and PhD degrees in computer science from the Universities of Lancaster and Essex, England, respectively.

James L. Jackson, senior software engineer for distributed and mid-range systems at DEC, is project leader for DECnet implementations under RSX-11M/S and RSX-11M PLUS operating systems. Mr Jackson has earned the BS in electrical engineering from the University of Waterloo, Canada, and the MS in electrical engineering from the University of Queensland, Australia. His interests include networks and communications.

Joining DEC in 1976 as a member and later project leader of DECnet-11M development team, Jeffrey Schriesheim currently supervises engineering of communications software for the distributed and mid-range systems group at Digital Equipment Corporation. Mr Schriesheim holds the BA from Harpur College and the MS degree in systems design and analysis from the State University of New York.

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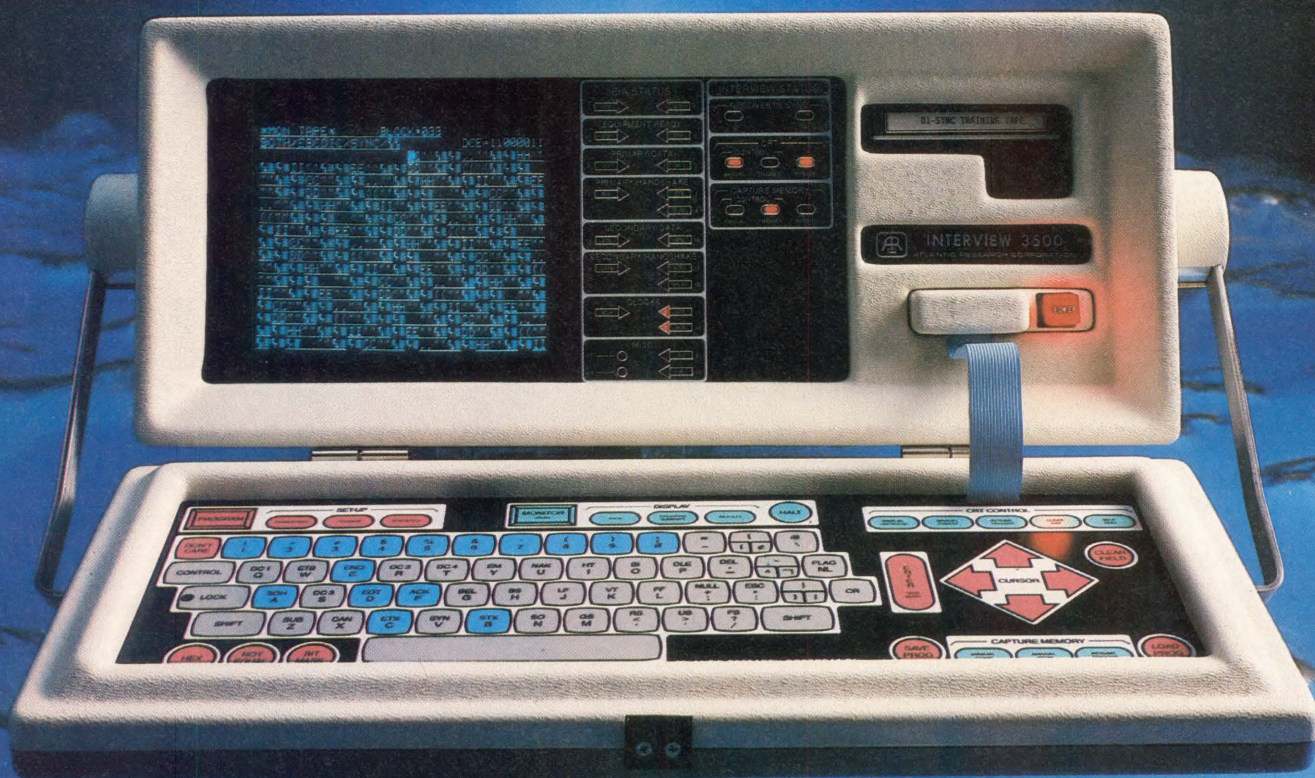
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PERFORMANCE MEASUREMENT IN DATA COMMUNICATIONS NETWORKS

Evolving data communications technology has created a need for network performance measurement tools and techniques that help establish the cost of specific improvements in performance

David B. Kirby

TeleProcessing Products, Incorporated

4565 E Industrial St, Simi Valley, CA 93063

Performance measurement as applied to data communications networks is a relatively new concept. Historical perspective on the industry helps to explain this obvious anomaly in a marketplace where more than \$8 billion is spent annually on equipment and services—a market that accounted for less than \$1 billion ten years ago. The current explosion in data communications technology began in 1968 with the so-called Carterphone decision. Up until that time, American Telephone and Telegraph permitted only equipment that had been manufactured or approved by its subsidiary, Western Electric, to be attached to its telephone lines. From the user's point of view, this was tantamount to renting electric appliances from the power company.

Prior to the Carterphone decision, commercial data communications was limited, for the most part, to low speed (1200-bit/s or less) asynchronous networks of a more or less specialized nature and to batch oriented point to point systems operating at 2400 bits/s. Virtually all of these applications used Bell System modems and lines; in the event of problems, the user's only recourse was the local telephone company. High speed modem technology had not progressed much

beyond 2400 bits/s, and any increase in traffic required a relatively expensive dedicated telephone line as part of the incremental cost of expanded service to remote sites.

The Carterphone landmark made it financially attractive for independent manufacturers to develop higher speed modems for the commercial marketplace. Within the next few years, several companies introduced reliable 4800-bit/s modems for use on dedicated circuits, realizing the tradeoff between increased initial equipment cost and the ongoing cost of additional dedicated circuits. As so often happens, increased capability led to increased demand, and this same period saw a proliferation of high speed data circuits, an extraordinary growth of the demand for 4800-bit/s modems, and considerable pressure in the marketplace for even higher speed modems (Fig 1).

During these early years, when dedicated data circuits were inherently unreliable and 4800 bits/s represented current state of the art in modem technology, maintaining data link integrity was a primary concern. Although by this time network users had gained considerable insight into cost factors and some degree of control over costs, performance was largely a matter of being up or

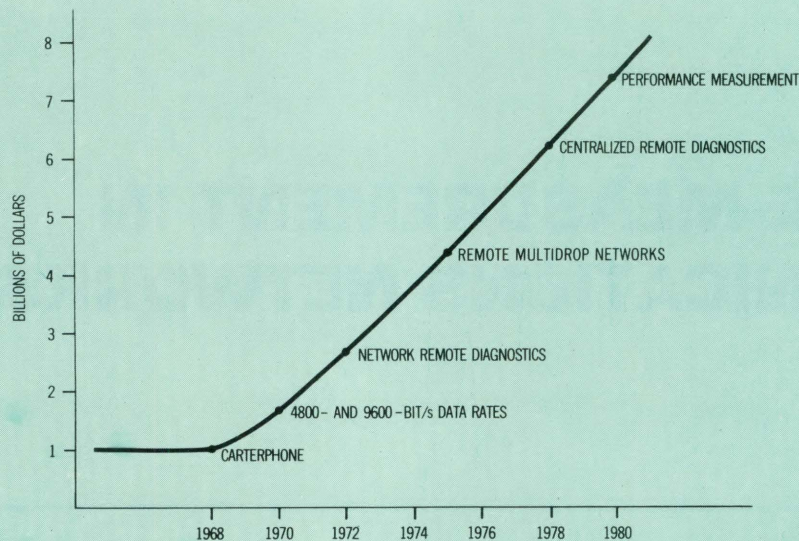


Fig 1 Growth in data communications marketplace. Historical perspective explains why performance measurement is new concept in what has grown to be \$8 billion industry

being down, and the latter always meant trouble. There was much pressure to keep things running, but little incentive to evaluate network performance.

In response to the growing need for performance measurement, manufacturers began to address the problems of network maintenance and the need for network diagnostics during the early 1970s. Initial solutions took the form of external equipment such as bit error rate testers, which could be inserted into a data link, and test modes and sequences built into the modems or terminals, used as troubleshooting aids. Both methods presented two serious drawbacks. First, the existence of a problem (ie, the presence of an inoperative terminal) had to be established by some means other than test equipment before the test equipment or procedure could be implemented. Second, early diagnostics interrupted the data link during the testing period.

Nevertheless, the availability of test equipment and procedures contributed substantially to network reliability and helped to trigger the next round of expansion in the marketplace. Other major factors in this new expansion included development of reliable 9600-bit/s modems; online high speed multipoint networks; and widespread availability of moderately priced, semi-intelligent terminals capable of operating in such networks. A key to this growth was provided by the semiconductor industry in the form of reliable large scale integration components and increased microprocessor capability.

By the mid-1970s, medium and high speed multidrop networks supporting hundreds of remote locations were not uncommon. Planning and implementation of such networks typically involved the evaluation, procurement, and eventual tying together of equipment and services from at least five or six different vendors. Conse-

quently, successful network management required equipment and techniques not previously available.

The latter 1970s saw the development of sophisticated network control centers capable of conducting extensive network diagnostics from the central site on a largely noninterruptive basis and of isolating remote site equipment problems as well as line problems in a very short period of time. Such diagnostic centers were generally microcomputer or minicomputer based and used a low speed secondary data channel on the same telephone circuit as a remote site reporting mechanism. Usually, extensive provision was made both for line monitoring of analog and digital links and for reconfiguration through switching or patching.

For some years it has been possible to predict and control the cost of networks with reasonable accuracy. As costs have accounted for an ever increasing percentage of data processing budgets, management has become more conscious of the need for cost/performance comparisons in the planning and operation of networks. This leads directly to the problem of evaluating performance in a data communications network.

Often characterized as an inquiry/response system, one typical medium to high speed online network illustrates a general type that is used widely in applications such as stock brokerages, airline reservation systems, telephone company billing systems, and bank teller systems, to name only a few (Fig 2). Since the concept of performance measurement in such networks is relatively new, it is helpful to establish some performance criteria. Detailed analysis has developed three broad indicators of network performance: utilization, number of messages, and response time. As will be seen, the values of these indicators are somewhat interdependent.

Utilization

One indicator of network performance, utilization, is expressed as a percentage derived from the ratio between the time various network elements are actually in use and the total time they are available for use. Specific knowledge of these values, when integrated with peak and average load requirements, can be of considerable help in optimizing a network. For example, a particular circuit or group of circuits in a given network may appear to be underutilized as compared with the rest of the network, while other circuits might appear to be overutilized. Armed with this knowledge, engineers can balance the network accordingly. Performance would improve in any event, and reconfiguration would most likely achieve a savings in transmission line costs. Even if line costs go up instead, users benefit from exact knowledge of the tradeoffs involved in the cost increase. A good handle on network utilization can prevent costly overkill in network design and operation.

Number of Messages

As a critical parameter, the total number of messages transmitted in a network is probably the best gross indicator of network performance. It becomes even more important when an exact measurement is made for each remote terminal location and inbound messages are differentiated from outbound message traffic. Exact knowledge like this is invaluable when selecting the proper remote site terminal. For instance, some terminal

families have a choice of line printer speeds available at various cost premiums. When selecting a terminal, the number of messages can be used to chart a line loading curve against the time of day or the terminal location.

Response Time

By convention, response time is generally defined as the interval perceived by the remote terminal operator from the time the ENTER or SEND key is pressed until the time a computer response is received. Used in conjunction with the other two performance indicators, an exact measurement of this time provides a useful network performance indicator.

Not many years ago, the branch manager at a remote field office had to send his source data to the home office for batch entry, waiting up to two or three weeks for a report that his staff would then scan for approximately ten minutes per transaction. Later, it became possible to enter information directly on a remote batch terminal and have a report returned the next morning. Eventually, the same manager would complain if terminal operators had to wait as long as 20 seconds when online system response time was slow.

Components of Response Time

A network can be optimized by distilling the elements that contribute to response time and analyzing the way in which these elements interact (Fig 3). For a typical network using half-duplex protocol, consider first the events that occur between the time the remote terminal operator strikes the ENTER key and the time a reply is

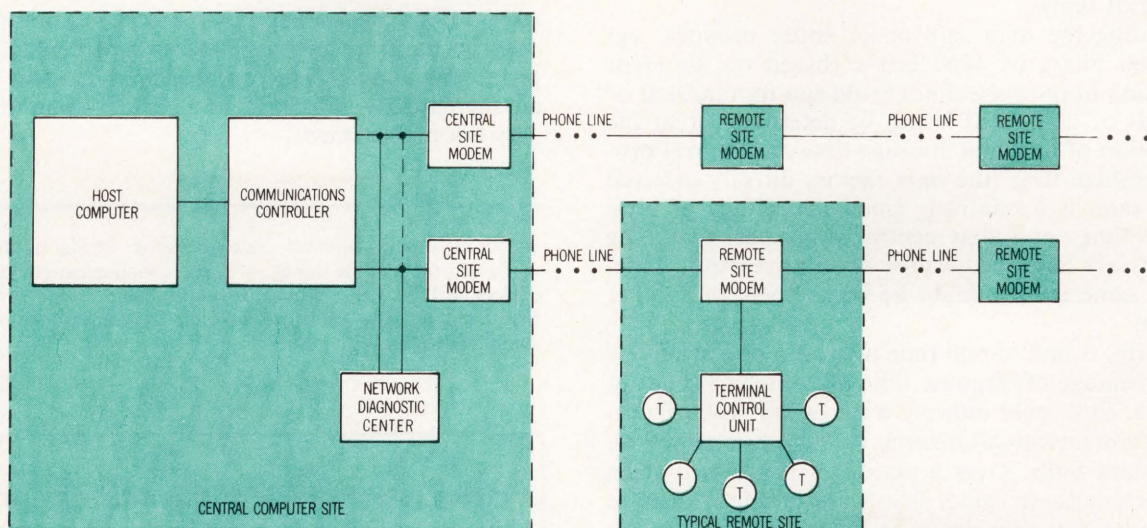


Fig 2 Typical network diagram. Generalized medium speed network is widely used in online applications.

Related parameters of utilization, message volume, and response time determine level of performance

received from the computer. Each terminal in the network has a unique address; the host computer scans the universe of active terminals by issuing inquiries called polls, in sequence, each containing the address of one terminal. A terminal can elect to transmit a message to the host computer by answering its unique poll. Activating the SEND or ENTER key on the terminal initiates this process.

Interspersed with polls from the computer are selects that allow the computer to respond to a particular terminal with messages, as determined by its address. The elapsed time in the scanning sequence between polls to a particular terminal is the maximum interval between the time when the ENTER key is depressed and the moment the computer recognizes that the terminal is ready to communicate—the poll to poll time. Next, the terminal transmits its inquiry message to the computer through the data line. The time required to accomplish this transmission is “terminal message time.”

Usually in conjunction with a frontend communications processor, the host computer next processes the inquiry, formats a reply, and sends the reply back across the data link. When observing this phenomenon in terms of the external data communications network, the time interval between receipt of the last character of the inquiry and transmission of the first character of the response is “central processor wait time;” the time required for the computer’s reply to be transmitted through the data link is “central processor message time.” There are some delays, usually very small, associated with such factors as clear to send in the modem, latency in the terminal, and propagation delay in the data link. These can be measured by detecting poll response time, the interval between sending an inquiry to a particular terminal address and receipt of the first character of reply.

Upgrading the data rate in an entire network, eg, from 2400 bits/s to 4800 bits/s (based on apparent degradation in response time) could run to hundreds of thousands of dollars. If it can be determined that the combination of terminal message time and central processor message time (the only factors directly affected by data rate) is a relatively small percentage of total response time, and that central processor wait time is a relatively large percentage of total response time, then the same money might be better spent in another direction.

Similarly, if poll to poll time proves to be a relatively large percentage of response time on some lines but not on others, this could indicate a necessary reconfiguration of remote terminals in terms of their distribution on specific data links. Over a period of time, measuring and recording these values relative to terminal location and time of day provides a useful profile of network performance that can be an invaluable aid during network upgrades and cost-reduction.

Recently, a family of protocol sensitive network analyzers has appeared in the marketplace, addressing the problems of network performance measurement.

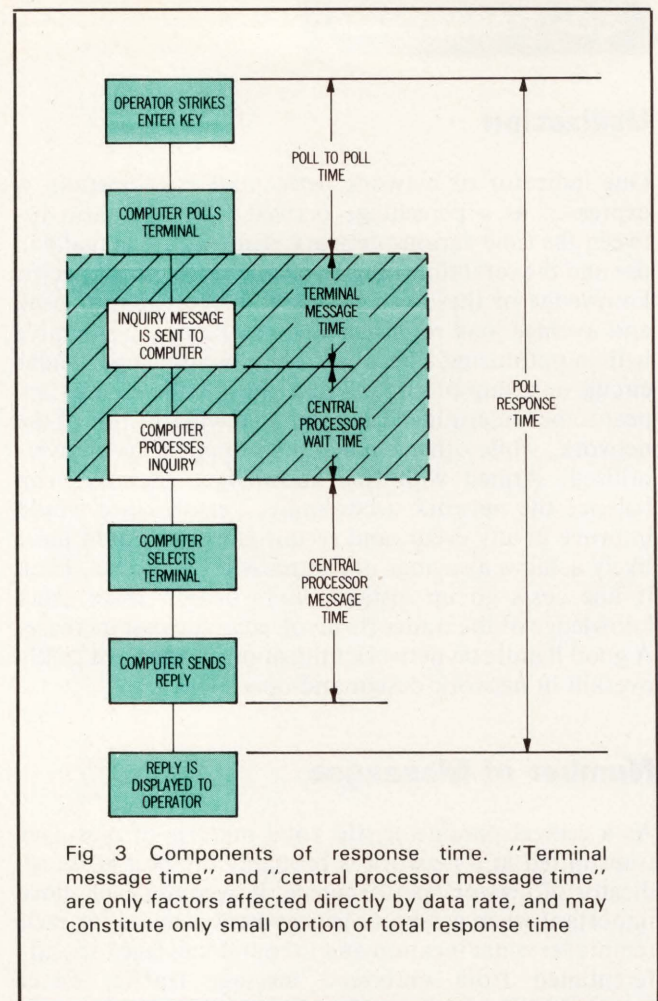


Fig 3 Components of response time. "Terminal message time" and "central processor message time" are only factors affected directly by data rate, and may constitute only small portion of total response time

Capable of measuring network performance from the central computer site, these devices collect the performance statistics necessary for cost/performance analysis in the planning and operation of data communications networks. As network communications costs account for an ever increasing percentage of data processing budgets, performance measurement becomes an increasingly important aspect of communications network management. **CD**

David B. Kirby founded TeleProcessing Products, Inc, which manufactures a wide range of data communications networking devices, in 1975. Prior to this, he was president of Kirby Associates, a firm handling sales and manufacturers' representation for the data communications field.

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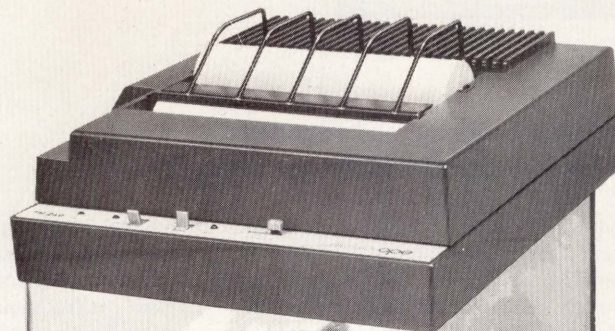
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Local System Range and Functions Extended by Broadband Packet Network

Terminal oriented packet network System 20 can support more than 24,000 terminals operating at 9600 bits/s for an aggregate data rate of more than 14M bits/s on broadband community antenna television (CATV) installations. The system is part of the LocalNet™ family of modular broadband based local area network communications devices from Sytek, Inc., 1153 Bordeaux Dr., Sunnyvale, CA 94806.

The LocalNet concept combines broadband frequency division multiplexing (FDM), a distributed control mechanism based on carrier sense multiple access/collision detection (CSMA/CD), and packet network protocols. It allows transparent communications between all network terminals, provides for data encryption, and interfaces to long haul as well as to internet and intracity connections, covering up to 50 km on a single coaxial cable.

The packet network system is based on frequency agile modems in conjunction with intelligent packet communications units (PCUs). Channel capacity is 200 users and hosts at 9600 bits/s with a system (120 channel) capacity of 24k users.

As a whole the network appears to the user as a public packet network operating under CCITT X.28 conventions. The backbone network operates in contention mode, using CSMA/CD techniques and layered packet protocol architecture, resulting in system error rate said to be less than 1×10^{-12} .

The system is functionally based on packet mode transceivers operating on common logical channels. A modular PCU accepts data from the subscriber interface and formats them into packets composed of source, destination, function, integrity, and flow control information. The distribution system is compatible with broadband midsplit single or dual 75-Ω coaxial CATV cable in star, tree, or hub topologies. Virtual circuit network protocol incorporates both error and flow control. Data terminal equipment (DTE) protocol is compatible with CCITT recommendation X.28, asynchronous, ASCII, 300 to 9600 baud, auto-selected, providing CCITT X.3 services with DTE flow control and speed matching. (A 9600-bit/s CRT terminal can select and communicate directly with a 300-bit/s printer.) End to end data encryption method is based on the data encryption

standard (DES) algorithm with electronic session key distribution.

System elements include model 100 TBox*, a frequency agile rf modem integrated with a PCU and having a single DTE interface, and model 200 Tmux*, with multiple DTE interface. Modems in these units serve 120 program selected channels with 156.25-MHz offset, full duplex, and 300-kHz separation. Carrier frequency synthesis is by program controlled phase locked loop referenced to a crystal time base, and modulation is phase coherent fm. Receive and transmit frequency ranges are 226.25 to 262.25 MHz and 70 to 106 MHz, respectively.

The Z80 based PCU has 2k bytes of non-volatile RAM buffer and 2k bytes of ROM, both expandable to 16k. Channel control is via Z80 PIO, and channel port is a USART with onchip HDLC protocol implementation. The Z80 SIO DTE port provides asynchronous communications to 9600 baud with automatic baud rate selection via RS-232-C interface. Firmware includes P/ROM resident packet assembly/disassembly, error and flow control, and DTE driver routines, including programmable use of X/ON, X/OFF, and RTS-CTS functions.

Tbridge* model 300, another element of the system, provides an internal bridge between up to four system channels, and Tverter* central retransmission and frequency conversion unit performs broadband spectrum upconversion of the entire 120-channel lowband to highband for retransmission to the distribution system. All elements meet rf radiation specifications as set forth in FCC docket 20780.

The system can be piggybacked on CATV systems already installed for security or educational TV purposes. Application areas include engineering, office automation, manufacturing operations, financial districts, and universities.

*Patent pending

Communications Products Enhance Capabilities of MicroNOVA Line

An asynchronous/synchronous line multiplexer (ASLM), a 4-line asynchronous interface, and a communications software package have been introduced by Data General Corp., Rte 9,

Westboro, MA 01581, to enhance flexibility and provide hardware support to the microNOVA™ MP/100, MP/200, and MBC board computer product line. According to the company, the offerings will improve functionality at lower systems cost for OEMs building multiterminal and communications application systems.

ASLM model 4336-S, especially useful for control devices such as terminal clusters or communications concentrators, has four serial communication lines with modem control. Each of the lines supports either character-controlled synchronous protocols including Bisync, or asynchronous communications. Each line's characteristics can be programmed independently.

Model 4336-AS 4-line asynchronous interface is designed for networking applications, as a terminal concentrator, or where cost effective communications interfaces are needed. All line characteristics of each of the four interfaces are fully programmable, with an operating speed of 19.2k baud max. Line interfaces are RS-232-C.

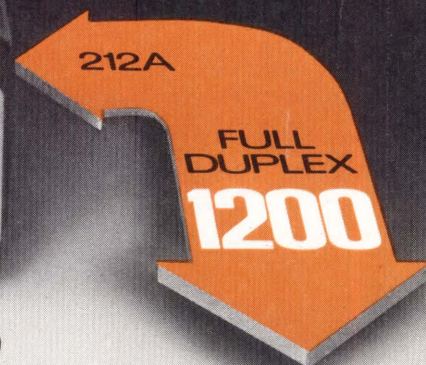
MP/OS synchronous communications package (MSCP) software supports up to eight synchronous communications lines. MSCP supports the ASLM on microNOVA computers and the SLM, ULM, and CSI communications products on the NOVA^R 4 product line. Circle 555 on Inquiry Card

X.25 Product Program to Support Packet Network Services in Six Countries

A program developed by Digital Equipment Corp., Maynard, MA 01754, will supply X.25 packet-switched network products, protocols, interfaces, and support services for its 16-, 32-, and 36-bit computer families. The program, called Packetnet™, has products available immediately for Datapac in Canada and Transpac in France. Future releases will support GTE Telenet in the United States, Datex-P in Germany, PSS in the United Kingdom, and DN1 in the Netherlands. Ultimately, users in each country will be able to tie into DECnet, the company's networking software.

(continued on page 84)

TWO FOR THE PRICE OF ONE



The Penril 300/1200 212A Bell Compatible Data Modem

Save once by handling both 300 and 1200 bps rates with a single modem, a single phone line and a single computer port. Save again by mating with your existing low-speed system, then upgrading to higher speeds whenever you're ready.

Older terminals, new terminals, mixed data streams — you can handle them all, over switched or leased telephone networks with the Penril 300/1200, the full duplex 2-wire dial line modem manufactured under license from Western Electric for both synchronous and asynchronous operation.

FCC Registered; No. ABE976-67837-DM-R

Designed for use with an exclusion mode telephone set for manual calling or answering, this versatile FCC certified modem gives you an automatic answering option, too. Lift the telephone handset for dialing and voice conversation. Activate the exclusion key for the data mode, and answering is automatic with no operator intervention required. You can select either 300 or 1200 bps to originate a call; when answering, the incoming data mode is automatically recognized and accommodated.

Easy to Use; Easy to Service

With 16 switch-selectable options on the modem printed circuit board, you're in control all the way. Use of

high quality active filter networks keeps data transfer accurate, even over inferior telephoned lines. Integral diagnostics keep servicing simple.

For details, contact;
Penril Corporation,
Data Communications Division,
5520 Randolph Rd.
Rockville, Maryland 20852.
Telephone (301) 881-8151.

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CIRCLE 34 ON INQUIRY CARD

CD DATACOMM

Program software will run under the RSX-11M, -11S, and -11M-Plus operating systems for PDP-11 minicomputers and under VAX/VMS operating system for the VAX-11/780 superminicomputer. As part of the program, product implementations for selected countries will be expanded to run under TOPS-10 and -20 operating systems for DECsystem-10 and -20 families of mainframes. Packetnet software adheres to CCITT X.25 standards and recommendations.

The software also enables terminals to communicate on public packet-switched networks through implementation of CCITT X.3, X.28, and X.29 recommendations; X.29 allows data packets to be converted into a form that terminals can handle and converts data from terminals into packets. X.29 implementation is embedded into the host computer system. Currently available with Transpac, it will be integrated into all Packetnet program products.

X.25 standard eliminates vendor-specific protocol requirements. Packetnet program products allow users to interface DEC and non-DEC computer systems to packet-switched networks, enabling them to share data resources with a variety of systems. The link to DECnet for each X.25 implementation enables current users of such networks to couple systems to existing public packet networks and allows migration from one communication scheme to another without requiring modification of application programs.

Datapac and Transpac products are available through license at \$5000 each. Circle 556 on Inquiry Card

INTELLIGENT MODEM™



BIZCOMP 1022 for Computer Applications

Looking to have your small business system do late-night polling over the telephone net? Or how about store-and-forward electronic mailing, distributed networking or automatic data downloading? IMPOSSIBLE using acoustic couplers. FAT CHANCE with a "DUMB" modem. BIZCOMP's new 1022 Intelligent Computer Modem is designed for the versatility and performance needed in computer applications—at a price you can afford!

There was a time when business applications required a modem, an auto-calling unit, a DAA and a messy computer interface board. Not to mention a bear of a headache trying to write the comm software. Well now you can wash your hands of the mess and hassle of outmoded "DUMB" modems. Plug in a BIZCOMP Intelligent Modem and discover the simplicity of a full control, 3-wire RS-232 interface. An integral serial dialer with both tone and dial-pulse capability. Direct connect, FCC registered auto-answer. And reliable Bell Standard 103 compatibility at up to 300 baud. The 1022 even does double duty as a remote maintenance/diagnostics device. Whatever your application, BIZCOMP Intelligent Modems open the road for advanced communications.

BIZCOMP Communications...
Why not start with the best?

BIZCOMP

P.O. Box 7498 • Menlo Park CA 94025 • 415/854-5434

Rentals and leasing available from Leasametric, 800/227-6773; 415/574-5797 in Calif.

Patent Pending

Bit Error Rate Tester Covers Data Rates from 100 to 5M Bits/s



A 4-digit 5-decade frequency synthesizer allows the 852B bit error rate tester (BERT) to select rates from 100 to 5M bits/s, with a range from 1 to 10M bits/s offered as an option. The integrated unit, from Aydin Monitor Systems, 502 Office Center Dr, Fort Washington, PA 19034, provides signal generation, perturbation, comparison, and readout of data quality.

Outputs are MIL-STD-188C and 50-Ω TTL, selectable as pseudorandom 2047-bit, programmable 48-bit, or external data patterns. Data output may be offset, jittered to $\pm 20\%$, or have noise added by means of internal buffering and mixing of externally applied sources. A selectable internal delay of 0 to 50 bits compensates for transmission delay in data link tests, and a front panel readout immediately indicates errors per unit time (BER). Measured range is 1×10^{-9} to 2.5×10^{-1} with 3-digit resolution.

The tester is packaged in a 5.25" (13.3-cm) high rack mountable chassis. All test points, readouts, and controls are mounted on the front panel. The broad range of the instrument covers low baud rate wire communications through high rate satellite links. Applications range from offline PCM bit synchronizer/signal conditioner testing to determination of bit error probability of a complete PCM link. Circle 557 on Inquiry Card

CD DATACOMM

Handheld Instrument Provides Data Entry, Retrieval, Troubleshooting

Microprocessor controlled terminal/test set 920 enables data entry or retrieval and testing in duplex synchronous and asynchronous modes. The instrument, from Nu Data Corp, 32 Fairview Ave, Little Silver, NJ 07739, supports synchronous (single or double sync) and asynchronous (1, 1.5, or 2 stop bits) operation with 5,

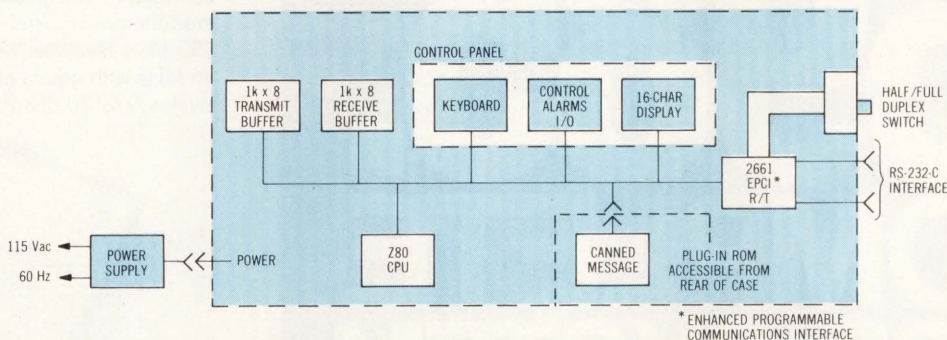
6, 7, or 8 information bits plus optional parity bit at 16 popular rates from 50 to 19.2k baud, with external clock in synchronous mode.

All ASCII, EBCDIC, TRANSCODE, and BAUDOT codes can be sent, received and displayed on a 16-char, 16-segment display in either alpha or hex format. BAUDOT is in hex only. The 64-key keyboard and 3 shift keys enter data either into buffers or directly to the line in asynchronous mode. Two 960-char buffers are provided for transmit and receive data. Buffer contents are displayable, and buffers have search and edit provisions. The buffers may be loaded from received data, from the keyboard, or from canned

"fox" or up to 128-char custom messages from a plug-in user-accessible P/ROM.

The buffers may be searched for bad parity in ASCII 8-bit odd or even parity. Buffer search will stop on the first error encountered; reinitiating the search will lock onto the next error. Either transmit or receive buffer may be searched offline, while online search is for receive only. LEDs are provided to display errors in either parity or framing. Interface to the device is via a fully active RS-232-C connection. The unit, measuring 4.75 x 9.5 x 1.5" (12.1 x 24.1 x 3.8 cm) and weighing 1 lb 6 oz (0.62 kg), operates from an external power supply.

Circle 558 on Inquiry Card



Test set block diagram. Optional interface includes EIA monitor and breakout interface, EIA random character generator/analyzer, and current loop interface with loop supply and regulation

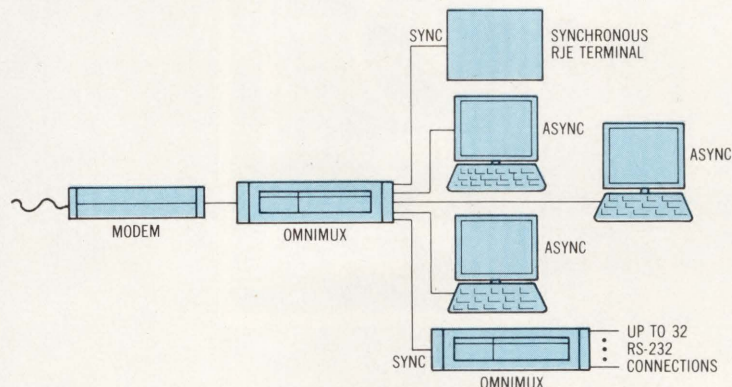
Family of Statistical Multiplexers Performs Variety of Functions

Statistical multiplexer OMNIMUX series, consisting of 8-channel model 80, 16-channel model 160, and 32-channel model 320, includes such network management functions as diagnostics, statistical reporting, and remote control. The series, from Racal-Milgo Information Systems, Inc, 8600 NW 41st St, Miami, FL 33166, is capable of statistically multiplexing a mixture of synchronous and asynchronous data channels with full protocol transparency and with all channels operating up to 9600 bits/s. Aggregate link speed is up to 19.2k bits/s.

A 16-bit CRC block check with ARQ assures end to end error free transmission. Autobaud allows multiplexer channels to accommodate dial-in applications from 110- to 1200-bit/s terminals, using Memorex or carriage-return signon characters. Fixed or adaptive speed control allows each channel to independently accommodate speed conversion, so that devices with different operating speeds

can communicate over the same channel. Speed conversion rates can be either fixed or combined with autobaud. The flow control feature controls data flow both into and out of individual channels using inband X-ON/X-OFF or the clear-to-send (CTS) control signal. This is im-

plemented at peak traffic periods when buffers are full and prevents loss of data. The aggregate link, operating synchronously at 1200, 2400, 4800, 9600, and 19.2k bits/s, uses CCITT X.25 Level II protocol. Interfaces are RS-232-C, V.24/V.28.



Mixed asynchronous and synchronous channels. Channels are fully transparent to protocols and have no delay. They can run continuous or switched carrier, half or full duplex, dedicated or dial-in. Other OMNIMUX aggregate links can be multiplexed over these channels

CD DATACOMM

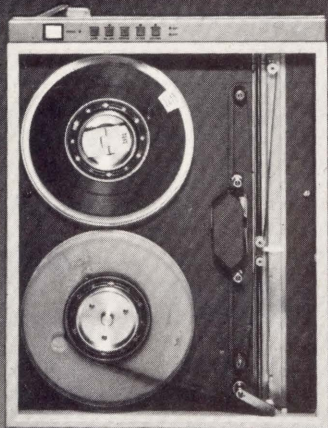
Local and remote monitoring and test capabilities include continuous monitoring of the aggregate link for both activity and error conditions. Full range diagnostics provide individual local and remote loopback combined with an internal test message generator. Local and remote aggregate link loopback is also included. Statistics reporting continuously

accumulates information on both individual channel and overall aggregate link efficiencies. This information is available from local and remote units via the front panel display. A supervisory control and monitor feature allows long term reports to be accumulated and shown on a user provided ASCII 50- to 9600-bit/s terminal. The multiplexer family is compatible with the company's CMS System 1000 and 2000.

Circle 559 on Inquiry Card

\$6985. COMPLETE TAPE SYSTEM

The 75ips TDX Series II complete with embedded microformatter and interface to PDP-11/VAX, LSI-11, NOVA/ECLIPSE, RS-232, IEEE-488 or Dual Buffered I/O. \$6985-800 bpi/NRZ or \$7885-NRZ/PE Dual Density in single unit quantity. Contact us today.



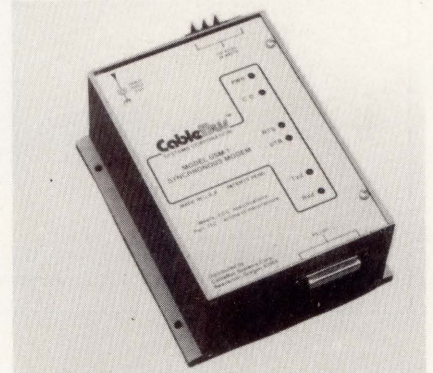
TDX PERIPHERALS

Division of GAW Control Corp.
150 New York Avenue, Halesite, NY 11743
(516) 423-3232

Synchronous Modem Has Applications in CATV or Industrial Cable Systems

Capable of data rates to 19.2k bits/s, USM-1 has full output filtering and adjacent channel rejection on the input to ensure satisfactory operation in loaded CATV and multicarrier industrial cable systems. The device is available from CableBus Systems Corp., 7869 S Nimbus, Beaverton, OR 97005. Operating mode is synchronous, full duplex. 600-, 1200-, 2400-, 9600-, and 19,200-bit/s data rates are selectable via internal DIP switch.

Transmit frequencies are 5 to 18 MHz with others available on request. Transmit levels are adjustable and range from 20 to 40 dBmV. FSK pulse duration encoded modulation is used, and bandwidth is 250 kHz. Receiver frequencies are 72 to 96 MHz with others available, and receive level is 0 to 30 dBmV.



RS-232-C data connection and type F rf coaxial fitting are provided. A set of LEDs indicates power, carrier detect, data terminal ready, data set ready/clear to send, transmit data, and receive data. The unit draws 0.4 A at 12 Vac, measures 5 x 7 x 3" (12.7 x 17.8 x 7.6 cm), and weighs 2 lb (0.9 kg).

Circle 560 on Inquiry Card

Network Management Software Centralizes Communications Monitoring and Control

Virtual Monitor™ includes three basic elements. The first, a software package written in COBOL called CRISP (call, response, information, and service program), runs on the user's mainframe and provides continuous records and reports on all network elements. The second, an overall network control center equipped with one or more "call directors," receives all incoming calls, problems, or inquiries and enters such data on online CRT terminals. Hardware requirement, the third, normally depends on the user's existing configuration and equipment. In

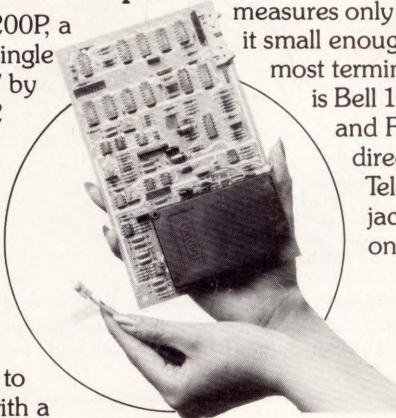


Now, OEMs can take the High Road or the Low Road with our Direct- Connect Modem Cards, small enough to mount inside Data Terminals.

As the auld Scottish tune suggests, Racal-Vadic now makes it easy for OEMs to take the high road (1200 bps) or the low road (300 bps), with low cost direct-connect "Modems-on-a-Card," small enough to mount inside CRT displays, teleprinters, POS devices, and other terminals and systems.

The High Road: 1200 bps

Meet the compact VS1200P, a complete modem on a single PC board measuring 5" by 8.35." That's a thrifty 42 square inches of space. It's fully compatible with Bell 202C and S modems. Only better, offering much more in performance, flexibility and test capability. It's registered for direct-connect, too. Connects to the switched network with a



cable that plugs right into a Telco voice or data jack. Built-in 20 pin ribbon connector easily interfaces the VA1200P to your terminal. Price is right, too. Just \$200 in quantities of 100.

The Low Road: 300 bps

The VS300P is a 300 bps full duplex, automatic originate/answer "Modem-on-a-Card." Like the VS1200P, it measures only 5" by 8.35," making it small enough to mount inside most terminals. The VS300P is Bell 103/113 compatible, and FCC Registered for direct connect via a Telco voice or data jack. Mounting holes on each corner make

it a cinch to install. And the price would put a smile on the face of the thriftiest Scotsman. Just \$200 in lots of 100.

Both Roads: The TI Story

Two of Texas Instruments new Silent 700* data terminals include Triple Modems custom made by Racal-Vadic. Although small enough to fit into TI's portable 17 pound terminal, this remarkable modem combines a Racal-Vadic VA3400, a Bell 212A, and a Bell 103. Imagine, a full originate/answer direct-connect modem with both 1200 bps full duplex and 300 bps full duplex in such a tiny package. And it can even be acoustically coupled.

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RACAL
The Electronics Group

CD DATACOMM

most cases no additional hardware is required. A typical configuration might include an IBM mainframe running online applications under CICS or IMS using 3270-type terminals.

The automated system, from Amdax Corp, 160 Wilbur Pl, Bohemia, NY 11716, is transaction driven. It stores a complete and current record of all operational events in a central data base, and this information is available to automatically warn network management of potential sources of trouble. The data are retrieved by entering a security access code into any CRT display terminal attached to the system. This interactive inquiry capability allows the manager to examine an entire network through a single monitor.

As the system is offered for a monthly license fee plus a one-time installation charge and as the package uses the customer's existing hardware, no capital expenditures are involved. In cases where an appropriate mainframe is not available, the company will arrange to set up the system on an offsite mainframe using its own personnel.

Circle 561 on Inquiry Card

Device Accesses Data Network through Rotary Dial Telephones



Placed over the mouthpiece of a rotary dial telephone, the M-101 acoustically coupled tone generator from Teltone Corp, 10801 120th Ave NE, Kirkland, WA 98033, allows access and data entry to a computer system via the telephone network. The device is designed specifically for tone controlled communications applications, and is not intended to control the switched network prior to connection to the terminal device.

An MOS digital IC generates standard Touch-Tone[®] signals by activation of 12 keypad buttons. Tones are coupled into the telephone system by a built-in speaker. The crystal controlled IC maintains accuracy of the frequencies, including drift and aging, to within less than 1% of nominal. Power is derived from a standard 9-V battery, and a high or low tone output switch is provided.

The tones can be received by circuitry such as the company's M-917 DTMF decoder that can translate the DTMF digit into logic level binary output and can drive Schottky TTL gate, low power transmitter, MOS, or CMOS. The device also has applications in remote access systems, centralized dictation/word processing access and control, access to control systems, mobile telephone, and programming access. In addition, it is compatible with standard tone decoders.

Circle 562 on Inquiry Card

Digital Satellite Communications Network To Connect Company Operations

MACOMNET is the name assigned to a proposed nationwide digital satellite business communications network to connect the headquarters of M/A-COM, Inc, Burlington, MA 01803, to operating companies in Maryland, California, and North Carolina. Using transponder time on Western Union's Westar satellite, the system will initially connect the Burlington headquarters building with Digital Communications Corp, Germantown, Md, Linkabit Corp, San Diego, Calif, and Valtec Corp, Catawba, NC. Each site will be equipped with a DYNAC 5-m earth ter-

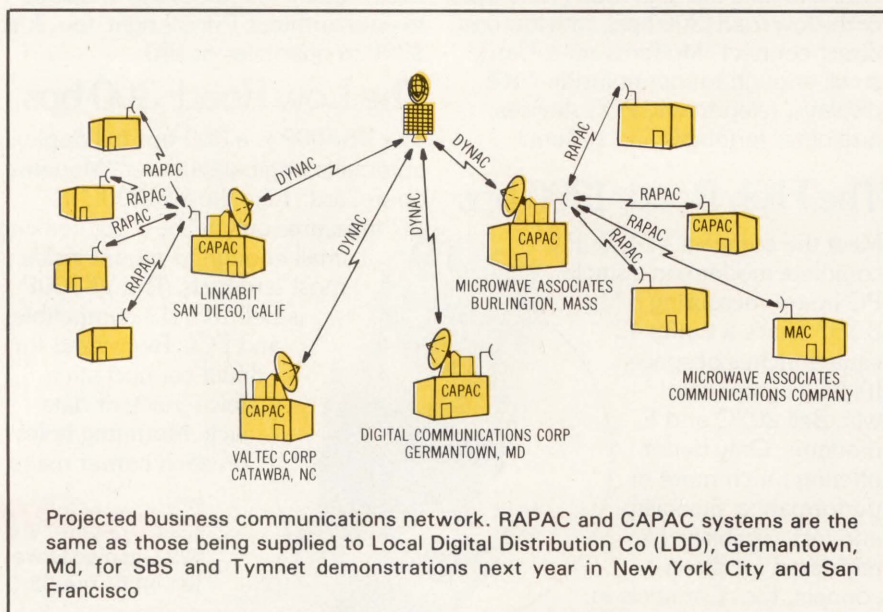
restrial terminal that will connect to terminals and conference rooms at each location via coaxial cable. DYNAC is a microprocessor based earth station using time division multiple access (TDMA) to optimize network and transponder capacity.

Phase 2 of the program includes an expansion of communications facilities to other M/A-COM buildings in the Burlington complex using the company's recently developed cable packet access communication (CAPAC-I and -II) systems and radio packet access communication (RAPAC) system.

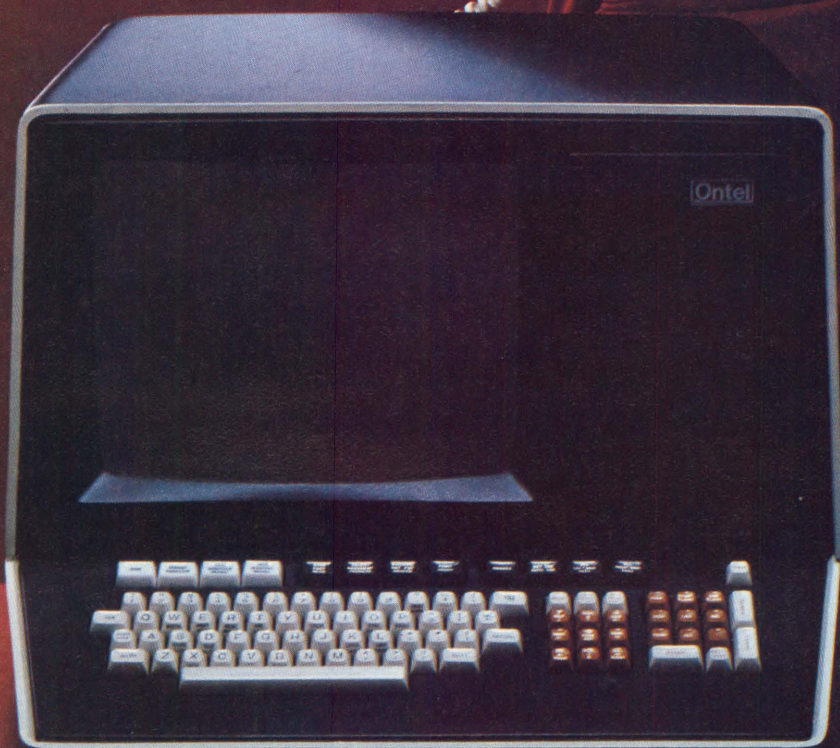
CAPAC-I is an intra-building system used to interconnect the earth station with computer terminals, intelligent typewriters, and other office equipment within a building. The system allows all such devices to communicate among themselves or to transmit via satellite through the earth terminal. RAPAC is an inter-building system for communication via microwave links throughout a complex of buildings or citywide. The CAPAC-II system uses CATV cable to provide this function.

According to Dr Lawrence Gould, M/A-COM chairman of the board and chief executive officer, this "office of the future" system is expected to increase management productivity and contribute to reductions in travel and other business communication costs. Using the new system, a 2-page letter can be transmitted from Burlington to San Diego in 6 s, business conferences can be conducted via teleconferencing, and reports and other critical data can be exchanged in seconds.

M/A-COM is planning to file for FCC approval on the system later this year. Work on the project is scheduled to be completed in January or February 1981.



TOREN/GAYNOR



Parliamo molte lingue.

(We speak many languages)

Over 15,000 Ontel intelligent systems are used worldwide with many languages—English, Italian, German, French, Spanish and Hebrew. Our software languages include—PASCAL, BASIC, FORTRAN and OP/L. Ontel provides everything for successful OEM installations... data processing... word processing... communications... delivery... customer support... operating systems. And certainly not least—highly attractive pricing. Contact me today. You'll find we speak your language.

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CIRCLE 38 ON INQUIRY CARD

BRIEFS

Limited Distance Modems

Modem Provides Medium Distance Data Distribution—Covering medium distances up to 50 miles (80 km), model 3002 4800-bit/s modem from Avanti Communications Corp., Aquidneck Industrial Pk, Newport, RI 02840, operates over unconditioned and dedicated 3002 lines, loaded metallic circuits, analog and digital carrier systems, microwave, and multiplexer systems. Operating modes are 4-wire full duplex, 2- or 4-wire half duplex, point to point, or multipoint. 3600-bit/s fallback rate allows reliable communications in event of lines going marginal. Dual channel option allows a single unit to handle two terminals operating independently at 2400 or 1800 bits/s. Asynchronous option allows either single 4800/3600 or dual 2400/1800-bit/s terminals to be connected directly without need for external converters. Units have local and remote loopback and diagnostic LED indicators. Circle 563 on Inquiry Card

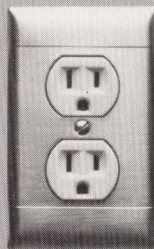
Modem Handles Local Data Distribution Up to Seven Miles—Limited distance modem 6210 is designed for asynchronous operation over Telco or private 2- or 4-wire nonloaded metallic conductors at up to 9600-bit/s data rates. Usable in both point to point and multidrop configurations, the device is particularly well suited to data distribution up to 7 mi (11.2 km) over conventional 26-gauge wire. The device, from International Data Sciences, Inc., 7 Wellington Rd, Lincoln, RI 02865, has a pulse modulation scheme that varies transmit signal polarity on a balanced line. Transmit and receive lines are transformer coupled. DTE interface is RS-232-C/V.24 and transmit signal level conforms to AT&T and Bell Canada requirements. Analog loopback mode provides diagnostic capability, and a 20-mA TTY current loop interface is also available. Circle 564 on Inquiry Card

Asynchronous Modem Transmits Data to 200 Miles—Designed for use in areas beyond the capabilities of short haul units but where distances do not justify the use of conventional long haul modems, LDM 414 can transmit data up to 200 mi (320 km) at rates to 4800 bits/s over 4-wire voice grade conditioned or unconditioned 3002 lines, T carrier, and most other carrier systems. The device, from Gandalf Data, Inc., 1019 S Noel Ave, Wheeling, IL 60090, has a built-in tuning meter to simplify alignment. Local and remote digital, and local analog loopback are provided. Operating modes include both constant carrier and simulated controlled carrier. A dual channel option enables two channels to be carried simultaneously. Interface is RS-232-C/V.24. Synchronous version LDM 404B is also available. Circle 565 on Inquiry Card

Short Haul Modem Transmits up to 30 Miles—Synchronous local dataset 421 from Micom Systems, Inc., 9551 Irondale Ave, Chatsworth, CA 91311, operates at speeds and distances ranging from 110 bits/s at 30 mi (48 km) to 19.2k bits/s at 1 mi (1.6 km) over unloaded private line metallic circuits. The device is compatible with Bell publication 43401. Versions come in rack mount chassis holding 16 units and occupying 5.25" (13.3-cm) height in a 19" (48.3 cm) computer cabinet, or as a tabletop unit weighing 2 lb (0.9 kg). No special tools are needed for installation. Integrated loopback tests and data activity displays facilitate troubleshooting. Circle 566 on Inquiry Card

Limited Distance Modem Available in Multispeed Versions—Short haul modem SLD-MKII comes in four different models ranging in speeds from 2400 to 9600, 2400 to 14,400, 2400 to 19,200, and 2400 to 28,800 bits/s for private line synchronous data transmission over distances to 20 mi (32 km). The device, from Prentice Corp., 266 Caspian Dr, Sunnyvale, CA 94086, operates 4-wire full duplex, or 2- or 4-wire half duplex in point to point or multipoint/pollled modes. Characteristic speeds and distances are up to 6 mi (9.6 km) at 4800 bits/s and up to 4 mi (6.4 km) at 9600 bits/s on 26 AWG nonloaded cable, and data rates are switch-selectable. Features include complete diagnostics with local and remote loopback, pseudorandom self-test generator, LED diagnostic indicators, internal/external clock or repeater timing modes, CMOS design, and code transparency. Circle 567 on Inquiry Card

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AC power poses tough problems for process controller designers.

That's why Gould designed the MG, SMG and LMG switching power supply lines especially for process controller applications.

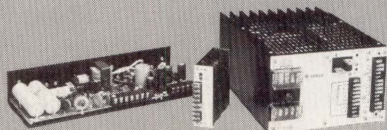
Our MG, SMG and LMG switchers offer unmatched reliability as well as excellent regulation and protection against AC line problems.

They're rated from 8 to 2250 watts

in single and multiple output versions. The open frame LMG and modular

SMG are ideal cost-effective switchers, while modular MG units meet the toughest international specs to handle your largest distributed systems.

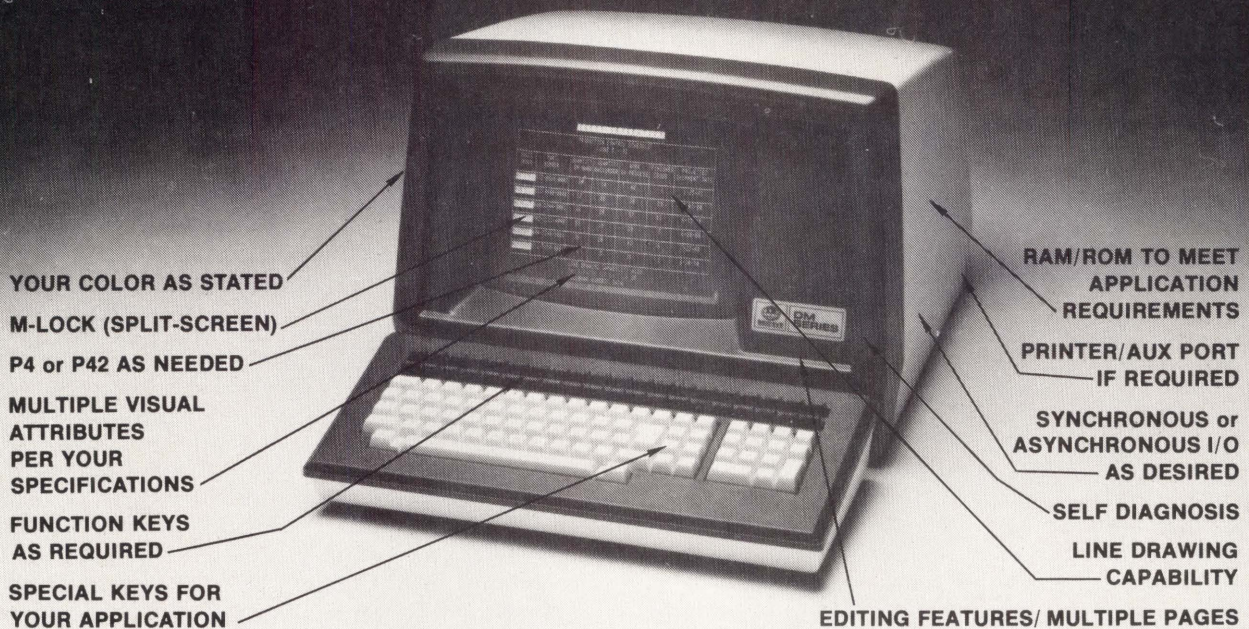
For more information and a copy of our short form catalog, circle the reader service number. Or call us toll-free: (800) 423-4848. Gould Inc., Electronic Power Supply Division, P.O. Box 6050, El Monte, CA 91731.



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BEEHIVE INTERNATIONAL

"A proven competitive manufacturer of smart terminals"



Device simulator and communications protocol converter T/7 provides economical access to all IBM 3270 application programs or information systems from any popular ASCII asynchronous CRT terminal. It allows these terminals, operating in conversational mode, to appear as 3271-attached 3277 display stations to a System/370 or compatible host computer.

The converter takes into account operational characteristics that are unique to each terminal type, adapting for such characteristics as cursor positioning sequences. For other functions, it either simplifies keyboard operation for the operator or improves performance.

It adds value to existing terminals by providing smart terminal capabilities to low cost dumb ASCII display terminals. In addition, it permits multiple access for one or two hosts and concurrent support of a variety of terminal models. A 25th line option indicates line, column, and status.

Extra cost features include fractional redundancy, by which spare printed circuit boards stored in the

unit are switched into the system, in event of a board failure, to minimize downtime. A native mode switching feature allows a number of ports to be directed to a minicomputer and permits attached terminals to function under native language.

The device supports all 3277 function keys and the 3278 home key, cursor select key (light pen emulation), and program function keys 13 to 24. It may share a multipoint line with other T/7 units or other 3271-compatible cluster controllers.

Specifications

Supporting up to seven ASCII display terminals (optionally up to 15) at rates from 110 to 9600 bits/s full-duplex with automatic speed detection over direct, leased, or dial-up lines, the device communicates with the host site on one or two multipoint lines using Bisync protocol at modem-clocked rates up to 9600 bits/s. Where two synchronous lines are used, the maximum asynchronous line count is reduced by one. Interface is RS-232-C.

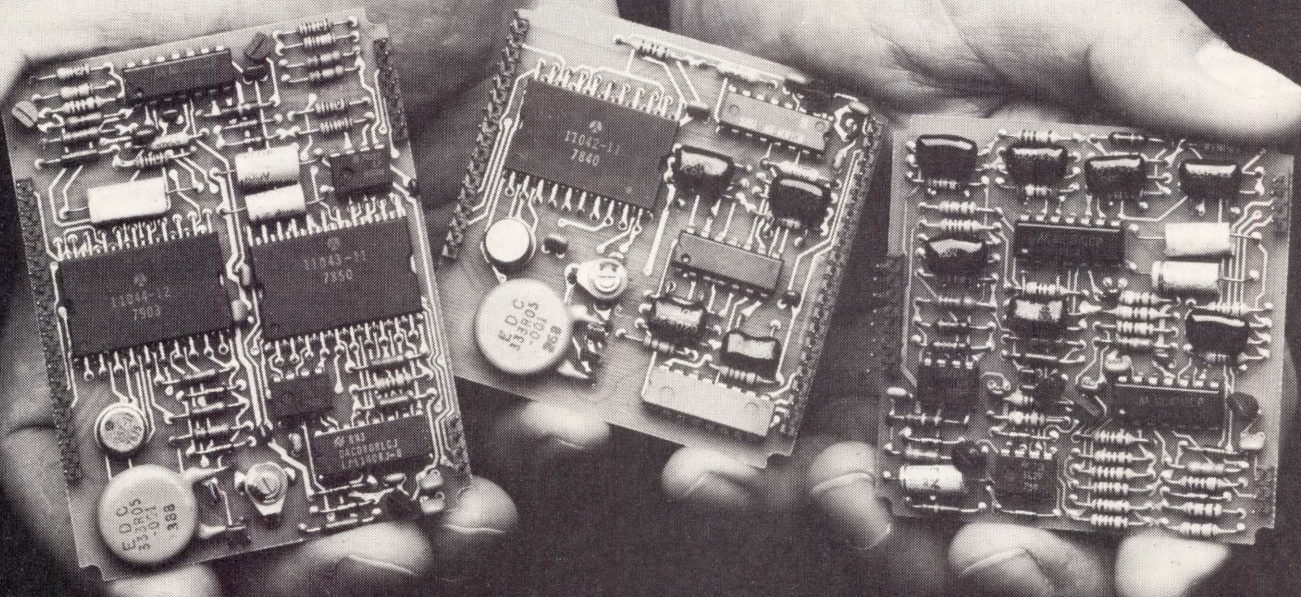
In desktop version the converter measures 19.3" W x 20.1" D x 9.1" H (49 x 51 x 23 cm). With cover removed the unit occupies 8.7" (22 cm) of height in a standard 19" (48-cm) rack. Its weight is 33 lb (15 kg). The power requirement is 115 Vac at 3 A or 230 Vac at 1.5 A, 47 to 440 Hz, single phase. Environmental parameters include 425-W heat dissipation with 106-ft³/min (3-m³/min) air flow, operating ambient temperature range of 0 to 40 °C, and 0 to 95% noncondensing relative humidity.

Price and Delivery

Single-unit price of the T/7 protocol converter is \$9350. In OEM quantities, the price is \$5145 each for lots of 100 to 199, \$4675 for 200 to 499, and \$4210 for 500 or more. Delivery is approximately 60 days ARO. Datastream Communications, Inc., 555 Ellis St, Mountain View, CA 94043. Tel: 415/965-9911.

For additional information circle 568 on inquiry card.

R24. The first 2400 bps modular modem.



**Rockwell's compact MOS-LSI modem
gives new physical design freedom.**

**Micro
Power**

Rockwell's R24 Modem is the most compact 2400 bps MOS-LSI modem available today. Its small size and modularity give designers a whole new form factor flexibility. Requiring only 25 square inches of system area, the R24 is ideal for terminals and communications equipment.

The R24 provides functional flexibility also. Of its 3 modules,

one is the transmitter, two the receiver. Terminal designers can offer transmit-only or receive-only options. And, the R24 is Bell 201 B/C and CCITT V.26 and V.26 bis compatible.

With its major functions in LSI circuits, the R24 is solid-state reliable and economical. It can be configured for operation on either leased lines or the general switched network. And, each low-

profile module can be plugged into standard connectors or wave soldered onto system PC boards.

A new generation of modems from the company that's delivered more high-speed modems than anyone in the world. That's Rockwell Micropower!

For more information, contact Modem Marketing, Electronic Devices Division, Rockwell International, P.O. Box 3669, RC 55, Anaheim, California 92803. (714) 632-5535.



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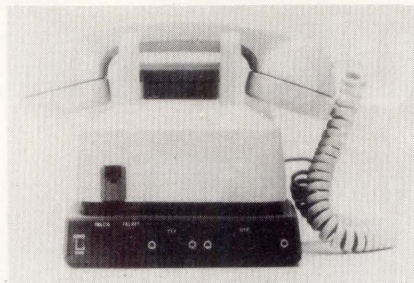
CD DATACOMM

CODE, SPEED, AND INTERFACE CONVERTER

Code translation and baud rate conversion in model 01-13-0090 converter are firmware (EPROM) programmed. 1k-byte RAM used as circular buffer stores input or output data when input baud rate is higher than that of output or when output conversion contains many more characters than input data. Unit accepts input and provides output of RS-232-C and/or current loop complete with battery and loop regulator. Among code translations are ASCII/TTY, TTY/ASCII, ASCII/EBCDIC, EBCDIC/ASCII, TTS/ASCII, ASCII/TTS, TTS/TTY, and TTY/TTS, Mexican or Spanish. Battery backup protects against transients and power failures. Device can also act as a protocol converter linking 2 computers. **Communication Devices Inc.**, 290 Huyler St, South Hackensack, NJ 07606.

Circle 569 on Inquiry Card

DIRECT CONNECT ORIGINATE/ANSWER MODEM



Full-duplex direct connect 300-bit/s originate and answer modem 103 O/A LP derives operating power from the telephone line and is fully compatible with modems in the WE103 family. Back panel switch selects either originate or answer transmit/receive bands and rocker switch selects either normal voice or data communications modes. A 25-pin RS-232-C socket provides interface to small computers, terminals, printers, and other peripherals. Modems are supplied with cables having RJ-11 modular connectors. **Universal Data Systems**, 5000 Bradford Dr, Huntsville, AL 35805.

Circle 570 on Inquiry Card

8- AND 16-PORT SERIAL I/O BOARDS

Eight-port serial asynchronous I/O board OCTOPORT™ connects line printers, modems, CRTs, and all types of RS-232-C or current loop terminals to S-100 based microcomputers and can also interconnect computers in networking systems. The board has 7 lines plus ground per port allowing it to be used for modem control. Features include realtime clock with selectable rates of 12.5, 25, 50, and 100 ms, and support for vectored interrupts in 8080 mode and Z80 mode 2. 12 selectable rates range from 110 to 19.2k baud. OMNIPOINT™ 16-port I/O board can communicate with up to 16 devices with RS-232-C interface at rates from 75 to 19.2k baud. It features 16 asynchronous channels with full handshake and has a 4-char buffer on each channel including the receive register. All operations except interrupt are enabled by push-on jumpers. Both boards meet all IEEE S-100 bus specifications. **Konan Corp.**, 1448 N 27th Ave, Phoenix, AZ 85009.

Circle 571 on Inquiry Card

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MDB makes synchronous communications interfaces for Q-Bus* and Unibus* that handle both bit and byte protocols.

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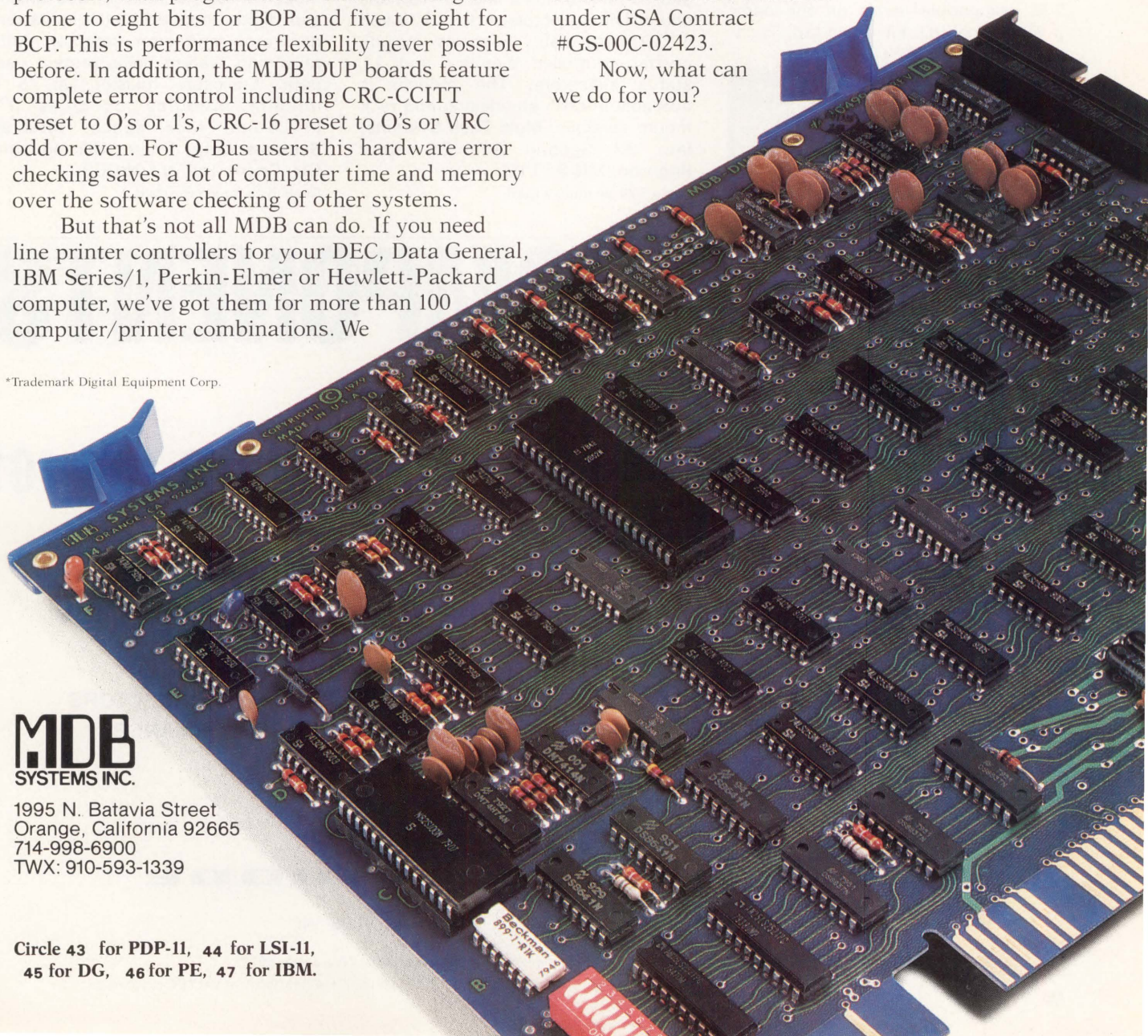
In addition to providing functional equivalency and software compatibility with DEC, the quad size MDB DUP-11 and MLSI-DUPV-11 interfaces will accommodate BI-Sync and DDCMP in byte-control and SDLC, ADCCP and HDLC bit-oriented protocols, with programmable character lengths of one to eight bits for BOP and five to eight for BCP. This is performance flexibility never possible before. In addition, the MDB DUP boards feature complete error control including CRC-CCITT preset to O's or 1's, CRC-16 preset to O's or VRC odd or even. For Q-Bus users this hardware error checking saves a lot of computer time and memory over the software checking of other systems.

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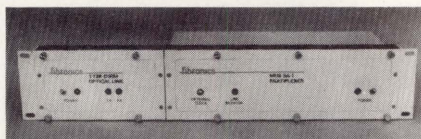
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Circle 43 for PDP-11, 44 for LSI-11,
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CD DATACOMM

8-PORT SYNCHRONOUS FIBEROPTIC MUX

Available in Europe, the MU8 SA-1 8-port synchronous/asynchronous multiplexer can transmit any combination of up to 8 duplex synchronous or asynchronous RS-232-C/V.24 channels. Data rates from 1.2k to 56k bits/s on each synchronous channel and from dc to 38.4k bits/s for each asynchronous channel can be handled by a single duplex fiberoptic cable over distances of more than 1 km. Internal and external clock synchronization and true handshaking features are standard. A total 2-sided system includes model TTK-D1 transmitter/receiver unit. The multiplexer uses TTL compatible levels on the composite signal I/O. **Fibronics Ltd**, Technion City, Haifa 32 000, Israel.



Circle 572 on Inquiry Card

ASYNCHRONOUS TO SYNCHRONOUS CONVERTER

Converter allows asynchronous data sources to communicate through synchronous single- or multiport modems, digital networks, TDMs, or encryption devices; 68- or 132-char buffer enables long message transmission even when synchronous data rate is not closely matched by that of asynchronous source. Buffer accommodates RTS/CTS handshaking delays and also allows asynchronous devices to be connected to a multidrop circuit. **Com/Tech Systems Inc**, 505 Eighth Ave, New York, NY 10018.

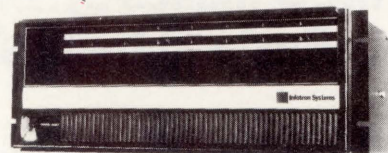
Circle 573 on Inquiry Card

300-BIT/s AUTO ANSWER MODEM

FCC-registered 300-bit/s modem FM327 provides automatic answering and RJ11 and RJ45 line connections and will directly replace Bell 113B and 113D data sets. Features include crystal controlled circuitry and 11 status indicators. The modem is available in both standalone and rack mount versions. **Multi-Tech Systems, Inc**, 82 Second Ave SE, New Brighton, MN 55112.

Circle 574 on Inquiry Card

300/1200-BIT/s DIRECT CONNECT MODEM

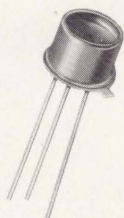


FCC-registered autoanswer modem DL 212B for central computer and remote multiplexer sites is compatible with all call-originating Bell 103, 113, and 212 data sets. The unit may be directly connected to the switched network without requiring a DAA. The modem operates 2-wire full-duplex at up to 300 bits/s asynchronous and at 1200 bits/s synchronous or asynchronous. It will automatically identify the calling modem and operating speed with no change to existing protocols. Master test module with 8 LEDs indicates status of selected modems. Diagnostics include analog and digital loopback, built-in pattern generator, and error detector. Anti-tailending feature helps protect user data. Enclosure housing up to 8 modem modules occupies 7" (17.8-cm) rack space. **Infotron Systems Corp**, Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003.

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Fully programmable, the 2653 packs a 128x2 RAM which distinguishes character classes. And that makes it easy to tell the difference between control and data characters—in EBCDIC, ASCII or six-bit codes.

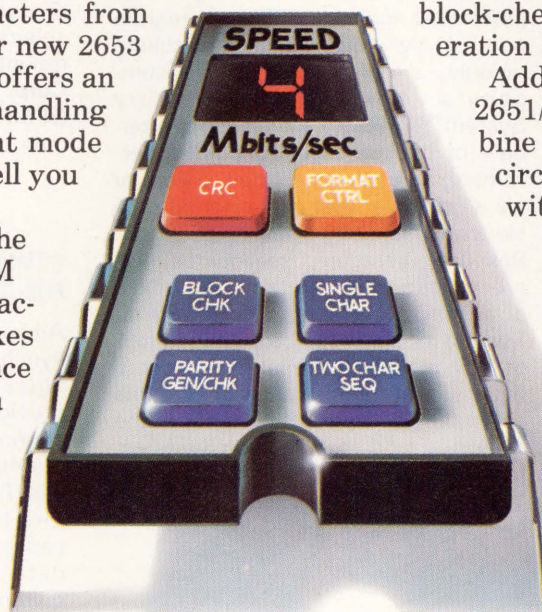
Riding atop your microprocessor's data bus, the 2653 *computes CRC intelligently and in parallel*. As a result, high-speed error detection via CRC is a breeze.

This powerful chip frees your CPU for other tasks. It also shrinks programming requirements, cuts design time and significantly reduces parts count. Specify the 2653 to lower your system development costs. And simplify error

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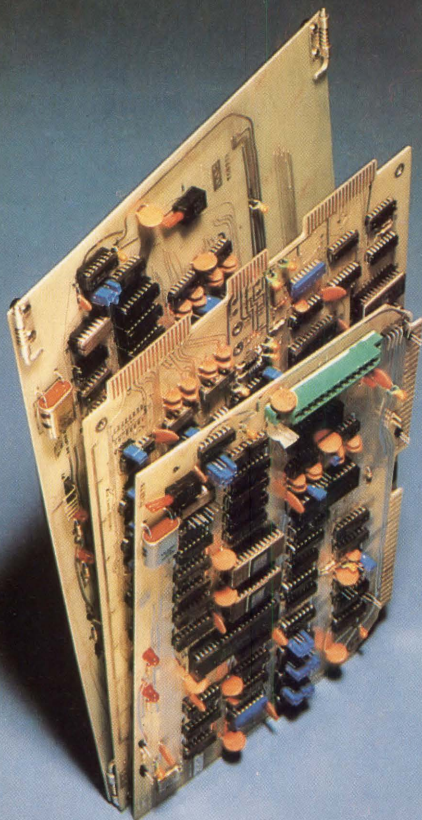
OEM's: Why Create Software For Protocol Conversion When We Have It Available Now?

Developing software to enable equipments with differing protocols to communicate is expensive and time consuming.

Air Land Systems has already created software programs that enable various types of terminals and computers to communicate in most IBM, Honeywell, UNIVAC and BURROUGHS protocol environments.

We'll build a protocol converter (with the necessary firmware which we have already developed) to fit into your equipment's card cage or we'll package it as a stand-alone unit.

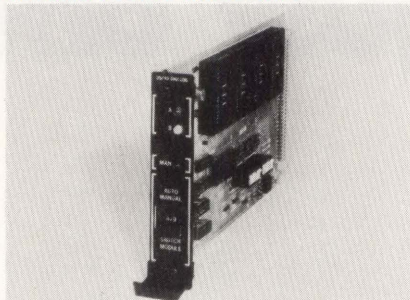
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NETWORK SWITCHING UNIT



Fallback or resource switching can be performed manually or under program control by the DS/40 switching module, a component of the company's Network Supervisory System™. Fallback switching to alternate or backup facilities can be performed manually by a single switch or via a controller that can automatically switch up to 256 lines or channels. Resource switching reallocates network resources to accommodate changing operator applications. System modules can be switched to 1 of 16 different preselected reconfiguration programs, each of which is entered by setting DIP switches in the individual modules. **Digi-Log Systems, Inc.**, Babylon Rd, Horsham, PA 19044.

Circle 576 on Inquiry Card

COMMUNICATION PROCESSORS

CP 9558 and CP 9572 offer up to 8 times the effective power of entry level CP 9552 processor announced earlier. CP series systems interlink remote EDP operations and local networks of terminals with each other and with central computers to form data networks of virtually any size. They can operate with other vendors' mainframes and terminals and can interface with packet switched networks. CP 9558 systems can have up to 6 processors and from 393k to 1.2M bytes of memory. CP 9572 can have up to 8 processors and 1.5M bytes main memory. Instead of a single multipurpose CPU, the systems use a number of autonomous simultaneously operating processors, each optimized and dedicated to a specific function. All processors operate concurrently and at their respective maximum rates. Comprehensive system software is licensed and priced separately. **Burroughs Corp.**, Detroit, MI 48232.

Circle 577 on Inquiry Card

READER/PUNCH CONTROLLER

Used in standalone mode or with other terminals and modems operating at 50, 75, 100, 110, 200, or 300 baud, RPC-586 reader/punch controller operates with 5- or 8-level codes in half-duplex communications circuits. Operating speed is 30 char/s max. Integral power supply requires 115 Vac, 60 Hz. Unit may operate on- or offline and can cut a tape blind while remaining online. Circuit breaker, two 25-pin connectors (for modem and terminal), half/full-duplex selector, and power switch are mounted on the rear panel. **Siemens Corp.**, 186 Wood Ave S, Iselin, NJ 08830.

Circle 578 on Inquiry Card

COMMUNICATION MULTIPLEXER FOR 990 FAMILY

Any mixture of asynchronous and synchronous channels may be configured on the CM990-1 board that provides 8 independent full-duplex channels between the Texas Instruments' 990 family of computers and RS-232-C peripheral equipment. The board supports modem control capability and 110- to 9600-baud data transfer rates. Power requirements are 5 Vdc at 980 mA, 12 Vdc at 125 mA, and -12 Vdc at 12 mA. The multiplexer is mounted on a 14.25 x 10.8" (36.2 x 27.4-cm) epoxy glass PC board. **National Data Corp.**, 1 National Data Plaza, Corporate Sq, Atlanta, GA 30329.

Circle 579 on Inquiry Card

DATA TRANSMISSION LINE DRIVERS

Complementing the company's existing family of line receivers, quad differential line drivers DS3487 and DS26LS31 are designed for digital data transmission over balanced lines. Both drivers feature single 5-V supply operation, LS-compatible inputs, and TRI-STATE[®] outputs. Typical input to output delay is 10 ns. The devices, built to meet EIA RS-422 interface standards, are packaged in 16-pin molded DIPs. Four independent driver chains are contained in a single package. **National Semiconductor Corp.**, 2900 Semiconductor Dr, Santa Clara, CA 95051.

CD DATACOMM

FIBEROPTIC TRANSMIT/RECEIVE MODULES

Fiberoptic TTL modules series 2100 are designed for high rfi immunity and with rugged construction required in harsh industrial environments and in high data security applications. Transmitter module operates in the 820-nm region using an LED source; receiver employs a PIN detector. Units are compatible with any fiberoptic cable terminable by Amphenol 905 series optical connectors furnished with the units. Additional vibration, moisture, and shock resistance for military applications can be furnished as an option. **Optelecom, Inc.**, 15940 Luanne Dr, Gaithersburg, MD 20760. Circle 582 on Inquiry Card

INFORMATION DISPLAY SYSTEM ENHANCEMENTS

Addition of 3440-char screen capacity and support of 9600-bit/s data communications has extended the capabilities of the PTS-2000 information display system (Computer Design, July 1980, p 28). PTS-2000 terminals operate as IBM 3270 types under both BSC and SDLC. The 3440-char display is configured as 43 lines of 80 chars on the 15" (38.1-cm) CRT screen. No additional charge is levied for the 9600-bit/s capability, but users must install modems operating at that rate. **Raytheon Data Systems Co.**, 1415 Boston-Providence Tpk, Norwood, MA 02062. Circle 580 on Inquiry Card

FIBEROPTIC INTEGRATED DETECTOR/PREAMPLIFIER

Functions of a sensitive photodiode detector and a transimpedance amplifier are contained on the single-chip MFOD404F. Device has responsivity of 30 mV/ μ W at V_{CC} of 5 V and will sustain data rates of 10M bits/s over medium distances (up to 500 m). Unit is designed for use with the AMP compatible metal fiberoptic connector barrel to provide rfi immunity. 200- Ω output impedance also provides less sensitivity to stray interference. Recommended input wavelength is 900 nm. **Motorola Semiconductor Products Inc.**, PO Box 20912, Phoenix, AZ 85036. Circle 581 on Inquiry Card

MULTIPLEXER/MODEM PACKAGE

Transmission system MTS-1 combines a series II MICROPLEXER™ and a 9600-bit/s modem in a single package for convenience in statistical multiplexing of up to 8 asynchronous or synchronous channels. System permits per-channel parameter programming to allow many different types of terminals, printers, and other peripherals to share a single telephone line. Local and remote loopback at both channel and data link levels is provided, as well as functional displays and fallback to 4800 bits/s in event of line degradation. Supervisory port option provides network performance statistics. System is available in either 4- or 8-channel configuration. **Timeplex, Inc.**, One Communications Plaza, Rochelle Park, NJ 07662. Circle 583 on Inquiry Card

COMMUNICATIONS SYSTEM TESTER/MONITOR

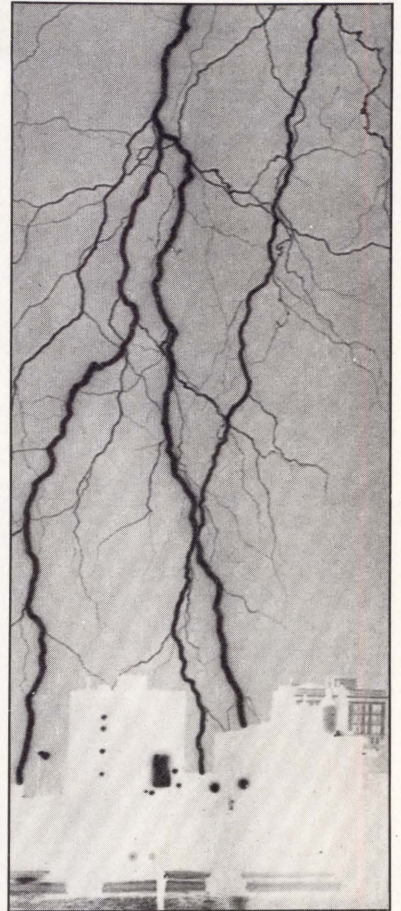


Programmable software based Dyna-Test™ 2000A monitors and traps data at 19.2k bits/s full-duplex, internally or externally clocked, with English or hexadecimal data display. All common data formats can be accommodated. Menu selection of such functions as monitoring, BERT, fox message generation, and various timing measurements is provided. Unit stores data including lead status for each character on a 200k-char tape. Macromode feature permits construction of custom programs from a list of approx 80 instructions. Data captured in the 4k-char buffer or on tape may be transmitted to a serial ASCII printer. An RS-170 output is available to drive an external CRT. The instrument contains a CRT, full keyboard, tape drive, and interface breakout panel. **Dynatech Data Systems**, 7644 Dynatech Court, Springfield, VA 22153. **CD**

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Guaranteed failsafe protection for computers, modems, data terminals. Stops 20,000 Amps lightning hits in 1 picosecond. Available as standalone, rackmount or OEM pcb module. From \$100 to \$500.

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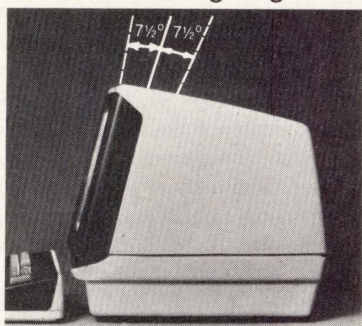
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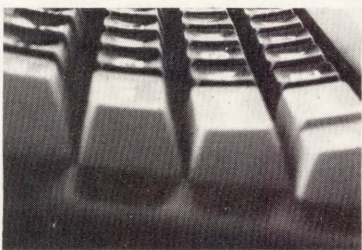
Smart moves

To make life easy for the operator, Hazeltine has added a few smart moves to the new Executive 80™ terminals.

The tilt feature lets you move the screen to the best viewing angle. The detachable



Tilt screen means more comfortable viewing.



Keys are precisely contoured for the most natural typing position.

keyboard can be moved to the best orientation for the working environment. The combination helps operators work comfortably, with less physical fatigue.

The typing position of the keys has been redesigned. The Executive 80 has a contoured, low profile keyboard where each row of keys has its own operating angle. It makes prolonged typing a lot less tiring.

Then there are smart moves you can make on the screen. You can vary the intensity, designate reverse and blinking fields, underline and even draw out forms. If you are working with full documents, you can order the 15-inch smooth scrolling monitor which lets you selectively display either 80 or 132 column formats, in normal size or double height and width. They're all features that make it easier to focus in on important data.

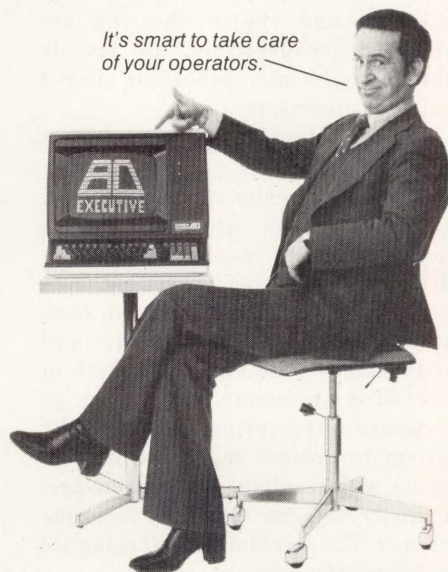
Whichever operating mode you select, you will be working with an anti-glare screen that's set into a non-reflective working surface. That means less eye fatigue.

Operator comfort and convenience mean higher operator productivity, which increases throughput and reduces costs. That's one more reason why Hazeltine Executive 80 is your smart move for the eighties.

Hazeltine Corporation, Computer Terminal Equipment, Greenlawn, NY 11740 (516) 549-8800 Telex: 96-1435 Hazeltine and the Pursuit of Excellence.

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TECHNOLOGY REVIEW

Multilevel Function Processor Concept Extends Multiprocessor Architecture

The B 5930 computer system, with 50% of the performance of the B 6900, is an entry level large scale data processing system that uses multilevel function processor architecture. This design, an internal structure of computers within computers, uses programmable microprocessors, each with its own memory in place of fixed purpose circuits. With this architecture, Burroughs Corp, Detroit, MI 48232, has combined high productivity with significant reductions in physical size and power requirements.

Multilevel function processor architecture as used in the 5930 is an extension of the internal multiple processor architecture used in other 900 family computers. In place of a single processor, these systems use multiple processors, each assigned a function. Operating concurrently they share the workload and offer high system productivity. In the 5930 major functions such as I/O control, data communications control, memory control, computation, and system checking are assigned, respectively, to largely autonomous microprocessor based function processors.

The central processing unit, which is a function processor, consists of a second tier of function processors each having its own area of responsibility—memory access control, instruction transfer and decoding, control code storage and execution, computation, message transfer, and maintenance. This implementation of imbedded processors, also known as recursive structuring, enables the system to achieve high internal efficiency with resultant high system productivity without resorting to exotic circuits. The machine is built using LSI logic and 16k memory circuits.

Internal CPU function processors transfer data to and from each other across a wide bidirectional bus that is capable of transferring a full 52-bit computer word (48 data bits), versus the 8-, 16- or 32-bit width common to other bus oriented machines. This wider bus enables the processor to

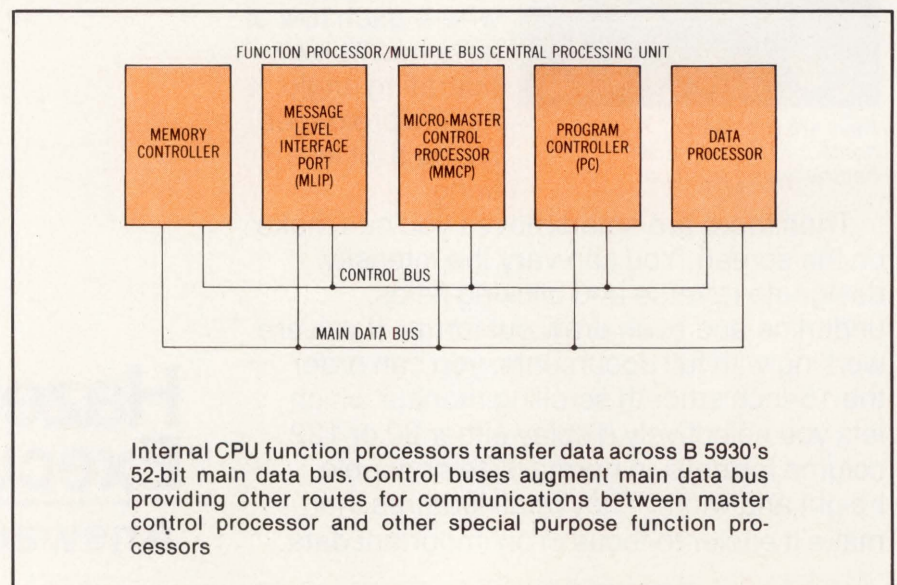
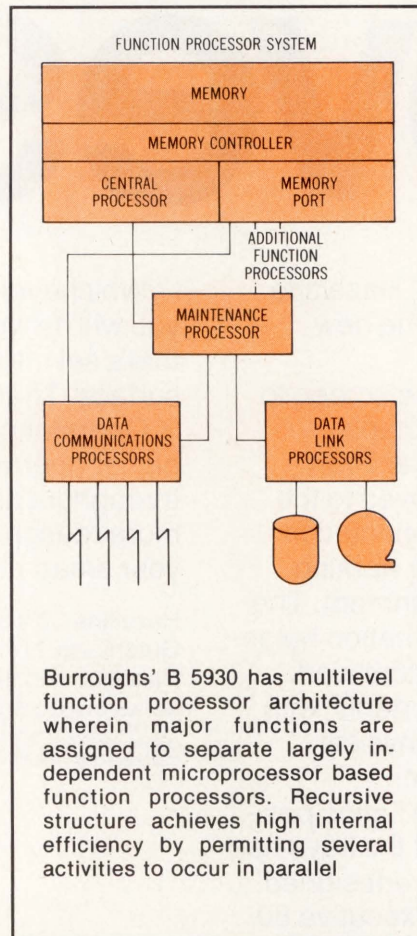
work on more data in parallel, and results in a high degree of reliability by providing for full-time, in-line error detection. Additional special purpose buses augment the main data bus.

One internal CPU function processor, called the micro master control processor (MMCP), coordinates the activities of the others. The MMCP contains a microcoded implementation of the full instruction set of the company's B 6000 class large scale systems. The other internal function processors (I/O control, program control, data processor, memory control) are programmed to execute this large system instruction set, thus providing program compatibility with B 6000 and larger systems.

To achieve this combination of productivity and intersystem compatibility, Burroughs devised an internal programming language for the MMCP. An extremely powerful high level computer language, it is based on extensive research into proper control structures. Each of its commands communicates hundreds or thousands of sequenced instructions. This internal language is transparent to the computer user; application programs are prepared using familiar programming languages—ALGOL, COBOL, FORTRAN, PL/1, BASIC, APL, RPG.

Information is transferred to and from peripheral devices through microprocessor based function processors. These data link processors (DLPs) relieve the central system of housekeeping tasks associated with I/O.

(continued on page 106)



A whole world. Because our parent company, C. Itoh Co., Ltd. (pronounced "C. Eetoe") is a multinational organization with resources and subsidiaries located in every corner of the globe.

As C. Itoh Electronics, Inc., we're fortunate to be part of this international network. It lets us seek out quality materials and technologies wherever they can be found. And for a company that specializes in computer peripherals for the OEM, that's just as important as price or the capability to deliver.

Today, we're offering the latest designs in dot matrix and daisy wheel printers, card readers, CRT monitors, floppy disk drives, and a lot more.

We're also seeing to it that our OEM customers get all the support they need. The engineering support to solve their system integration problems. Plus complete documentation and a service network that oper-

ates repair and refurbishment stations nationwide.

So when you deal with us, you can be sure you're doing business with people who are dedicated to the OEM. And a company whose parent organization has been around since 1858.

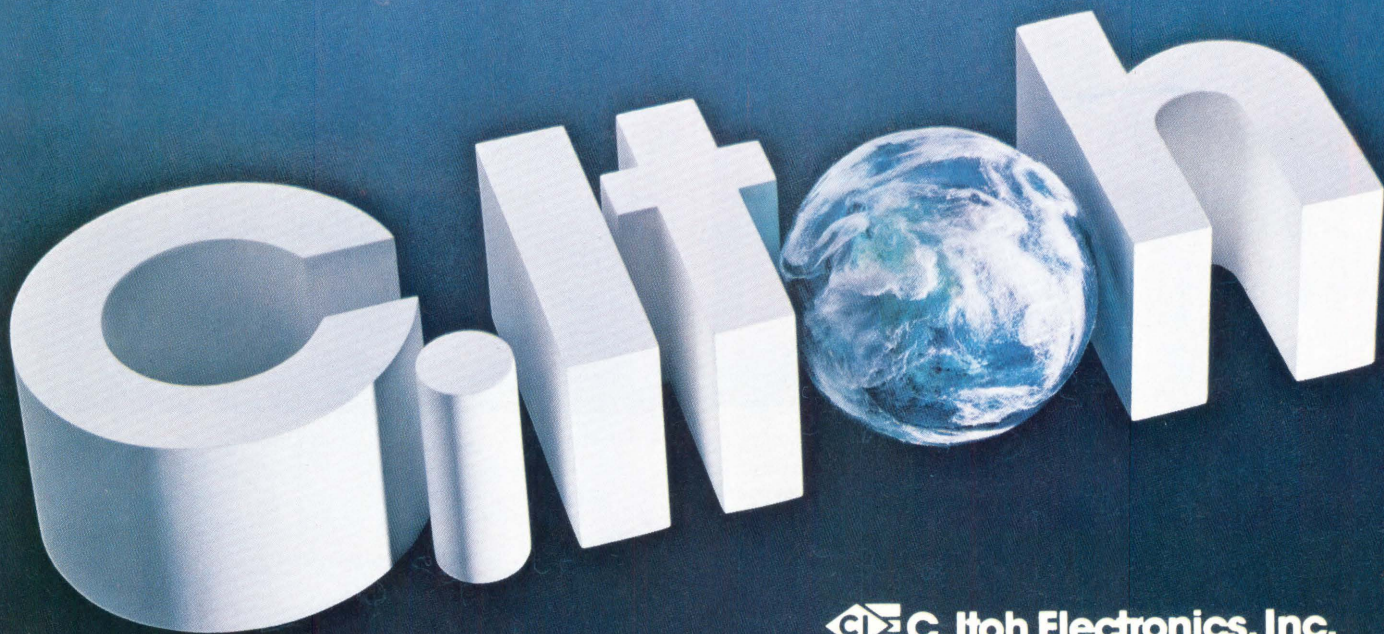
Our goal? To become the best OEM peripheral source in the country. Because with all our international connections, we haven't forgotten what our motto promises: One world of quality.


For information on our product lines for the OEM computer systems manufacturer, contact C. Itoh Electronics, Inc., 5301 Beethoven St., Los Angeles, CA 90066, Tel. (213) 390-7778; Midwestern Regional

Office: 240 East Lake St., Suite 301-A, Addison, Illinois 60101, Tel. (312) 941-1310; Eastern Regional Office: 666 Third Avenue, New York, NY 10017; Tel. (212) 682-0420.



A world of quality.



 **C. Itoh Electronics, Inc.**
One world of quality

Tektronix' new 7D02. logic analyzer with the

Now, a total solution to problems encountered either on or off the bus. Tektronix' new 7D02 Logic Analyzer. Featuring a unique user language that reduces even the most complex testing to a few simple statements. You supply the overview and the 7D02 does all the detail work for you. With a sophistication never before possible.

A simple, yet sophisticated user language.

Writing a test program is no more complicated than responding to a few simple prompts. A handful of basic phrases let you configure the 7D02's resources into almost any combination needed to solve the problem at hand. Often you'll find the 7D02 has an intelligence equal to the software you're integrating into your prototype.

Individualized 8- and 16-bit mnemonics.

Through a series of personality modules, the 7D02 can adapt to the characteristics of specific microprocessors. Familiar mnemonics let you work faster and more accurately. Support today extends to the 6800, 6802, 8085, 8086, Z80 and Z8002 with more to come. There's also a personality module available for general purpose logic analysis.

Up to 52 channels of information.

Flexibility is the key. You start with the basic 28 channels used for state acquisition, then the expansion option increases this to 44. For timing applications or wider state acquisition, there's an additional synchronous or asynchronous 8-channel timing option complete with its own memory, word recognizer and glitch trigger.

```

TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=3000
1 /NMI=X /IRQ=X FETCH=X R/W=X
1 BA=X INVAL OP=X EXT TRIG IN=X
1 TIMING WR=X
1 THEN DO
1   1
1   1 COUNTER # 1 2-MS
1   1 2-RESET AND RUN
1   1 GOTO 2
1
END TEST 1
TEST 2
2IF
2 WORD RECOGNIZER # 2
2 DATA=XX
2 ADDRESS=F820
2 /NMI=X /IRQ=X FETCH=X R/W=X
2 DISPLAY ← PROGRAM
    
```

All test parameters supplied by prompts.

IF clause defines a data stream event, which may be either single or compound.

THEN clause defines a response to the event. In this case, setting counter #1 to zero and then incrementing every millisecond.

At the same time the counter is set, branch to the second test. (bracketing allows simultaneous actions).

```

END TEST 1
TEST 2
2IF
2 WORD RECOGNIZER # 2
2 DATA=XX
2 ADDRESS=F820
2 /NMI=X /IRQ=X FETCH=X R/W=X
2 BA=X INVAL OP=X EXT TRIG IN=X
2 TIMING WR=X
2 THEN DO
2   1
2   1 GOTO 1
2 OR IF
2   1 COUNTER # 1 = 00100 2-MS.
2 THEN DO
2   1 TRIGGER 0-MAIN
2   1 0-BEFORE DATA
2   1 0-SYSTEM UNDER TEST CONT.
2   1 0-STANDARD CLOCK QUAL.
2 END TEST 2
2 DISPLAY ← PROGRAM
    
```

The 7D02 now monitors the data stream for an event to satisfy the second test's IF clause.

If the event occurs, then branch back to the first test and start the program over.

Or if counter #1 has reached 100 mS, then activate the trigger.

7D02 LOGIC ANALYZER

A user-programmable smartest triggering ever.

And there's more. The 7D02's user language takes advantage of four separate word recognizers, each up to 48 bits wide. Plus two counters usable in either the time or event mode. In addition to clock qualifications, there are two types of data qualification to provide selective data storage.

The Tektronix 7D02 Logic Analyzer can give you a whole new approach to μ P-based design.

Locating an intermittent fault. The following program gives a limited demonstration of the simplicity and power behind the 7D02's user language. Here the object is to trigger when a second event on the bus does not occur within 100 ms of a first event.

CTR1=00100 MS		TRIG LOC = 015	
CTR2=00000 EUT		TRIG IN TEST 2	
LOC	ADDRESS	OPERATION	TRQ/NMI
010	F834	BNE \$F82C	11
011	F835	F6 READ	11
012	F82C	INC \$0006	11
013	F82D	00 READ	11
014	F82E	06 READ	11
015T	0006	02 READ	11
016	0006	03 WRITE	11
017	F82F	BEQ \$F865	11
018	F830	04 READ	11
019	F831	TST \$0004	11
020	F832	00 READ	11
021	F833	04 READ	11
022	0004	0F READ	11
023	F834	BNE \$F82C	11
024	F835	F6 READ	11
025	F82C	INC \$0006	11
026	F82D	00 READ	11
DISPLAY ← ACQMEM 0-MAIN			
M-MNEMONIC			
0 ABSOLUTE			
1 MNEMONIC			

By using the proper personality module, software flow can be displayed using the mnemonics of the chip under test, here the Motorola MC6802.



The 7D02 is a 3-wide plug-in for the popular Tektronix 7000 Series oscilloscope. Shown above is a Tek 7603 mainframe housing the 7D02 logic analyzer with a personality module supporting the 6802 microprocessor.

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Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312

Canada Tektronix Canada Inc., P.O. Box 6500, Barrie, Ontario L4M 4V3, Phone 705/737-2700

These specialized processors each include one or more microprocessors, interface, and buffer memory. Aggregate I/O bandpass is 2.3M bytes/s. An I/O base module, which houses up to eight DLPs, can be connected to as many as four central processors. Any DLP can be switched from one processor to another under MMCP control. Other function processors called line and network support processors provide external control for data communications and networking. This functional distribution of the control workload eliminates unnecessary contention for central processor resources and enables efficient operation in situations that call for coordinating multiple data processing tasks with dynamic data communications requirements.

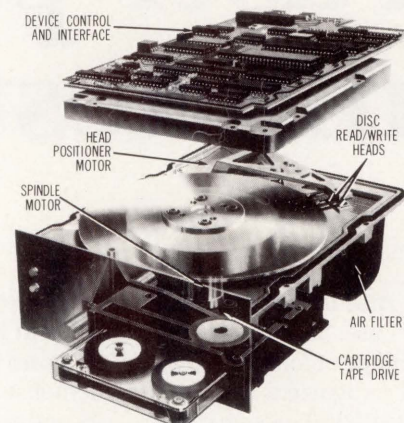
Because of its programmable logic the function processor concept offers ready adaptability to future requirements in application and cost/performance, and to future

developments in circuit technology. System reliability is enhanced by the CPU's constant tests on its own operation, and its ability to detect and correct errors each time data is transferred internally. Maintenance is eased by simplified construction.

In a basic configuration the 5930 consists of CPU with 1.5M bytes of main memory, two operator displays, peripheral subsystem with five data link processors, data communication subsystem with line support processor and four line adapters, and maintenance processor. Expansion options provide up to 6.2M bytes of main memory in 786k-byte increments, up to 32 data link processors for peripheral subsystem attachment, up to 2 line support processors of 16 lines each, and up to 2 network support processors with 64 lines each. Starting price for a system is \$200,000. Customer shipments are planned to begin during 2nd quarter 1981.

Circle 417 on Inquiry Card

Micro-Winchester Drive Incorporates Integral Cartridge Tape Backup



Single tape cartridge integrated into 5.25" Winchester disc drive package supplies backup storage for entire contents of 10M-byte platter. Average access time to data on model 510 MicroWinchester from Irwin International is 25 ms, almost seven times faster than comparable units

A 5.25" (13.3-cm) Winchester disc drive system with integrated cartridge tape backup fills the four major demands made on small disc drives. In the unit, Irwin International, 2000 Green Rd, Ann Arbor, MI 48105, has incorporated greater storage capacity, reliable backup, faster access time, and low price.

Memory capacity of the 510 Micro-Winchester unit is 12.3M bytes unformatted, 10.02M bytes formatted. This is achieved using one disc platter. All formatted data can be dumped in less than 4 min onto a single backup tape cartridge. Unlike systems using floppy disc backup, the unit requires no sophisticated software for selective dumping and no repeated stops and starts to change media. By fully integrating cartridge tape backup within the unit overall package dimensions are kept no larger than the standard minifloppy. Tape backup removes easily for storage. Cartridges are interchangeable.

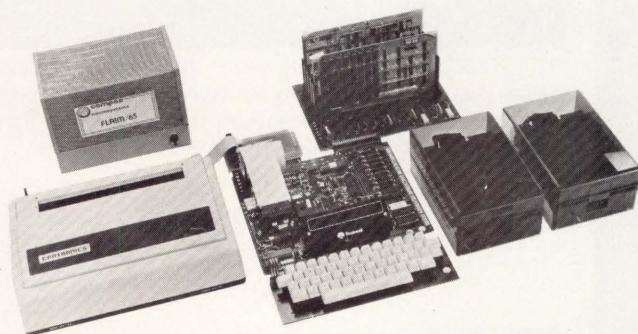
Access time to data written on disc is an average 25 ms, nearly twice as fast as 8" (20-cm) Winchesters. Maximum

(continued on page 108)



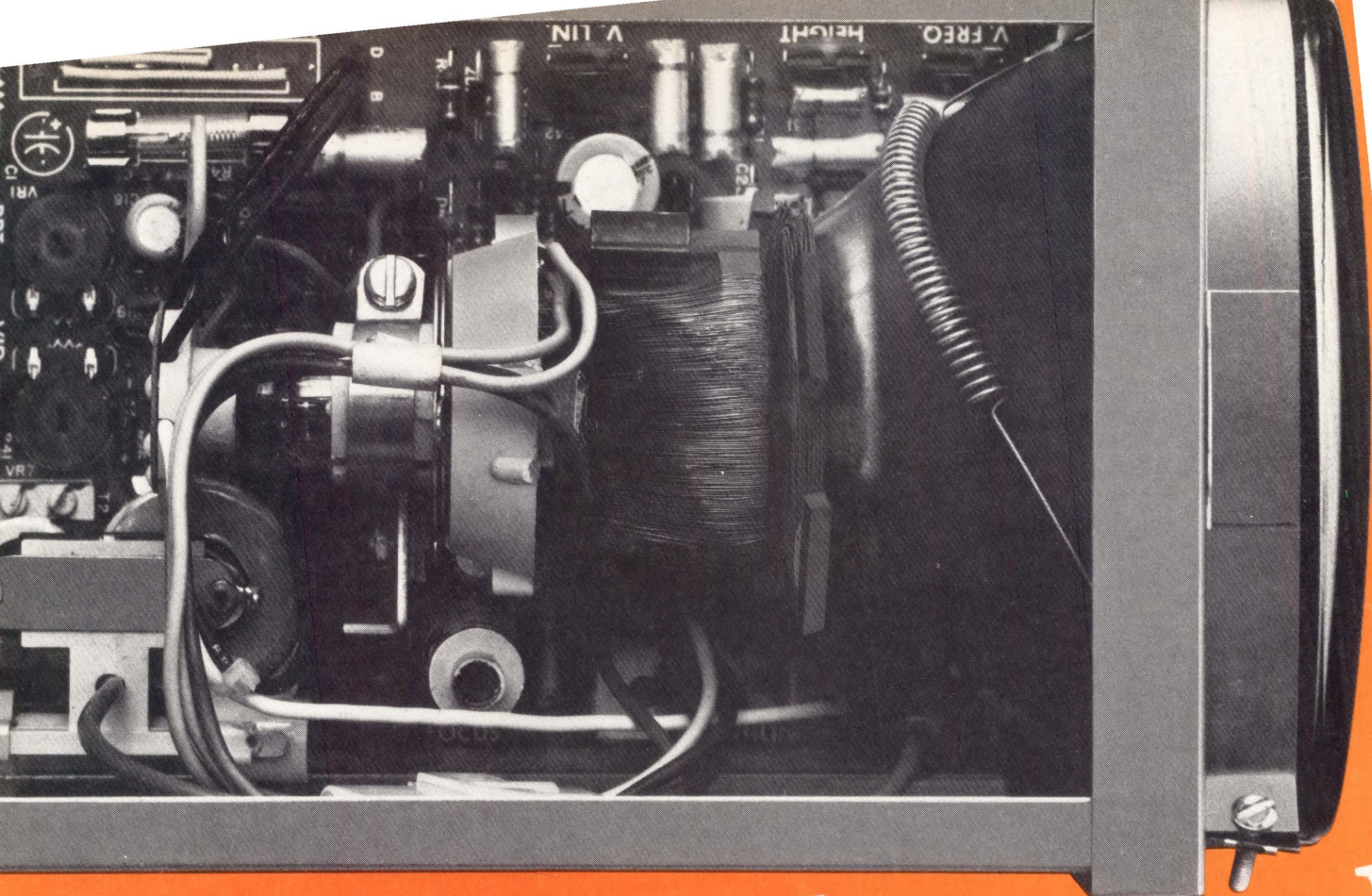
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FLAIM/65



FLAIM/65 is a complete, professional quality development system for the 6500 microprocessor family. FLAIM/65 includes a ROCKWELL AIM 65 (with 20 character display and thermal printer plus full size keyboard), five slot motherboard, 16 K static RAM memory, dual drive 5 1/4 inch disk system with full operating system in EPROM, CENTRONICS 730 dot matrix printer (100 CPS), assembler, PL/65 compiler and full system power supply. Best of all — the system pictured is priced well under \$4000 (U.S. only).

224 SE 16th St. P.O. Box 687 AMES, IA 50010 (515) 232-8187
CIRCLE 53 ON INQUIRY CARD



Audiotronics Model DC-946 Data Display

actual size

This popular Audiotronics data display is one of our 48 standard models. We have sold thousands of them to giants in the industry. Maybe it's perfect for your requirements. If not, talk to us about your specifications. We're dedicated to innovative product design, quality production standards and complete customer satisfaction. Whatever you need, we have the experience and talent to design it, or improve it. Contact us today.

Model DC-946 features:

- modular construction
- 5" cathode ray tube (12.7 cm)
- solid state
- DC operation—12V dc inputs
- choice of signal inputs:
 - TTL (standard)
 - Composite video (plug-in module)
- standard 15,750 KHz horizontal scan frequency
- 650 lines resolution



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CIRCLE 54 ON INQUIRY CARD

Termination System Improves Cables' Electrical Characteristics

access time is 45 ms. The unit's 5.3M-bit/s data transfer rate maximizes the speed and efficiency of systems.

To achieve high storage density the system uses a smart servo positioner instead of a stepper motor. Location information is imbedded on the disc. A closed loop servo controlled by a microprocessor brings the head directly to the correct track, compensates for disc eccentricity, and keeps it precisely on track. Speed of the spindle is regulated to 0.1% and a microprocessor eliminates static error. Together the positioner and spindle systems provide the ability to record 900 tracks/in (354/cm) at a density of 8000 bits/in (3149/cm). Fast access time also stems from the positioner. Microprocessor control allows faster arm movement, and lack of such error allows essentially zero settling time. By rotating the disc at 4000 r/min instead of 3600 r/min, average latency is reduced to 7.5 ms.

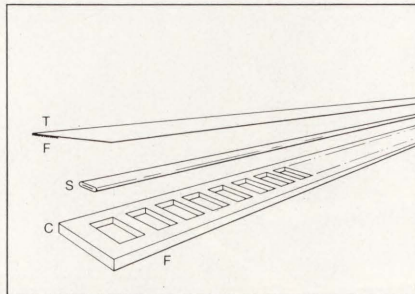
Tape cartridges are also prerecorded with servo information. This embedded servo approach allows a single positionable head to cover seven discrete track positions and permits a tape speed of 60 in (152 cm)/s to be achieved. These factors coupled with a bit density of 10k bits/in (3937/cm) provides 10M-byte capacity on a 140-ft (42-m) cartridge, and permits fast dumping.

Controller design is simplified; since disc drive and backup are integrated, there is only one logically consistent interface to deal with. The device level interface is a subset of the proposed ANSI standard for 8" Winchester.

The unit's 3.25 x 5.75 x 8" (8.2 x 14.6 x 20-cm) dimensions, mounting holes, and voltage requirements match those of the industry standard minifloppy. The unit can be mounted either horizontally or vertically. Heat dissipation is only 35 W. MTBF is estimated at 8000 power-on hours.

In OEM quantities of 500 the units are priced at \$1500 each. Evaluation units will be available in January. Volume production is scheduled to begin by May.

Circle 418 on Inquiry Card



Raychem's ribbon cable termination system uses SolderQuik tape to cut assembly time. Strip consists of cover (T) that holds solder (S) in position. Control layer (C) has windows corresponding to terminal spacings and serves to channel solder toward joints. Flux coating (F) faces metal to be cleaned. Photo shows strip in place on cable connector

SolderQuikTM terminates ribbon cable leads as much as 50% faster than either hand soldering or paddleboard methods, delivering solder quickly and accurately on closely spaced joints that are difficult and time consuming to do by hand. The system, developed by RayChem Corp, 300 Constitution Dr, Menlo Pk, CA 94025, utilizes solder filled plastic strips, each with up to 100 premeasured terminations, and produces finished cables with better electrical characteristics for computer and other digital logic applications, including less crosstalk and noise, and fewer signal mismatches.

The solder delivery strip shown in the diagram consists of soldering flux, solder, and a carrier strip. The top cover (T) is polyparabanic acid film coated with adhesive. The total thickness is less than 0.005" (0.012 cm) to allow thermal energy to pass through easily. The adhesive holds the solder (S) in correct lateral position and on the overhang provides a means of attachment to the connector. The solder (S) is a flattened, flux cored eutectic tin lead solder of a suitable size to provide for bonding the range

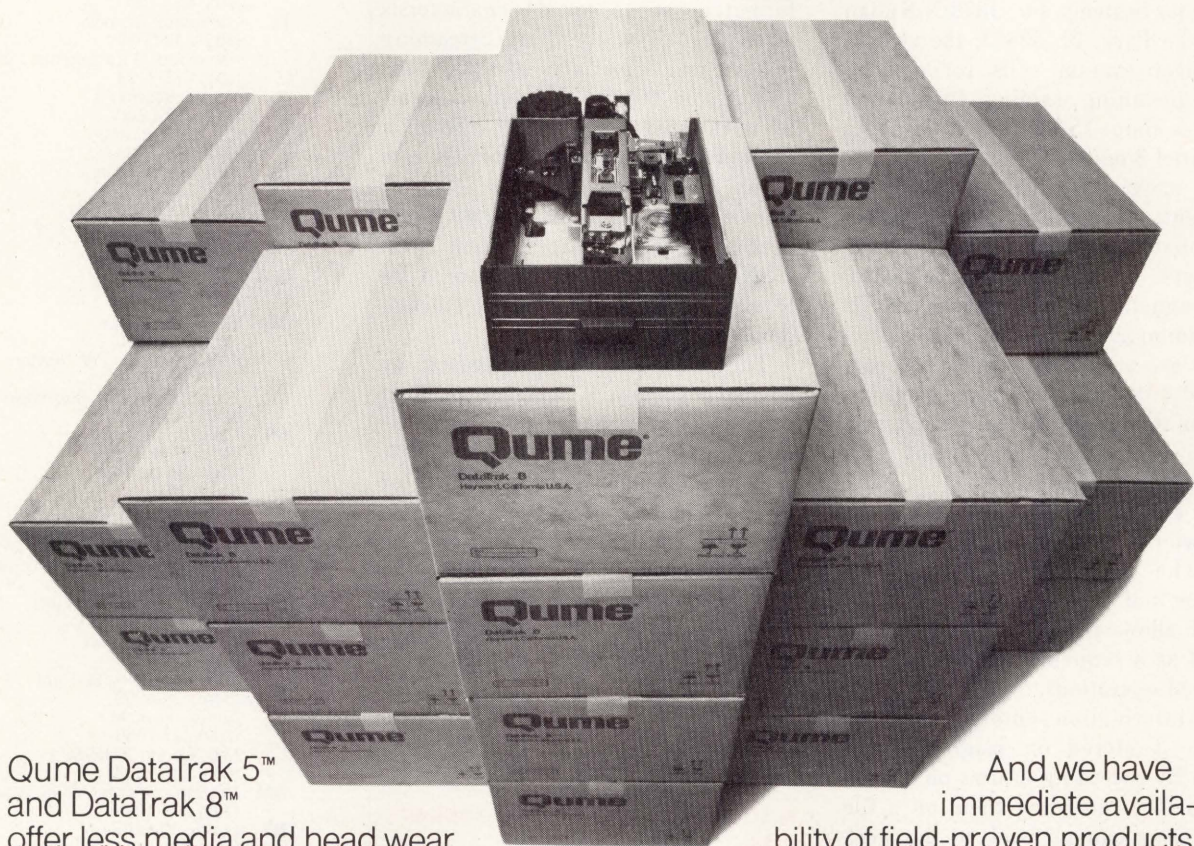
of wire diameters to the terminals. The solder is oriented crosswise to the conductor axis, initially "shorting out" all the circuits. The flux core is optional, providing a margin of redundant cleansing. The control layer (C) is fabricated from irradiation cross-linked polyvinylidene fluoride sheet having windows which correspond to the spacing of the wire terminals. During solder melting, the barriers divide the solder evenly between terminals. After the flux cleanses the joints and solder is molten, the window barriers channel the solder flow to form well shaped, uniform joints. A flux coating (F) is applied to the surfaces facing metal to be cleaned. The principal area is the windows where the flattened solder is exposed. To promote wetting of the grounding wires on the bus bar, flux is also applied next to the control layer on the overhang. Components are laminated together to form a tape less than 0.020" (0.051-cm) thick and 0.25" (0.635-cm) wide. It is packaged in spools and dispensed as required per connector length.

The system greatly simplifies cable terminations with what is essentially a 2-step process. After the conductor leads of a flat ribbon cable have been stripped with a conventional stripper, the leads and molded cable connector are inserted into a cable termination fixture along with a strip of the SolderQuik tape, which is placed directly over the leads to be terminated. A holding module, which contains the cable/connector/SolderQuik assembly is then removed and placed in an infrared heater for 15 to 20 s. During the heating process, infrared rays pass through thermoplastic windows in the tape, melting premeasured solder/flux packages so that they flow over the stripped leads and connector bus bar and form uniform terminations. The holding module is then removed from the heater, after which the plastic from the tape can be peeled off or left on the terminations for added protection.

Finished terminations are generally superior to those produced by wave soldering or vapor phase heating, and are more uniform than hand soldered terminations. The system eliminates the bridging associated with wave soldering. By providing exact amounts of solder and flux distributed precisely, it guarantees strong uniform joints.

Circle 419 on Inquiry Card

More tap-tap on tap.



Qume DataTrak 5™ and DataTrak 8™ offer less media and head wear than any other double-sided floppy disk drive on the market. That means less service cost and more disk life.

Look how they stand up to the competition. Independent tests have shown a tenfold improvement in error rate over industry-standard specifications.

	Qume Performance	Standard Specifications
SOFT ERROR	1 in 10 ¹⁰	1 in 10 ⁹
HARD ERROR	1 in 10 ¹³	1 in 10 ¹²
SEEK ERROR	1 in 10 ⁷	1 in 10 ⁶

And we have immediate availability of field-proven products, with production capabilities to meet your needs. So you can order our double-density, double-sided floppy disk drives for delivery now.

So what's it all add up to? More tap-tap, better performance, immediate availability and prices that won't boggle your memory. For an evaluation unit, hurry and call today. **(415)783-6100**. Ask for Dept. M. Qume Corporation, Memory Products Division, 2323 Industrial Parkway West, Hayward, California 94545. TWX: 910-383-0710.

Qume®

Memory Products Division

CIRCLE 55 ON INQUIRY CARD

Custom Software Tailors Programmable Calculator To Accounting Functions

The GASS™ system provides complete accounting for service station operations, including daybook, general ledger, payroll preparation, and perpetual inventory. Developed by Pocolator Systems, Inc, 1378 N Killian Dr, Lake Park, FL 33403, the custom computer system sells for around \$4000 including training. Installation requires about 15 min and training an estimated 3 hours.

The package consists of a Texas Instruments TI-59 programmable calculator that incorporates 5k-bytes ROM, 960 bytes of RAM, display, keyboard, and magnetic card mechanism, and its companion 20-col thermal printer. Programs are stored in a 5k-byte encapsulated ROM that drops into a compartment in the rear of the unit. These programs are driven by input and calculated data from RAM.

The system was designed to use the calculator's simplicity as an operator aid. The user need only enter a number and press a button. This approach allows all workflow to be represented as a sequence of optional and required operations.

All information entered into the system is stored on magnetic card strips. By recording entries on a work card before recording them on a file card, users can go back to the work card to correct any errors that may have occurred. The system weighs only 6.5 lb (2.9 kg) and can be simply unplugged and used anywhere.

Circle 420 on Inquiry Card

Added 4341 Processors Increase Performance, Extend Versatility

Model Group 2 4341 processors provide internal operating speeds 1.5 to 1.8 times those of Group 1 processors and double the main memory capacity. In introducing the units, International Business Machines Corp, Data Processing Div, 1133 Westchester Ave,

White Plains, NY 10604, also disclosed the availability of 3279 color display and 3287 color printer for use as system console devices on 4341 processors.

Available with up to 8M characters of main storage, the processors feature 16,384 characters of high speed buffer memory, twice that of Group 1 machines, to make data available to the processor more rapidly and efficiently. Standard equipment on the processors are one byte and five block multiplexer channels. Two of the block multiplexer channels can transfer information at up to 3M characters/s when used with the Data Streaming feature (see *Computer Design*, Sept 1980, pp 58, 60), the three others transfer at rates up to 2M char/s, offering a combined maximum data transfer rate of up to 12M char/s. These transfer rates allow users to attach 3380 direct access storage devices, each with 2.52G-characters capacity, and to intermix these with other storage devices.

The processors are supported by OS/VS 2 MVS with MVS system product programs for Group 1 processors, as well as DOS/VSE, OS/VS1, and VM/370. Customer shipments are scheduled for the 2nd quarter 1981. Purchase price for a model Group 2 processor with 2M-char memory is \$385,000. With 4M- or 8M-char memory, prices are \$416,000 and \$479,200 respectively.

Circle 421 on Inquiry Card

4300 Compatible Processors Offer Competitive Cost/Performance

Mainframe computer models 1636, 1638, 1641, and 1651 offer performance equivalent to IBM 4300 processors at lower cost. Like 4300 family units, the machines offered by Cambex Corp, 360 Second Ave, Waltham, MA 02154, use microprogrammed bus driven architecture to permit field upgrades of CPU, main memory, and I/O channels through PC board changes.

All 1600 series machines use ECL hardware circuits with 50-ns machine cycle time. Microcode control storage supports from 72k to 144k bytes. Main memories are formed of 16k dynamic NMOS RAMs with maximum capacities up to 4M and 8M bytes. Memories use

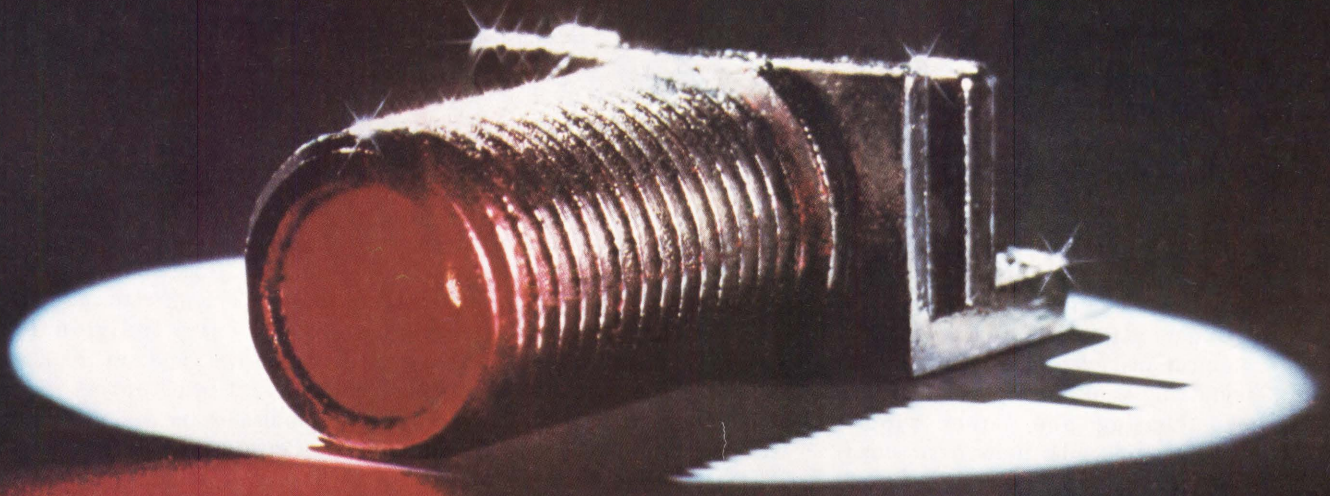
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We just coupled our Sweet Spot™ LED to this innovative AMP connector and gave it the highest fiber driving power it's ever had.

Of course, its low profile and easy coupling advantages are still the same. But the Sweet Spot gives it much more design flexibility.

For example, now it can be used with practically any cable. And coupled with the widest selection of optical receivers yet. Everything from high speed PIN diodes to low speed high sensitivity detectors. Plus, it provides the simplest circuit interface and most practical opto-mechanical interface available. Here are some Sweet Spot detector options:

SPX 4690 Medium Speed Detector

This high sensitivity detector utilizes an on-chip transistor preamplifier to simplify circuit design and has a broad operating bias range of up to 15V.

SPX 4691 Sweet Spot PIN Diode

With a response time of one nanosecond and 5V operating bias, this high speed detector opens the door to hundreds of new possibilities.

SPX 4692 High Sensitivity PIN Diode

For interfacing large core fibers of 200 microns or more, this 15V PIN diode provides a performance level that will simplify many applications.

SPX 4693 Schmitt Detector

This fully integrated detector/

interface circuit represents a major technology breakthrough. It's TTL and CMOS compatible and features a Schmitt Trigger output with total on-chip conditioning circuitry.

These are just a few of the endless new design solutions created by Sweet Spot LED power.

TYPICAL TRANSMISSION DISTANCE (METERS)

SPX 4689* (SWEET SPOT LED) WITH:	DUPONT PFXP140	DUPONT PFXPIR140	SIECOR 142	SIECOR 133	ITT T433	MAXIMUM DATA RATE (Mb/s)
SPX 4690* MEDIUM SPEED DETECTOR	10	40	1400	400	500	1
SPX 4691* SWEET SPOT PIN DIODE	10	35	—	650	950	30
SPX 4692* HIGH SENSITIVITY PIN DIODE	16	60	2400	1300	1900	10
SPX 4693* SCHMITT DETECTOR	13	35	1700	700	1000	0.1

*Part number describes component/connector assembly

Solutions that, coupled with AMP's sophisticated connector technology, bring fiber optics out of the lab — once and for all.

Contact Spectronics for more information at 830 East Arapaho Road, Richardson, Texas 75081. Telephone (214) 234-4271.



Spectronics
A Division of Honeywell

Light years ahead.

CIRCLE 56 ON INQUIRY CARD

error checking and correction techniques to automatically correct all single-bit errors. Redundant ALUs in the processor permit results of all functions to be compared for ensured accuracy. Maximum block multiplexer data rate is 1.86M bytes/s/channel; maximum byte multiplexer data rate is 50k bytes/s in byte mode and 180k/s in burst mode.

Offered with the processors are optional mechanically integrated peripheral controllers, a channel to channel adapter, and a data communications adapter. Mechanical integration permits controllers to use the CPU housing and power supply; however, since the units have stand-alone intelligence, they require no CPU cycles for their operations.

An internal service processor, a microprocessor/modem combination, facilitates remote hardware diagnostics and provides console capabilities

for hardware diagnosis and problem isolation. Extensive microdiagnostic programs can readily isolate hardware failures and check timing margins.

Loaded via floppy disc the diagnostics can be used in standalone operations or invoked through the processor's internal modem to a remote diagnostic mainframe. Tests begin by checking basic hardware functions starting with control storage memory and system register and proceed to higher levels in logical order. Final step is testing of system I/O channels in a simulated operating environment with randomly introduced operational sequences and background interference.

The units are totally software compatible with IBM /360, /370, and 4300 processors including DOS/VS, OS/VS1, OS/VS2, SVS, MVS, VM-370 and DOS/VSE operating systems. Processors include the System/370 universal instruction set as well as extended precision floating point instructions, advanced control support, extended control mode, and program event recording.

A typical 1636 processor with 1M-byte memory offers approximately 15% higher throughput than a 4331-Group II and sells for \$125,000. A 2M-byte 1641 performing in the range of the 4341 sells for \$190,000.

Circle 422 on Inquiry Card

1.2G-Byte Disc Subsystem Transfers at 1.2M Bytes/s, Accesses in 22-ms

A high speed direct access disc subsystem, the model 3652 stores 1.27G bytes, double the capacity of the IBM 3350. Containing two spindles and two head-disc assemblies, the Winchester module has a data transfer rate of 1.2M bytes/s and average access time of 22 ms.

Available with an interface designed for OEM integrators, the unit is fully attachable to System/370, models 158 and 168, 303X, 4341, 470/X, and equivalent processors. In the subsystem Memorex Corp, San Tomas at Central Expwy, Santa Clara, CA 95052, has incorporated a design aimed at ensuring total data availability.

The intelligent dual interface (patent pending) provides two simultaneous and independent paths to every spindle on the string. Appearing operationally equivalent to string switch to both storage control unit and operating system, the interface ensures that loss of string controller does not mean loss of string. The alternate string controller automatically assumes the role of primary control unit and processing continues uninterrupted. The interface also allows users to execute individual spindle diagnostics and to repair spindles without interrupting functioning spindles on the same string.

Performance improvements occur because the dual-access path permits fewer string busies to occur. CPU overhead is reduced because contention is resolved at the string level rather than at the processor. Other features playing a part are proprietary read/write heads that are designed to recognize changing track bit densities, and to reduce data error rates, noise, and crosstalk; variable settling time circuitry that reduces data checks, seek times, and read delays; proprietary damped servo system that reduces frequency and amplitude of head oscillation across a data track; and advanced mapping of data tracks to reduce arm movement from track 0 to the desired track.

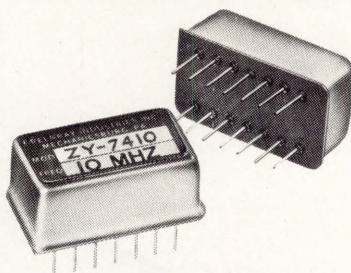
A head-disc assembly (HDA) switching technique further enhances data availability. Each module contains two HDA assemblies each with its own electronics and separate power supply. If either electronics or power supply becomes inoperative on one of the drives, data are accessed by switching to the other side of the module.

Because the subsystem is a double capacity unit with two strings of drives occupying the same physical space, floor space savings of 100% are achieved. An additional 23% savings is achieved by the physical access design. Energy consumption is 6% lower than competitive units with a 3% reduction in heat dissipation to cut air conditioning requirements.

Unit price for the 3652 in quantities of 100 is \$32,250. First shipments of units with IBM interfaces are scheduled for fourth quarter of this year.

Circle 423 on Inquiry Card

ECL COMPATIBLE CRYSTAL DIP OSCILLATORS



MODEL ZY-7410
10 MHz to 100 MHz

CALL OR WRITE



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Mechanicsburg, PA 17055
Phone 717-766-0223

IDT SATISFIES ALL YOUR BASIC DRIVES.

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The simple fact is, IDT makes the finest line of tape drives available. How else can you explain the fact that so many people are getting all wrapped up in tape today?

*Trade name of Intel Corp.



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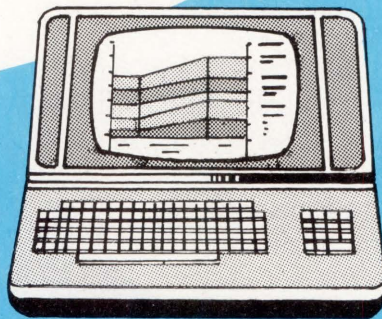
I'm interested in the following IDT products:

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Now you can display computer colorgraphics on a standard NTSC color television monitor, or videotape the information for distribution.



Lenco's CCE-850 Color Encoder is specifically designed to encode high-resolution RGB colorgraphics computer displays regardless of scan rates.

This small, self-contained unit may be used in either tabletop or 19" rack-mounted configurations, and includes a built-in color reference bar test pattern to ensure proper NTSC color monitor alignment.

Check these outstanding features:

- RGB-to-NTSC
- Detail Enhancement
- Color Test Pattern
- Auto Sync Detector
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- Self-Contained

Call or write today for detailed specifications, application notes, and price.



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7303 Poplar Lane, Middletown, MD 21769, (301) 371-5588

5456 Blossom Acres Dr., San Jose, CA 95124, (408) 356-0221

TECHNOLOGY REVIEW

Audio-Visual Courses Cover Computer Related Subject Areas

Multimedia courses developed by Deltak, Inc, 1220 Kensington Rd, Oak Brook, IL 60521, as part of the Advanced Technology Library cover computer security, VSAM debugging, user command language design, FORTRAN, database systems, and computer network software mechanisms. In general, the courses consist of video tape, student text, audio tape, and exercise handout, and provide from 2 to 15 hours of instruction depending on the topic.

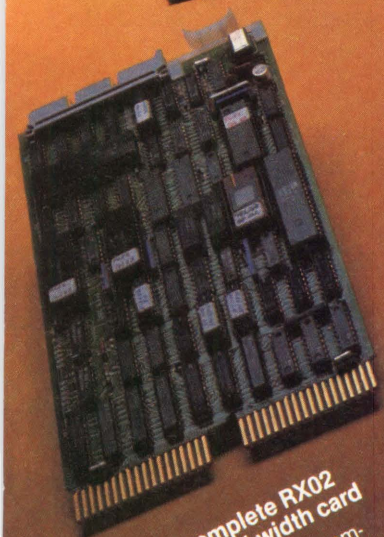
Concentrating on broad strategic issues regarding the security of computer systems and facilities, 80-61X is 2 hours of instruction broken down into Threats, Techniques, and Strategies. 12-79X, dealing with VTAM debugging, provides 3 hours of instruction covering basic techniques used in solving ABENDS caused by errors related to file processing. A series A course, 83-11X examines the basic structures used in alphanumeric dialog design techniques. After completing the 15-hour program the student will be able to plan, design, and implement an alphanumeric dialog.

Consisting of 10 units, representing between 30 and 40 hours of instruction, 31-7XX is structured to allow those familiar with another programming language to proceed from basic FORTRAN, to functional FORTRAN, and on to Extended FORTRAN. 24-2XX discusses database concepts, illustrating them with experiences taken from a large financial institution. This package consists of five courses, geared to project managers and systems analysts.

Specific software mechanisms and protocols used in data communication networks are covered in 82-2XX. Descriptions of HDLC and SDLC physical link protocols and CCITT Recommendation X.25 are provided, and packet switching, and control and compression mechanisms are explained. The package, aimed at managers, administrators, and systems analysts, consists of 20 hours of material broken into 5 subsections.

Circle 424 on Inquiry Card

DEC COMPATIBILITY

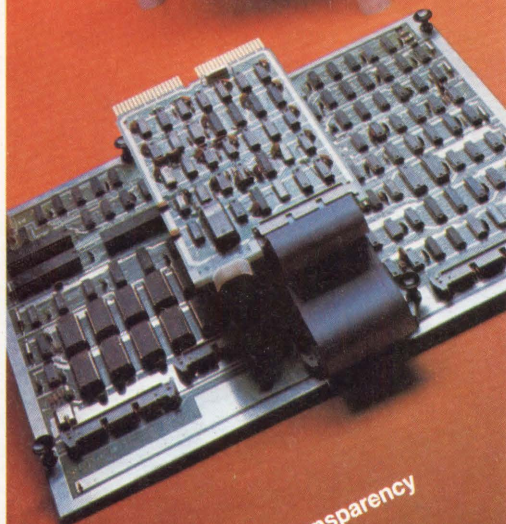
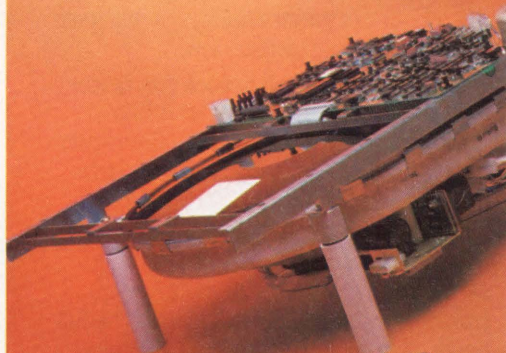


FLEX 02 offers complete RX02 emulation on one dual-width card

Media compatible and software compatible, the FLEX 02 card plugs directly into your LSI-11, 11/2 or 11/23. This low-priced controller has built-in bootstrap; handles single or dual-head floppy disk drives. Order now for 30-day delivery!



DEC COMPATIBILITY



WINC 01 offers RL01 transparency for Winchester-type drives

Software transparent to RL01 driver, WINC 01 maps the data of three RL01 cartridges (15.6 MBs) on one Winchester. Dual-width interface card plugs into LSI-11, 11/2 or 11/23; low-cost controller mounts onto Marksman drive. Call today, they're going fast!



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CA 94086 408-733-3555

Boston 617-275-6400
Los Angeles 213-705-0379
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Switzerland (022)32 97 20
India 79281
Japan 03-437-5471
Australia (02)438 2444
New Zealand 499 197

FROM AED

CIRCLE 194
ON INQUIRY CARD

DEC COMPATIBILITY



STORM 02 provides RM02 emulation for PDP-11 users

This single hex card, embedded in your PDP-11, runs under standard RM02 drivers. STORM 02 accommodates up to four 80 MB storage module drives and provides disk pack interchangeability with DEC. 30-day delivery and quantity discounts!



CIRCLE 193 ON INQUIRY CARD

CIRCLE 195 ON INQUIRY CARD

The intelligent disk architecture in STC 2700 Series Disk

STC's new 2700 winchester disk family combines the intelligence of a micro-processor, 64 Kbytes of RAM, and a high-speed bus interface to offer you a versatile new disk architecture. An architecture that can help you achieve new dimensions in system effectiveness. Relieve CPU overhead burdens. Slash interfacing costs, and more.

Yet, even without its advanced architecture, you'd still choose the 2700 disk family for its attractive price/performance and reliability values.

The 2700 family features formatted capacities of 39, 91 and 195 Mbytes, 27 msec average seek time, and an OEM price of less than \$5,000 (195 Mbytes). With a predicted 8000 hour continuous

operation MTBF, the 2700 will not just keep your customers happy--it will keep your warranty expenses low.

Powerful bus architecture for faster data rates and greater flexibility.

Gone are the speed and configuration constraints of serial, synchronous data-line interfacing. The 2700 disk family incorporates a high-speed, byte-parallel asynchronous interface, with internal serial/parallel conversion, to give you transfer rates up to 2 Mbytes/sec. The full handshake protocol and built-in dual ports support radial, daisy chain or inter-mixed configurations.

The μ p can unlock your system's hidden resources.

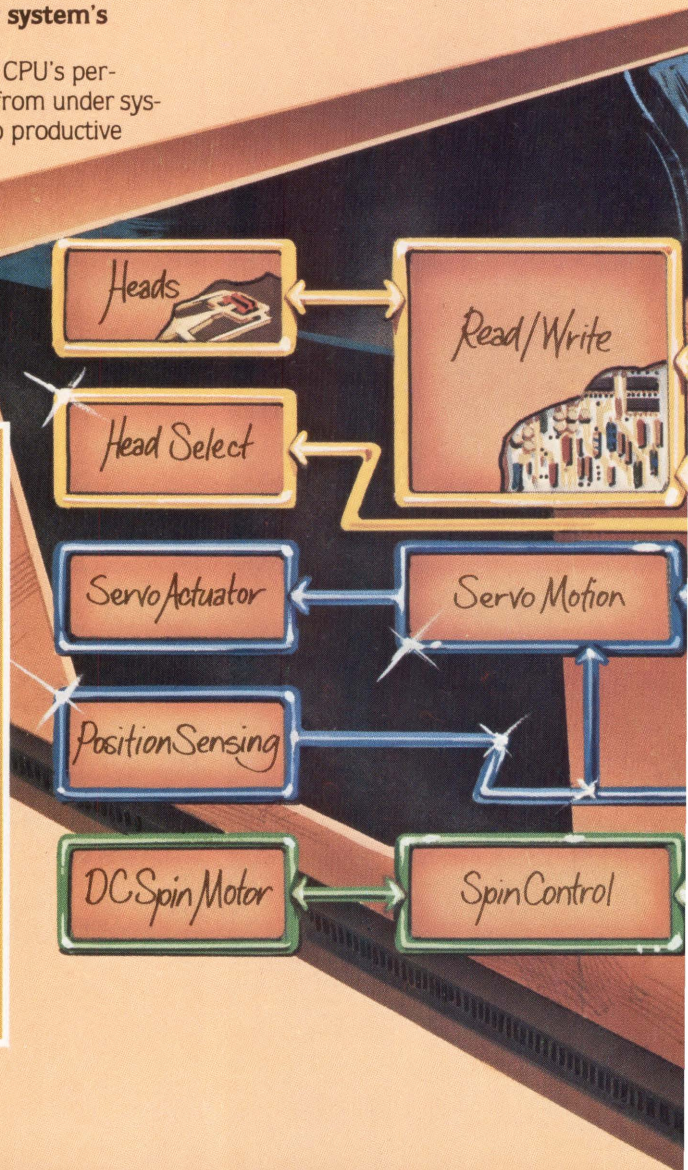
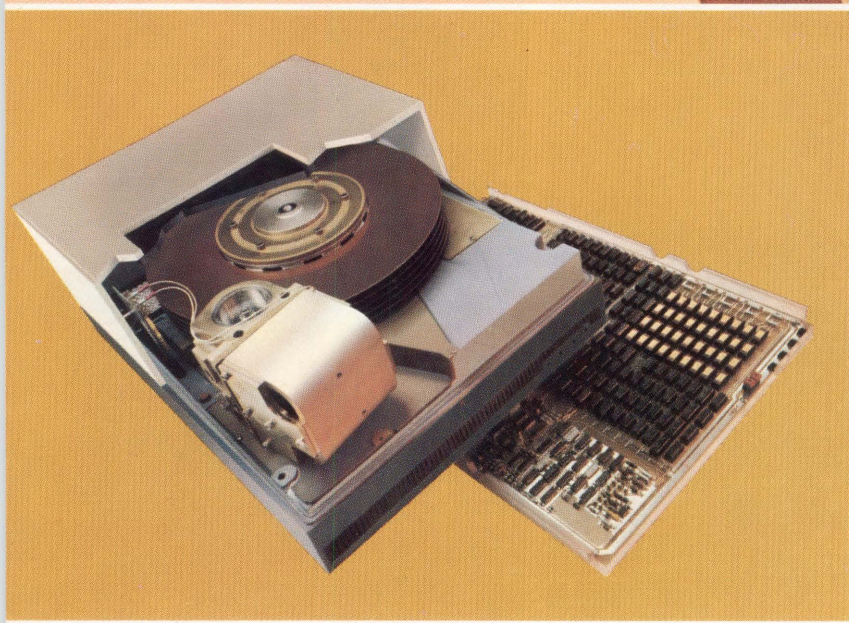
One way to boost your CPU's performance is to get it out from under system overhead and back to productive

computing. The on-board intelligence of the 2700 gives you that capability. Routines such as drivers, data management and utilities can be offloaded to the micro-processor, freeing the CPU and bus for other tasks. But that's only the beginning.

High-level software, including on-board editor and compiler, simplifies algorithm development for custom applications. And you can use the built-in RS-232 port to program right on the disk.

An intelligent controller in each drive. For free.

To help you get to the system level faster and easier, we placed most of the



of tomorrow is shipping today... Drives.

traditional controller functions within the 2700. This includes address mapping, defect management, error detection/error recovery procedures and all device-dependent functions. Since you now only have to build a low-cost interface adapter — your attachment costs are significantly reduced.

Low cost of ownership.

Fewer parts mean fewer failures. So the 2700 contains a minimum number of mechanical parts, only three of which move: spindle, actuator and power system fan. The microprocessor contributes

to this simplicity by replacing all sequencing and servo logic with firmware.

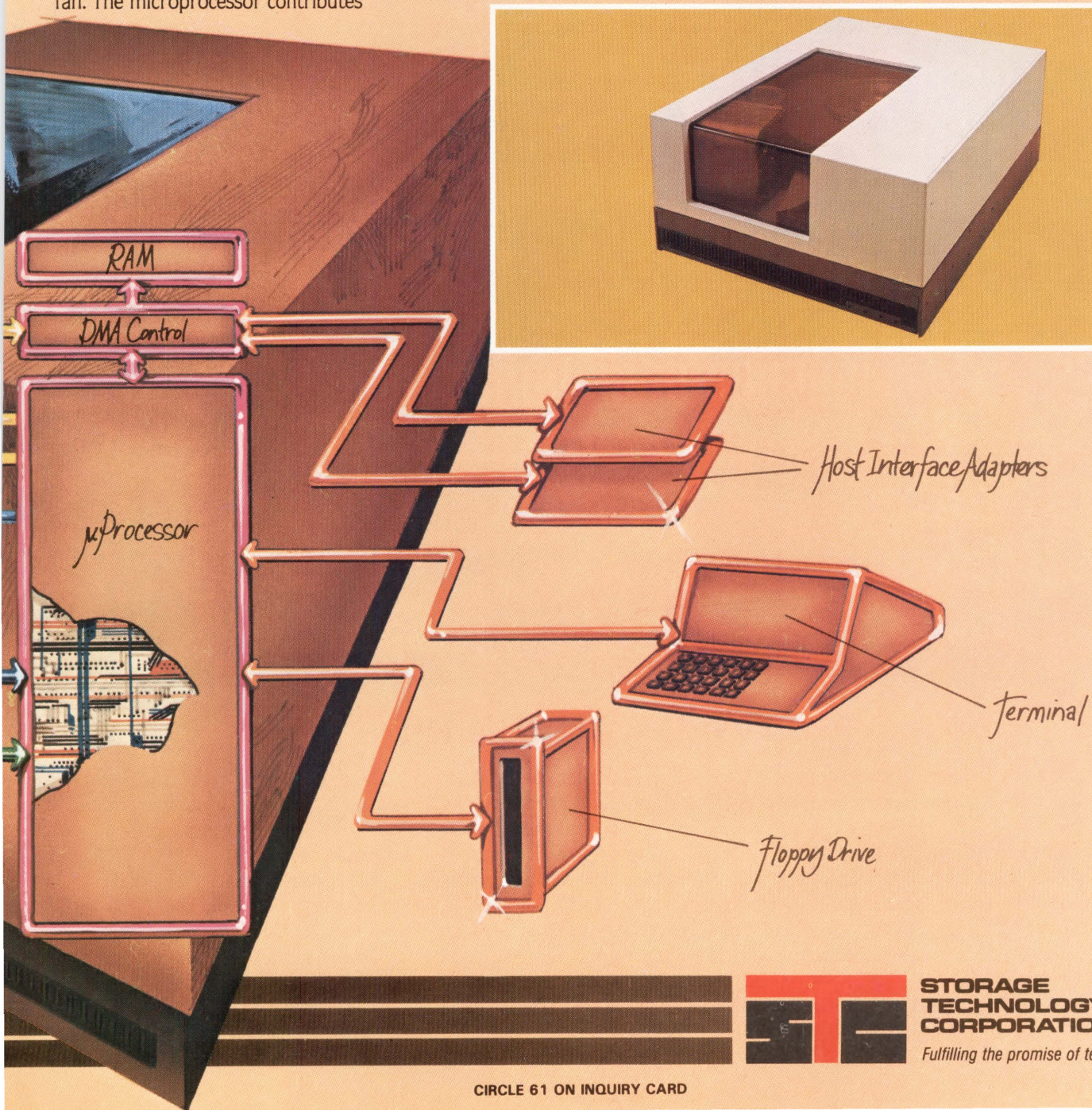
To eliminate scheduled maintenance, the 2700 dispenses with potentiometers. Dynamic adjustments are made internally under microprocessor control. And the 2700's closed-loop air system means no filter changes.

If there's ever a failure, internal diagnostics isolate the problem to one of three subassemblies: logic board, head/disk assembly or power system. And these components uncouple quickly

for fast replacement. All of this translates into high MTBF, low MTTR, to reduce your warranty and field service costs.

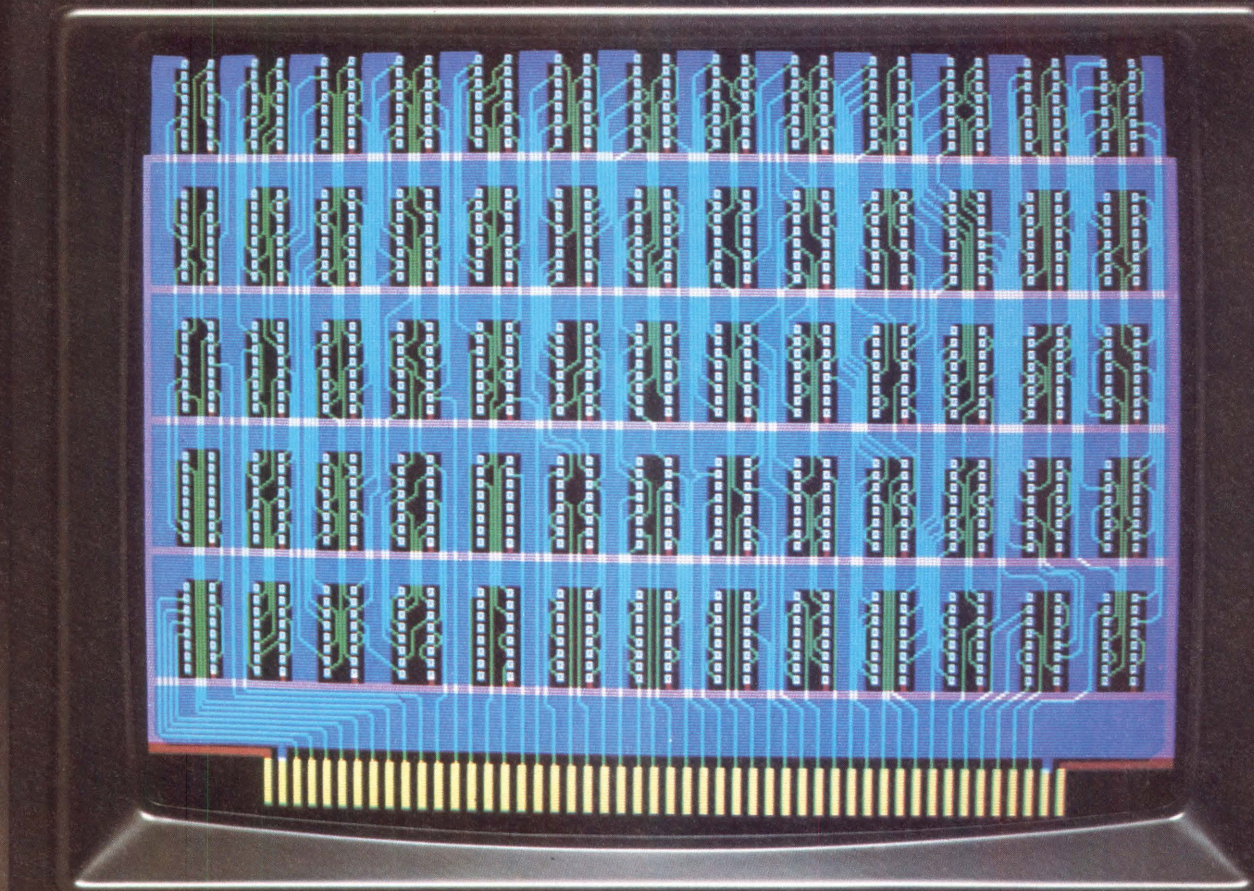
To learn more. . .

about tomorrow's disk architecture, today, contact OEM Marketing, Storage Technology Corporation, P.O. Box 6, Louisville, Colorado 80027. Or phone Frank Gunn at (303) 673-3051. In Canada: Ron Reardon, STC Ltd., 272 Galaxy Blvd., Rexdale/Toronto, Ontario M9W 5R8. Phone (416) 675-3350.



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Fulfilling the promise of technology.



End fuzzy thinking.

It's high time that your computer graphics match the precision of your computers.

High time that you look beyond the two-dimensional, indistinct, monochromatic technology of ordinary TV monitors. And see what an amazing difference Mitsubishi high-resolution color can make.

Mitsubishi high-resolution monitors are available in a dozen models.

In sizes to 26" With scanning frequencies to 35kHz available off-the-shelf now, and soon, way into the 60kHz's.

We got to be the world's largest manufacturer of high-resolution tubes because we've been able to establish an enviable record of superior quality control and electronic stability. Which means you don't need to hire color convergence experts in order to catch what the factory missed.

So if you're an OEM, you could save yourself a lot of trouble by calling us at (213) 979-6055* for complete information.

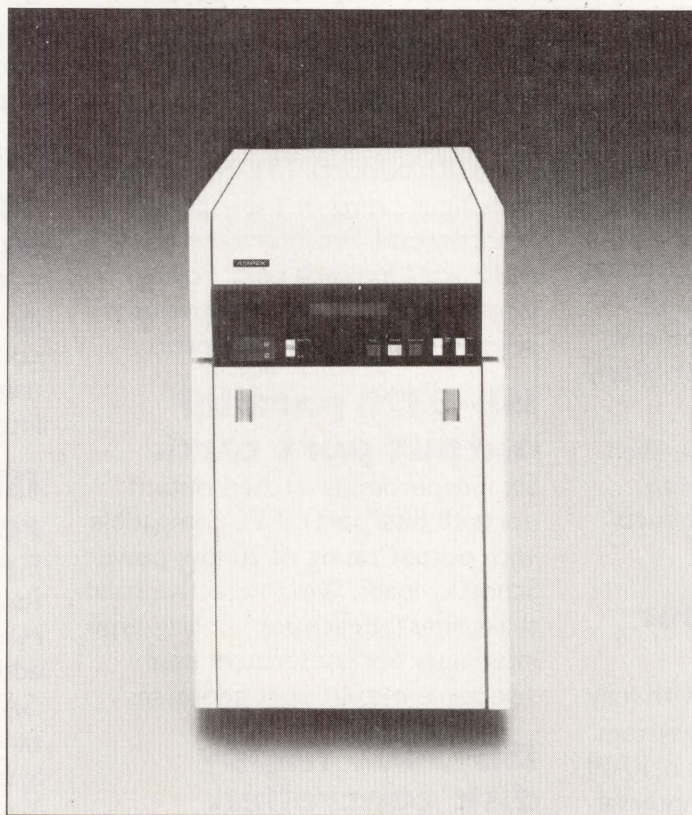
Or if you're an end user, call us at the same number for the names of interested OEMs.

And, together, we'll paint a cleaner, brighter future for everyone.



For more information write Dept. 31, Mitsubishi Electronics of America, Inc., 2200 W. Artesia Blvd., Compton, CA 90220. *New Jersey sales office (201) 753-1600.

TOTAL CDC COMPATIBILITY AND GREAT DELIVERY, TOO!



The only thing worse than not having enough disk storage, is not being able to get enough disk storage.

Fortunately, the Ampex DM-9300AQ solves both problems. With 300 megabytes of reliable disk pack storage and off-the-shelf delivery.

But the advantages of the DM-9300AQ don't stop with delivery. It's completely compatible with CDC's 300 megabyte drive. So disk packs can be interchanged, written on, or read by either drive. Of course, the industry standard SMD interface, and power sequencing of both units are also compatible.

DM-9300AQ disk pack swapping is as easy as using them. Its large front opening has been designed with the convenience of a top loader, and human engineered for minimal lifting. So even a 20-pound pack is easy to insert

and remove. It's such a good idea, we're surprised somebody didn't think of it sooner.

But then, the DM-9300AQ is full of good ideas. Like highly reliable on-track servoing, and a single port daisy-chain interface with ribbon cable that can be converted—in the field—to an internal dual port.

And the same goes for maintenance. Service requires only front, rear, or top access. Side access is eliminated, so you can

arrange the units side by side. What's more, the logic chassis in the rear of the unit swings out to provide easy access to all test points and connections. And extensive use of LEDs simplifies troubleshooting.

The DM-9300AQ has a lot to offer. But what's even better, is that it's all offered right now. With delivery that's ready when you are.

The DM-9300AQ. Just one of a complete line of Ampex plug compatible disk drive memories for nearly any CPU.

For more information, contact Gary Owen at Ampex Memory Products, 200 North Nash Street, El Segundo, California 90245. If you're really in a hurry call him at 213/640-0150. Or contact your local sales office.

Either way, we won't keep you waiting.

AMPEX

MAKES THE DIFFERENCE.

CIRCLE 62 ON INQUIRY CARD

STD

New: STD Bus products from Intersil's Systems Division.

Introducing the ISB-3000 Series: A cost-effective and ultra-reliable new line of STD Bus compatible products. A full family—from processor cards to memory, from digital I/O cards to peripheral controllers. All supported by a general-purpose operating system for software development. And an on-line CPU-resident binary debugging monitor.

And all available now. Off the shelf. From Intersil's Systems Division. (And *more* new STD Bus products are to be announced soon!)

ISB-3100 processor card (Z80).

Z80-based processor card with fully buffered signals for maximum system expandability. Up to 4K bytes of RAM, 8K bytes of EPROM and four interval timer/counter channels. Programmable power on restart address.

ISB-3110 processor card (8085).

8085-based processor card with fully buffered signals to give maximum system expandability. Up to 4K bytes of RAM, 8K bytes of EPROM and three interval timer/counter channels. Programmable power on restart address.

ISB-3216 CMOS memory card.

Up to 16K x 8 bits of CMOS RAM storage. Battery back-up for six-day

data retention. Low power consumption. Flexible memory mapping. (Previously designated MCB-216.)

ISB-3310 parallel input port card.

Six independently latched input ports (8 bits/port). TTL-compatible with input rating of 1 low-power Schottky load. Two interactive handshake lines for each port. Polling-type interrupts. Six consecutive user selectable input port addresses.

ISB-3320 parallel output port card.

Six independently latched output ports (8 bits/port). TTL-compatible with output rating of 20 low-power Schottky loads. Two interactive handshake lines for each port. Polling-type interrupts. Six consecutive user selectable output port addresses.

ISB-3400 floppy disk controller.

Double density disk control of up to four floppy disk drives. Diskette formatting. Automatic track seek with verification. Automatic CRC generation and checking. On-board ROM plus 1K bytes of scratchpad RAM. Compatible with IBM3740 and other formats.

ISB-3500 triac output card.

Eight independent solid-state relays (40 to 280 VAC, 2A). Optical isolation of

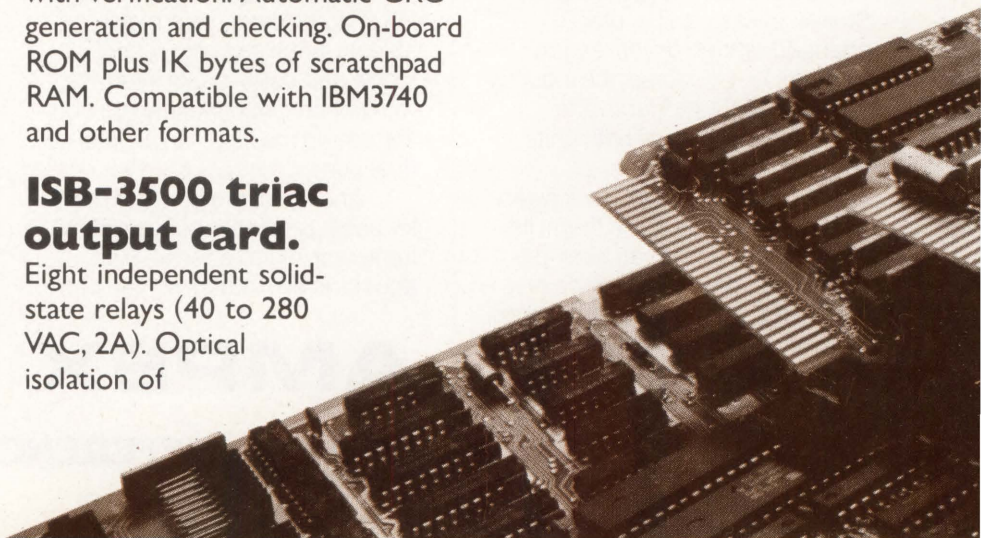
ac and TTL signals. Power switching at zero voltage crossing points. Built-in snubber networks. Keyed edge connector for ac power. User-selectable port address. On-card display of ac outputs. Safety shields.

ISB-3510 optoisolated input card.

Eight independent ac or dc signal input lines (70 to 280V). Keyed edge connector for interfacing input signals. User-selectable port address. Interrupt capability. Safety shields.

ISB-3520 reed relay output card.

Eight independent SPST Dry Reed Relay outputs. On-card display of relay closures. User-selectable port address. Contact rating: 200V, max.; .5A, max.; 10V.A., max.; 2 Ω resistance; 300VDC min. breakdown. System reset opens all relays. Typical open or closure time: <500 μ s. Keyed edge connector for outputs.



BUS

ISB-3600 arithmetic card.

High-speed card using a versatile Arithmetic Processor Unit. Fixed point 16- and 32-bit operations. Floating point 32-bit operations. Add, subtract, multiply and divide. Trigonometric and inverse trig. Square root, logarithms, exponentials. Floating to fixed, fixed to floating. Stack-oriented operand storage. Software programmable interrupts. User-selectable port addresses.

ISB-3700 synchronous/ asynchronous communications card.

Two independent communication channels, using a Programmable Communications Interface device. RS-232-C and 20mA current

loop connections. Selectable baud rates: 50 to 19.2K baud. Vectored or polled interrupts. User-selectable port addresses.

Call our hot line: (408) 743-4442.

Here's a very broad STD Bus product offering. From the people who've been building cards and systems for the last ten years. Who have shipped over five billion bytes of memory systems. And who have a reputation for quality and service that didn't happen by accident.

So when you think STD Bus — think Intersil's Systems Division. Call us for the details.

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INTERASIL SYSTEMS DIVISION

Marketing Department, 1275 Hammerwood Ave., Sunnyvale, CA 94086. (408) 743-4300 or Hot Line (408) 743-4442.

Please tell me more!

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| <input type="checkbox"/> ISB-3100 | <input type="checkbox"/> ISB-3320 | <input type="checkbox"/> ISB-3520 |
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| <input type="checkbox"/> ISB-3216 | <input type="checkbox"/> ISB-3500 | <input type="checkbox"/> ISB-3700 |
| <input type="checkbox"/> ISB-3310 | <input type="checkbox"/> ISB-3510 | |

Name/Title _____

Company _____

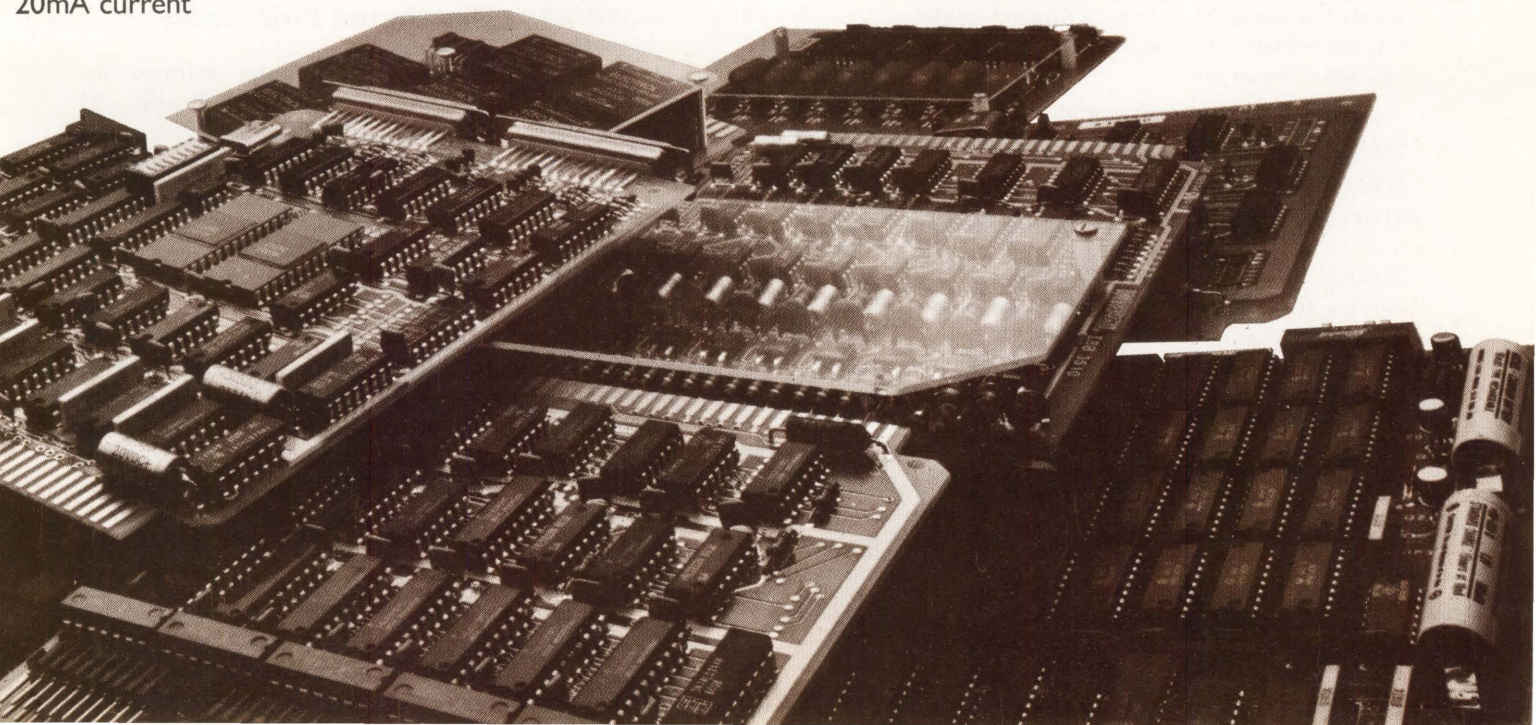
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City/State/Zip _____

Phone _____



CD11/80



Improved Software Offers Increased Speed, More Efficient Storage

INFORMATION™ system software has been enhanced to offer more efficient storage, dynamic reorganization capabilities, and three times faster execution speed. Prime Computer, Inc, 40 Walnut St, Wellesley Hills, MA 02181, has also incorporated features that make the relational-like data base easier to work with in the software.

To improve data file storage and execution time and give the programmer more flexibility, the system lets users organize files on a "what if" basis to avoid wasting disc space. A record distribution report reflects the storage efficiency of an existing file if the file type or modules or both are altered. When an appropriate file organization has been verified, reorganization is accomplished without need to copy the file.

The sequence of logical operations in the query and report generator is designed to reduce a file subset to its final size as quickly as possible. Users can access the database by the way a word sounds when its spelling is unknown. Other features include a sorter that permits items to be filed in ascending or descending order and a recorder that monitors user operations. Output presentation has been improved by a vertical format feature that allows data to be changed from a default horizontal to a vertical format to accommodate size restrictions.

Circle 430 on Inquiry Card

Pascal Revision Offers Assembler Interface Facilities

Release 2.10 of Pascal features facilities for assembler interface and the separate compilation of procedures and functions. Announced by Rational Data Systems, 245 W 55th St, New York, NY 10019, for Data General computers, the Pascal package retains its closeness to the proposed standard for Data General Pascal implementations while providing extensions demanded by users.

Circle 431 on Inquiry Card

Pascal Compiler Produces Optimized, Sharable Code For 32-Bit Machines

A Pascal compiler that produces optimized sharable code (from the Computer Systems Div of Perkin-Elmer Corp, 2 Crescent Pl, Oceanport, NJ 07757), takes full advantage of the 32-bit architecture of the company's minicomputers, including models 3220 and 3240. Full integration with software for the family provides comprehensive support for all phases of the program development cycle. Up to 64 users can share access to the compiler for development and testing of Pascal programs.

Conforming to the ANSI draft language standard, the implementation offers a number of language extensions appropriate to various applications areas. Among these are support for modular program development, separate compilation of Pascal procedures, easy access to external library routines written in Pascal, FORTRAN, or Assembler, and facilities providing access to executive service routines for commonly needed functions such as time of day, date, device assignments, and file positioning.

For the scientific user, Pascal provides considerable flexibility and power. REAL and SHORTREAL variables are supported by the processor's floating point facilities, giving 16 digits of precision for REAL numbers and 6 digits for SHORTREAL. INTEGER and SHORTINTEGER allow the user to choose between the range of 32-bit values and the memory economy of 16-bit half-words. The package uses the mathematical function library to provide accurate results. For time-critical applications, a microcode version of this library is also available.

The implementation supports Pascal Identifiers unique to 140 characters, sets of up to 128 elements including set of characters and record compares. Additionally, the compiler generates code for runtime range checking of subscripts, case labels, variant tags, and pointer values to help ensure application integrity. This code may be optionally eliminated for time-critical applications.

Circle 432 on Inquiry Card

High Performance PL/I Compiler Executes on VAX-11/780

A high performance PL/I language compiler for VAX-11/780 systems extends the proposed ANSI X3.74 subset to maintain full file organization and access support and to allow calls to the VAX/VMS operating system. In the compiler Digital Equipment Corp, Maynard, MA 01754, has provided the ability to call routines written in all VAX-11 languages as well as use the common VAX runtime library, including mathematic and trigonometric functions.

Combining scientific features of languages such as FORTRAN and ALGOL with commercially oriented features of COBOL, the block structured language supports floating point, binary, and decimal data types; arrays; and structures of data, character strings, and bit streams. Support is provided for sequential, relative, and indexed file organization as well as sequential, random, and keyed file access.

Intended for VAX configurations containing 512k bytes or more of physical memory, the compiler compares with VAX FORTRAN in speed—between 2000 and 3000 lines/min—and generated code has equivalent execution speed. Available in December, the package has a single use license fee of \$12,000.

Circle 433 on Inquiry Card

Data Entry Software Extends Floppy Disc into Distributed Processing

Prompted Data Entry software expands performance of Flexifile 21 floppy disc subsystem beyond message handling. Announced by Tri-Data, 505 E Middlefield Rd, Mountain View, CA 94043, the program provides the tools needed to format input data on an interactive step by step basis.

By displaying or printing questions and statements at the terminal, the program aids untrained operators entering data. Menus and prompts enable relatively untrained personnel to develop formats for a variety of transaction processing workstations. In addition, the software is capable of detecting syntactical errors and generating corrective messages.

Circle 434 on Inquiry Card

OUR MICROCOMPUTER TALKS TO YOUR WORLD.

When you need a powerful processing system that talks to your world... you need a COMMANDER COMPUTER. Four standard RS-232C ports handle serial data to 19,200 baud, allowing you to add low speed peripherals or even communicate with remote devices over a phone line. But if you need higher speed or more flexibility, use COMMANDER's parallel I/O under program control. And, if that's not efficient enough, select the optional DMA port to process parallel data on a cycle-steal basis direct to memory. COM-

MANDER's optional IEEE/488 controller gives you direct interface to the world of instrumentation and a host of compatible devices readily available. The optional Real Time Interface module gives you individual bit I/O to input status lines and digital sensor signals...or to output alarms and commands. And you can use up to four independent programmable real time clocks for precise time interval control without wasted processor time. Inquiries for custom features are welcome.

BUT THAT'S NOT ALL...Select the

COMMANDER configuration to fit your system need. The models 500 and 900 have an integral CRT and keyboard while the models MX and FX (not pictured) can be married to a simple terminal for operator interface. Add the optional arithmetic unit for high speed fixed point or floating point processing. And, if your application requires graphics, optional memory is added to provide 512x256 video graphics capability.

All COMMANDER models will execute higher level programs in BASIC, FORTRAN or COBOL or machine level programs in MACRO-80 Assembler. Operating programs are executed under CP/M™ FDOS, the new MP/M™ operating system or UCSD Pascal™.

COLUMBIA

DATA PRODUCTS, INC.

Computer Systems Division

8990 Route 108
Columbia, MD 21045
Tel: 301-992-3400 TWX: 710-862-1891

CIRCLE 64 ON INQUIRY CARD



The best of both worlds for DEC[®] users



**Data
Systems**

Data Systems Design's DSD 880



**Introducing the DSD 880 —
A DEC-compatible
disk system combining
eight-inch Winchester and flexible disks**

For DEC users who need more capacity and performance than a dual RX02, the DSD 880 now offers a more cost effective alternative than a dual RL01. Consider these benefits offered by the DSD 880:

- significantly lower initial and total life-cycle costs
- the reliability of a Winchester, with 7.5 Mbytes, emulating RL01
- the removability of a flexible disk, with 1 Mbyte, emulating RX02
- valuable saving in rack space (5¼" vs. 21" for dual RL01)
- unique "hyperdiagnostics" enabling fast and easy trouble-shooting to the modular level
- built-in bootstrap eliminating the need for an expensive DEC bootstrap board and saving a backplane slot
- one half-quad backplane slot vs. two quad boards for the RLV11
- versatile interface card for easy integration with any LSI-11 backplane, unlike DEC's RLV11 interface that needs a special backplane and cannot be used with the VT 103 terminal

Compare for yourself and see why nothing compares to the DSD 880.

**Data
Systems**

The Intelligent Alternative to DEC Disk Systems

To get more information on the DSD 880 call or write:

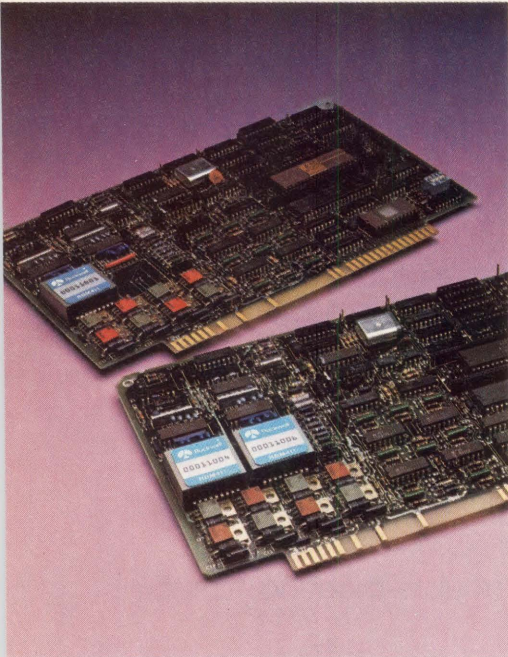
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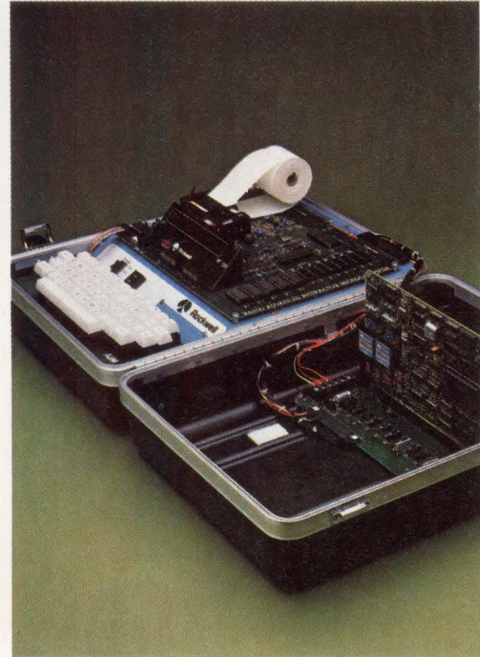
128K or 256K bytes on a single board.

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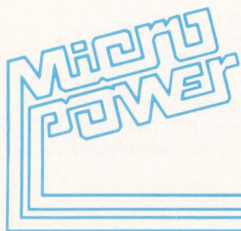
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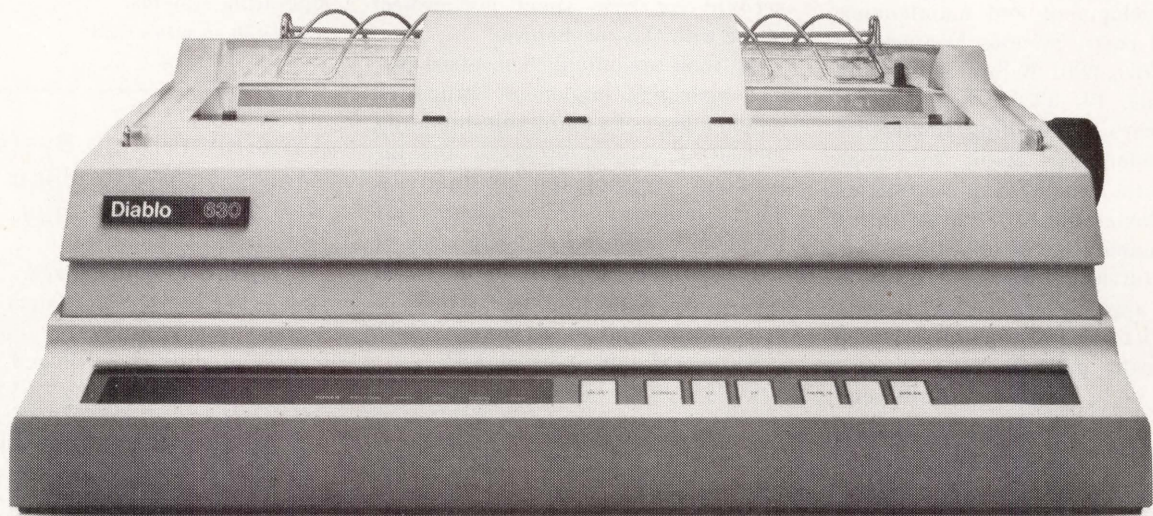


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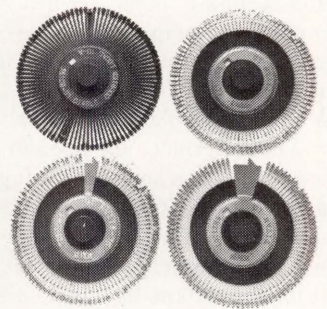
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Diablo Systems

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SOFTWARE

Software Tools Aid in Program Development and Project Management

FORTTRAN Formatter, Interface Documenter, Documenter A, Symbolic Debugger, and project accounting mechanism in the MPX-32 operating systems assist managers to control program development and maintenance time and costs. Systems Engineering Laboratories, 6901 W Sunrise Blvd, Ft Lauderdale, FL 33313, has targeted the packages to help programmers using the company's 32-bit word computers with structured programming methodologies and MIL-STD-1644 coding and documentation standards.

The FORTRAN formatter standardizes the appearance of FORTRAN-66+ and FORTRAN-77+ programs by automatically indenting and aligning FORTRAN code. Regardless of the current source coding conventions, output is formatted with logic structures indented appropriately to reveal top-down block structures.

Documenter A expedites uniform documentation of source programs and provides timesaving features for editing source programs and libraries. Management defines documentation templates which detail both topics to be documented and their formats. Programmers simply write code and documentation in shorthand format, with the software extracting comments and aligning them according to the predefined template. The tool operates on any source program including FORTRAN-66+, FORTRAN-77+, COBOL, Macro Assembler, and Pascal.

The interface documenter can be used by programmers during debugging, system integration, documentation, and maintenance phases of a project. It documents subroutine module interdependencies and assists in verification of design criteria by producing five cross-references and memory requirement reports.

The symbolic debugger speeds location and correction of programming errors, and provides symbolic access to global symbols, statement labels, and

local variables for FORTRAN-66+, FORTRAN-77+, and Assembler programs. The package enables users to interactively control and monitor program execution, allows programs to explicitly call the debugger, and permits users to interrupt any executing program to dynamically initiate debugging activities.

The MPX-32 operating system provides project accounting facility to supply data on programmer programming sessions including log-on time and CPU utilization, and to summarize this information per programmer or project. Managers implementing structured programming techniques can account for time spent per project phase with this mechanism.

All tools are intended to assist project managers implement structured methodologies by enforcing standards, measuring project progress, and improving programmer productivity. These tools and methodologies are capable of reducing software costs by half. They are available under either RTM or MPX-32 operating systems, except for the symbolic debugger, which is supported only under MPX-32.

Circle 435 on Inquiry Card

Automatic Software Documentation System Cuts Maintenance Costs

SS/80 cuts software maintenance costs by automatically documenting whole systems of programs written in COBOL and ADPAC. Introduced by ADPAC Corp, 120 Howard St, San Francisco, CA 94105, the system treats user programs as data and produces from them a complete set of graphics and narrative text that documents source programs at any level of detail down to individual subroutines. Since documentation is source driven, it is up to date.

The software also functions as a design tool for building structured program shells in computer maintained text. It generates its own progress reports and, when design is complete, stored structures form the beginning of actual code.

Documents are produced in both graphic and textual form. Among the graphic displays are structure charts showing function of subroutines, structure diagrams showing program and

module names and titles, system package diagrams showing housekeeping features of large systems in compact form, and I/O file structures showing I/O requirements for any program in system. Textual printouts include system profiles with descriptive details indented to show hierarchical structure of system, narrative descriptions outlining function of each program module, and system wide cross-references showing where every I/O parameter is used and where every program or entry point is called.

SS/80 works on IBM System 360/370 and 4300 computers as well as on compatible equivalents. It runs with all IBM operating systems.

Circle 436 on Inquiry Card

Data Encryption System Meets Growing Need for Security and Privacy

PSYPHER, a generalized software system for encryption of data and programs, provides privacy and maintains confidentiality of privileged information. MBS Consulting, 6407 Irwin Court, Oakland, CA 94069, designed the system to transform files (binary or ASCII/EBCDIC) into unintelligible randomized bit patterns or random character streams. The system offers maximum protection because each copy is distributed with its own algorithm.

Input can be binary or character coded files with record length fixed or variable. The system operates in one of two user selected modes: binary or character processing. Binary processing transforms the input file into a completely unintelligible stream of random bit patterns. The resulting encoded binary file has records of random length. Character processing produces a file of random printable characters—!#\$%&'()*—0 through 9 and A through Z. Output records are 80 characters and fixed length.

Approximately 8k 16-bit words of memory are required to run the system. It is presently available in load module form for operation on Data General, DEC, IBM, and CDC systems. Standalone runtime on an Eclipse S/130 is approximately 71k 8-bit bytes/min in binary processing mode; this time is significantly reduced on mainframes.

Circle 437 on Inquiry Card



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Minicomputer Tracks Other Computers From Final Assembly to Shipping

Bottlenecks and long transit times between a minicomputer manufacturer's production line and its shipping department have been eliminated and reduced, respectively, by a system based on minicomputers. A "data capture" system in operation at Hewlett-Packard's Grenoble Div in Grenoble, France, uses an HP 1000 model 40 minicomputer and 11 terminals to locate and track the position of HP 1000 computers and HP 3070B CRT terminals from the time they are fully assembled to the time they are ready to be shipped to customers. The results show a reduction in the period needed for a finished product to reach the shipping department, a lower finished goods inventory, and an improvement in meeting promised ship dates.

Interfacing the System

In addition to the minicomputer and CRT terminals, the data capture system contains two HP 2645 data display stations and a 1250-line/min printer. Memory consists of 128k bytes in the minicomputer and 19.6M bytes on disc. A tape drive is included for backup storage. The HP 1000 is linked to and acts as the frontend unit for an HP 3000 central computer that ties into an online inventory control and material requirements system.

Using the HP 1000 as a front end reduces the CRT load on the HP 3000 (already running 30 CRTs) and enables a response time of 1 s or less to be maintained. The small computer oversees data capture and terminal control functions and passes prevalidated data to the larger computer for processing. DS/1000, a combined hardware, firmware, and software feature on the small computer communicates with its counterpart—DS/3000—on the larger machine to establish a distributed processing link.

IMAGE/1000, the database manager for the small computer, automatically stores and retrieves data and allows different data sets to share the same data. It eliminates the need for reprogramming when the data base changes. QUERY/1000, an English-like data entry and inquiry language that lets order control clerks and plant managers use the system without programming knowledge, complements IMAGE. Only a series of simple commands are required to access the IMAGE data base with QUERY. DATACAP/1000, another software feature, generates the applications programs required to support the different transactions conducted on each of the data capture terminals and interfaces these programs with the database manager.

The system's data base handles a monthly throughput of some 5000 different products and involves entering and updating this data base with 40,000 separate transactions/month. In addition to products actually built, information is maintained on an additional 10,000 products in various stages of planning or production—for use by the order control department to match customer orders with products.

Each product listing in the data base contains 34 separate information fields, such as model, serial number, customer order number, due date, actual production date, projected ship date, actual ship date, box weight, and box identification number. Information storage and access are governed by four master sets (files) or keys provided by the IMAGE software. By maintaining only a relatively small number of files the IMAGE data base is held to a level that can be understood and used by employees with a minimum of training.

Operating the System

A 2-part traveler card (Fig 1) is generated for each product: one part contains a mark sense code with product data that can be read by the terminals; the other contains a hardcopy printout of the same information (the latter prevents card mixups). These cards are generated weekly to match the

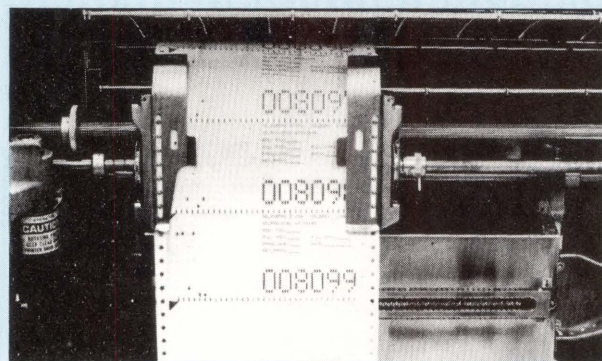


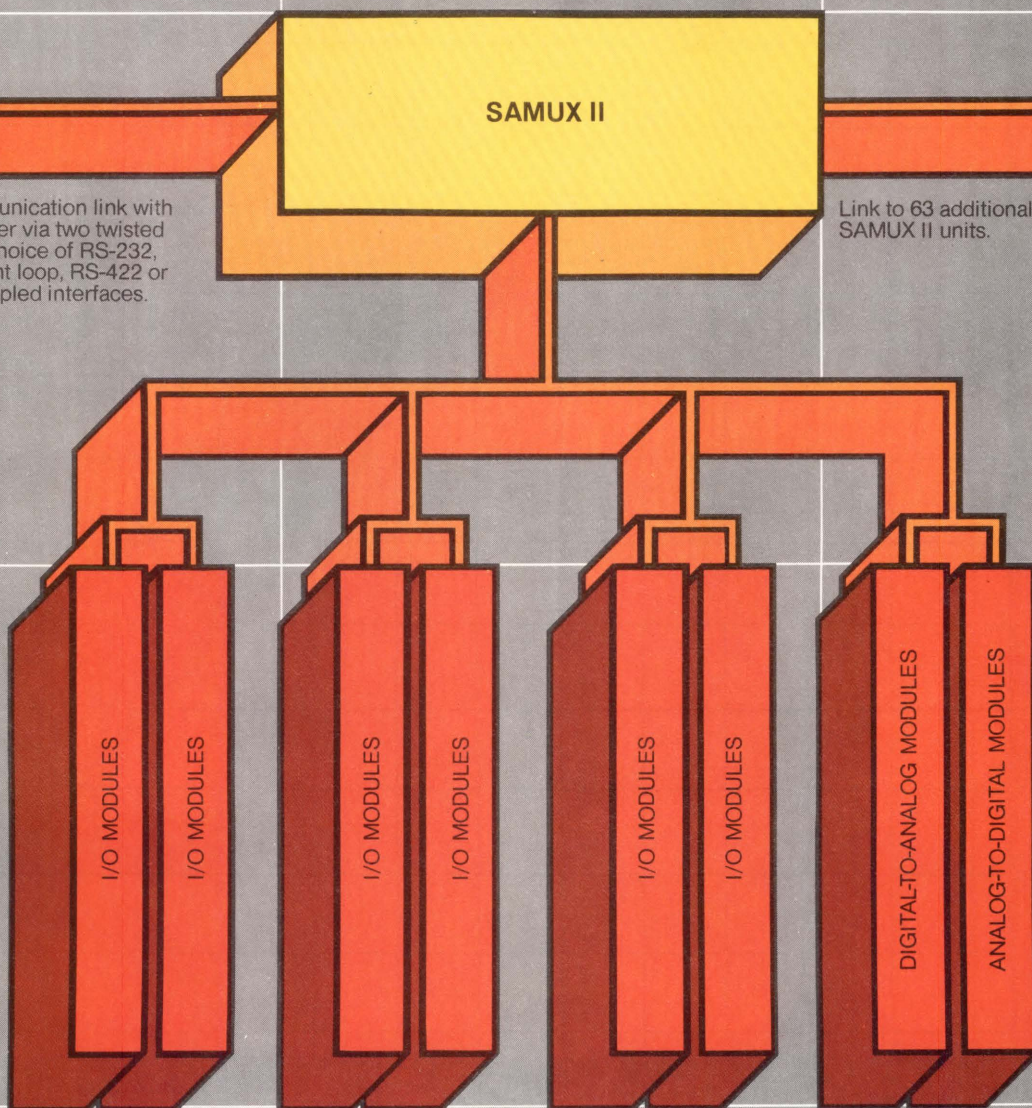
Fig 1 Traveler cards. These 2-part cards, generated weekly for all products scheduled to be manufactured during that relevant period, contain machine readable mark sense code on one side and hardcopy printout on other side for use by plant personnel

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Get more than bubbles

Intel's bubble memory is a complete set of bubble components for microprocessor-based applications. This set consists of six special support ICs: a controller, a formatter/sense amp., three packages for coil driving and a current pulse generator. It interfaces to Intel® and other microprocessor system buses via the controller, which handles up to eight bubble memory packages, and provides built-in power fail protection and error correction.

The bubble element and its small set of associated ICs can be

treated as a peripheral subsystem. This allows designers to concentrate on higher level system objectives, instead of spending time learning the intimate details of bubble device interfacing. Thus minimizing expense in hardware and software development.

Add more value to your product

With Intel's solid-state bubble memory, all that moves is the information. That means high reliability and low maintenance for your products, even in harsh or unclean environments—the kind where disks and tapes won't go. And since the memory is completely nonvolatile, your data

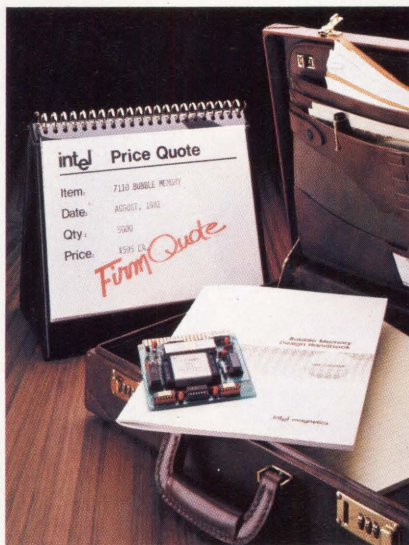
remains secure when the power goes off. No battery backup or replacement is necessary.

As the natural mass storage for LSI microprocessor-based systems, Intel's megabit bubble memory makes it practical to design more features into your equipment. So now you can build in program-mability. Portability. Reduced service and repair costs. All with ensured data integrity, even in hostile environments. Consider what that means in your applications.

Start designing now

Everything you need to start designing your next generation product is included in our Bubble Memory Prototype Kit (BPK72), available now from distributor stock. It contains all the components necessary for a 1-megabit system, plus a printed circuit board and complete documentation.

To find out how bubble memories can give you that competitive edge in your next project—and to receive our bubble brochure, contact your local Intel sales office/distributor. Better yet, have one of our field sales engineers give you a firm quote based on exactly what you need for your next product. Write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

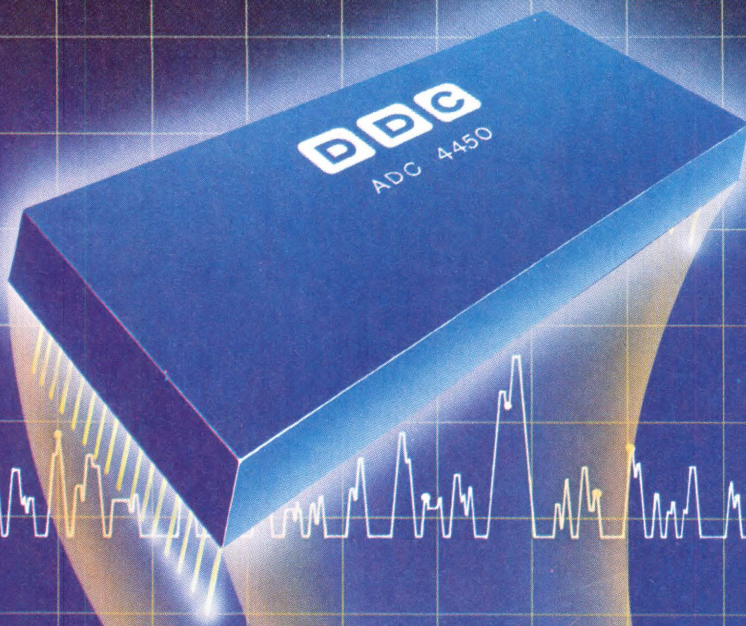


remains secure when the power goes off. No battery backup or replacement is necessary.

Furthermore, Intel's bubble memory system is small, lightweight and silent. By packing over 1 million bits into less than 100 square centimeters of board space, it allows you to reduce the size, weight and power con-

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LONDON: DDC United Kingdom Ltd., Dept. L-2, 128 High Street, Hungerford, Berkshire, RG17 0DL, England 04886-2141/2142, TLX: 851-848826

PARIS: DDC Electronique, Dept. L-2, 4 Rue de l'Abreuvoir, 92400 Courbevoie, France, (1) 333-5888, TLX: 842-630609

planned production and are filed at the appropriate production lines until the respective products are completed.

When generating cards, an operator uses a small FORTRAN program to enter latest production information. The program automatically assigns a tracker identification number that accompanies each product up to the time it is shipped. A second program is then used to actually print the cards in batches of 50 to 200. Operators insert the machine readable portion of the card into their terminal's card reader at various checkpoints to "capture" product data (Figs 2 and 3). DATACAP software provides for simple card reading at some checkpoints and more complex interactive procedures at others.

Actual tracking of a product begins when a production line operator passes that product's traveler card through one of the data capture terminals to record product data and the date and time the product was completed. The card is then attached to the product and both are sent to quality control.

At quality control, an inspector first passes the card through the card reader on a terminal to record product data and the date and time of inspection. The data capture terminal then prompts the inspector for a 2-digit inspector identification code and coded answers relating to the condition of the product and its appearance. If the terminal



Fig 3 Closeup of HP 3070B terminal panel. Information is sent to HP 1000 minicomputer to update product status record maintained by that unit for HP 3000 central processor



Fig 2 Data capture terminal in use. Operators at each of several checkpoints insert mark sense code side of traveler card into card reader on terminal. DATACAP software is formatted to accept simple data at some checkpoints and more complex information at others

already shows a previous inspection for a product, a duplicate routine is called up on the terminal to prevent the new inspection data from replacing results of the original inspection. After the quality control check, the product is transferred to the finished goods storeroom. Again, its traveler card is scanned so that its presence at this location will be recorded.

When the product is removed from the finished goods storeroom for delivery to a customer, its card is scanned to record the departure date, and the product goes directly to the packing department or to the systems integration center for assembly into a larger system. Here, the terminal scans the traveler card for each component as well as a separate traveler card for the assembled product.

At the packaging site, the product's traveler card is again scanned and the weight of each box number is entered. Using DATACAP, packers identify box number and weight with all products that were assembled into systems by simply pressing a terminal key. Traveler cards are scanned for the last time as the product is loaded onto a truck for shipping.

Information entering the system through scans of the various traveler cards is readily available both for generating complete hardcopy reports and for answering online questions, such as the location or status of a product. Online information is displayed on the CRT screen; hardcopy reports on production levels, inventory, transit times between checkpoints, product and customer shipments, and component quality control are generated by the high speed line printer. Shipping and quality control reports are generated on the first working day of the month, and shipped products are removed from the data base.

Engine Management System Saves 7.5M Gallons of Aviation Fuel

Installation of flight management systems on its fleet of Boeing 747 jumbo jet aircraft is expected to save Pan American World Airways 7.5M gallons of aviation fuel—equivalent to roughly \$5.55M by today's prices—per year. Although that saving amounts to only 1.5% of the fuel normally used, the effect on energy conservation is impressive.

The flight management systems are made by Delco Electronics and are based on that company's F-130A flight management computer. Fuel consumption is minimized through closed loop control of aircraft pitch and thrust. Throttle adjustments made by the system maintain the optimum speed selected by the pilot and minimize accelerations during maneuvering to reduce unnecessary fuel consumption. Pitch control is achieved through the plane's automatic pilot. Adjustments are made by the management systems continually through climb, cruise, and descent phases.

A year of flight test and evaluation on a 747 in regular scheduled service, in which over 400 hours of controlled flight time was compared with over 900 hours of uncontrolled flying time on the same aircraft under similar condi-

tions, preceded the decision to install the systems on the entire fleet. Installation of the flight management systems began early this year on 10 long range 747 SP aircraft and on 29 standard 747-121 models; contract options allow for later installations on 6 all-cargo 747s. Production certification is scheduled for early next year.

Each system consists of four separate packages: the computer, an alphanumeric control display, a switching unit for electrical hookup, and an engine data monitor. The computer, measuring 4.5 x 6 x 20 in (11.5 x 15 x 51 cm) and weighing about 28 lb (13 kg), uses NMOS LSI circuits designed and developed by Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036. Motorola's integrated circuit application research laboratory participated with Delco Electronics in designing and developing the chip set and was later qualified to provide the LSI circuits. Included in the chip set are a programmable communications interface, memory controller, input/output controller, digital input processor, central processing unit, and arithmetic unit.

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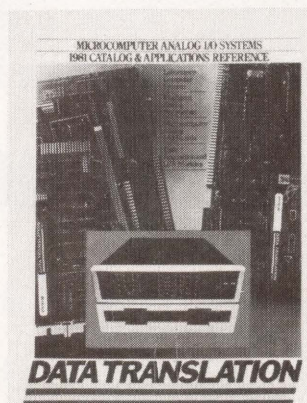
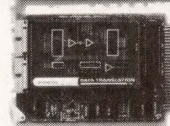
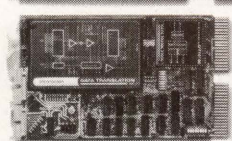
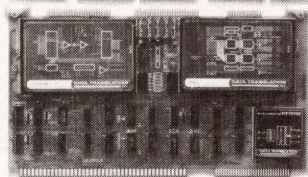
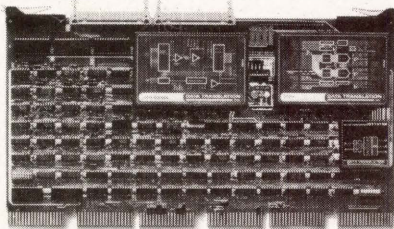
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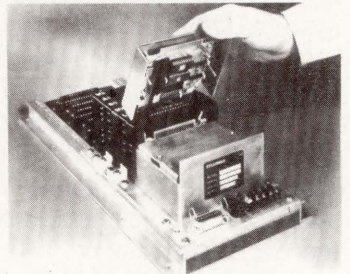
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DIGITAL CONTROL AND AUTOMATION SYSTEMS

DC & AS BRIEFS

Microprocessor Based Control System

An integrated network of I/O modules connected to a microprocessor on a motherboard, the MECA (modular electronic control assembly) system automatically monitors operating functions such as temperature, time, position, and switch closures and openings and issues control commands. An English-like language called SYBIL (Sylvania BASIC industrial language), a subset of American National Standards Institute BASIC, is used to program user specifications into erasable ROM. I/O modules are directly addressed with data from the flow diagram. After the program is verified, it is burned into P/ROM (2k or 4k bytes). Completed programs can also be stored on a floppy disc.



In operation, the system from GTE Electronic Control Operation, 400-2 Totten Pond Rd, Waltham, MA 02154, transmits programmed logic through the input modules, processes it as directed by the program, and commands output modules to turn on or off as required. A realtime clock can be used to program up to 26 timing functions and permits control of time of day functions. Four terminals serve as a communications loop.

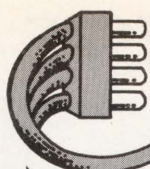
Circle 445 on Inquiry Card

12-Bit Data Acquisition Module

Digitally programmable gain options over a range of 1 to 1000 (with corresponding throughput rates of 40 and 3.8 kHz, respectively) and a jumper selectable input configuration of either 16 single-ended or 8 differential input channels are key features of the DT5712 data acquisition modules. Included in the device are 16-channel MUX, instrumentation amplifier, sample/hold amplifier, 12-bit ADC, and timing and control logic. The basic general purpose module offers relative system accuracy ranging from ± 0.5 LSB to $\pm 0.1\%$ from low to high gain. All versions can accept unipolar or bipolar analog inputs of between 10 mV and 10 V, and deliver 12 bits of TTL compatible, 3-state digital outputs in straight binary (unipolar) or offset binary and 2's complement (bipolar) data formats.

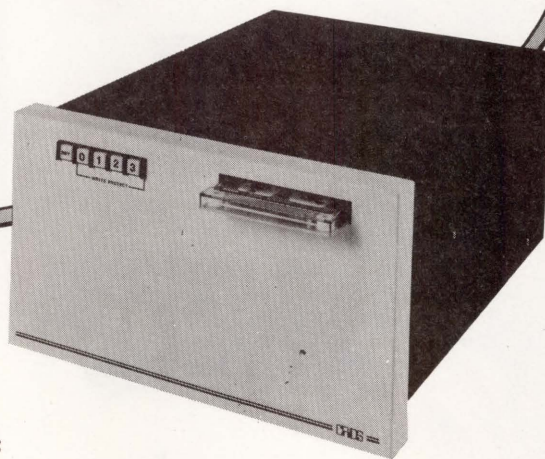
Monotonicity of the microcomputer compatible modules offered by Data Translation Inc, 4 Strathmore Rd, Natick, MA 01760, is maintained over a 0 to 70 °C operating temperature range. Either of two oncard gain options are available for software programmable operation: 1, 2, 4, and $8 \pm 0.05\%$ and 1, 10, 100, and $500 \pm 0.1\%$. The number of channels can be quadrupled by adding a DT02EX DTI expander module.

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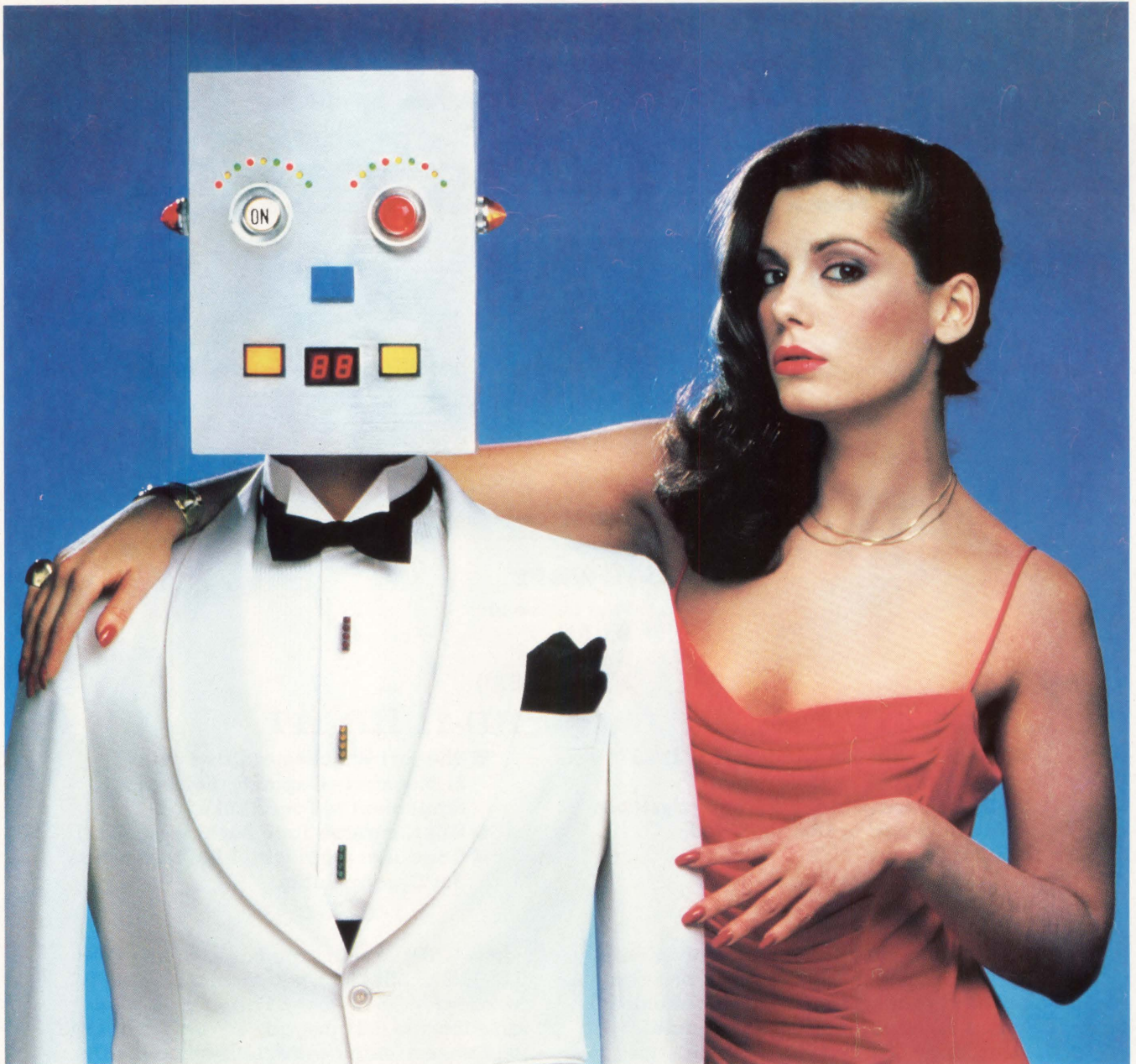
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DESIGN IN DIALIGHT

DC & AS BRIEFS

Data Acquisition and Control Systems and Components

Single-Chip Microcontrollers

Several low power devices have been added to its COPSTM family of single-chip microcontrollers by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Included are five n-channel silicon gate and four CMOS microcontrollers and a CMOS RAM and timer peripheral. Because all are MICROBUSTM compatible they can serve as microprocessor peripherals and communicate with a host microprocessor in less than 1 μ s.

There are 21 variations of n-channel silicon gate devices. COP444L/445L dissipate 55 mW of power at 5 V, and feature true vectored interrupt plus restart. The 444L is a 28-lead DIP with 23 I/O lines; the 24-lead 445L has 19; both contain 2k x 8 bits of ROM and 128 x 4 bits of RAM.

COP444L as well as COP410L/411L are available at a high range of 4.5 to 9.5 V and a narrower range of 4.5 to 6.3 V. 410L, a 24-lead DIP with 19 I/O lines, and 411L, with 20 leads and 16 lines, have 512 x 8 bits ROM and 32 x 4 bits RAM. The 40-lead COP404L has 32 x 4 bits of RAM but no ROM; up to 2k external P/ROM can be used with it. Extended temperature range versions (-40 to 85 °C) are also now available for the 410L/411L; similar versions of the other three devices will be available soon.

COP420C, 421C, 320C, and 321C—the CMOS microcontrollers—contain all system timing, internal logic, ROM, RAM, and I/O needed for dedicated control functions and use the same instruction set, pin-out, and architecture as other family members. Power dissipation is typically 50 μ W. 420C and 421C are identical except that the former has 23 I/O lines and the latter has 19. 320C and 321C are extended temperature range versions of the 420C and 421C, respectively. Vectored interrupt plus restart and 3-level subroutine stack are features.

MICROWIRETM compatible, the CMOS devices can be used with LCDs; ADCs; external RAM, ROM, or P/ROM; and frequency measurement and control peripherals. Other features include 2.4- to 6.0-V, single-supply operation; 15- μ s instruction time; internal time-base counters; LED direct drive outputs; and general purpose and TRI-STATE^R outputs. All devices are TTL compatible.

The COP498 is a 14-pin CMOS RAM and timer peripheral that enables n-channel microcontrollers to operate at power levels approaching those of CMOS circuits. It can turn off power when the microcontroller is not in use and then turn it back on at a preset interval or when activated by an external interrupt. Four registers of 64 bits each hold the contents of the microcontroller's RAM while power is off, then reload it when the device turns power back on.

DESIGN IN DIALIGHT READOUT PRODUCTS.

READOUT ASSEMBLY

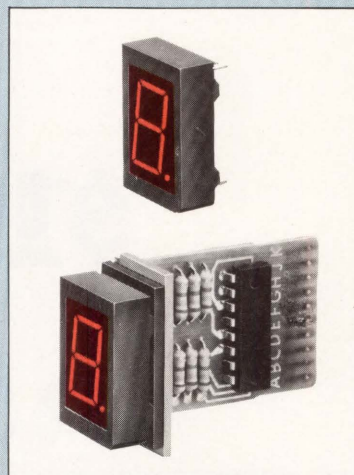
Series 739 are 0.600", seven-segment LED readout displays designed in a package with their associated decoder-driver circuitry and mounting bezel. The entire assembly, with as many digits as you need, is ready for instant panel mounting.

Series 749 assembly uses 0.300" display modules.



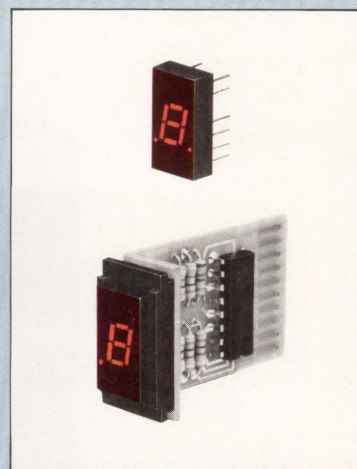
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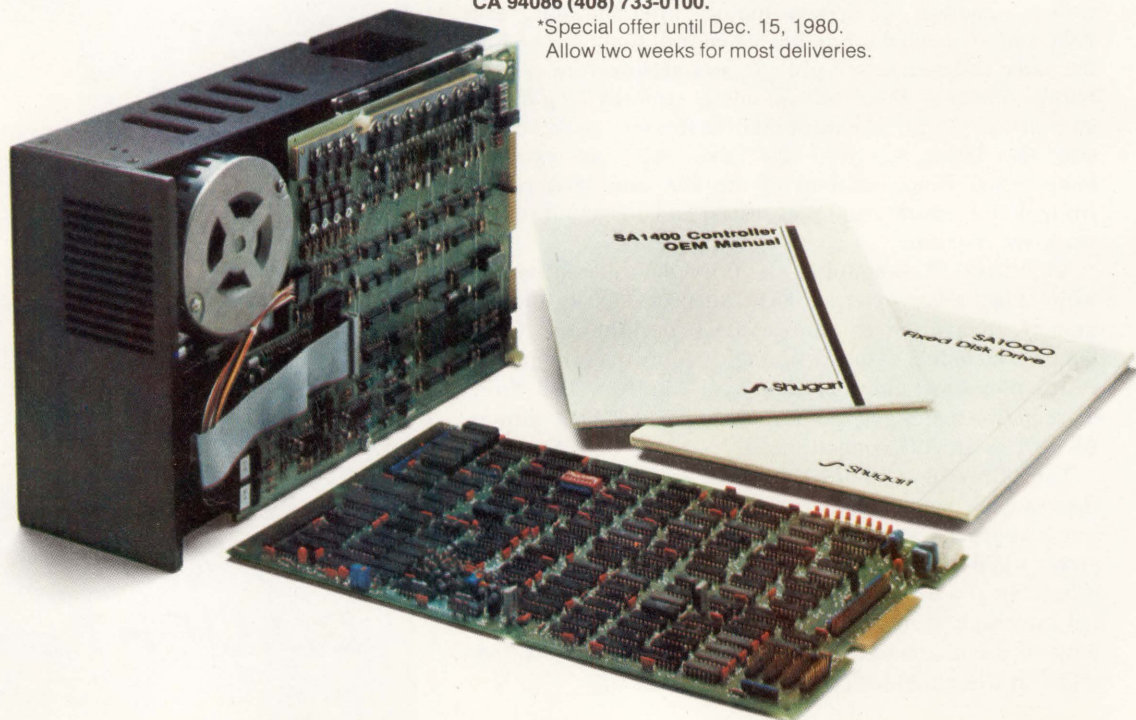
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DC & AS BRIEFS

Process Control and Display System

Metrascope M/S 99, a color CRT terminal with 16-bit microprocessor, displays up to 64 channels of analog input data in bar graph format with engineering unit scales. Four alarm setpoints are provided for each channel under operator control with a variety of control outputs available under software management. The display includes derived data, such as averages and deviations, as well as the original input data, with the digitized value of each channel. Information on the display can be output in serial ASCII format through an RS-232 interface for connection to peripherals or a host computer. A cartridge recorder retains data on all input channels for a playback in simulated real time, in slow motion, or frame by frame. An optional 80-col printer provides hardcopy on alarm, operator command, or a preset time cycle on any of the channel setpoints. This terminal is available from Metra Instruments, Inc, 2056 Bering Dr, San Jose, CA 95131.

Circle 447 on Inquiry Card

Input/Output Systems and Devices

8-Channel I/O Processor

Two microprocessors onboard the F6420 I/O processor operate in parallel, one dedicated to I/O and the other to applications code (with resident multi-user BASIC). Half the address space of each is paged to a 0.25M-byte multiport synchronous common memory; the other half is used for on-board private memory. The 8-channel processor, announced by Gould Inc's Functional Automation Div, Nashua, NH 03060, is an independently functioning element of a microprocessor based mainframe made up of loosely coupled groups of specialized I/O and computational processors. Among the other components are disc I/O and switching elements.

Circle 449 on Inquiry Card

BCD Decoding Board

Interface of computer controls to manufacturing and process systems and NC/CNC units to machine tools is achieved through use of a BCD decoding board introduced by DNH Industries, 2807 Oregon Ct, Bldg D1, Torrance, CA 90503. As many as 18 isolated inputs and six unlatched outputs can respond to any 2-digit BCD number. Other relay contacts are available for interlocking or sequencing, and time delay relays can be used for further expansion. Relay contacts function in ac or dc circuits and are not polarity sensitive. Output contacts are 3 A resistive at 120 Vac or 30 Vdc and are dedicated to BCD numbers by the location of programming matrix pins.

Circle 450 on Inquiry Card

High Performance Data Acquisition Devices

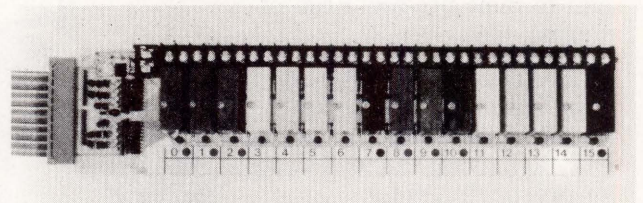
HI-5900 and -5901 have been introduced as the first of a series of data acquisition ICs from Harris Semiconductor Group, PO Box 883, Melbourne, FL 32901, that are fabricated with that company's leadless chip carrier (LCC) technique. (Monolithic dice are packaged in LCCs and soldered to both sides of a multilayer ceramic substrate to form a 32-pin DIP.) All features of the two devices are identical except that the -5900 has 8 differential input channels while the -5901 has 16 single-ended input ports. Input signals are multiplexed and amplified into an output track and hold amplifier. Fault protected inputs and channel expansion capability are provided for the MUX, and programmable gains of 1, 2, 4, and 8 are implemented in the instrumentation amplifier.

A multichannel data acquisition system can be formed by combining one of these ICs with a commercially available ADC such as the HI-5712. Channel to channel acquisition time is 9 μ s. Power consumption is 250 mW. All functions are compatible with DTL, TTL, and CMOS logic levels.

Circle 448 on Inquiry Card

I/O Module Board

Because it uses industry standard modules, the MBE-16 I/O module board eliminates the need for inventories of many different types of higher priced buffered modules. Introduced by duTec Inc, 4801 James McDivitt Rd, Jackson, MI 49204, the boards feature color coded barrier terminal blocks to ease wiring and an onboard LED logic voltage monitor that reduces troubleshooting time. Plug-in logic supply, field wiring fuses, positive module hold down, card edge logic connector, and pull-up resistors are standard.



Circle 451 on Inquiry Card

Miniature Transmitter System

A 2-wire miniature temperature transmitter with integral sensor, the CT-850-A Sensitron is an air measurement system for energy monitoring and industrial control applications with 4- to 20-mA MUX interface. Signal transmission can be over several miles with two small gauge unshielded wires without signal interference. Available from Hy-Cal Engineering, 12105 Los Nietos Rd, Santa Fe Springs, CA 90670, the 2 x 2 x 1" (5 x 5 x 2.5-cm) devices have linear output with temperature over a range of -50 to 250 °C. Power requirements are 12 to 28 Vdc. □

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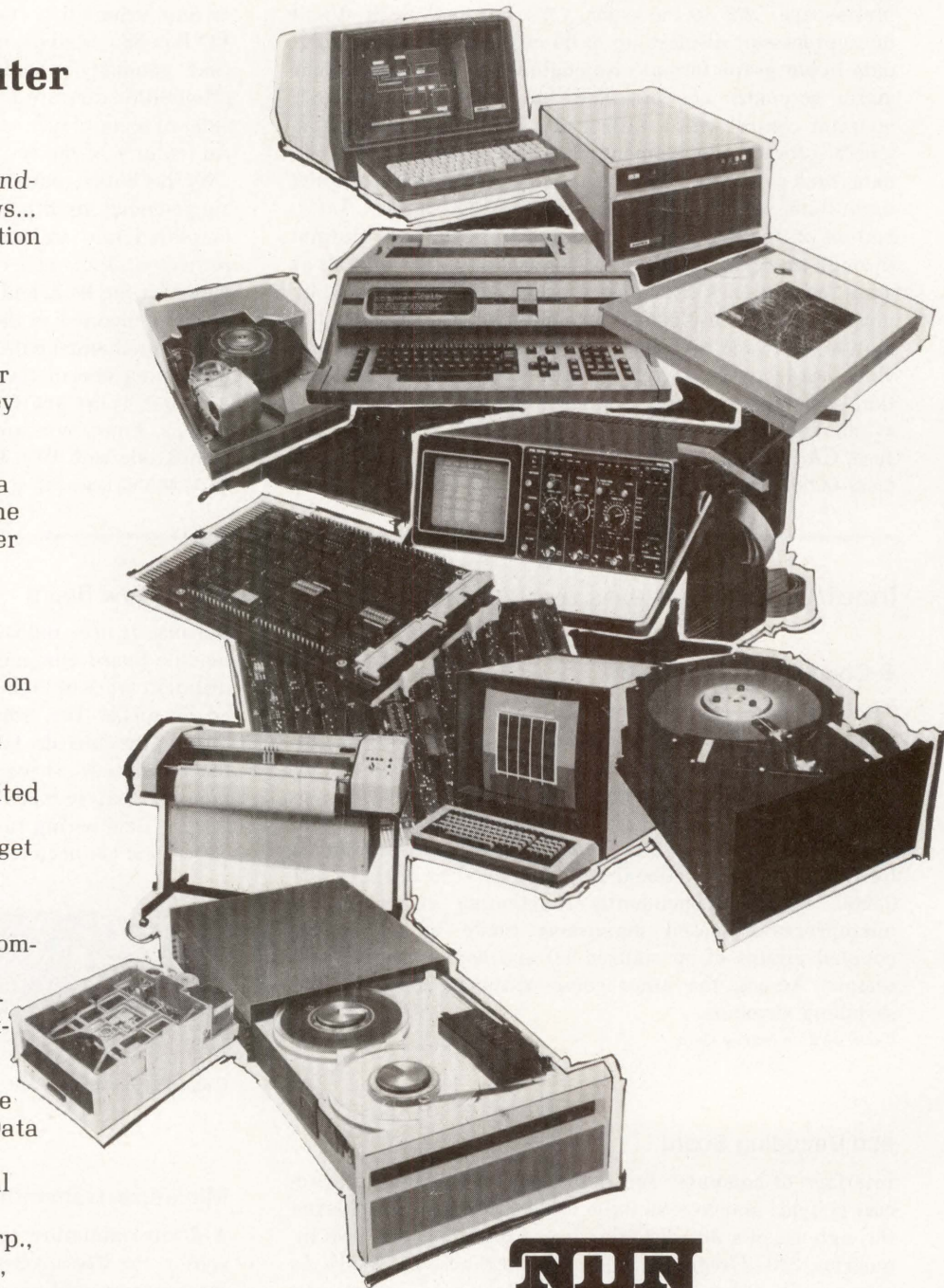
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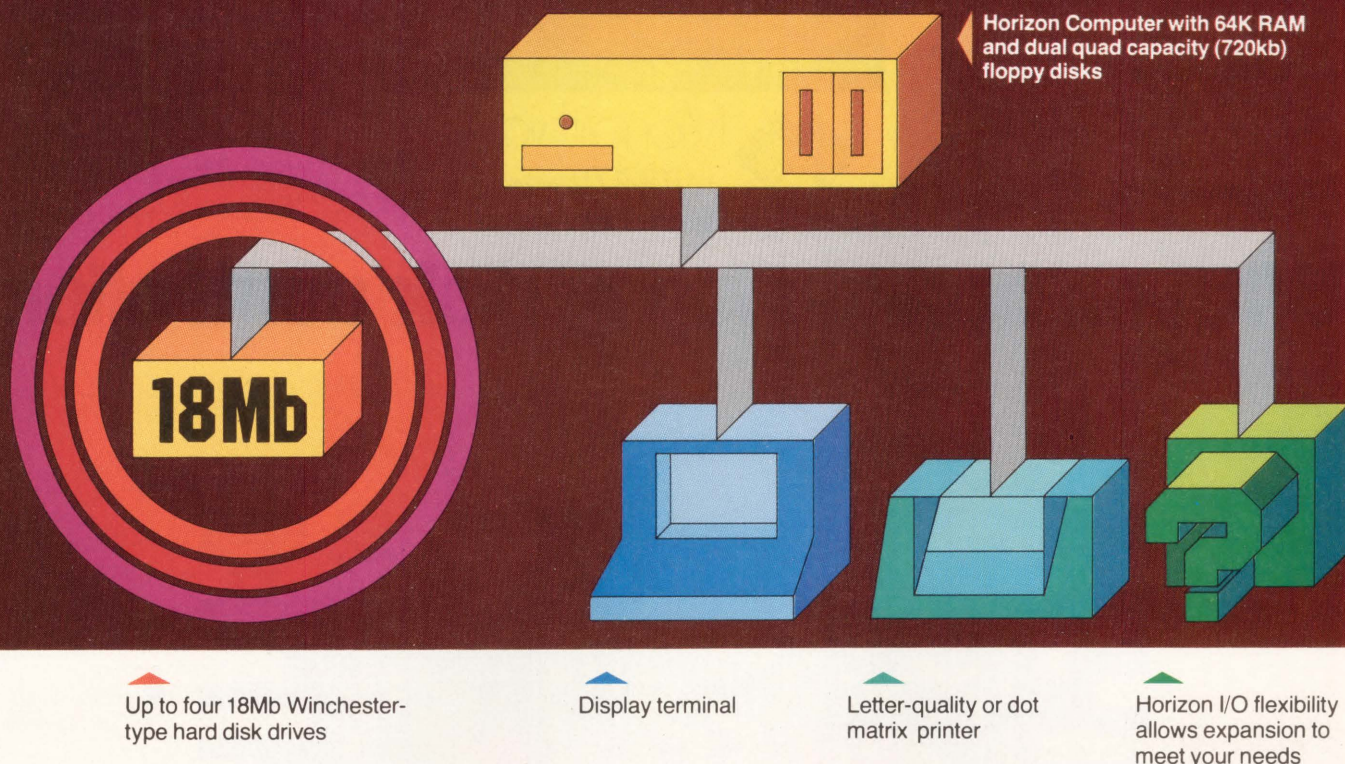
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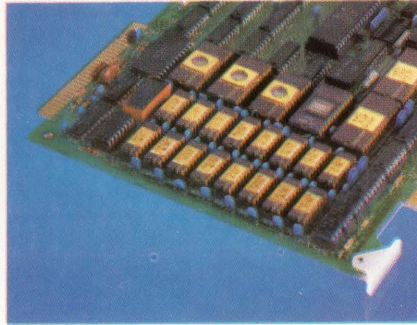
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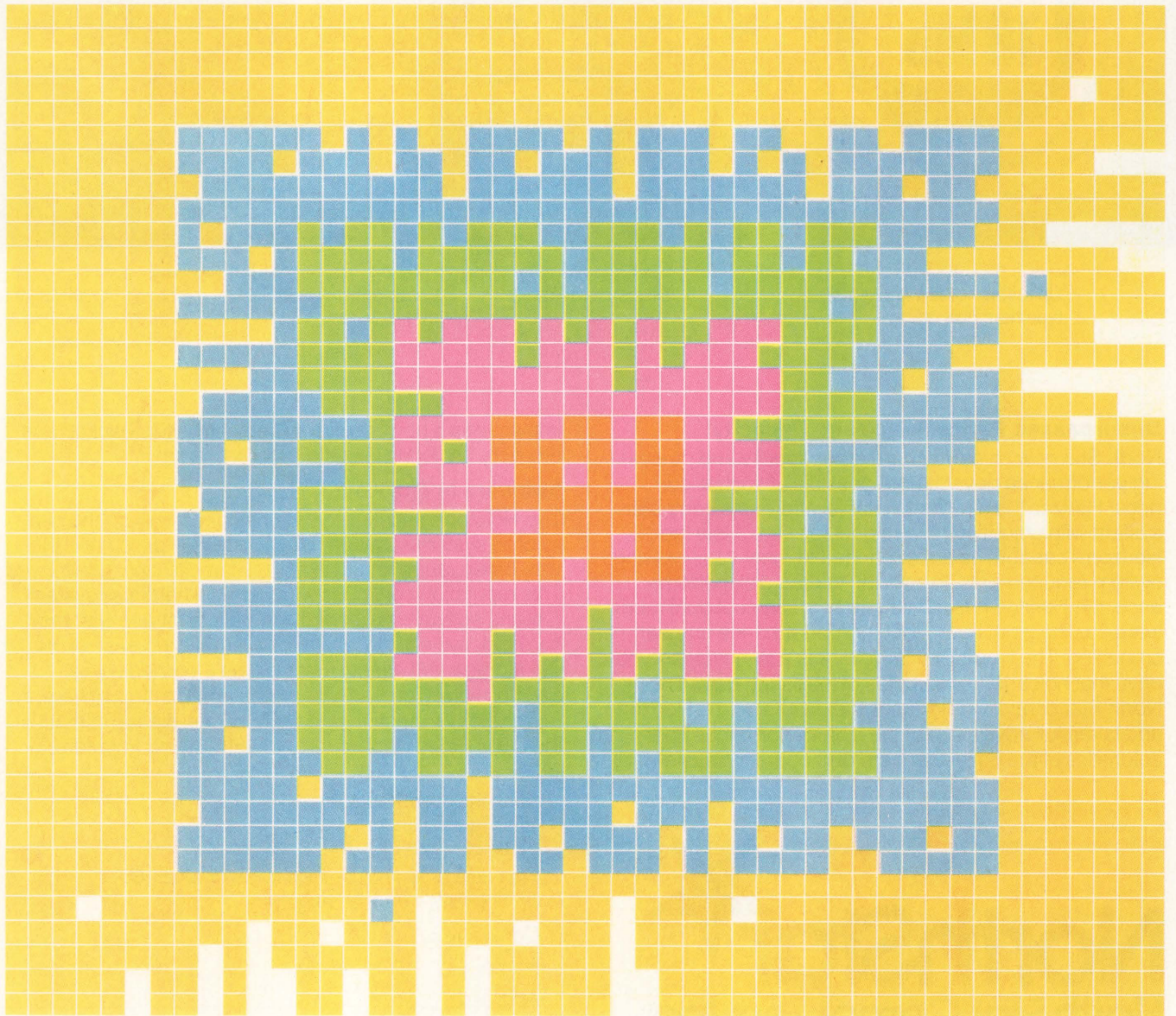
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CIRCLE 80 ON INQUIRY CARD

ADVANCES IN INTERACTIVE GRAPHICS SYSTEMS ARCHITECTURE

Formerly dominated by the rapid growth of minicomputer technology, interactive graphics systems now reflect current microprocessor, RAM, and display technology trends that combine to make established architectures increasingly cost-effective

Walter M. Anderson

Lexidata Corporation

37 North Ave, Burlington, MA 01803

While the roots of computer graphics technology go back to the late fifties and early sixties, applications at that time were restricted by economics to military command and control, a few universities, and research and development laboratories of large corporations. Through the late sixties, available hardware was expensive and of limited capability. Graphics terminals were connected to large mainframe computers and, therefore, were expensive to operate. Finally, lack of commercial vendors forced potential users to develop their own systems and software.

Two technological developments in the late sixties spawned the birth and rapid growth of an industry devoted to the design, manufacture, and support of turnkey interactive computer graphics (ICG) systems that the end user can make productive in a variety of applications—without need for software development and with only a modest investment that quickly pays for itself. These new technologies were the direct view storage tube, first developed for radar, and the minicomputer. The direct view storage tube provided low cost, high density graphics display without the expensive electronics required to support a stroke refresh display, while the 16-bit minicomputer made available low cost computing of sufficient power to support the interactive graphics applications of the time with adequate responsiveness to the operator. Evolution of systems during the past decade has closely paralleled the evolution of the 16-bit minicomputer, with its memory and peripherals. While the direct view storage tube has undergone less spectacular change during this period, ICG systems have taken advan-

tage of larger screen sizes, lower costs, and advances such as limited stroke refresh.

During the last decade, ICG system architecture has evolved to take advantage of higher performance, lower cost central processing units (CPUs), lower memory costs, and advances in peripherals—particularly mass storage systems. The driving forces have been economic, ie, to provide more functionality at lower cost. Performance requirements have grown as more complex applications have been attempted. ICG systems are used today for a wide variety of activities in design, manufacture, and documentation. Applications include drafting, electrical design of integrated circuits and printed wiring boards, schematics, architectural engineering, mapping, 3-dimensional mechanical design, and finite element modeling. Hardware and software have advanced to such an extent that it is difficult to find an application where manual methods are more cost-effective than those of computer systems, providing that the user's volume of work is sufficient to keep the ICG system busy.

Design of systems under development is based on technologies that have evolved in the last few years. New architectures are designed around single-chip microprocessors, low cost semiconductor random access memory (RAM), low cost mass storage peripherals, and color raster display technology. A major slice of system cost in the past decade has been ICG software. While the prospects for software development are not as bright as they are for hardware, major progress is being made in the form of transportable ICG software, ICG system design standards, database

standards, and ICG software modules available from hardware vendors that can vastly decrease development costs. Over the next few years, these advances will benefit the user in the form of ICG workstations in myriad applications and as widespread as the alphanumeric display terminal.

Evolution of ICG Architecture

The earliest turnkey ICG systems consisted of a single terminal connected to a dedicated CPU and disc, as shown in Fig 1(a). The terminal shown in Fig 1(b) consists of a direct view storage tube (DVST), an alphanumeric keyboard for input of text and commands, and a graphic input device, often a data tablet but occasionally a gantry or free cursor digitizer. The terminal is sometimes augmented by a second DVST to display an auxiliary view of the graphic data, an alphanumeric video display terminal for commands and error messages, or an auxiliary function keyboard. A few terminals have combined a pen plotter on the digitizer surface to plot back data captured by operator input.

Additional components of the system in Fig 1(a) are a 16-bit minicomputer with 16 to 24k bytes of core memory and a disc containing less than 1M bytes of secondary memory. In addition, some form of compatible input/output such as magnetic tape was usually part of the system, as was an online plotting device for graphics hard copy. The disc retained the graphics data base as well as core images of the heavily overlaid software. Architecture of this early ICG system was constrained by a relatively small amount of main memory; core memory was extremely expensive and required laborious assembly language programming in order to obtain good performance.

Earliest turnkey ICG systems cost more than \$100,000 in 1970. Although they could interactively digitize input, edit graphics data bases, do check plots, or generate output for external processes, they could perform none of these tasks in combination. Few applications justified a system that could execute only one task at a time, and those that could had to employ them during two or three shifts daily.

First applications of these turnkey systems were for electrical design—the layout of integrated circuit (IC) masks and printed wiring boards. Since the growing complexity and precision of mask sets precluded manual drafting of an IC layout, and data required for numerically controlled pattern generators could be obtained only with the aid of a computer (most naturally through a man-machine graphics interface), use of an ICG system for IC layout was indicated regardless of cost. Justification of early ICG systems for the layout of printed wiring boards was more difficult because of the expense when hand taped designs were acceptable. First users of ICG systems for printed wiring boards acted in conjunction with automatic routers where the required manual connections and rerouting could be easily accomplished on the computer generated data base through an ICG terminal.

While early ICG systems were capable of generating schematics, 2-dimensional mechanical layouts, and general drafting, payback was insufficient to justify their use. The ICG industry had to cut costs and break into much larger markets involving nonelectrical applications in order to grow. A software solution was the first technical approach to this problem of lowering costs; it improved system func-

tionality yet increased hardware costs by only a small increment.

This single-user ICG system was augmented with a small amount of additional core memory that allowed it to execute more than one task at a time. Two ICG terminals could not, initially, be used from one CPU and disc. Eventually, the single-task ICG system was expanded to allow operation of the pen plotter output device and/or a blind digitizer workstation simultaneously with the interactive graphics terminal. For a small increase in cost, an ICG system in new applications accomplished up to three times as much work, provided that there were equal amounts of digitizing, graphics editing, and plotting to be done. Since equal loading requirements for digitizing, editing, and plotting are not the norm, however, optimal hardware utilization was not achieved. The multitasking, single-terminal ICG system was only marginally more cost-effective than the single-task, single-terminal system.

The next evolutionary step in the advance of ICG design [see Fig 1(c)] was also, essentially, a software approach to increase cost-effectiveness. It shared the single CPU and disc among several interactive graphics terminals, as well as blind digitizers and plotting devices. Operators used core resident, interrupt driven software. Processing of the data base, redisplay on the DVST displays, and generation of plot vectors were handled on a round-robin basis as different tasks were swapped into and out of main memory from disc. Performance was degraded somewhat over a single-user system, but since the most demanding tasks (eg, redisplay on the DVST) had a low duty cycle and occurred asynchronously between users, each user could operate nearly as effectively as is possible on a single-user system. With the new freedom afforded by mixing graphics editing workstations, digitizers, and output tasks, the user could assemble a system balanced to meet the needs of a specific application. Hardware was more optimally utilized and the full value of task simultaneity more completely realized.

As the cost of memory dropped, the next innovation in ICG design incorporated into the CPU much more memory than the 16-bit minicomputer's address space had allowed. Memory was managed by the operating system in order to retain more tasks in memory at the same time. Thus, reduced traffic between disc and memory improved performance and allowed finer quantization of timesharing so that several users could redisplay their data bases simultaneously.

From the first appearance of the timeshared ICG system, evolution proceeded in the direction of improved performance at cost comparable to or lower than that of the status quo. During the past five years, technology applied toward improved performance has developed more and better hardware. Need for increased performance has been motivated by several factors. First, although early timeshared ICG systems performed adequately when evaluated in terms of the system software then available, higher performance was important to reduce operator response time. Second, increased performance allows more terminals to share a single processing facility, leading to lower cost per terminal. Finally, as new application areas—particularly 3-dimensional mechanical design—have opened up and older applications have become more complex, increased performance becomes necessary simply to maintain previous throughput rates.

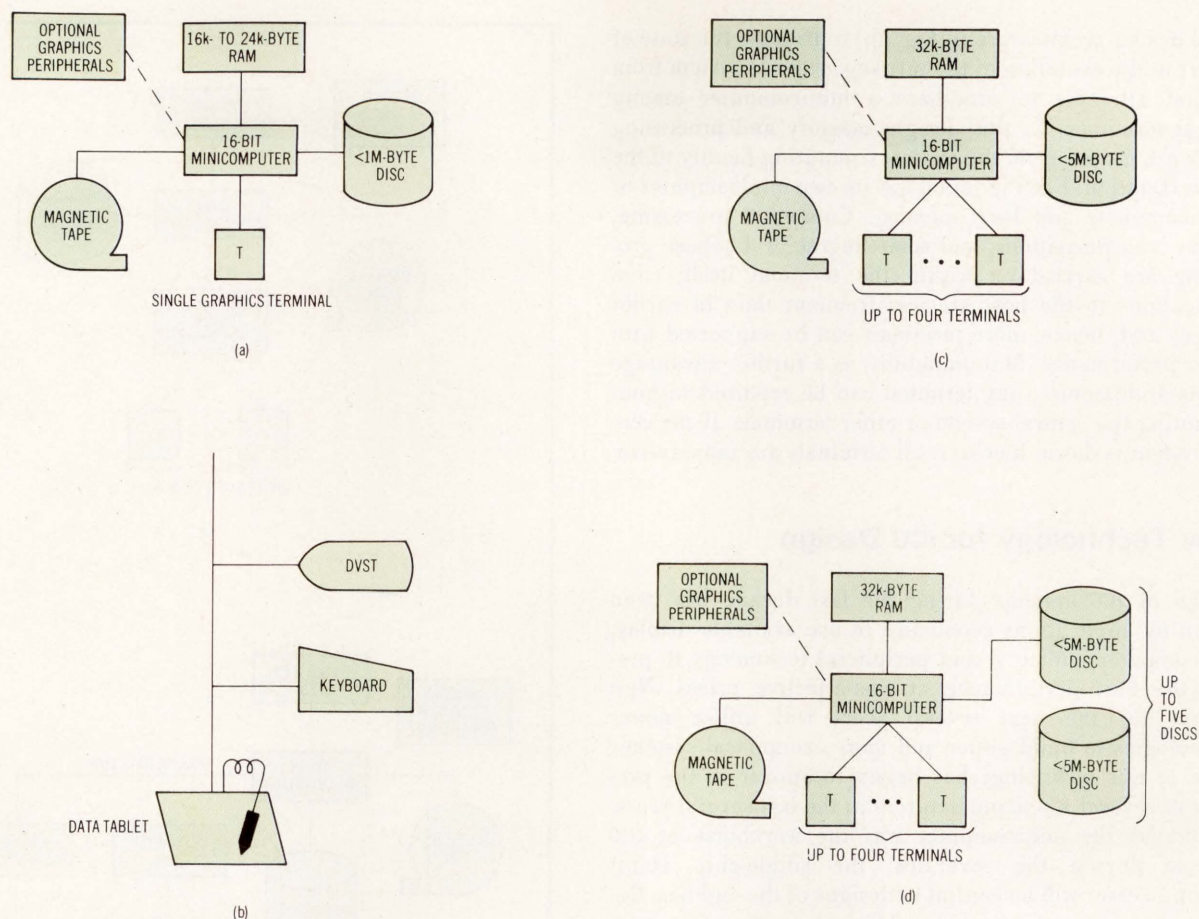


Fig 1 Evolution of ICG architecture. Early systems (a) utilized single terminal per CPU and disc. Each terminal (b) consisted of graphic display, alphanumeric keyboard, and graphic input device, typically data

tablet. Later systems (c) and (d) pursued increased cost-effectiveness by sharing expensive system components between terminals and other tasks

Ingenuity of the system designers, striving to improve technology and optimize performance, has developed new system architectures with low incremental cost impact on existing software. Established turnkey ICG manufacturers have a large customer base of installed systems, and a commensurate software investment. Changes in system architecture are feasible for established ICG manufacturers only if they can be accomplished in such a way that their vast base of applications software is preserved. In the newer architectures of established vendors, it is not unusual to find the application software of much earlier systems running largely unchanged under several layers of operating system software that emulates earlier generation environments. New entries in the industry, however, can be more innovative and take better advantage of recent hardware technology because they are not encumbered by an existing software history.

The architecture of Fig 1(d) illustrates one effort to increase performance of ICG systems. Its design is based on the assumption that the latency for random database accesses on a single disc is a major factor restricting performance. For this reason, it includes a disc for the overall

system as well as one for each ICG terminal on the system. The operating system optimally positions heads for each terminal's disc independent of what other terminals require. This architecture ignores processing bandwidth requirements and has not survived because the system in most ICG applications is processor limited, not disc limited.

Current systems often employ variations of the architectures shown in Fig 2. In Fig 2(a), a second processor is added to the primary host CPU to share the processing load of the interactive terminals. Designs of this type exemplify that 16-bit minicomputers have topped out in their performance and that further increases in performance of an ICG architecture require multiple CPU elements operating in parallel. The second CPU is often a special purpose processor designed to speed up terminal processing for device input and display computations. The first CPU is used to control system operations, process the data base, maintain the file structure, and communicate to peripherals other than the terminals. Terminals in this design are essentially those of earlier systems, devoid of all local memory and processing power, and totally dependent on the central processing facility to function.

ICG design architecture in Fig 2(b) represents the state of the art in the evolution of the turnkey graphics system from its first attempts to timeshare a minicomputer among several terminals. In this design, memory and processing power are moved from the central computing facility to the ICG workstation. Each terminal has its own minicomputer or microcomputer and local memory. Command processing, display transformations, and some degree of database processing are carried on within the terminal itself; communications to the host are less frequent than in earlier designs and, hence, more terminals can be supported with better performance. Maintainability is a further advantage of this architecture; any terminal can be repaired without disrupting the central system or other terminals. If the central system is down, however, all terminals are inoperative.

New Technology for ICG Design

Design of ICG systems during the last decade has been driven by applications economics to use available display, minicomputer, memory, and peripheral technology to provide the best performance at cost-effective prices. New designs for the next several years will utilize newer technologies to build better and more economical systems. Some of this technology has begun to appear in the products of several ICG manufacturers in the last several years.

Whereas the minicomputer was the workhorse of ICG systems during the seventies, the single-chip 16-bit microprocessor will be central to designs of the eighties. Recent microprocessors display architecture and performance that rival those of high performance minicomputers. This processing power is available at a small fraction of the cost of a minicomputer, allowing individual ICG workstations to contain one or more microprocessors.

Semiconductor RAM costs have been declining rapidly as more bits are placed on a single chip and as manufacturers have improved manufacturing technology. Low cost memory has already found its way in large quantities into ICG designs of the late seventies. The central processing facility of a contemporary ICG system may contain 256k bytes or more of main memory to support four terminals; and 64k bytes per terminal is two to four times the memory contained in the CPUs of early single-user ICG systems. Increasing quantities of RAM, perhaps reaching 1M bytes or more per terminal, will soon be common. Recent mass storage peripherals have appeared at prices commensurate with the costs of microprocessors, RAM, and the other technology from which an ICG system is built. Floppy discs have been used in low cost single-user systems of the past several years. Winchester disc technology of higher capacity, performance, and reliability will find its way into the central processing facilities and even the terminals of future ICG systems.

The remaining major element of technology that is beginning to appear in ICG systems is raster video displays. Raster technology is now cost-competitive with the direct view storage tube and offers a number of advantages to the ICG system designer. Display is bright and can be viewed in normal room light. Single points or lines can be erased, avoiding the total erase and redraw required with the DVST.

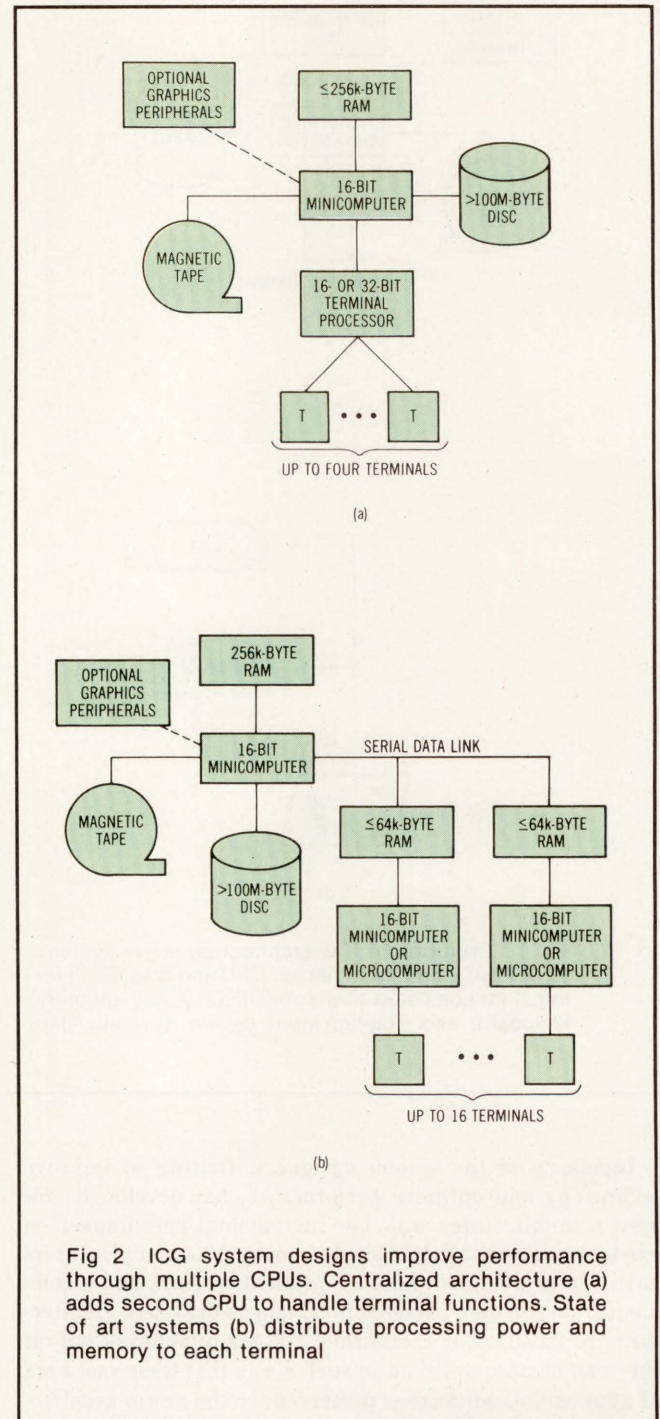


Fig 2 ICG system designs improve performance through multiple CPUs. Centralized architecture (a) adds second CPU to handle terminal functions. State of art systems (b) distribute processing power and memory to each terminal

Dynamic displays for dragging or rubberbanding graphics are possible at high graphics density and without the cost or flicker of stroke refresh displays. Raster displays up to 1280 by 1024 pixels provide high resolution 60-Hz flicker free refresh, as shown in Fig 3. Finally, only raster video technology can offer the user full color display, which is important to increased operator productivity and improved error rates. Cost-competitiveness of raster technology is due to the same rapid declines in semiconductor RAM costs that have pervaded other parts of ICG system design.

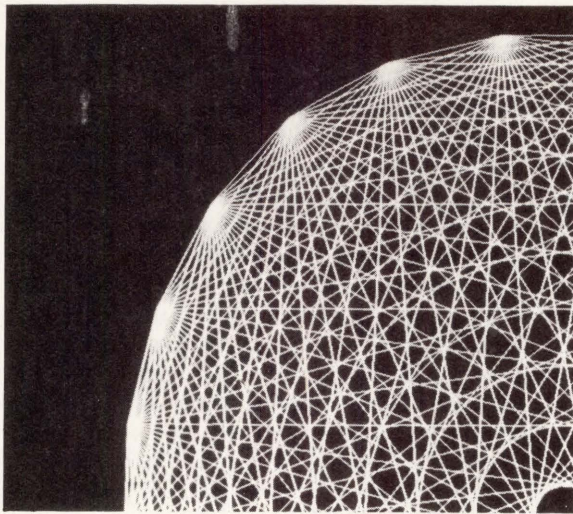


Fig 3 Raster display features outweigh drawbacks. Architecture supports high resolution, flicker free raster displays whose low cost and unique features overcome inherent disadvantage of staircase effect, which is made visible only by enlarging this quadrant from a 1280- x 1024-pixel, noninterlaced, 60-Hz display

Recent and Future System Design

Recent ICG systems have begun to take advantage of the technologies discussed above. The standalone ICG system of Fig 4(a) is being offered by an increasing number of vendors. It utilizes low cost microprocessors, memory, and floppy discs to achieve the same level of performance and functionality as in the earliest single-user minicomputer based systems. Design of ICG systems has come full circle; the newest systems have the same basic architectures as the first system designs. The difference is that newer technology has made this design even less expensive than the per terminal cost of a centralized system architecture.

Centralized system architecture as shown in Fig 4(b) is going to endure, however, because functions that can best be accomplished by a large central processing facility for large scale users will remain—such as plotting, pre- and post-processing of graphics data bases, and database archiving. The major difference between this central processing facility and previous system designs will be that the processor will not handle the interactive terminal users. It will grow instead in word length (to 32 bits), in memory size, and in disc capacity to the point at which it resembles a mainframe; indeed, for many users the traditional mainframe will become the central processing facility.

The major difference in large ICG systems of the future will be that the terminal will be capable of doing all the interactive tasks of current centralized systems (except database archiving) within the local workstation. This will allow a single central processing facility to support more terminals than current designs permit; even small companies will be able to operate their own local graphics capabilities. With much lower communications bandwidth

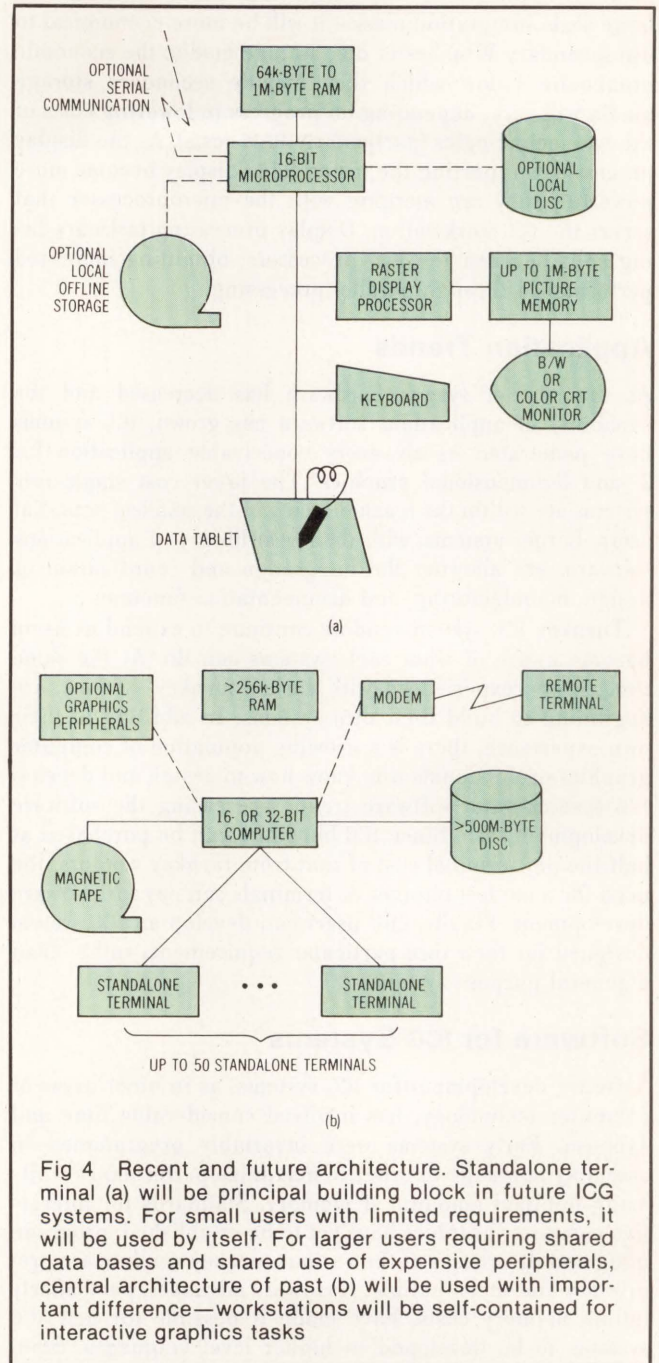


Fig 4 Recent and future architecture. Standalone terminal (a) will be principal building block in future ICG systems. For small users with limited requirements, it will be used by itself. For larger users requiring shared data bases and shared use of expensive peripherals, central architecture of past (b) will be used with important difference—workstations will be self-contained for interactive graphics tasks

to central processing facility required (only for archival storage and retrieval), terminals can be remotied over long distances via modems. Maintainability is improved because local terminals, especially those with local offline storage, can continue with limited capability even when the central processing facility is down.

Within the terminal, ICG design will evolve along performance and cost lines that are indicated by the underlying technology. Powerful microprocessors will do all the processing required to support the ICG user in creating or editing graphics data bases. For many applications with relatively small data bases, all programs and data will reside

in programmable read only memory (PROM) and low cost RAM. In applications with large data bases such as very large scale integration masks, it will be more economical to use secondary Winchester disc storage media; the economic breakpoint below which they include secondary storage media will vary, depending on progress in lowering costs of the two technologies (particularly RAM costs). As the display processors supporting the raster video display become more powerful, they are merging with the microprocessor that serves the ICG workstation. Display processing tasks are being split between the two processors, obtaining increased performance through parallel processing.

Application Trends

As the cost of system hardware has decreased and the capability of applications software has grown, ICG systems have penetrated nearly every conceivable application for 2- and 3-dimensional graphics. The lower cost single-user systems are within the reach of many of the smallest potential users. Larger systems, with their vast library of applications software, are allowing the integration and coordination of design, manufacturing, and documentation functions.

Turnkey ICG system vendors continue to expand as users become aware of what such systems can do. At the same time, users, experienced with earlier turnkey systems, are beginning to build their own systems. In addition to their own experience, there is a growing population of computer graphics professionals who know how to design and develop ICG systems, and software trends are easing the software development task. Since ICG hardware can be purchased at half the per terminal cost of that from turnkey vendors, the need for a modest number of terminals can pay for software development. Finally, end users can develop an ICG system designed for their own particular requirements rather than a general purpose system.

Software for ICG Systems

Software development for ICG systems, as in other areas of computer technology, has involved considerable time and expense. Early systems were invariably programmed in assembly language in order to maximize performance while using minimal amounts of memory. Standards for interactive computer graphics have yet to be established; programming and data bases of the various turnkey vendors are proprietary and incompatible. Hardware advances, particularly falling memory costs, have made it possible for new ICG systems to be developed in higher level languages. Standards for ICG software design and translations between data bases have also advanced. Further, manufacturers of display systems are offering increasingly more powerful software building blocks for ICG system designers.

For an end user assembling his own system, there are a number of available transportable software packages that can be used to integrate hardware from several manufacturers into a complete system with limited development effort. There has been a recent effort to standardize ICG data bases or, at least, provide a means of translating between them. This will benefit the user, who will be able either to choose between vendors or to mix various vendors and still maintain system compatibility. Moreover, database standardization will preserve the option to develop individual systems.

Conclusion

Interactive computer graphics systems have advanced dramatically during the last decade, spurred on by the development of the 16-bit minicomputer, falling memory costs, and other electronics technology. Microprocessors, semiconductor RAM, and raster video display technology are going to dominate new ICG designs in the eighties. While turnkey system vendors will flourish during the next several years, efforts at standardization of software and ICG design, database compatibility, and modular software building blocks available from display product vendors are making it feasible for users to develop their own systems. Current design architectures are moving towards the single-user terminal that was prevalent in early designs, but with use of lower cost technology and often, in a distributed, hierarchical network. Design options available to turnkey manufacturers and end users in the future will be dominated by the available electronic technology; accurately forecasting that technology and its cost five years from now will reveal the future of ICG system design. It seems almost certain that costs will fall, performance will rise, and the installed base of user workstations will increase severalfold.

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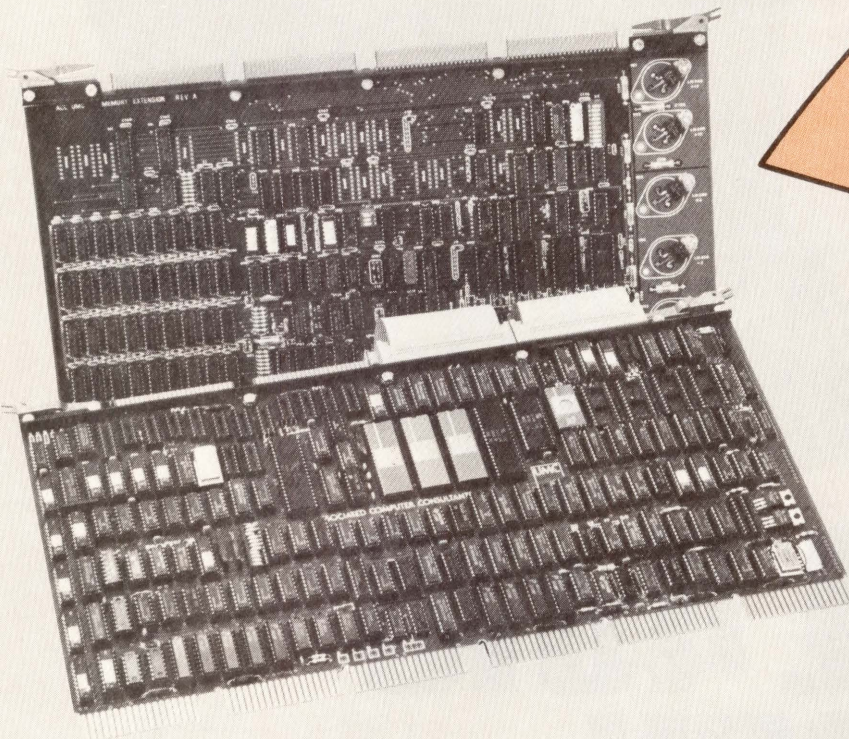
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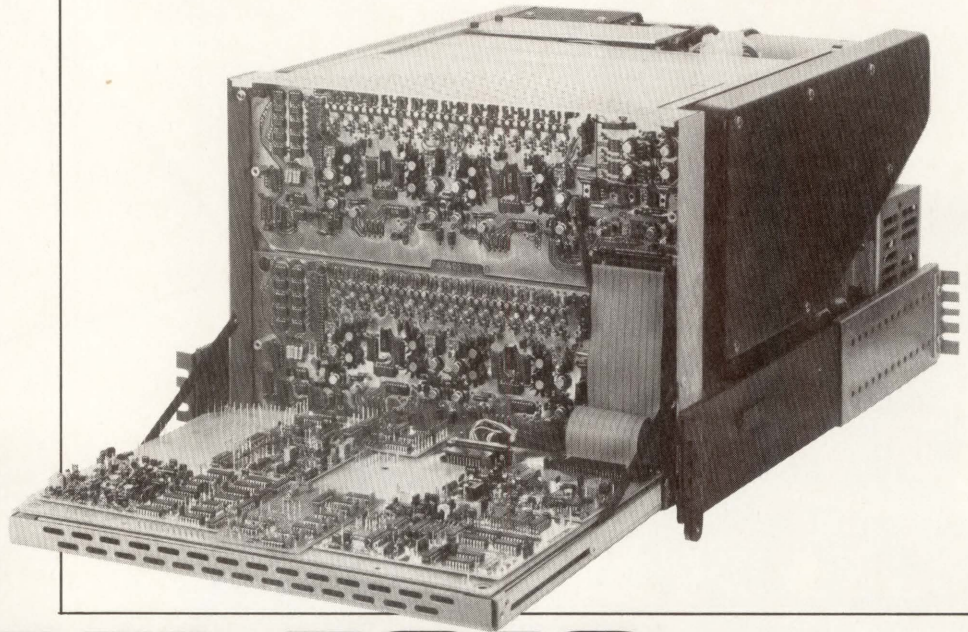
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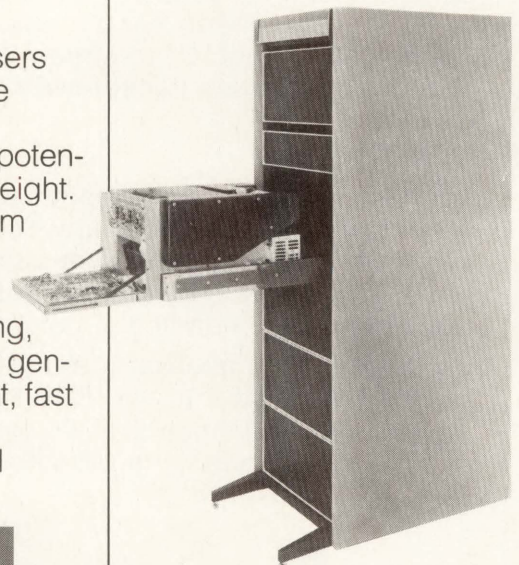
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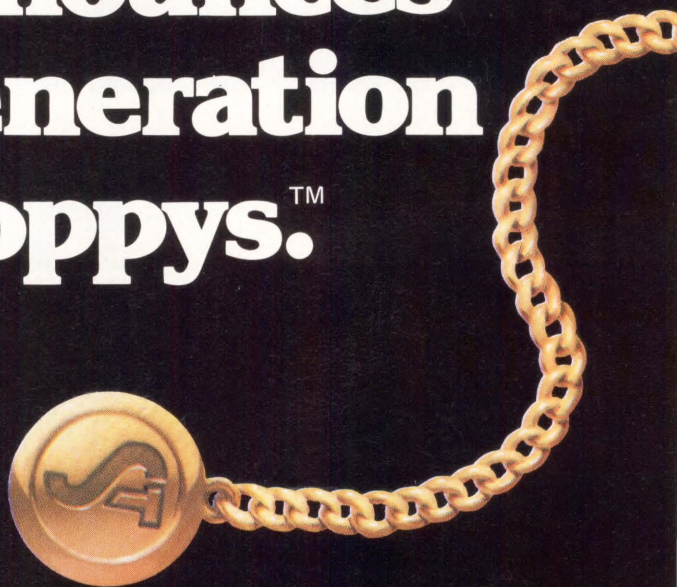
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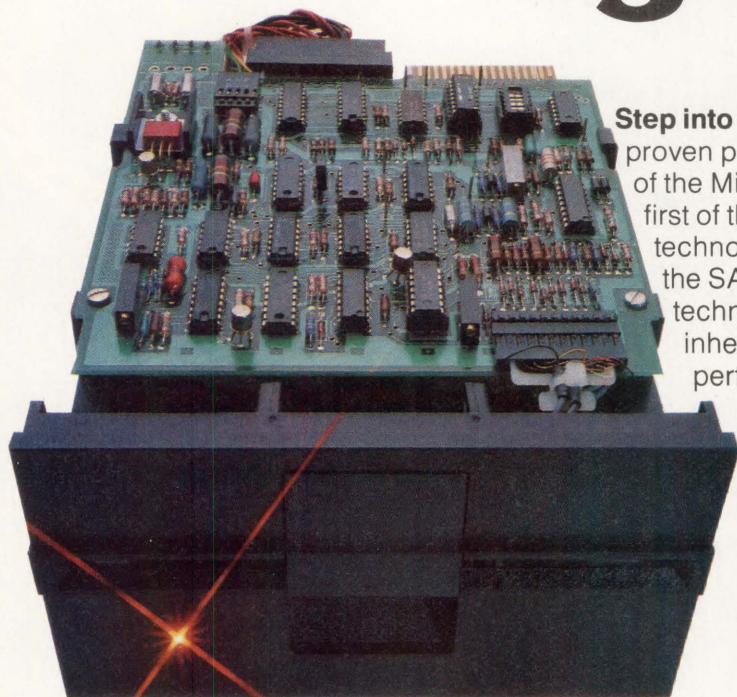




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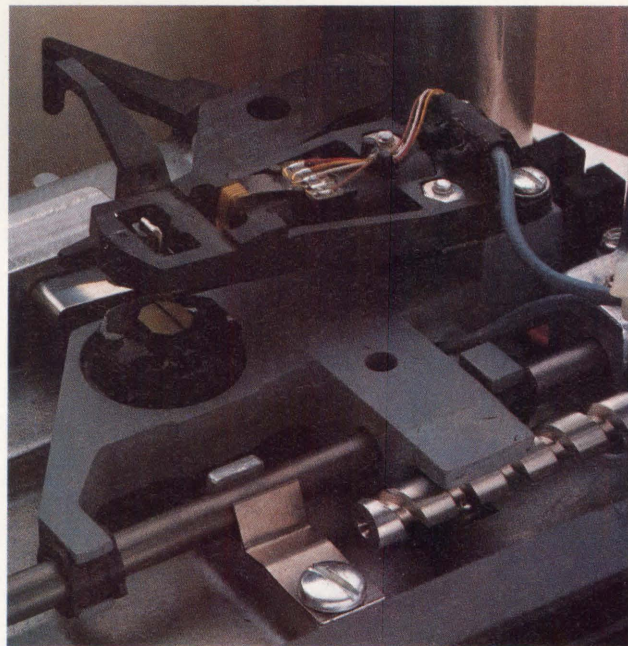
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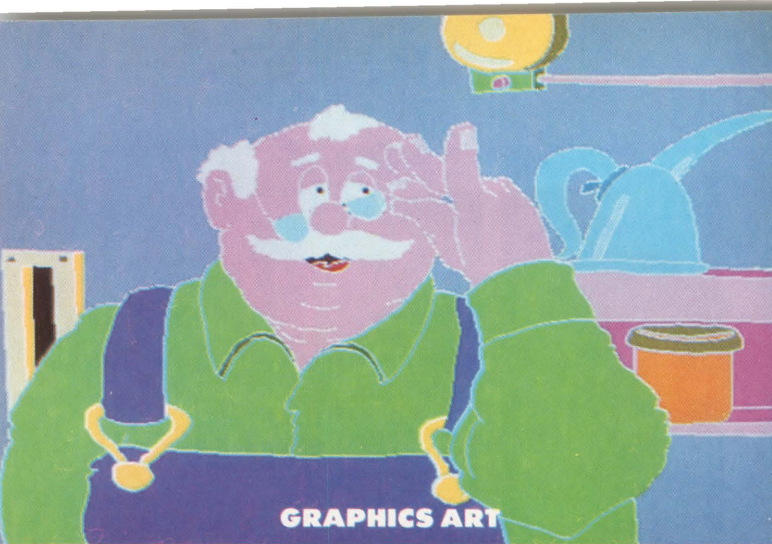
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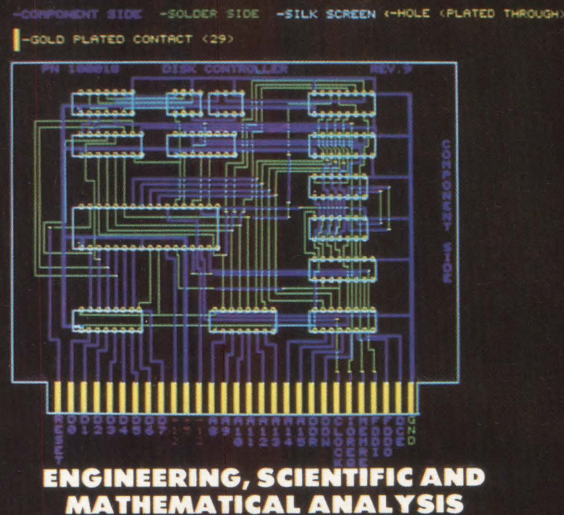


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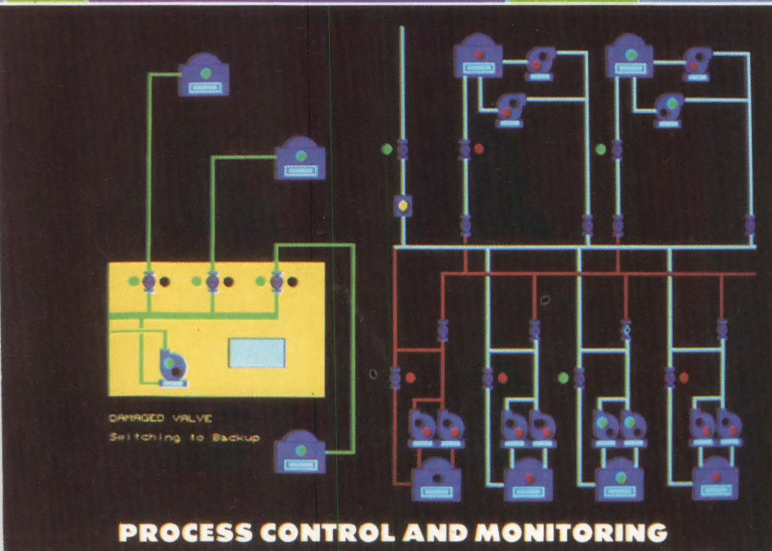




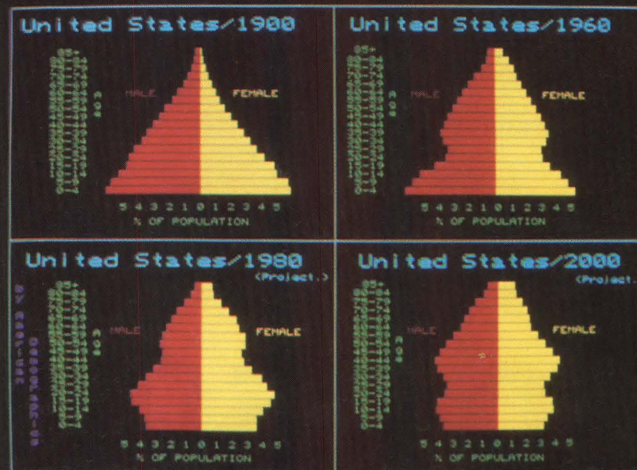
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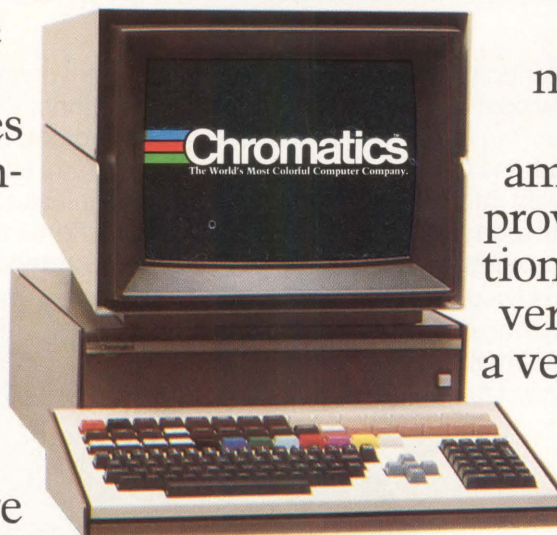
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A large scale integration controller, eight each of five other single-chip devices, and a standard microprocessor interface enable this flexible, 8M-bit bubble memory system to achieve reliable, nonvolatile, solid state storage with 40-ms average access time and automatic error correction. Since all devices are designed in parallel, device tradeoffs optimize not just one component, but the total system solution.

Six different processes (garnet, VMOS, CMOS, bipolar, NMOS, and HMOS) optimize power dissipation, package count, page size versus transfer rate flexibility, self-contained power failure security, system initialization, and multipage block data transfers. Also included are automatic error correction with a system error escape rate of 10^{-14} bits per bit read, a complete status reporting strategy for identification of errors, and a complete but easy to use instruction set with unprecedented diagnostic capabilities including soft and hard error analysis. This overview of bubble memory configuration, operation, and application potential discusses the individual support components and the ways in which they interact when customized for typical applications.

As shown in Fig 1, an 8M-bit bubble memory system consists of the following, all in dual-inline packages: eight 7110 1M-bit bubble memory modules; one 7220 bubble memory controller (40-pin); eight 7230 current pulse generators

(22-pin); eight 7242 dual data formatter/sense amplifiers (20-pin); eight 7250 coil predrivers (16-pin); and eight pairs of 7254 quad transistor packs (14-pin). Implemented as a dual-channel device, the Intel 7110 bubble memory module consists of two half-chips that share a single set of field coils and bias magnets. The assumption is made that chip halves will be accessed simultaneously, each half supplying 160 storage loops, each with 4096 bubble positions. Each half contains two bootstrap loops (bootloops), only one of which is bonded; two bubble generators; two 80-element swap gates, operated in parallel; four 40-element replicate gates, also operated in parallel; two single-element boot swap gates for writing the bootloop; two single-element boot replicate gates for reading the bootloop; and two chevron stretcher detector elements for sensing all bubble data.

Having a redundantly coded stream of data loop status and address information, a bootstrap loop indicates whether each of the 320 storage loops on both halves of the bubble memory module is good or bad and defines page address 0 for the module. One of the two bootstrap loops is selected during prepackage testing, and the appropriate boot swap and boot replicate elements are then bonded to the BOOT.SWAP and BOOT.REP pins on the module. When writing or reading any page of bubble data except the bootstrap data, two bits are written to or read from each storage loop.

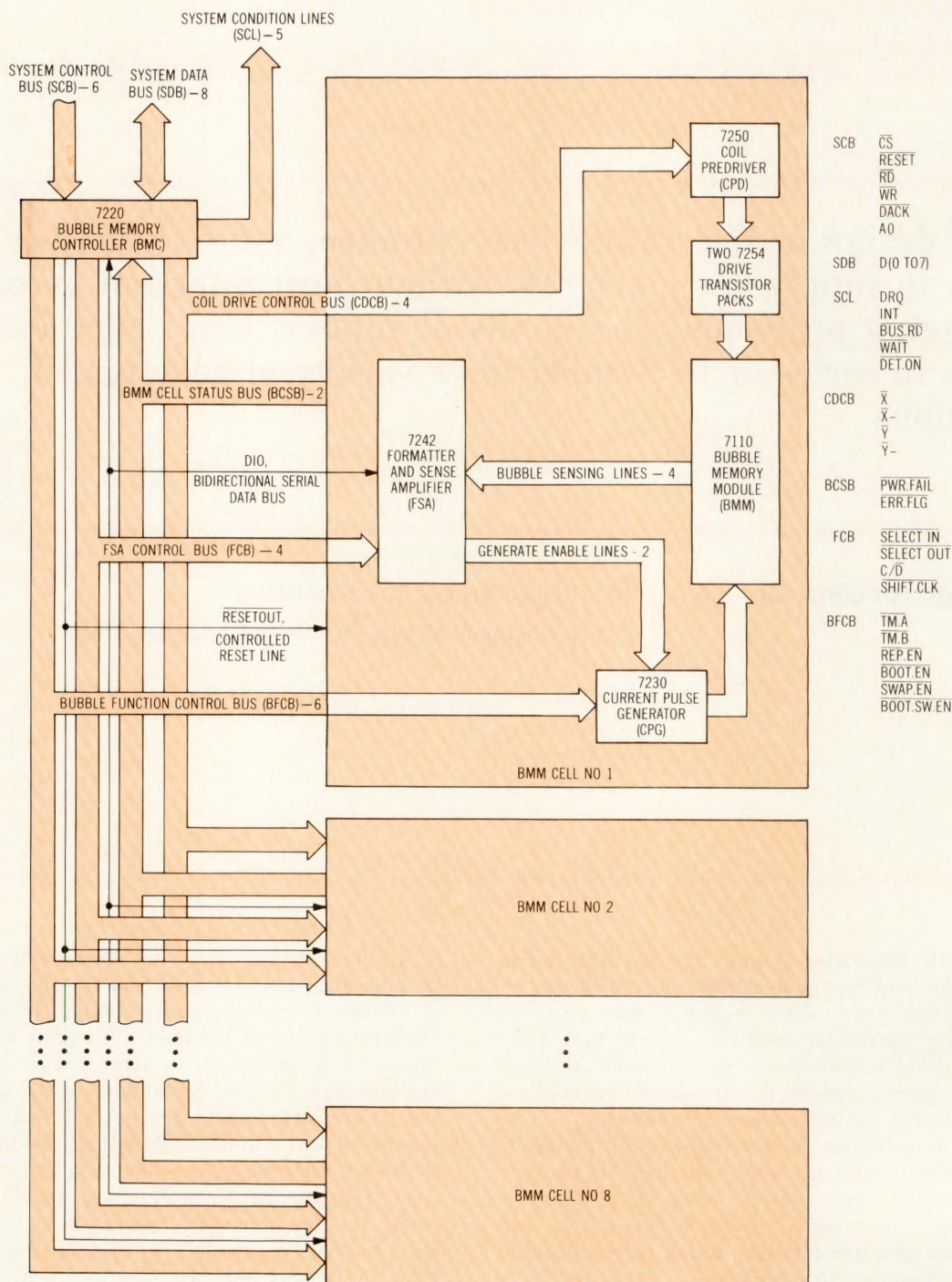


Fig 1 Bubble memory system block diagram. One bubble memory controller connects up to eight 1M-bit modules for maximum 1M-byte storage capacity. Each bubble memory module cell contains five major components (drive

transistors are paired). Cell level FSA data handling achieves configuration flexibility. Operating different numbers of cells in parallel increases system page size while reducing number of system pages

Thus, there are 2048 pages of 320 bits in each half of the module. Of the 320 bits per half page, the memory system will use only 256 bits for data and 14 bits for an error correcting code, leaving an excess of 50 bits per half page. This means that as many as 25 loops need not function in each half of the device. However, since screening is performed at 24 bad loops per half chip, when error correction is disabled, use of an extra loop gives the host a 16-bit utility field for each 256-bit data field.

Support circuitry handles the intricate timing required to accomplish a read or write memory by the many bubble memory module elements. Basically, to write data into the device, a bubble pattern is produced by pulsing the two bubble generators during alternate memory field rotation cycles, propagating the bubbles down the input tracks, and finally pulsing the swap gates to exchange input track data with storage loop data. To read, the replicate gates are pulsed, nondestructively copying the storage loop data into

the output tracks, and then output track bubbles propagate to the detectors for sensing. Each half of the device is implemented in two quadrants (Fig 2), with separate detectors for the two quads tied in a bridge configuration. Since sensing may then be achieved during each field rotation, the channel data rate is doubled without stretching bubbles in adjacent detector stretcher elements. For the bridge detector, bubble data must be multiplexed into the two quads during a write operation, explaining why each quad has its own bubble generator.

System Functional Description

One 7250 coil predriver (CPD) and two 7254 quad transistor packs (QTPs) combine to provide the current drive required for the two orthogonal field coils in each module. Drive

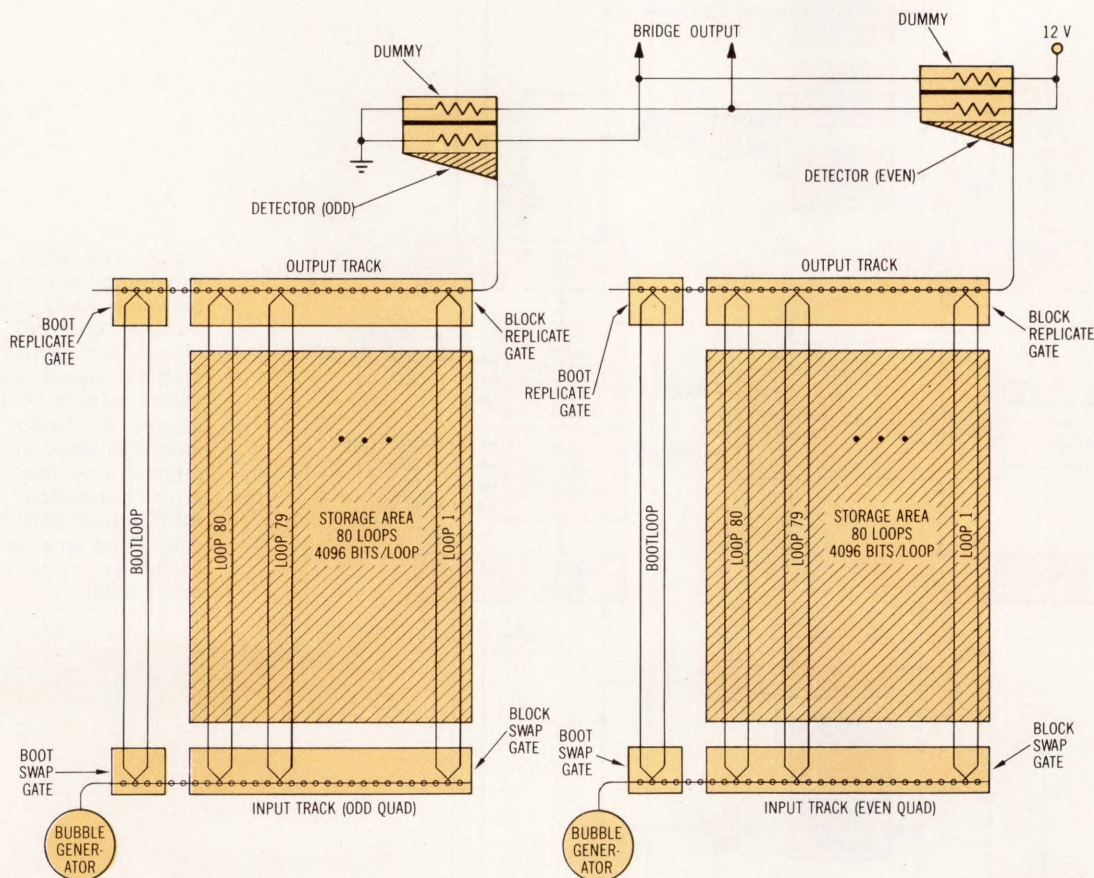


Fig 2 Bubble memory module architecture. Module half, shown here, is organized into two quads with bridge detector that doubles throughput. Read and write operations access two

bits per loop; thus each module half contains 2048 pages of 320 bits. Fifty of the 320 bits/page are redundant bits assigned to bad loops that never receive bubbles

currents are triangular in shape and 90° out of phase, producing a rotating magnetic field in the plane of the bubble chip. Standby power requirements are quite low because the field is energized only when the bubbles must be rotated. The 7230 current pulse generator (CPG) provides all current pulses required for generating, swapping, and replicating bubbles. Timing signals, produced by the 7220 bubble memory controller (BMC), enable current pulse drivers at the proper times and for the correct duration. The DATAOUT pins on the 7242 data formatter and sense

amplifier (FSA) enable the bubble generator current pulses when a bubble must be generated for binary 1 and disable the pulse when the bubble position must be left empty for binary 0. Current amplitudes are metal mask programmable for each current pulse output.

Each half of the FSA device, called an FSA channel, contains a 272-bit, first in, first out data memory (FIFO); a 160-bit bootloop register implemented as a 160×1 -bit RAM; a 14-bit error correction shift register (ECR); a sense amplifier; and control logic (Fig 3). Although the FSA FIFO

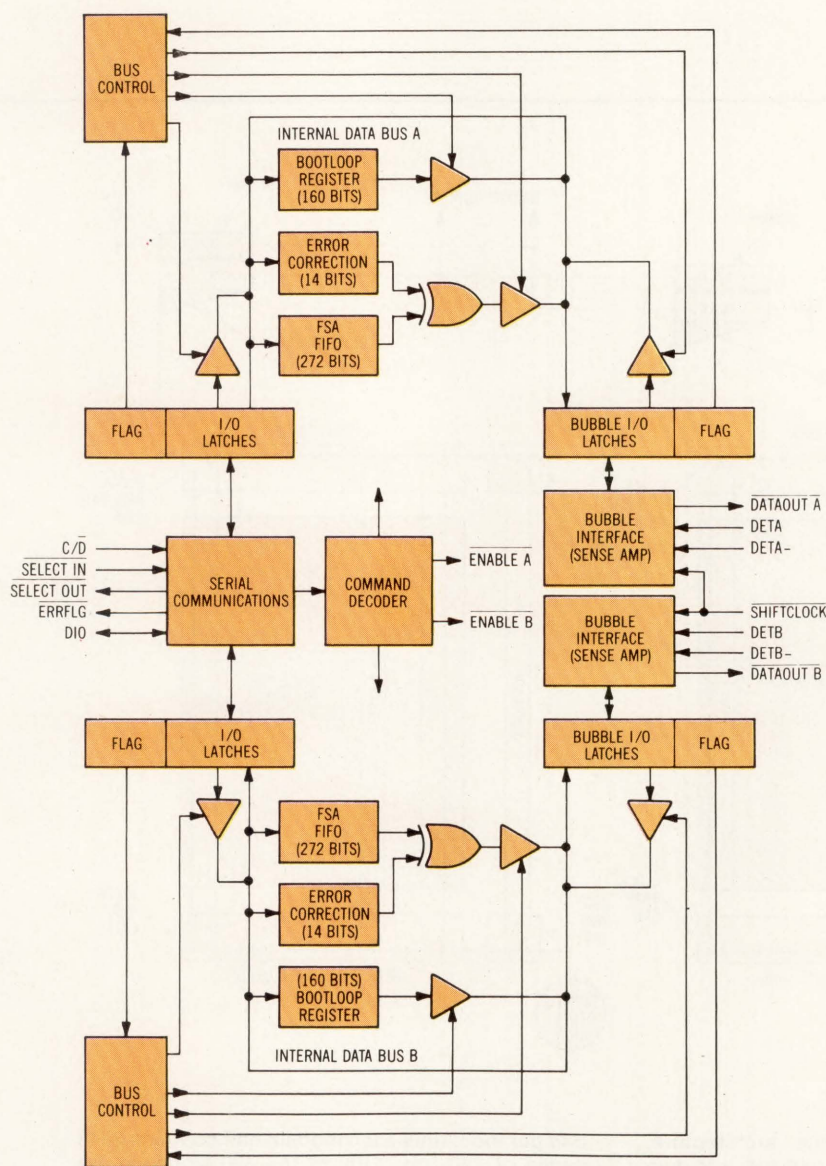


Fig 3 FSA block diagram. Providing communication between BMC and other bubble memory system components, FSA has symmetrical layout that drives each module half separately. Bootloop register identifies good loops. ECR register provides 5-bit burst error correction. Internal FIFO buffers 256-bit page of data along with 14-bit error correction code (or 16-bit utility field)

has 272 physical locations, the error correcting mode uses only 270 bits. Therefore, the FSA FIFO has two free locations when holding a complete half page of data—from one of the bubble module channels—consisting of a 256-bit data field followed by its 14-bit error correction code. These free bits accommodate the 16-bit utility field available when error correction is disabled.

During initialization, redundantly coded information contained in the module bootstrap loop is used to load the bootloop register with a masked good loop map for its companion channel. A module channel must have at least 135 good loops, of which the first 135 will be used and coded as a binary 1 in the corresponding bootloop register position. In the error correction mode, the bootloop register must contain 135 binary 1s and 25 binary 0s. Thus, the BMC loads 1s into the first 135 bootloop register positions that correspond to good bubble data loops and, regardless of whether more good loops exist, masks subsequent bootloop register positions to 0.

The ECR determines the 14-bit fire code that will be appended to the 256-bit data stream during write operations and is used to detect and correct error bursts up to five bits long anywhere in the data stream (or in the error correcting code itself) during read operations. Error correction remains transparent to the host computer unless an error occurs. Barring a system failure, which causes a timing error, errors are possible only during a read operation. When an error exists, the FSA pulls the $\overline{\text{ERRFLC}}$ pin low to notify the controller, which identifies the type of error by reading the FSA status word.

Basic FSA Operation During Read

During a read operation, the FSA becomes involved only after three events have occurred. First, a read seek rotates bubbles until the proper page address is positioned at the replicator elements, resulting in a read match. Storage loop bubbles are then replicated into the output tracks. Since two bubbles have been taken from each loop, two replicate pulses are required; the second pulse occurs two shift cycles (field rotations) after the first. Finally, the bubbles propagate down the output tracks to the detectors and, after all of these events have taken place, the BMC sends 320 bubble interface control pulses ($\overline{\text{SHIFTCLK}}$), which cause the FSA to detect the bubbles. Resulting data bits are loaded into the FSA FIFO and simultaneously shifted into the ECR. However, data are loaded and shifted only if the bootloop register shows, by having a binary 1 on its output port, that the originating loop was a good loop.

Whether or not the most recently sensed data bit was valid, the bootloop register pointer is adjusted to address the next location in preparation for the next data bit. The bootloop pointer does not increase in a simple binary fashion because, if it did, a 320-bit bootloop register would be required. Since two bits per page are read from each storage loop, each bit in the bootloop register can be used twice by incrementing the pointer as follows: 0, 1, 0, 1, 2, 3, 2, 3, 4, After 320 $\overline{\text{SHIFTCLK}}$ pulses, 320 bits of data have been sensed, only 270 of which were passed as valid. The FSA FIFO is now full, since it is logically a 270-bit FIFO in the error correction mode, and all 256 data bits plus the error

correction code bits have been shifted through the ECR. At this point, if the ECR contains all 0s, the FSA FIFO data are correct; otherwise, $\overline{\text{ERRFLC}}$ is pulled low to signal the controller that an error has occurred.

Either of two techniques will determine whether an error in FSA FIFO data might be corrected. Using one approach, a Read Corrected Data (RCD) command is sent to the FSA. This reads back the data while the FSA attempts to correct it. After transfer, the FSA informs the controller whether or not the error was corrected successfully. Another approach is to send an Internally Correct Data (ICD) command, requesting the FSA to attempt internal correction. No data is transferred. Upon completion of the ICD sequence, the FSA informs the controller whether the data was corrected successfully, preventing invalid data from reaching the controller. If no error occurred, the controller, after filling the FSA FIFO, simply reads the data on the bidirectional 1-bit data bus, DIO.

Basic FSA Operation During Write

In the write mode of operation, the controller loads the FSA FIFO with 256 bits of data by means of the serial DIO bus. The ECR then contains the error correction code for this 256-bit data stream, and the FSA channel is ready to write a half page of data to its corresponding bubble channel in three basic operations. First, the controller rotates the bubbles until a write match indicates that they have reached the correct position to begin the write sequence. Second, the controller sends 320 $\overline{\text{SHIFTCLK}}$ pulses to the FSA channel; the 256 bits of data are eventually swapped into the first 128 good loops; and the error correction code is loaded into the last seven active loops. The bootloop register contains information required to interleave two logical 0s (absence of a bubble) for each bad loop. If a bubble must be generated (logical 0 on the 7242 $\overline{\text{DATAOUT}}$ pin), a generate pulse is associated with each $\overline{\text{SHIFTCLK}}$ pulse. Finally, when the bubble generator has completely built the bubble pattern in the input track, pulsing the swap gates loads two bits into each storage loop. Bubbles are never swapped into bad loops, thus preventing bubbles from leaving the bad loops and contaminating active storage loop data.

BMC Functions

The BMC is capable of interfacing up to eight bubble modules to obtain a 1M-byte system; however, any number of bubble modules may be used in a system by adding an FSA for each module. The BMC (Fig 4) provides a standard 8-bit Multibus[®] compatible interface for the 8080, 8085, 8086, or 8088, along with multiple bubble module operation in conjunction with the FSA, and generates all timing signals required throughout the integrated bubble memory system, affording three modes of data transfer through the Multibus interface: direct memory transfer handshake (DMA), half full interrupt, and polled data transfer. The BMC also implements parallel module operation and provides complete error handling and reporting via a status word and interrupt logic. Parallel operation allows a variable system page size of 512, 1024, 2048, or 4096 bits.

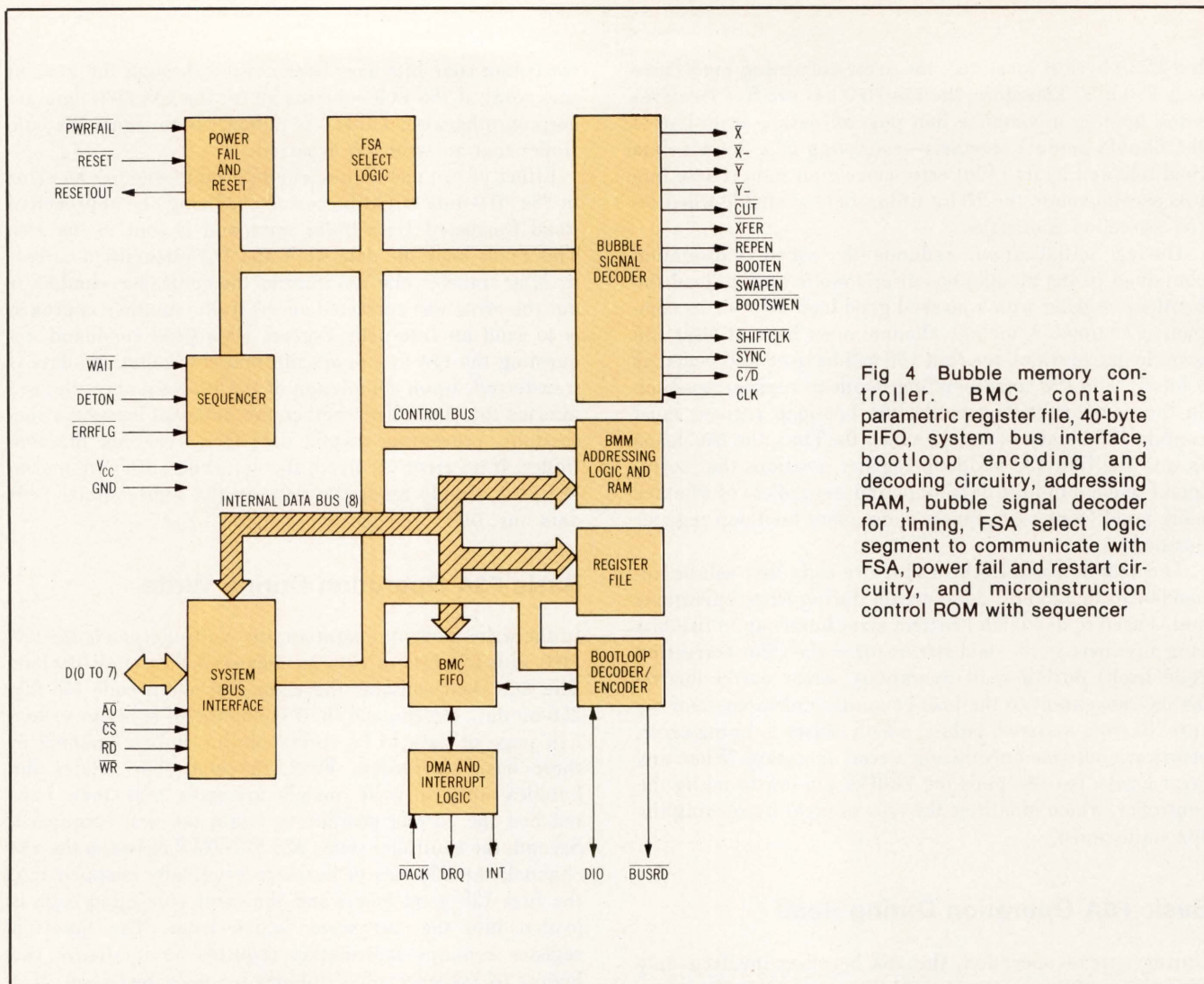


Fig 4 Bubble memory controller. BMC contains parametric register file, 40-byte FIFO, system bus interface, bootloop encoding and decoding circuitry, addressing RAM, bubble signal decoder for timing, FSA select logic segment to communicate with FSA, power fail and restart circuitry, and microinstruction control ROM with sequencer

BMC Parametric Registers

BMC parametric registers inform the controller of various system options and data transfer specifications. A command register, loaded with the 4-bit command code only after all other registers have been initialized, starts a command using specified parameters. A block length register designates the number of pages to be accessed and the number of FSA channels to be used in the transfer. The starting address register supplies the starting page address for the transfer and specifies which bubble modules are to be accessed in parallel. For example, if a total of eight modules are used and the block length register indicates that only four FSA channels should be accessed in parallel during data transfers, there will be four separate module groups, each consisting of two modules. At that point the starting address specifies both the module group and the page address, within that group, at which the transfer will begin. The enable register enables or disables the interrupts, direct memory access, bootloop writing, and two error correction modes. The register address counter (RAC), a 4-bit autoincrement register, can be loaded to address any

of these parametric registers, or the FIFO, during a subsequent load operation.

BMC Data Handling

Although it contains a 40-byte, double buffered BMC FIFO to store bubble related read/write data (including FSA bootloop register data), the BMC appears to the host processor as only three 8-bit data registers (Fig 5). The host writes all data into the BMC input latch (IPL). The ultimate data destination depends on the content of the RAC and on the state of BMC input pin A0, the only BMC address pin. When the host reads data from the BMC, it receives the Status Latch (STL) information if A0 is high or output latch (OPL) information if A0 is low. The OPL can contain either FIFO data or parametric register data, depending only on the RAC. Although this arrangement may seem confusing at first, it is quite simple to load the BMC registers, put data in the FIFO if desired, and send a BMC command.

Each time a register read or write occurs, the RAC is incremented and the OPL is updated with the content of the

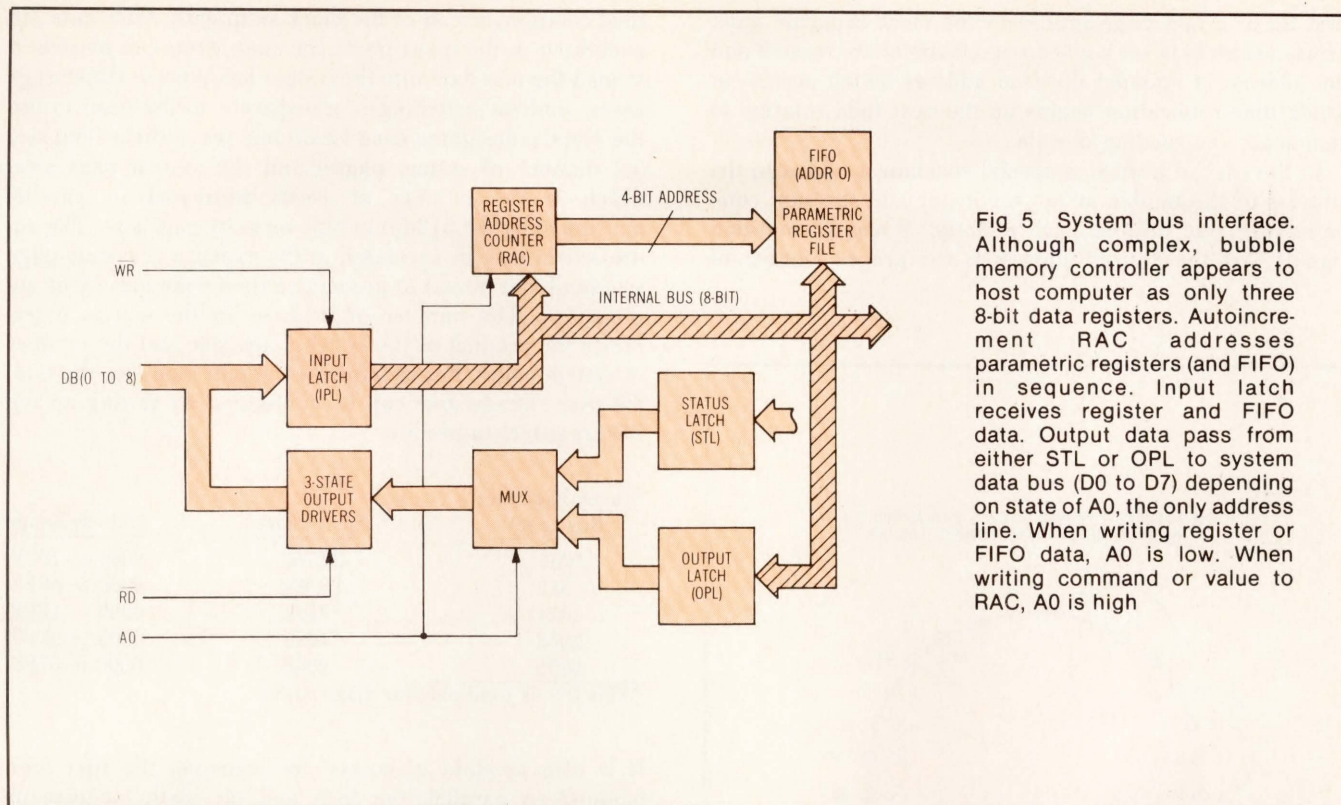


Fig 5 System bus interface. Although complex, bubble memory controller appears to host computer as only three 8-bit data registers. Autoincrement RAC addresses parametric registers (and FIFO) in sequence. Input latch receives register and FIFO data. Output data pass from either STL or OPL to system data bus (D0 to D7) depending on state of A0, the only address line. When writing register or FIFO data, A0 is low. When writing command or value to RAC, A0 is high

addressed register. For example, to write all of the BMC registers and place 20 bytes of data into the FIFO, the RAC must first receive 1011—to address the block length register—and A0 must be high. Then, five bytes of register data can be written to the IPL, followed by 20 bytes of FIFO data. Once the RAC has incremented to 0, after the last register write, it remains at 0 until it is reinitialized with a write RAC command. If the host used the sequence just described to prepare to write bubble data, it would simply send the write command and ensure that the FIFO is kept supplied with enough data to complete the transfer. Here again, A0 must be high when writing a command to the BMC. Bit 4 of the data bus distinguishes a command write from an RAC write.

System Initialization

The BMC must perform an initialization sequence before data are transferred to the bubble module. First, RESETOUT is used to purge system components. Next, the number of FSA channels tied to the SYNC, SELECTIN, and SELECTOUT daisy chain is determined by the BMC and stored in a counter. Then, for each FSA and bubble module combination, three major operations are required. The bootloop on each bubble module is read into the BMC, decoded into a good loop map (40 bytes) for that module, loaded into the BMC FIFO, and masked into the active loop map (40 bytes) and written into the corresponding FSA bootloop registers (for two channels operating in parallel). The bootloop contains good loop information for both chip halves; these data are interleaved within the loop and separated when written into the FSA bootloop registers. To generate the active loop map, the BMC counts the number of binary 1s loaded into

each bootloop register and masks subsequent 1s once the proper number has been reached. To protect against accidental bubble module writes with erroneous bootloop register information, the BMC must execute the initialization command or abort command before any other command can be executed.

Addressing Strategy

Upon conclusion of an initialization sequence, the bubble modules are positioned at page address 0 and the BMM addressing memory is cleared. From this point, whenever the bubbles shift within the minor loops, the BMC address increments to reflect the address assigned to the bubble positioned at the block replicate gate. Because two bits are written to or read from each storage loop during each page read/write operation, both storage loop data positions will have the same logical address. However, their physical addresses will differ by two because instead of numbering the pages in sequence, they are numbered in a fashion that yields a minimum of field rotations between successive page addresses. This optimizes the transfer rate when reading or writing several consecutive pages.

Fig 6 shows one of the minor loops in a bubble module. Physical page addresses are labeled on the interior of the loop, while logical addresses appear on the exterior. For any desired number of field rotations between successive pages, a constant (N equals 589 hexadecimal) can be determined allowing the sum of N to be added to the present address (modulo the number of addresses) yielding the next valid logical address in the loop. This constant will not be added on each field rotation; instead, it is added only when the

first bit of a new page rotates to the block replicate gate. Thus, if searching for a given page, bubbles are rotated and the address is updated until an address match occurs, at which time replication begins on the next field rotation to commence the reading of data.

In the case of a write, a special constant is added to the address of the bubble at the replicator and the sum compared with the desired page address. A match condition signals that the desired address is the proper number of

field rotations ahead of the block swap gate. After data are generated in the input track, the swap gates can be pulsed to load the new data into the proper locations in the storage loops. Address matching is transparent to the host; to use the system, designers need know only the address field size (ie, number of system pages) and the system page size, which is the number of BMMs addressed in parallel multiplied by the 512-bit bubble memory page size. The address field may be increased at the expense of system page size (and vice versa) to accommodate a wide variety of applications. The number of modules in the system determines the product of the system page size and the number of system pages. For example, with eight modules, the total 1M-byte storage area can be configured by setting up the BMC registers to produce

System Page Size (Bits/page)	No of Pages	Address Range
*256	32,768	0000 to 7FFF
512	16,384	0000 to 3FFF
1024	8192	0000 to 1FFF
2048	4096	0000 to 0FFF
4096	2048	0000 to 07FF

*This line is used only for diagnostics.

It is also possible to access, for example, the first four modules in parallel, the fifth and the sixth modules in parallel, and the seventh and eighth modules separately in a variable system page size scheme offering pages of three different sizes in a single system.

Separation of FSA data handling functions from the BMC makes the configuration flexibility possible. To achieve the full range of operating modes, only the number of bubble modules operated in parallel need change. The first line of the above table corresponds to a system whose modules are not used in parallel, one in which a system page consists of a single bubble module page as only one module is accessed at a time. When a page boundary is crossed, during data transfer, the next module in the chain will be accessed. In the last line of the table, all eight modules are used in parallel. There are eight module pages in each system page, and all eight modules are accessed as a single group.

Data transfer rate improves by a factor of two with each increase in the number of modules operated in parallel. As shown in the table, up to 15 bits of address information may be required, of which the four most significant bits actually select among groups of parallel modules. Since one BMC operation can transfer up to 2048 pages, an 11-bit block length specification is required. Four bits determine the number of modules involved in a read/write operation. The starting address register and the block length register supply this information.

Starting Address Register															
Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FSA Group Select					11 LSBs of Starting Address										
Block Length Counter															
Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
No of FSA Channels Operated in Parallel					Block Length for Next Transfer										

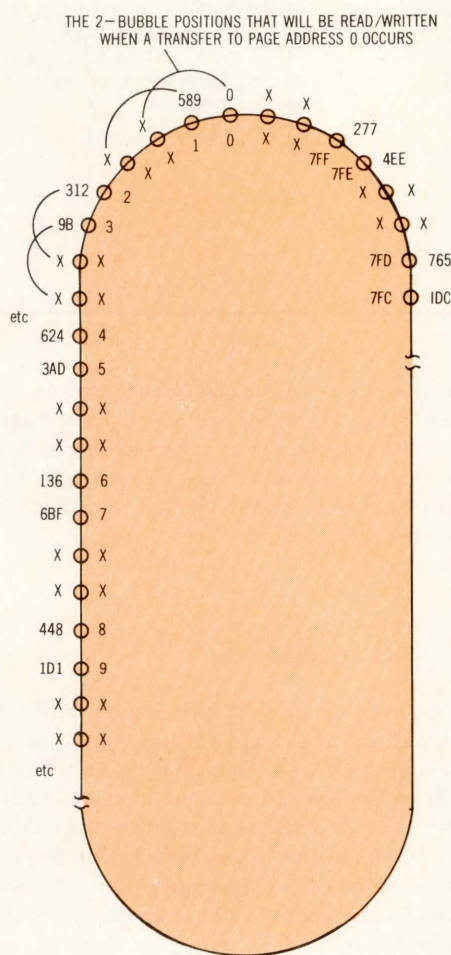


Fig 6 Storage loop address strategy. Read/write operations access pairs of bubbles (four such pairs are marked). Physical page addresses, shown inside loop, reflect inefficient page numbering scheme. Use of logical page addresses, shown outside loop, yields minimum number of field rotations between successive page bits, achieving fastest multiple page transfer rate

Using the System

Once the bubble memory system has been powered up, writing 1011 to the RAC selects the block length register, as previously described, preparing BMC to accept parametric data. The host now loads the parametric registers, sends a BMC initialization command, waits for completion, and checks to ensure that the command was successful. The enable register content determines the mode in which the BMC will respond.

The STL contains the actual status information, the STL BUSY flag asserting while the BMC processes a command. Its TIMING ERROR flag signals any initialization problems. Once the operation has been completed, either an OPERATION COMPLETE flag or an OPERATION FAIL flag will be set. If the INTERRUPT NORMAL enable bit is set in the enable register, operation completion will activate the INT pin; if the INTERRUPT ERROR enable bit is set, a timing error will activate INT. Therefore, status information can be obtained either by polling the STL or through use of interrupt service routines. Next, the parametric registers are loaded again to describe the desired write operation, and a write command sent to the BMC by loading the address of the first BMC register to be modified into the RAC and writing data into the IPL as before. The FIFO must be addressed before a command that accesses FIFO data is sent. Autoincrement logic may automatically address the FIFO, at address 0; however, the FIFO can be addressed explicitly by clearing the RAC.

Even after a write command is issued, the BMC will not begin a write transfer until at least two data bytes have been loaded into the FIFO. Once data transfer begins, the host must keep pace with the data transfer rate. Thus, if a direct memory access channel is used to supply data, its data transfer rate, accounting for priority, must exceed that of the bubble memory system. The bubble memory data rate (BDR) depends primarily on the bubble clock frequency, the level of parallel operation, and the average number of valid data bits written to a single channel in each clock period, while the bubble clock rate is one-fourth of the external clock rate. Therefore, at 4 MHz, given that there are 20 clock pulses per field rotation, the rotating field rate is $4 \text{ MHz} / (20 * 4) = 50 \text{ kHz}$. In a 1M-byte system with four channels used in parallel, then a data rate of 136k bits/s would be required. In general,

$$\text{BDR} = 0.034 * N * f_B$$

where N = No of parallel BMM channels
 f_B = bubble clock rate

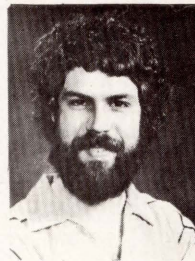
When the DMA enable bit is reset, the DMA pin doubles as a FIFO half-full interrupt pin. During a write operation, it will be asserted when there is room enough in the FIFO for 22 bytes of data. The host should transfer this data in a burst, at many times the minimum required data rate, to avoid spending most of its time servicing this particular interrupt, which would then require a higher priority than is necessary. In the lowest performance systems, the host can simply poll a FIFO READY bit in the STL which, during write operations, remains active while the IPL is empty and ready to accept a byte of data. Insufficient or excessive FIFO data causes a timing error and generates an interrupt.

To read bubble data, parametric registers are loaded as in the case of a write operation, and a read command sent to

the BMC. Various transfer modes are available, as with a write data operation, and the host must keep up with the BMC to avoid FIFO overflow resulting in a timing error. Read operations admit to a larger variety of error conditions than do write operations. If any FSA channel detects a data error (ECR not 0 at the end of a page transfer), it will pull down the open drain ERR.FLG line and then, depending on the content of the enable register, the BMC will direct subsequent FSA operation. In any event, upon completion the STL is updated with FSA status and uncorrectable errors generate a host interrupt.

Summary

A family of large scale integration chips support the use of high density bubble memory modules by providing all of the data handling and interfacing functions required to use bubble memory effectively. Although they are normally not of concern to designers, specific details of system timing and operational sequencing illustrate their capabilities. In addition, owing to the great number of diagnostic commands, error correction and various redundancy schemes, and a complete means for enabling interrupts on different error conditions, the system can be used at a very low error rate without host intervention or data logging problems.



Sam Joseph Nicolino, Jr. is a senior components engineer at the System Development Group of Intel Magnetics, Inc, where he has been primarily involved in designing the 7220 bubble memory controller chip and the error correction portion of the 7242 formatter/sense amp chip. He holds an MS degree in electrical engineering from Iowa State University.

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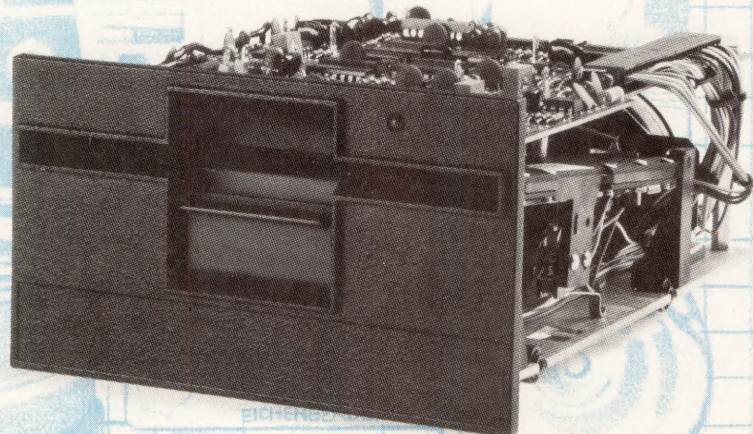
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Micropolis 1016/1015	1,100K	60,000	steel lead screw	96/100	365

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Making PL/M Programs More Understandable

PL/M compiler directives enhance the self-documenting characteristics of PL/M and implement simple extensions of this powerful high level microcomputer language

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High level language programs are the easiest to design, debug, and maintain. Used creatively, the self-documenting features of PL/M can be further expanded to augment program understandability and maintainability.

Self-documenting programs can be generally understood by a reading of their source code alone, without reference to additional comments. Yet even though conscientious programmers document their programs with clear, explanatory comments, no program can be entirely self-documenting in practice. The problem surfaces as a program goes through its inevitable evolutionary changes—programmers invariably neglect to update program comments consistently.

In self-documenting programs, a certain amount of commentary is automatically revised with the code. Consider the following PL/M statements

```
CALL OPEN (.INFILE,.FILENAME,1,0,  
          .STATUS);  
CALL READ (INFILE,.BUFFER,80,  
          .ACTUAL,.STATUS);
```

Without knowing anything about pro-

cedures OPEN and READ, it is reasonable to assume that OPEN establishes some sort of logical input/output (I/O) channel and that READ transfers data through the channel to memory. Yet, from the statements themselves, the relationships between the various parameters are not entirely clear. Consider, instead, the statements

```
OPEN$CHANNEL (.INFILE  
              USING .FILENAME FOR  
              READ$ACCESS  
              NO$ECHO RETURNING .STATUS);  
READ$FROM (INFILE INTO .BUFFER  
           UP$TO 80 CHARS$RETURNING  
           .ACTUAL, .STATUS)
```

These two statements are equivalent to the previous statements; however, they are much more explicit about the way in which they perform the same task. The READ statement, for example, shows quite clearly that the program will read a record of up to 80 characters from a channel identified by INFILE into memory at location BUFFER and return the ACTUAL number of

characters that were transferred, along with STATUS of the operation.

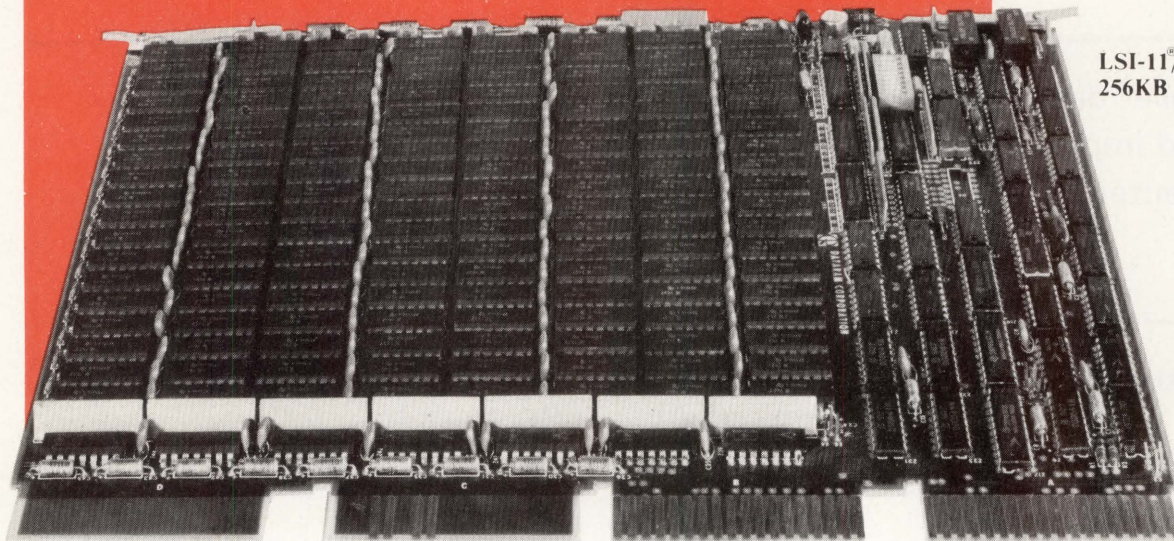
Simple text substitution transforms the first pair of statements into the second pair, replacing mode constants with text that describes the specified mode and substituting meaningful text for the delimiting commas. The LITERALLY declaration, which permits a symbol to represent a string of text, achieves text substitution under PL/M in much the same way that assemblers implement macros. Whenever the PL/M compiler encounters a symbol defined in a LITERALLY declaration, it replaces the symbol with the associated text string.

In the simple example of Fig 1, statement number 2 declares FLAG to be a logical variable, one that can take on only the values TRUE and FALSE. However, the compiler substitutes the string BYTE for the string LOGICAL and defines FLAG as a BYTE variable. In statement number 3, the numerical constant FF (hexadecimal) replaces the symbol TRUE so that, in effect, executing statement number 3 sets FLAG

(continued on page 171)

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CIRCLE 86 ON INQUIRY CARD

to contain all ones. Only the compiler encounters the substituted text; the listing retains the original literal symbol.

Of course, declaring FLAG to be a logical variable does not make it one in the true sense of the term because PL/M does not recognize logical variables as such. As far as PL/M is concerned, FLAG can assume any value between 0 and 255. The LOGICAL declaration programmed in place of the BYTE declaration aids program documentation and understanding by highlighting the use of FLAG as a synthetic logical variable without any need for additional explanation. In this manner, LITERALLY declarations contribute to a self-documenting program.

Two other features of PL/M, the \$INCLUDE directive and the \$LIST and \$NOLIST directives, can also simplify programming and enhance program readability. The \$INCLUDE (file name) directive implements another form of text substitution. It designates a file whose entire content is inserted into the source file at the point where the \$INCLUDE directive was encountered and also printed on the source listing. It is particularly valuable when supplying predefined declarations for external procedures. Instead of writing out the declarations for library procedures in every program, a file consisting only of procedure declarations can be prepared, and the \$INCLUDE directive can insert this file into every source program that uses library procedures. Placing declarations for each library procedure in a separate file is usually more convenient than using one file for all of the declarations; then, a program can \$INCLUDE only those declarations that are required. Commonly used literal declarations can be handled in the same manner (Fig 2).

The type of \$INCLUDE file described here contains procedure declarations or literal constants whose meanings are known to the programmers using them. Thus, it is neither necessary nor even desirable for these declarations to appear in the source listing because they would constitute unnecessary and distracting detail. The \$NOLIST directive is a PL/M feature that contributes to program readability by suppressing unnecessary detail. Input source text between a \$NOLIST directive and a subsequent \$LIST directive is not

```

1  DECLARE TRUE LITERALLY 'OFFH',
    FALSE LITERALLY '0',
    LOGICAL LITERALLY 'BYTE';
2  DECLARE FLAG LOGICAL;
    .
    .
    .
3  FLAG = TRUE;
    .
    .
    .
4  IF FLAG THEN DO;
```

Fig 1 Defining logical variables. Statement 2 declares FLAG to be logical variable, type not supported under PL/M. Compiler substitutes BYTE for LOGICAL, 0 for FALSE, and OFFH for TRUE to effect simple extension of language

```

$  NOLIST
DECLARE TRUE LITERALLY 'OFFH';
DECLARE FALSE LITERALLY '0';
DECLARE LOGICAL LITERALLY 'BYTE';
DECLARE WORD LITERALLY 'ADDRESS';
/*
                                SPECIAL ASCII CHARACTERS
*/
DECLARE
    NULL                LITERALLY '0',
    BELL                LITERALLY '7',
    TAB                 LITERALLY '9',
    LF                  LITERALLY '0AH',
    VT                  LITERALLY '0BH',
    FF                  LITERALLY '0CH',
    CR                  LITERALLY '0DH',
    ESC                 LITERALLY '1BH',
    QUOTE               LITERALLY '22H',
    LCA                  LITERALLY '61H',
    LCZ                  LITERALLY '7AH',
    RUBOUT              LITERALLY '7FH';
$  LIST
```

Fig 2 Suppressing unnecessary detail. Auxiliary file of literal declarations, to be inserted into source program through use of \$INCLUDE declaration, contains distracting information with limited value as documentation. \$NOLIST and \$LIST directives suppress statements on source listing. \$INCLUDE statement appears on listing to document name of included file

IMAGINE

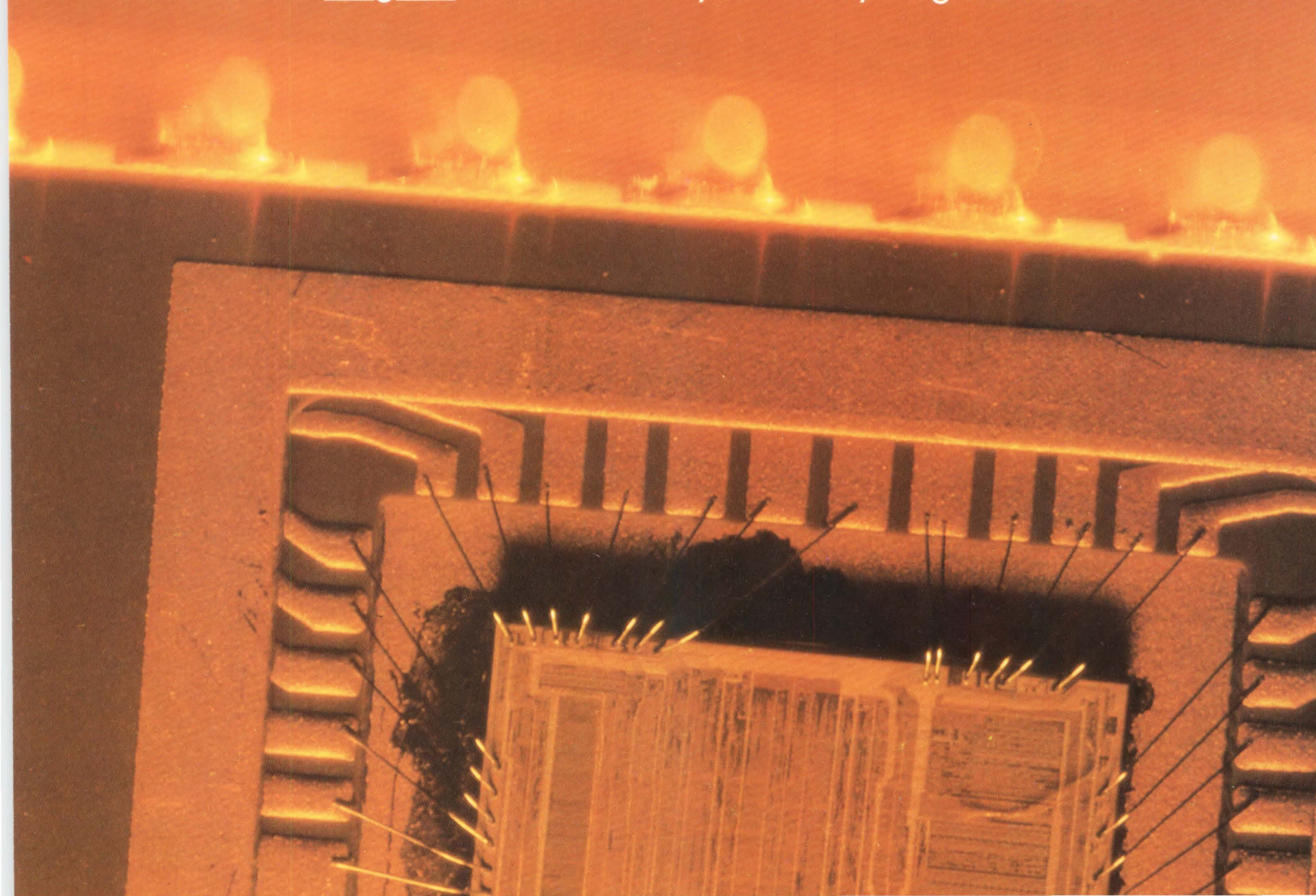
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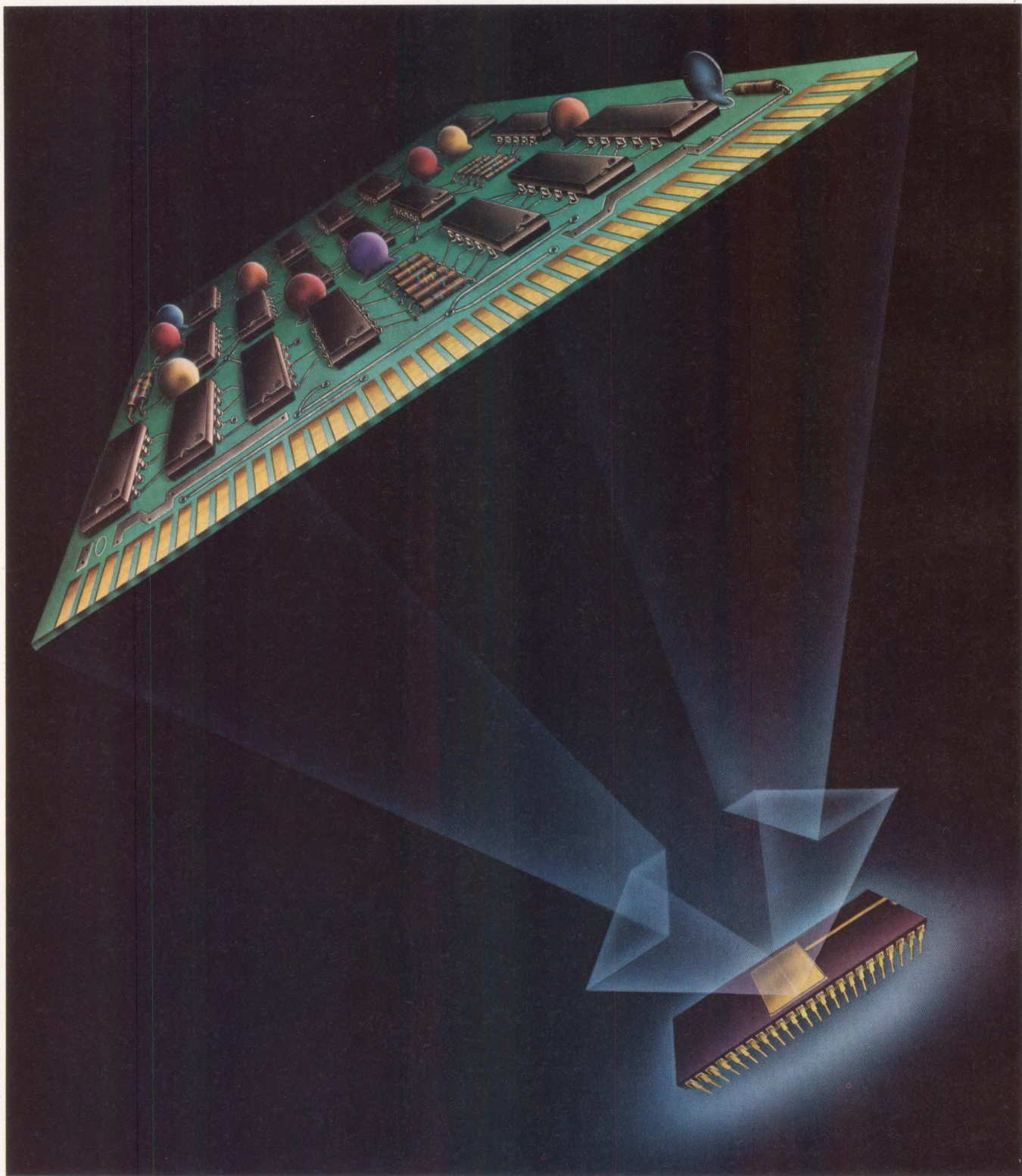


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interfacing problems.

File: OPEN.EXT

```
OPEN: PROCEDURE (CHANNEL$PTR,FILE$PTR,ACCESS$MODE,LINE$EDIT,STATUS) EXTERNAL;  
  DECLARE (CHANNEL$PTR,FILE$PTR,ACCESS$MODE,LINE$EDIT,STATUS) WORD;  
END OPEN;  
DECLARE OPEN$CHANNEL LITERALLY 'CALL OPEN',  
  USING LITERALLY ',',  
  FOR LITERALLY ',',  
  READ$ACCESS LITERALLY '1',  
  WRITE$ACCESS LITERALLY '2',  
  UPDATE$ACCESS LITERALLY '3',  
  ECHO$TO LITERALLY ',',  
  NO$ECHO LITERALLY '0',  
  RETURNING LITERALLY ';;';
```

File: READ.EXT

```
READ: PROCEDURE (CHANNEL,BUFFER$PTR,COUNT,ACTUAL,STATUS) EXTERNAL;  
  DECLARE (CHANNEL,BUFFER$PTR,COUNT,ACTUAL,STATUS) WORD;  
END READ;  
DECLARE READ$FROM LITERALLY 'CALL READ',  
  INTO LITERALLY ',',  
  UP$TO LITERALLY ',',  
  CHARS$RETURNING LITERALLY ';;';
```

Fig 3 Enhancing external procedure declarations. If OPEN and READ procedures are contained in library of I/O routines, special files that supply necessary external procedure declarations can be inserted into routines that use OPEN and READ by means of \$INCLUDE directives. Included files can also contain literal declarations to augment self-documenting nature of PL/M

included in the source listing. \$INCLUDE files containing commonly used declarations should begin with a \$NOLIST directive and end with a \$LIST directive to suppress listing of the file; however, the \$INCLUDE statements themselves will be listed to record the names of included files.

Assume, for example, that the OPEN and READ procedures described earlier are contained in a library of I/O procedures. Special \$INCLUDE files, such as those shown in Fig 3, might contain not only the external procedure declarations, but also the literal declarations of all those symbols that contribute to program readability. Then, programmers can use either the conventional CALL statement, the more conversational form previously described, or any intermediate combination.

Literal declarations can implement simple semantic extensions of PL/M. For example, PL/M declares 16-bit variables to be of type ADDRESS, a somewhat misleading and potentially confusing term. By declaring the symbol WORD to be, literally, ADDRESS, 16-bit variables can be declared to be of type WORD, which is easier to understand. It might be equally useful

to declare the symbol POINTER as, literally, ADDRESS for use with pointer variables that are, in fact, addresses of other variables.

Control structures can be similarly extended. By defining FOREVER to be, literally, WHILE 1, the DO FOREVER statement can designate the beginning of an infinite loop, a common structure in realtime applications. The ability to write DO UNTIL would, in many cases, be clearer than an equivalent form of DO WHILE. Of course, DO UNTIL is identical to DO WHILE NOT; thus, declaring UNTIL as, literally, WHILE NOT, creates the DO UNTIL structure.

The iterative DO construction,

DO I = 1 TO N;

can be replaced by

FOR I = 1 TO N;

Notice, however, that this use of FOR conflicts with its usage in the OPEN\$CHANNEL statement, described earlier, and a literal symbol, like a reserved word, can have only one definition in any program. It is up to the programmer to make the tradeoffs necessary to arrive at an optimally useful set of unique literal symbols for each application. As with much of pro-

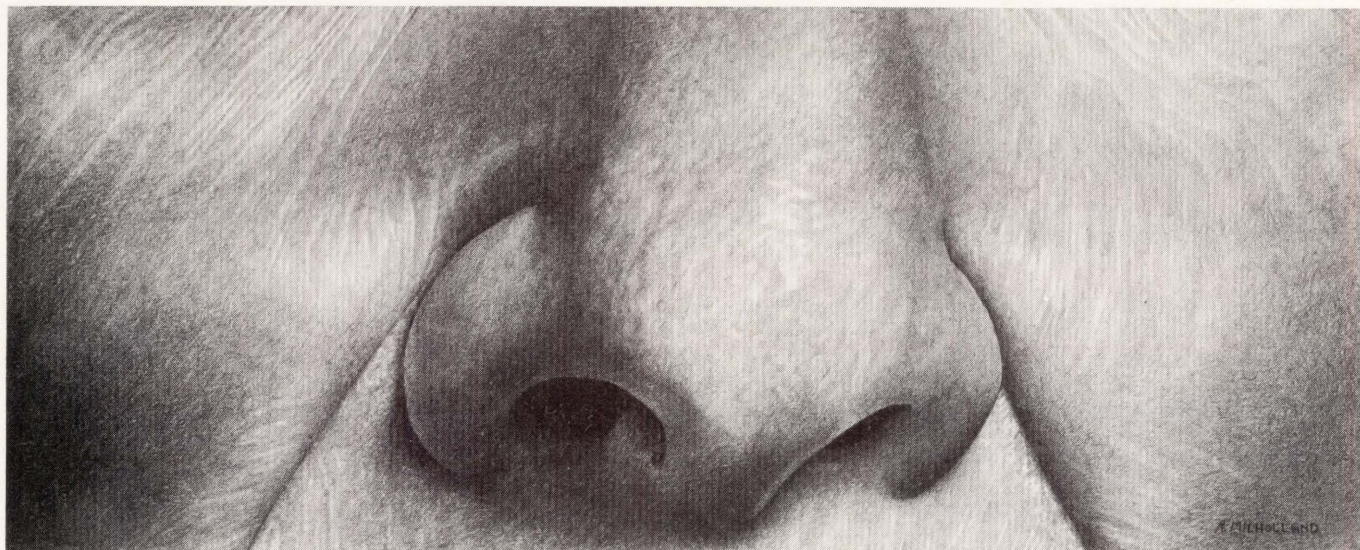
gramming, it may come down to a matter of personal taste.

There are other restrictions and limitations on the use of literal declarations. PL/M reserved words cannot be redefined; for example, in the READ statement, TO would be just as readable as INTO, but TO is a PL/M reserved word. Also, it is important to avoid giving the same symbol different literal definitions in different included files. Apart from these limitations, familiarity with and creative use of the \$INCLUDE, \$NOLIST, and \$LIST directives provides a valuable programming tool that enhances the self-documenting nature of PL/M programs by making them easier to understand and maintain.

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Mask and Menu File System Eases Operator Handling

File system uses masks, menus, and function keys to streamline operator interaction in an information retrieval design optimized for use with microprocessors

K. Buchmann

Siemens AG

Otto-Hahn-Ring 6, Munich 83, Federal Republic of Germany

Effectiveness of microcomputers is determined by the way in which they handle and process data. Because their capabilities differ considerably from those of larger computers, microcomputers require innovative concepts for data handling and file management and modification of terminology generally associated with computers. Data base is an example. The data base used by the microcomputer file system described here is incomparably different from those used by larger computers. This system, designed around the SME-800, includes four SAB 8080 microprocessors acting as the system, file, peripheral, and remote data communications processor that can communicate with as many as four double-density floppy disc drives, for a total storage capacity of 2M bytes. Of course, part of the 2M-byte capacity is used for programs, data organization, and buffer files.

As floppy disc access speed and the volume of data to be processed are factors limiting system throughput, it is not surprising to find neither the processors nor the programs responsible

for bottlenecks that develop in the processing of data. Rather, it is management of and access to the floppy discs that are the critical factors. Floppy disc data storage and organization are implemented through an interface to the ISIS-II operating system or, for the multiprocessor system, through a similarly defined interface. It is this interface that implements data handling macros such as OPEN, CLOSE, READ, and WRITE.

Hardware and Software

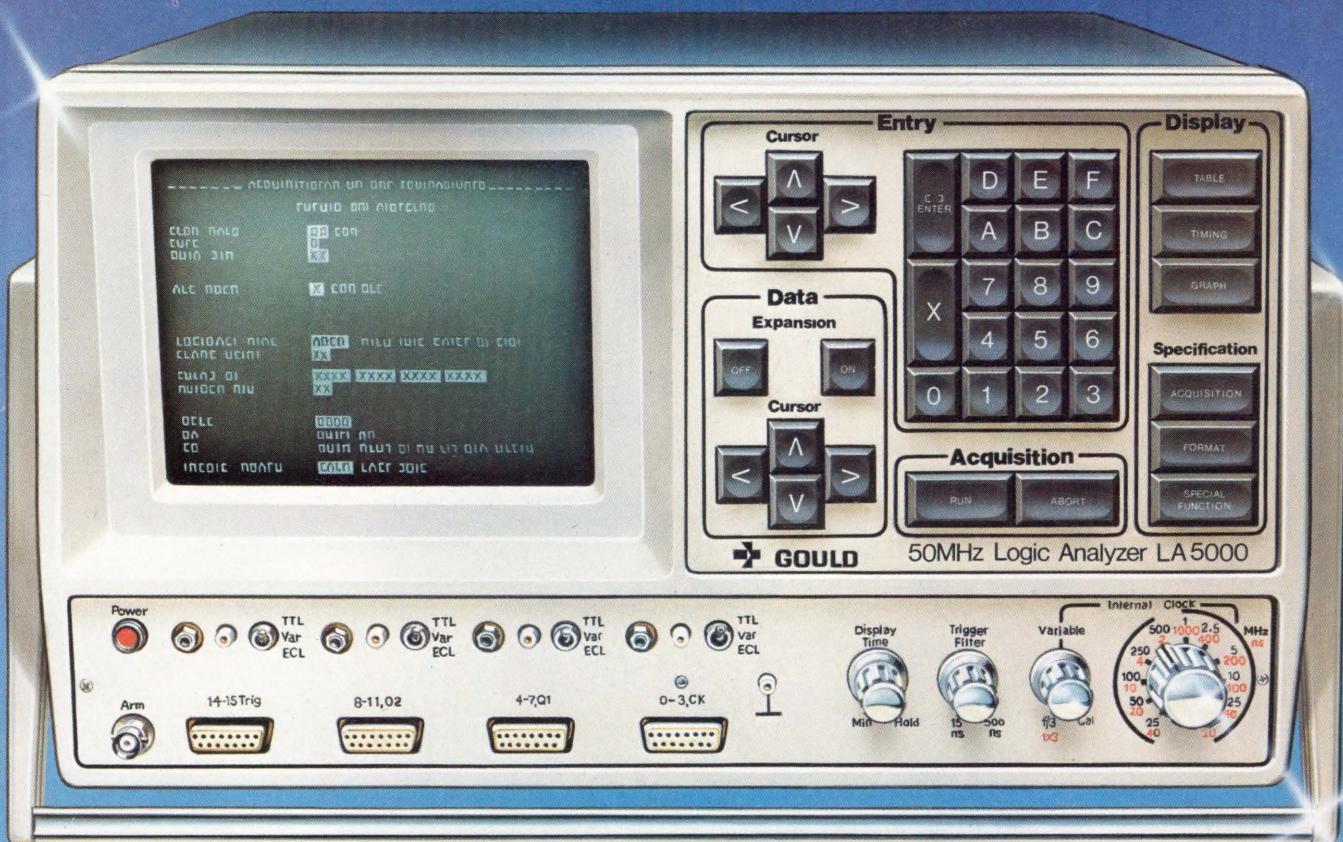
In this system the data base is accessible to a microcomputer system whose central processing unit (CPU) is a SAB 8080 with a memory capacity of 64k bytes. Required peripherals include a data display terminal with block mode capability and write protection, a floppy disc unit with at least two drives, and a printer. Since the file system was developed on the SME-800, it is accessible from this system as well. The full system implementation is configured as an office computer consisting of several microcomputers,

each of which is an autonomous subsystem including a CPU, memory, and input/output (I/O) capability. The microcomputers communicate by means of a direct memory access (DMA) channel. In addition, the system processor serves as the console processor and has a full memory capacity of 64k bytes. The file processor, to which the floppy disc drives are connected, includes the floppy disc driver and the DISC interface circuitry, while the peripheral processor connects the standard I/O devices such as printer, paper tape reader, and paper tape punch. The communication processor handles remote data transmission with large mainframes or other office computers.

One of the major advantages of the multiple microcomputer system is its ability to use any component module on its own. For example, a minimum version, for less sophisticated applications, would employ the system processor as a standalone computer, allowing configuration of a low cost version without sacrificing expansion capability. Individual microcomputer modules

(continued on page 182)

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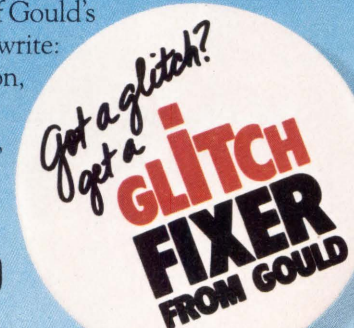
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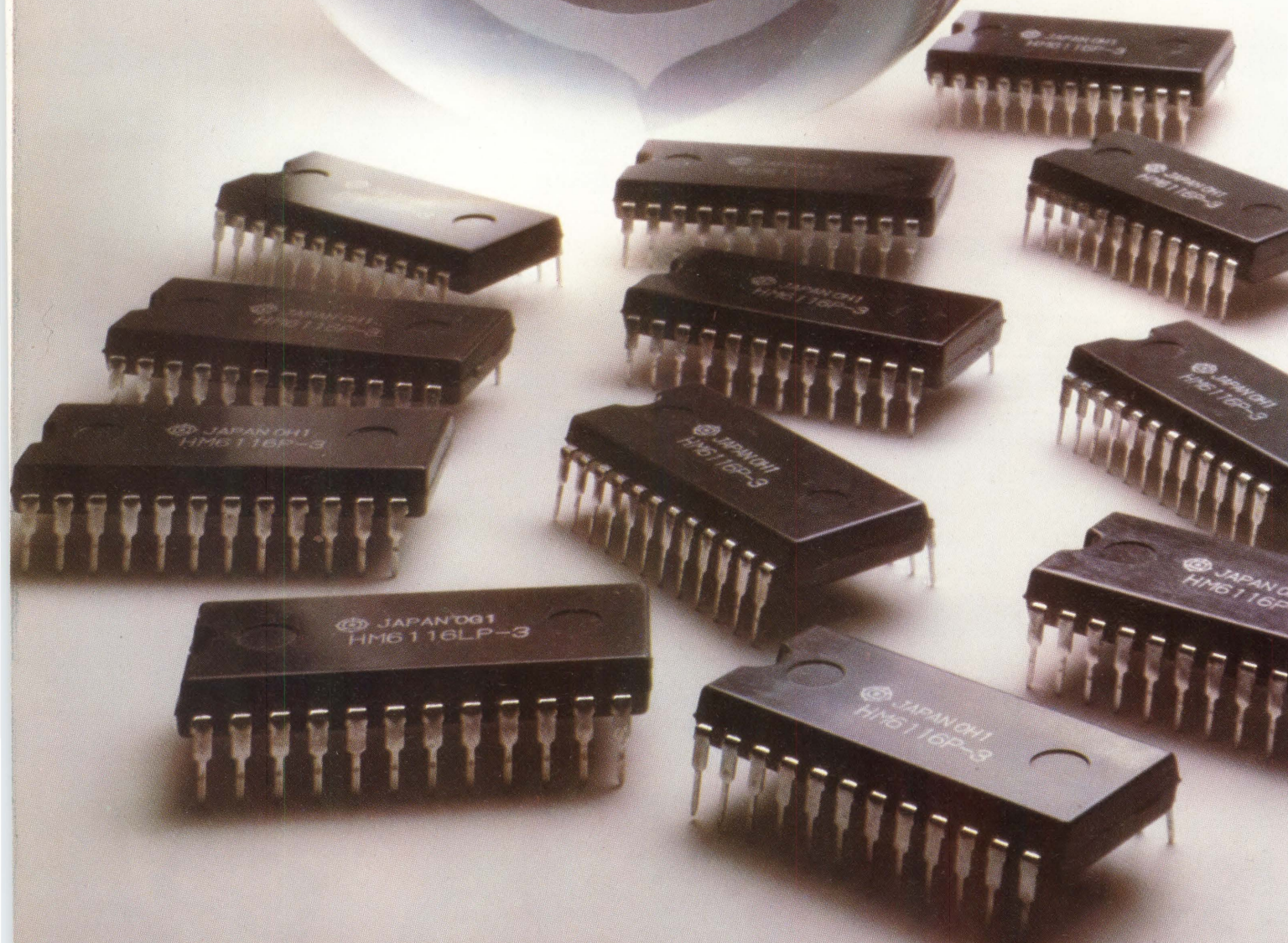
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using basically identical hardware differ mainly in the interfaces but, more importantly, in their software.

It is the operating system that provides the basis for the file system and interfaces the file system to the console and the printer. All microcomputers are equipped with send and receive programs for mutual data exchange. The central processor executes additional programs for console I/O, function key processing, system bus control, and distribution of functions among the other processors, leaving the file processor to handle the floppy disc interface using such calls as OPEN, READ, WRITE, and CLOSE. The peripheral processor executes the printer interface software, accepting as much data as its storage capacity permits, while routing data to the printer, allowing the system processor to continue with unrelated tasks. The communications processor executes software that implements the communication protocols.

File System

The file system was designed specifically for the distributed ar-

chitecture just described. Its key feature is that it permits several autonomous processors to perform parallel, independent file access concurrently. The file system occupies 32k bytes of system processor memory and uses the remaining system processor memory as a buffer area for floppy disc I/O. File system software is stored on floppy disc and loaded to the appropriate processor by the operating system in response to a console function key.

Access to the data base is achieved by executing a command or by using a function key. All file system requests conform to a structured dialog carried on by using the masks and menus. Because file system operation is based on masks, no data can be accepted or accessed without first defining the mask.

Mask Processing

Mask generation is accomplished through the definition section of the system. Each mask is assigned a name, and the mask, along with all data for the corresponding data structure, is titled with this name. The various

mask fields are defined by aspect names, listed in an aspect catalog, and the data entered in these different fields are known as aspect values.

While a mask is being created, write protection is disabled. Once a mask has been transferred to the file, the computer sends back an echo of the mask as it is to be used, including all protected fields. The mask generator then works with data shown as the table "Mask Generator Automation." The top line indicates various states the mask generation process can pass through, while the first column lists the possible characters each state accepts as input. The matrix fields then specify the state into which the process passes after receiving the corresponding character.

In the start state, the system waits for a heading. The heading is terminated with a carriage return. If a carriage return is the first input character, there is no heading and the first aspect name follows immediately. As shown, any characters may be used within the heading. The start of name state is entered with the first aspect name only. The system waits for a character that is permissible in names, and then passes into the "name" state; the colon character terminates this state. Explanations or comments may be inserted between the name and the colon terminator. After the colon, the area for the aspect value begins, marked by points whose number determines the aspect value length. Aspect name and value form within the mask an entity, which may be followed by comments enclosed between slashes.

A close relationship exists between a mask and its data. Deletion or modification of an existing mask must be done with care because, since the mask defines the data fields, changing or deleting the mask may change or delete the data. Deleting aspect names within a mask will delete the corresponding aspect value, and modifying a value length while keeping the aspect name will involve reducing or expanding the data field, which may cause truncation of data. (See Fig 1).

Data Manipulation

Once a mask has been defined, data can be manipulated by overwriting them with new data or by modifying the original data. In modifying the

(continued on page 186)

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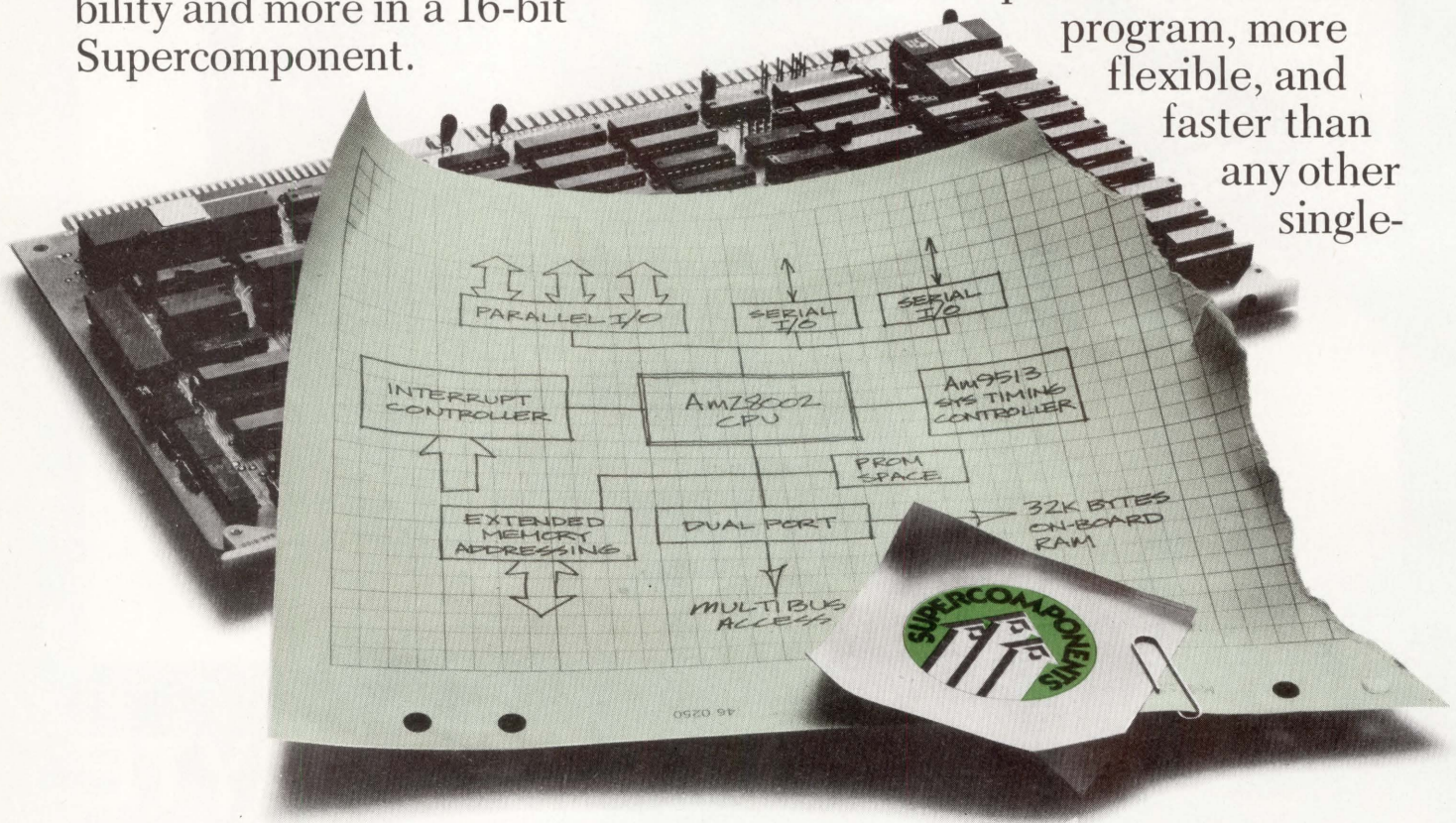
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Mask Generator Automation

State	Characters	Start	Title	Name Begin	Name	Parenthesis	Colon	Point	Comment
Carriage return		Name Begin	Name Begin	Name Begin	Name	Parenthesis	Colon	Point	Comment
Colon		Title	Title	Error (no aspect name)	Point	Parenthesis	Point	Error (no aspect name)	Comment
Parenthesis (left)		Title	Title	Error (no aspect name)	Parenthesis	Error (double left)	Error (second parenthesis)	Error (parenthesis in value)	Comment
Parenthesis (right)		Title	Title	Error (no parenthesis left)	Error (no parenthesis left)	Colon	Error (no parenthesis left)	Error (parenthesis in value)	Comment
Point		Title	Title	Error (no aspect name)	Name	Parenthesis	Error (no colon)	Point	Comment
End		Error (no input)	Error (end in title)	Error (no aspect name)	Error (no aspect value)	Error (no parenthesis right)	Error (no aspect value)	End	Error (end in comment)
Blank		Title	Title	Name Begin	Name	Parenthesis	Colon	Point	Comment
Diagonal streak		Title	Title	Comment	Error (comment in name)	Parenthesis	Error (comment after name)	Comment	Name Begin
Other characters		Title	Title	Name	Name	Parenthesis	Error (no aspect value)	Name	Comment

original data, it is possible to search the data with an I/O mask, sort the data with a sort mask, modify the data under I/O or search masks, display data with mask, or output the data in a table (Fig 2).

When searching with the I/O mask (Fig 3), the screen displays the user defined mask for data I/O, allowing entry and transmission of any available information. The file system searches

out and displays all records that match initialized mask positions. These records are neither buffered nor made available for further processing; instead, this search operation supplies fast access to the data base. Searching with the search mask (Fig 4) permits formulation of linked searches that specify, for each function, one aspect name, one criterion for comparison, and one aspect value. Upon termina-

tion, the system displays on the screen or printer the number of records that were located, which are buffered for use in the next operation.

A sort mask (Fig 5) can specify up to three sort criteria, effecting linkage only if the preceding criterion produced a match. Modification is always preceded by a search operation, which can be executed by either the I/O or the

(continued on page 190)



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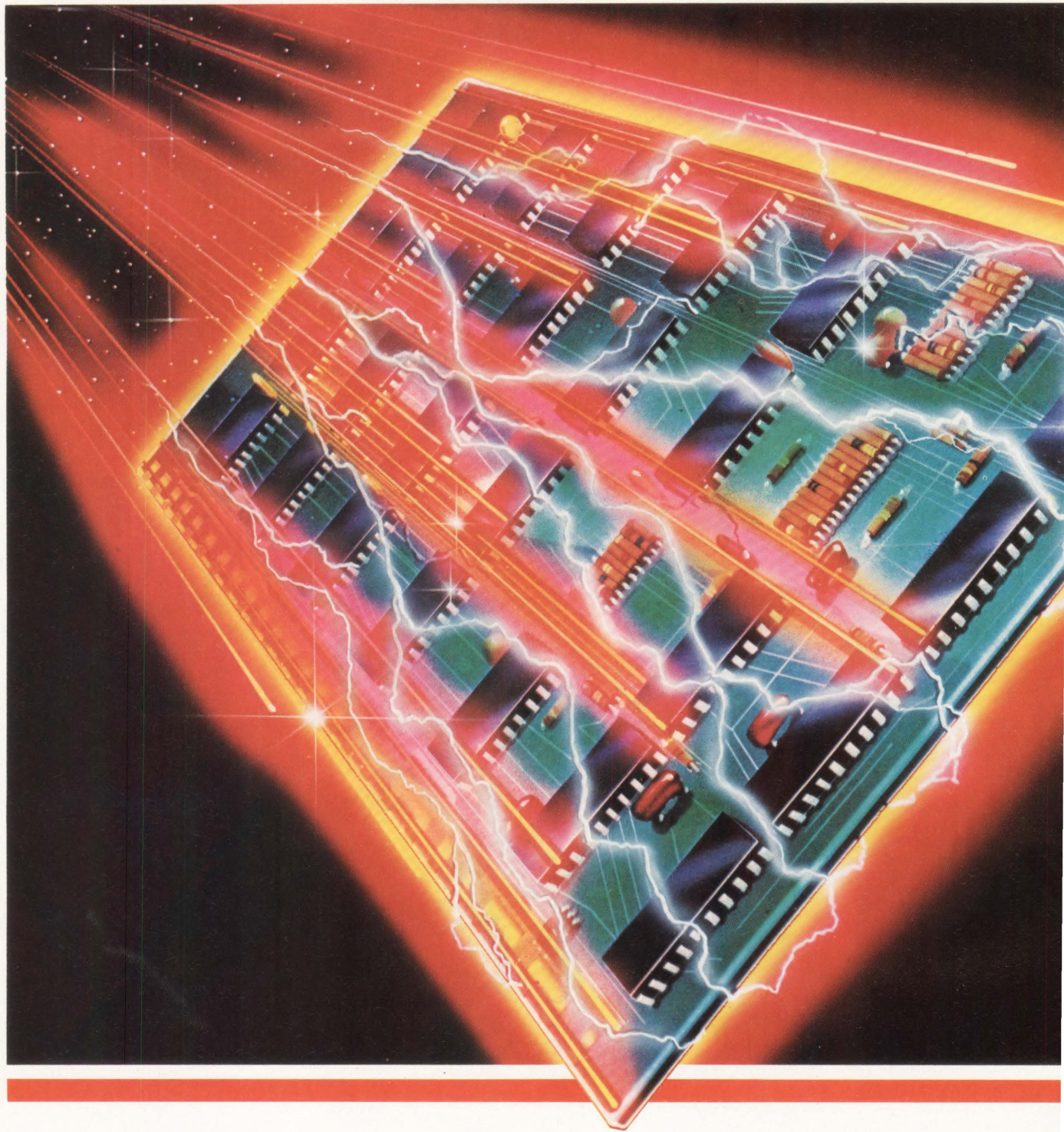


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I_{CC} . . 74F533—61mA max
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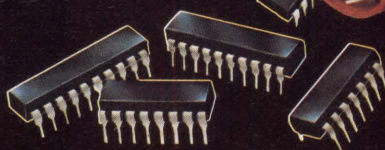
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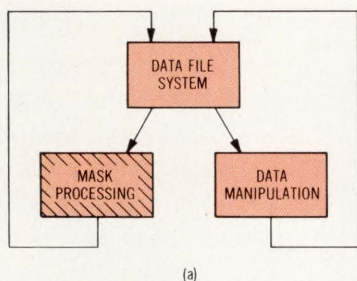
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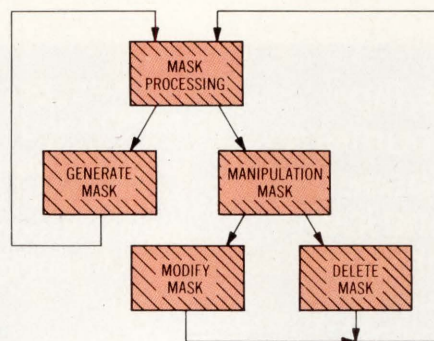
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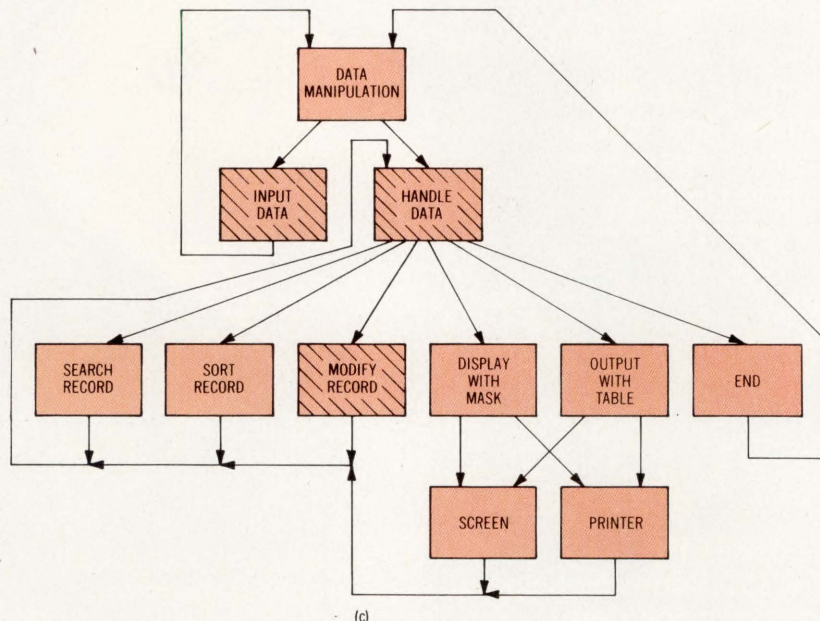
across the board.



(a)



(b)



(c)

Fig 1 File system software block diagram. Mask and its data are closely related; changes to mask can change its data. Mask processing section defines or modifies mask, which can also modify or delete associated data. Data manipulation section provides for data entry, search, sort, modify, or display stored data, all in accordance with appropriate mask

search mask. Search for modification involves the entire data volume. When using the I/O mask, the display shows the actual records that were located. These can be modified by overwriting the original data. When using the search mask, the display shows only the number of records that were located. The search operation may be continued at will; after termination, one record after another is displayed for modification.

The I/O mask is used to display data on both the screen and the printer. Whereas the screen can display only

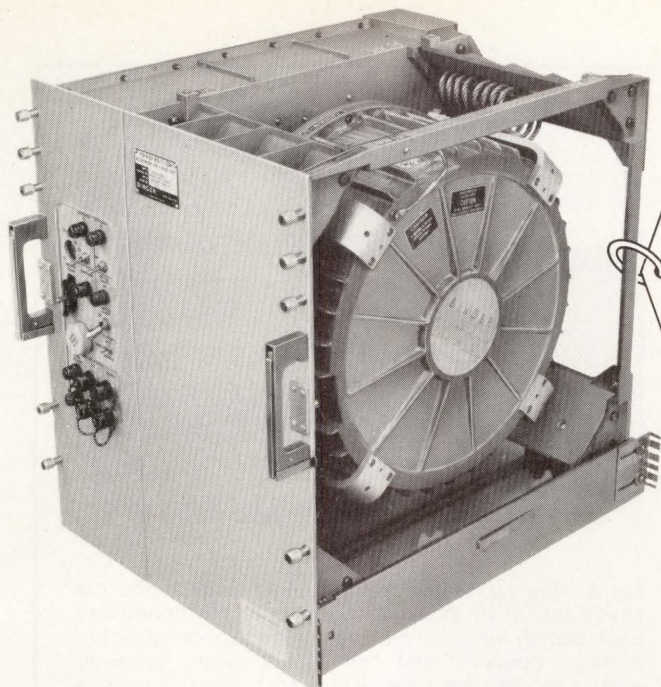
one record at a time, the printer outputs each record with the entire mask. If needed, data can be displayed in a table either on the screen or on the printer. All data manipulations except data modification are carried out in a loop whose operation is always based on those records that were produced during the preceding function.

Access Strategy

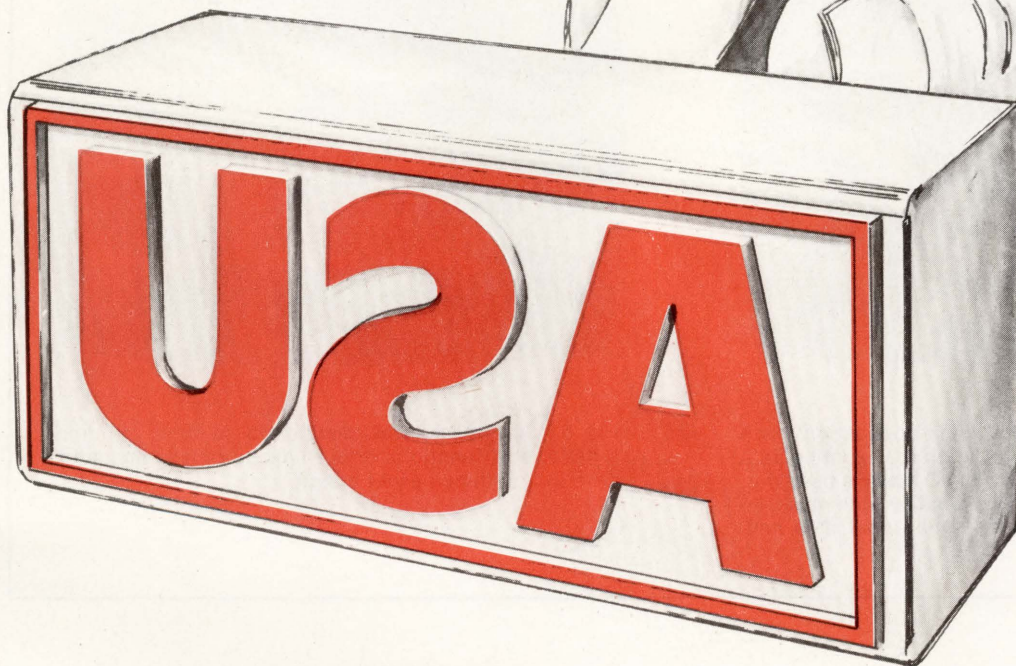
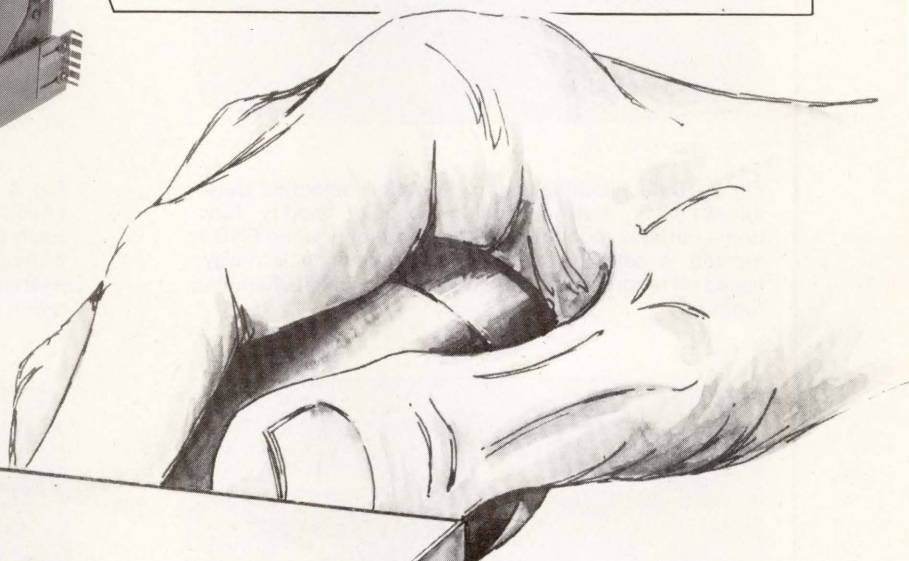
Because access to the floppy disc is very slow compared with processing in the computer, data manipulation must

be implemented with as few access operations as possible. In this file system, all of the main memory space not occupied by the database program is used for data buffering and divided into two buffers: the data buffer, for records that are read and updated, and the intermediate buffer, for records that are written to or read from the buffer file. As many records as possible are read from the floppy disc to the data buffer when a read job comes in from the data base. A processed block must be written back to the disc before

(continued on page 192)



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CIRCLE 97 ON INQUIRY CARD


```

MENU FOR DATA HANDLING

SEARCH
  WITH SEARCH MASK: ☐
  WITH I/O MASK: ☐

SORT   WITH SORT MASK: ☐

DISPLAY WITH I/O MASK: ☐
OUTPUT  WITH TABLE: ☐

MODIFY
  SEARCHING WITH SEARCH MASK: ☐
  SEARCHING WITH I/O MASK: ☐

END OF DATA HANDLING: ☐

```

Fig 2 Data handling menu. Function selection determines mask and—except in case of modify function—initiates loop that will terminate only when END is marked in selected mask. Loop processing is always based on records selected during previous data handling function

```

END(E)/HELP ASPECT NAMES (H): ☐
SEARCH MASK

ASPECT NAME: 
OPERATOR (= . < > #): 
ASPECT VALUE: 

COMBINATION (AND/OR): ☐
ASPECT NAME: 
OPERATOR (= . < > #): 
ASPECT VALUE: 

COMBINATION (AND/OR): ☐
ASPECT NAME: 
OPERATOR (= . < > #): 
ASPECT VALUE: 

```

Fig 4 Typical search mask. Linked search jobs can check for up to three independent match conditions. Each search function designates one aspect name, one criterion operator, and one aspect value. Following search, records that were located are buffered for subsequent processing

```

BLOOD DONOR

NAME:  FIRST NAME: 
BIRTHDAY (DDMMYY):  SEX (M/F): 

BLOOD GROUP (ABO):  RHESUS FACTOR: 
Vel (P/N):  DUFFY:  Mg (P/N):  MNSs: 
Wra (P/N):  LEWIS:  P (P/N):  KELL: 
Xga (P/N):  KIDD:  LUTHERAN: 

DATE OF DONATION (DDMMYY): 
NUMBER OF PRESERVE (LAST): 
NUMBER OF DONATIONS: 
PATHOLOGICAL RESULTS: 

```

Fig 3 Typical I/O mask. Blood bank application mask allows entry of new data or modification of existing data by overwriting original entry. When I/O mask is used during search function, records whose data match mask entries are flagged for processing during next data handling function

```

END(E)/HELP ASPECT NAMES (H): ☐
SORT MASK

ASPECT NAME: 
COMPARE FROM SIGN:  TO SIGN: 
ORDER ASCENDING: ☐ OR DESCENDING: ☐

ASPECT NAME: 
COMPARE FROM SIGN:  TO SIGN: 
ORDER ASCENDING: ☐ OR DESCENDING: ☐

ASPECT NAME: 
COMPARE FROM SIGN:  TO SIGN: 
ORDER ASCENDING: ☐ OR DESCENDING: ☐

```

Fig 5 Sort mask. Designating up to three different criteria, sort functions effect linkage only if preceding criterion produced exact match

the next block can be read. Write jobs are similarly executed. The records are stored in the buffer, and when the buffer is exhausted, the entire block is written to the floppy disc.

As the heart of the file system, the mask catalog contains the names of all masks defined in the system, and each entry has three files assigned to it: a mask file, an aspect catalog file, and a record file. When a new mask is created, its name is entered into the mask catalog at the time the mask file and aspect catalog entry are created. The record file is generated when data

are actually entered. The aspect catalog, containing the aspect names and the corresponding aspect value lengths, determines the structure of the data records. The record lengths are fixed; the arrangement of the records in the file is linear, and the fields within a record, which, by definition, have the same length in all records, are determined by the value lengths.

In developing the file system, emphasis was placed on easy to learn operator interaction. This ease of handling is achieved through consis-

tent operator prompting by masks and menus, and because the operator need not be concerned with the details of file management.

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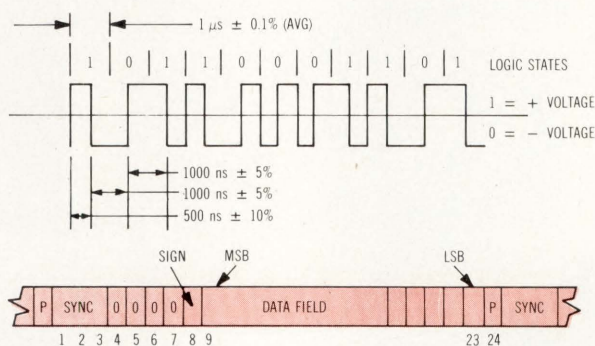
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The top part of the figure shows the biphasic code that represents data bits in the Manchester format. In this scheme, a logic 1 is represented by a 1 to 0 transition within a 1-μs bit period, and a logic 0 is represented as a 0 to 1 transition. The 24-bit format used to transmit a data word is shown in the bottom part of the figure. The first 3

bits are either the message or word sync; bits 4 through 7 represent 0s; the 16 data bits reside in bits 8 through 23; and the last bit is a parity bit. Four 16-bit words are stored in a register file, converted to the 24-bit Manchester format, and then transmitted serially along a 71-Ω twisted shielded pair. A 24-bit test word is sent after every four words.

Note

This work was done by Richard H. St. Cyr III of Rockwell International Corp., and W. Hu and R. Latshaw of The Garrett Corp for Johnson Space Center.

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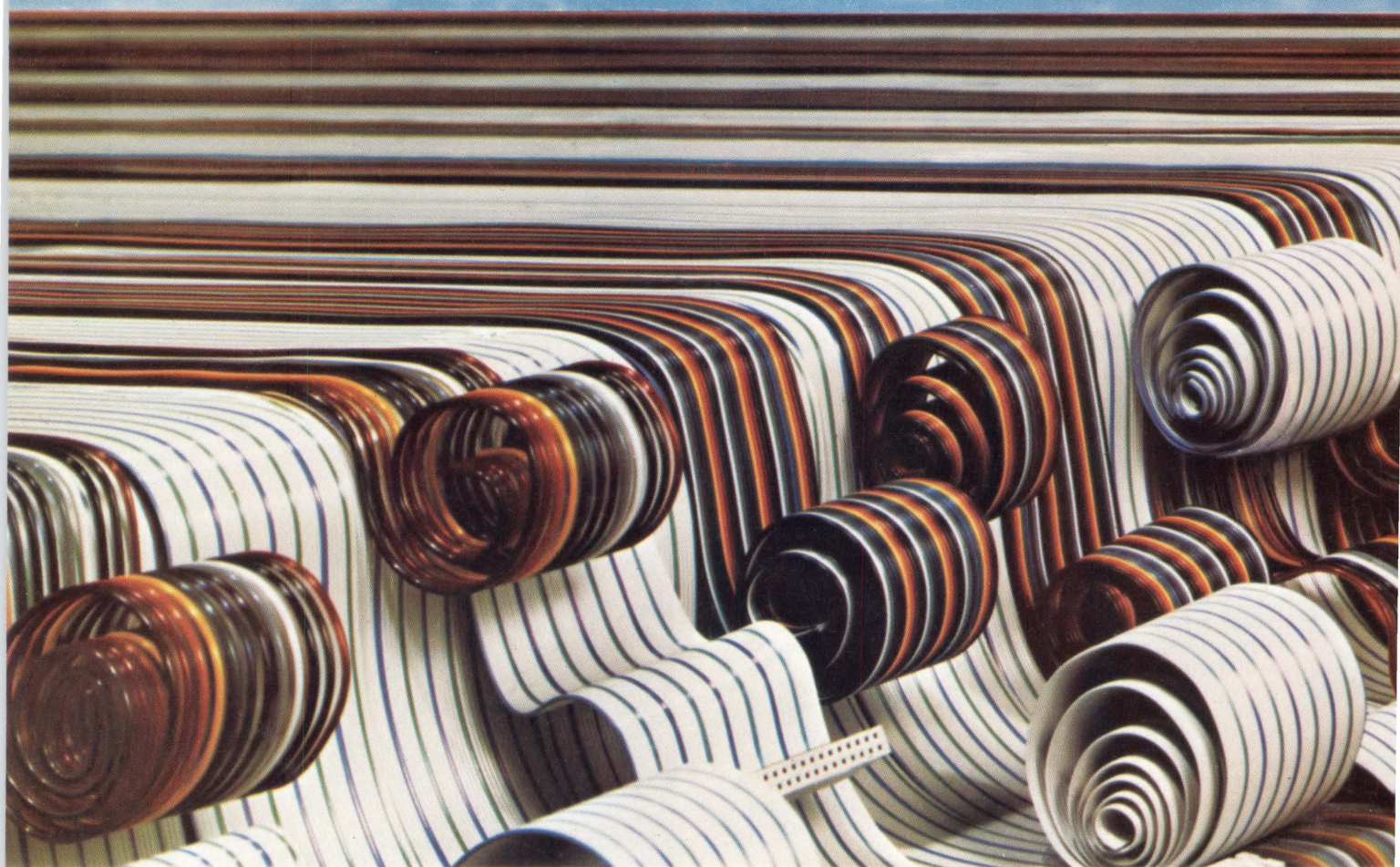
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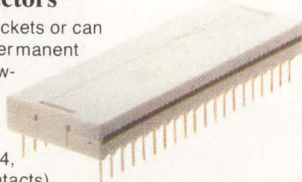
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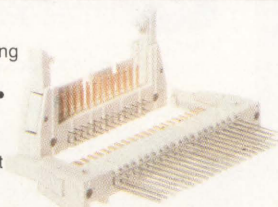
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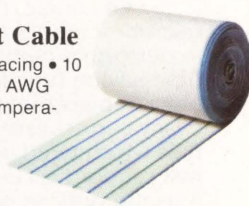
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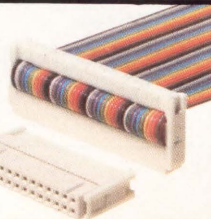
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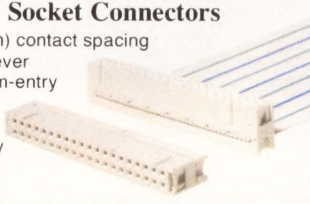
Socket Connectors

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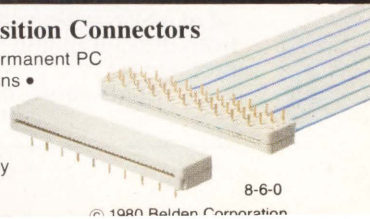
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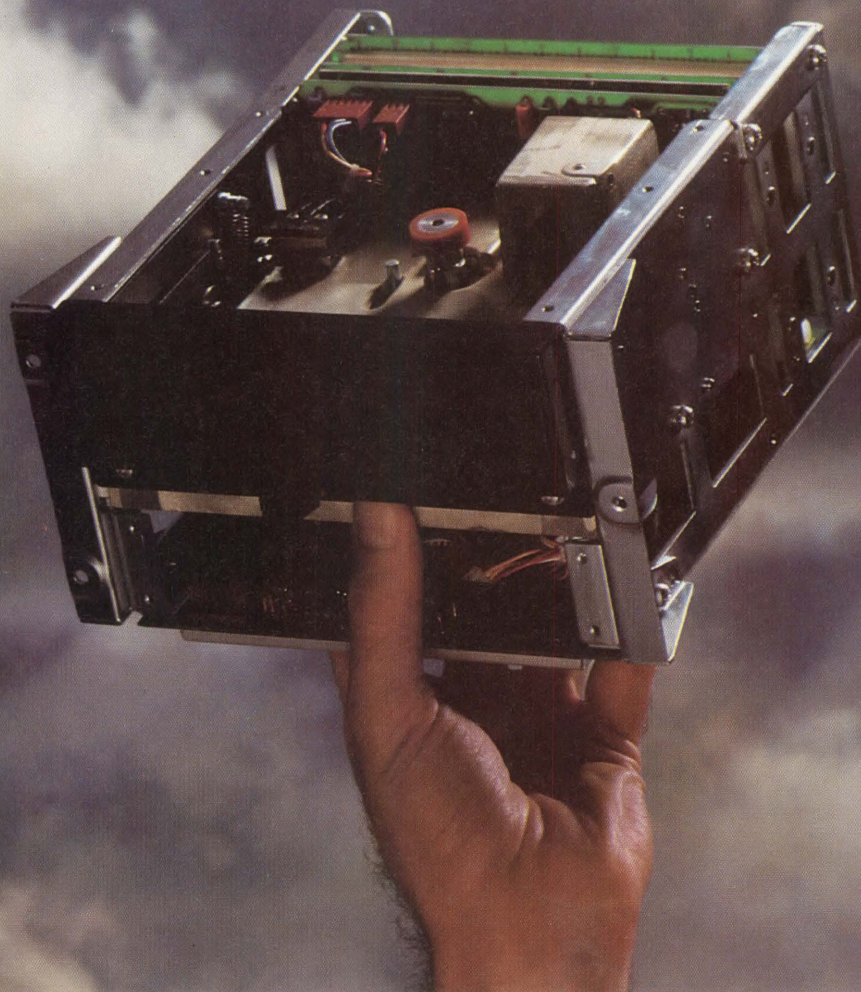


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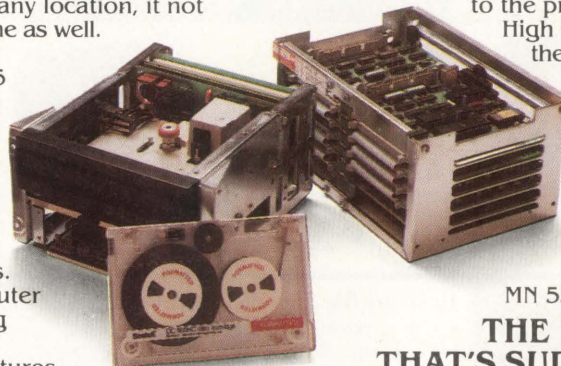
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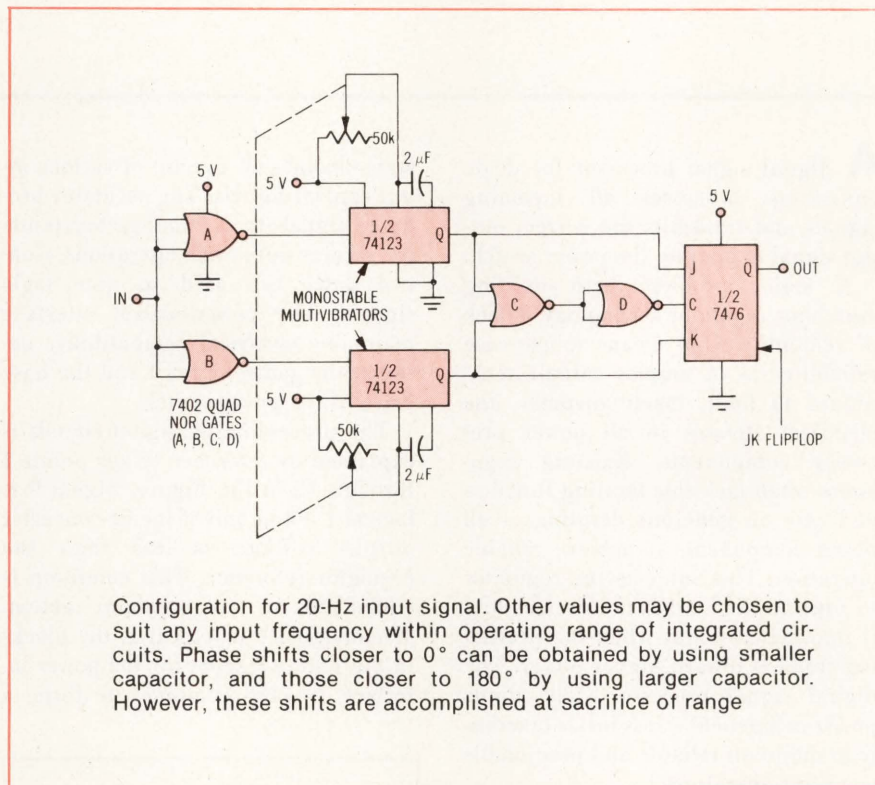
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TECH BRIEF

Digital Phase Shifter

Wide range phase shifter employs simple circuitry



Phase shift of a digital input may be varied over the approximate range of 15 to 165° with the circuit shown. Only TTL ICs and a single 5-V power supply are required.

One monostable multivibrator is triggered on the leading edge of the input signal; the other is triggered on the trailing edge of the input signal. A flipflop is toggled on the trailing edge of a clock pulse generated by ORing the two monostable outputs. Thus, the output of the flipflop is a replica of the input signal delayed by the on time of the monostables. The on time may be varied by adjusting the two ganged potentiometers.

Advantages of this system are a wide range of control and good stability provided by relatively simple circuitry.

Note

This work was done by Murray G. Perry of Vought Corp for Langley Research Center, Hampton, Va. No further documentation is available.

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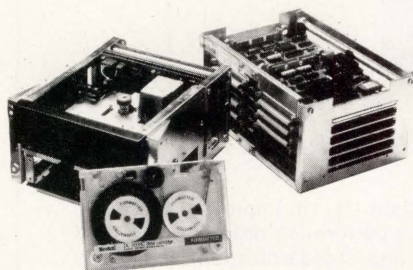
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Versatile Digital Signal Processor for dc-dc Converters

DSP works in unison with all types of power circuits and analog controllers

A digital signal processor for dc-dc converters processes all incoming signals and transmits the correct output signal to operate the power switch.

A major problem with existing switching regulator technology is lack of reliability. One means to increase reliability is to employ circuit techniques to limit, instantaneously, the electrical stresses in all power processor components. Existing regulators often lack this limiting function and rely on generous derating of all power components to achieve reliable operation. This subjects the regulator to uncontrolled transient stresses and is impractical today when the prevailing trend is toward higher power. The digital signal processor (DSP) limits power component stress instantaneously to maintain reliable and predictable transient operations.

A dc-dc converter must be oscillatory because of the finite flux capability of its inductive elements. The converter control system must therefore provide the proper discrete time intervals in controlling the on/off function of the power switch. For timing implementation, the various means of duty cycle control include (1) constant "on" time T_n , variable "off" time T_f , (2) constant T_f , variable T_n , (3) constant $(T_n + T_f)$, variable T_n and T_f , and (4) variable T_n , T_f , and $(T_n + T_f)$.

Basic building blocks of the DSP consist of isolator, time delay, memories, oscillator, control gates, and power/control interface.

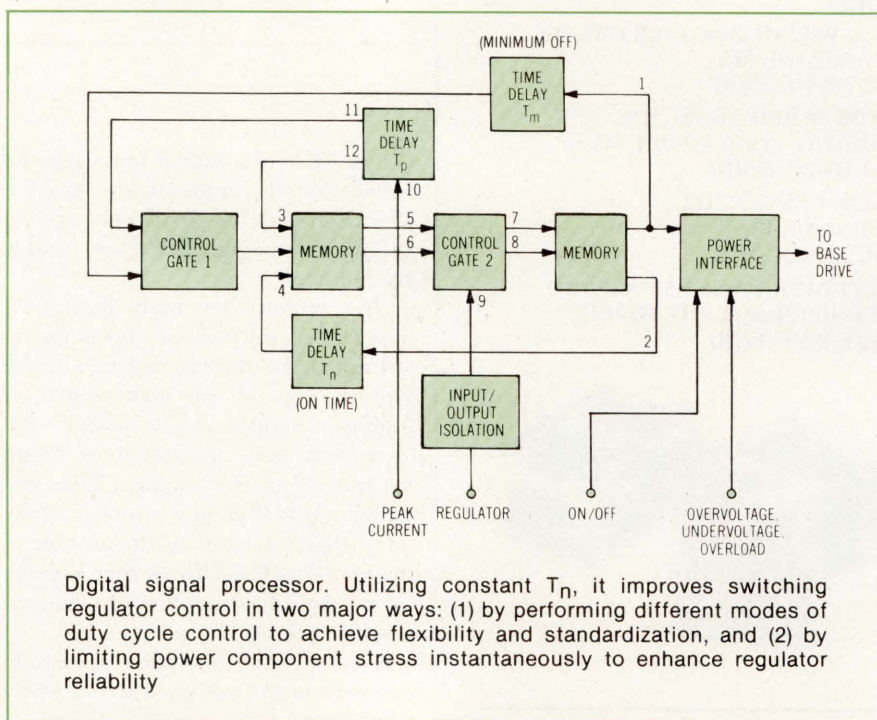
The function of the isolator is to provide control circuit input/output isolation. Time delay is used to effect proper duty cycle control during either steady state or transient operations. Memories are used to effect logical

state changes as a result of various input control signals. The oscillator produces signals to set timing constraints for various duty cycle operations. Control gates are used to gate logic signals. The power/control interface maintains electrical compatibility between the control circuit and the base drive of the power switch.

The processing of digital signals is explained by reference to key points 1 through 12 in the Figure. Signal 9 is logical 1 if and only if the dc-converter output voltage is less than the regulator reference. This condition is equivalent to no regulator action. When signal 9 is logical 1, the blocks in the Figure (except for the power interface blocks) combine to form a

freerunning oscillator. Oscillating frequency depends upon whether signal 10 is logical 1 or logical 0. Signal 10 is defined as the peak current protection signal and is logical 1 when the inductor current is less than the predetermined peak protection current.

When the DSP receives the converter "on" command, a few cycles of current buildup must occur before the peak current in the energy storage inductor reaches the predetermined protection level. During this time of buildup, signal 10 is logical 1, and the time delay T_p is not actuated by the peak current sensor. The oscillating frequency of this DSP is $1/(T_n + T_m)$, where T_n is "on" time and T_m is minimum "off" time of the converter.



These time intervals are coupled to the base drive circuit to control the power switch through the power interface block. Also, during this time of (peak current) buildup, the output voltage is less than the regulator reference so that signal 9 remains logical 1 throughout.

The time required for peak current buildup is less than that required for output voltage buildup. Thus, when the time of peak current buildup has ended, signal 10 becomes logical 0 in each cycle before T_n is timed out, while signal 9 remains at logical 1. Time delay T_p is activated, T_n is shortened to T'_n , and T_m is replaced by $T_p \geq T'_m$. The oscillating frequency during this interval of output voltage buildup is $1/(T'_n + T_p)$.

Eventually, the converter reaches its intended regulation level. Signal 9 becomes logical 0 in each cycle as the output voltage intersects the voltage reference. The circuit design ensures that the inductor current remains below the peak current protection level at all times so that signal 10 is always logical 1. Minimum "off" time T_m is

disabled and "on" time becomes T_n , while "off" time is increased to T_f . Oscillating frequency in steady state is thus $1/(T_n + T_f)$.

The converter on/off command signal and the converter shutoff signal are processed by the power interface block. These signals respond either to external command or internal protection for the initiation or termination of the converter operation. A logical 0 input always terminates the operation, and reset is required before restart.

Because of the latching function associated with the overvoltage, undervoltage, and overload shutoff, these signals are normally processed by another memory block before entering the power interface. This is different from the peak current signal and the regulator signal, which are required to exhibit both logical 0 and logical 1 cyclically. Consequently, the regulator signal 9 and the peak current signal 10 are generally obtained from a threshold detector.

A constant frequency DSP can also be developed by using some of the basic building blocks of the constant

"on" DSP by processing the same signals. By utilizing an oscillator to define a constant "on" time plus "off" time, the regulator signal determines both T_n and T_f . The time delay block T_n is thus eliminated. Furthermore, because of the availability of essentially the entire period as the time delay following an excessive peak current detection, time delay T_p can also be eliminated. Excluding these blocks along with their control gates results in a simple constant frequency DSP.

Note

This work was done by John L. Biess, Leonard Y. Inouye, and Yuan Yu of TRW, Inc, for Lewis Research Center, Cleveland, Ohio

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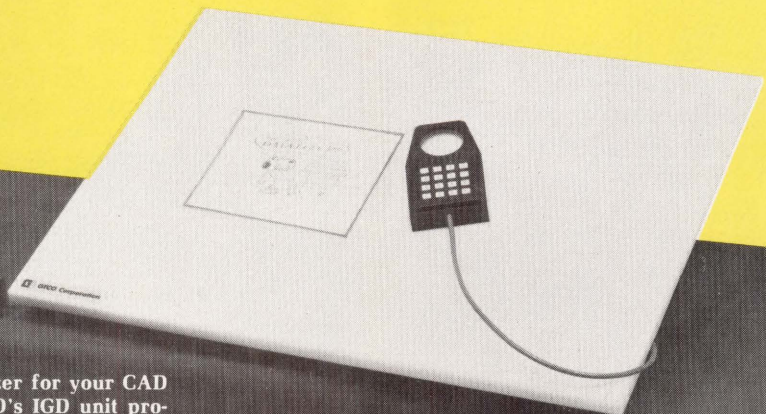
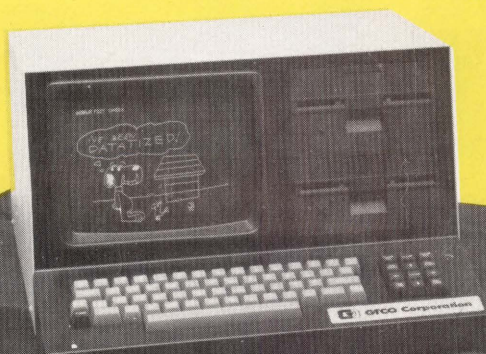
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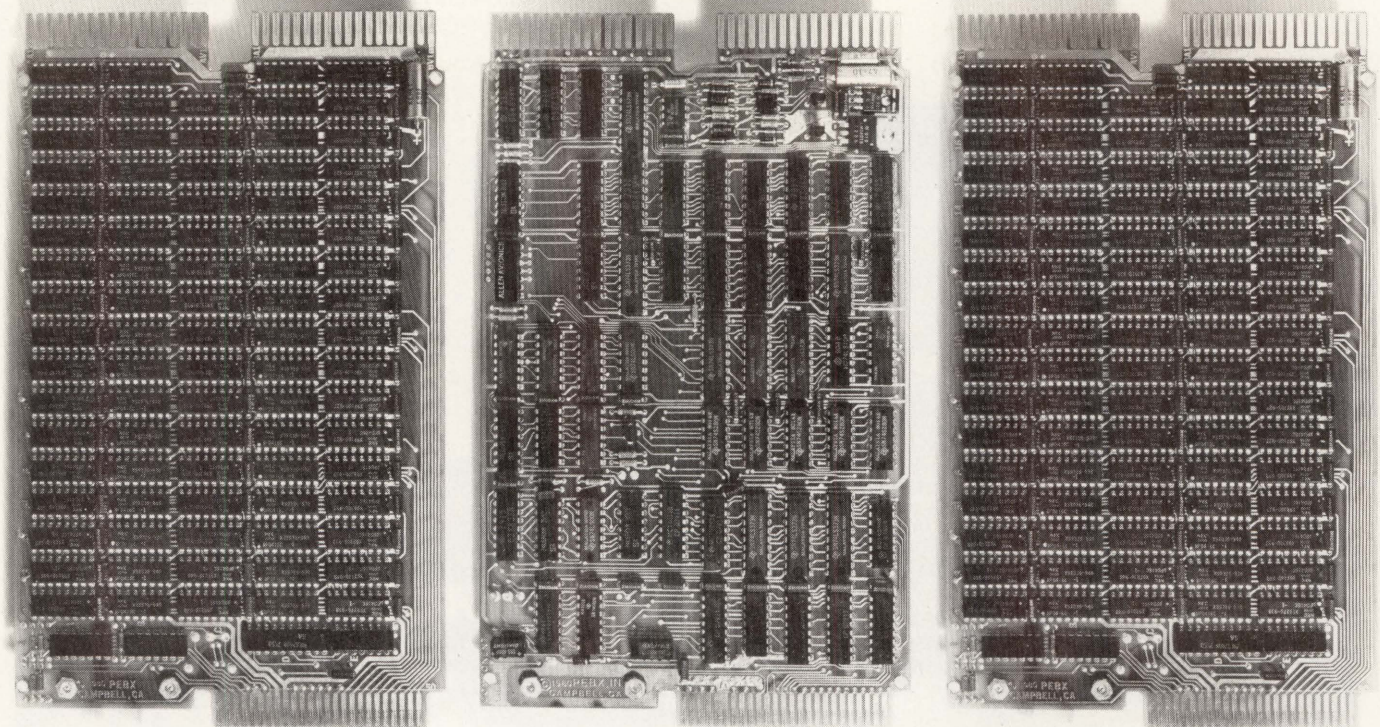
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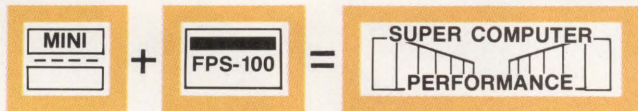
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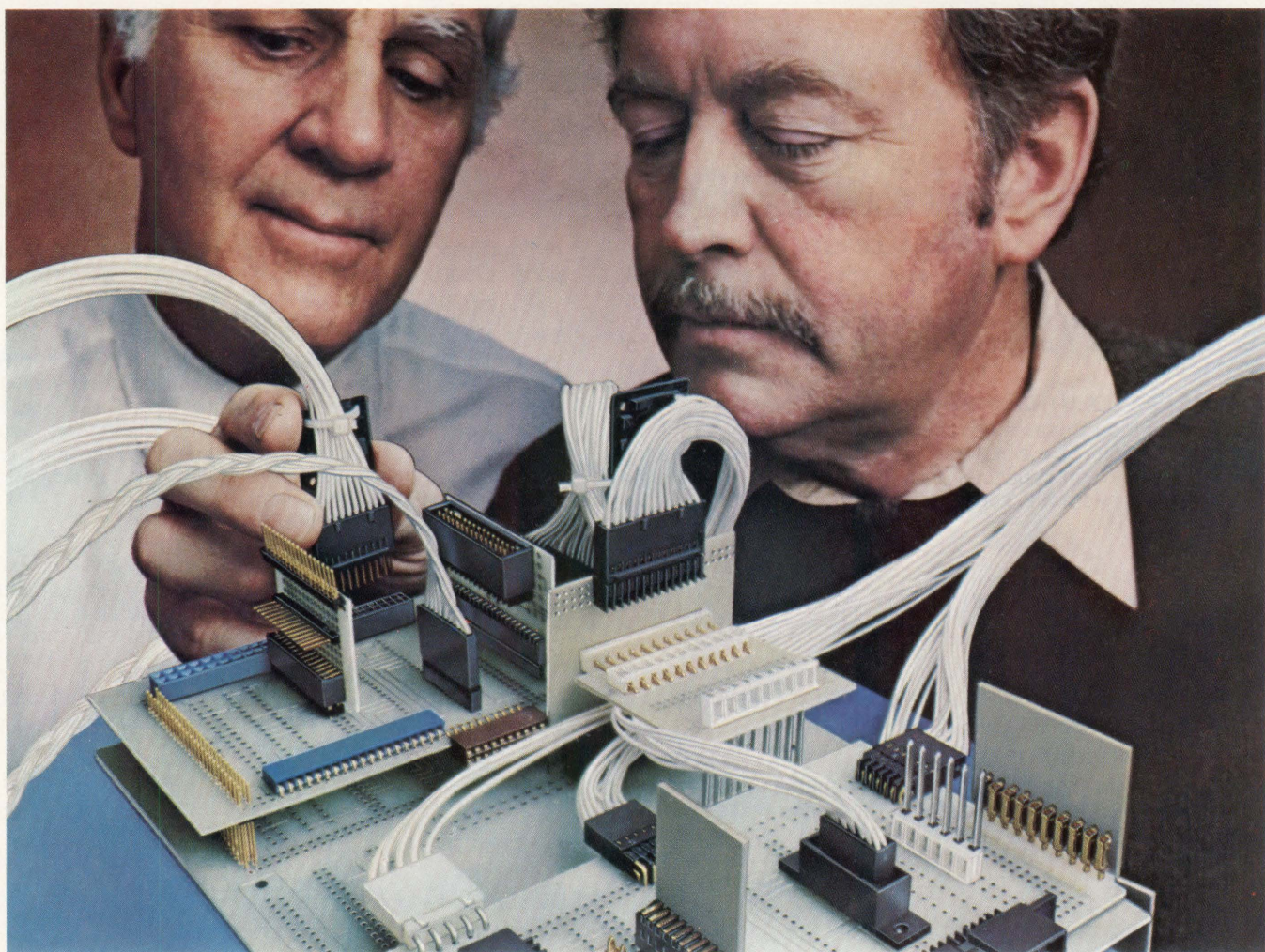
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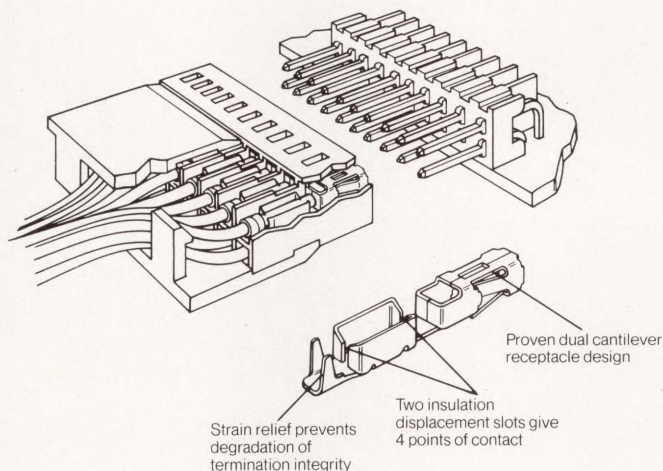
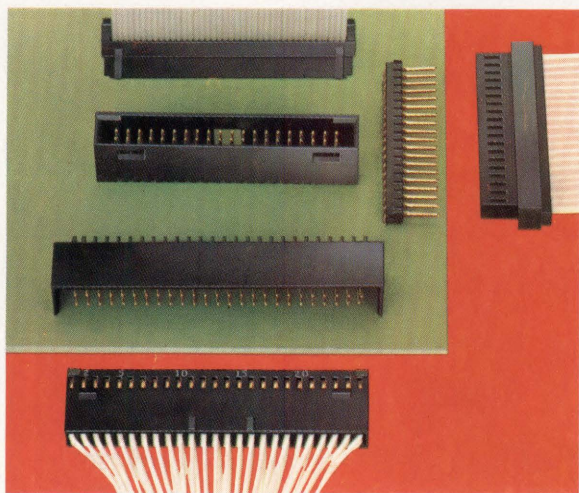
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Benefits and burdens of using high level languages in microprocessors are often different from those of using high level languages in larger computers. Principal motives for using high level languages in microprocessor applications include a high degree of machine independence, ease of transporting and upgrading software to run on newer machines, and reduced programming cost per byte of generated object code. Some of the major deterrents to the use of high level languages in a microprocessor environment are the relatively inefficient use of storage by compiler generated object code, the somewhat slower execution speed, and the inefficient use of specific machine features such as registers or bits on input/output ports. Many microprocessor based systems are produced in large volume and therefore cannot tolerate program storage inefficiency. For example, when building a product that will sell one million units, it is worthwhile to invest thousands of programmer man-hours for the purpose of eliminating one read only memory unit costing about \$15 (when purchased, inserted, documented, supported, maintained, ordered, and inventoried).

A high level language for the 650x family of microprocessors, CSL/65 (also available as PL/65 from Rockwell International) addresses these software development issues. It has proven to be easy to learn, capable of increasing programmer productivity, and useful for easing software documentation tasks. Although certain microcomputer designs must avoid the small inefficiencies that are in-

evitable in even an optimized high level language, many programs or program segments lack stringent speed and size limitations, and for these CSL/65 offers a high level language that is both economical and easy to maintain.

Specifically designed for use on the KIM, SYM, AIM, APPLE, PET, and other 650x based microcomputers, CSL/65 does not attempt to convince programmers that a more powerful architecture is present. Instead, it provides well formed, block structured code subject to all of the limitations imposed by its target machine, thereby helping programmers make the sometimes frustrating transition from assembly language programming to high level language programming. Also, because it provides many of the language constructs found in ALGOL and Pascal, CSL/65 is a natural stepping-stone that can ease minicomputer programmers into the hybrid software/hardware environment of microprocessor software engineering. Moreover, source programs written in CSL/65 are relatively easy to comprehend without supporting documentation. Development teams can therefore use CSL/65 code segments from previous projects almost as they would use assembly language macros. In fact, libraries of procedures are beginning to develop.

Additional characteristics of CSL/65 illustrate criteria that should be considered whenever deciding between assembly language and any high level language candidate. Its learning time is short, typically 8 to 16 hours, even less for those skilled in programming other high level languages. Because it was designed for a specific machine architecture, it offers

an easy transition both from 650x assembly language and from other high level languages. Programmer intervention at the assembly language level permits greater flexibility and manual optimization. Without optimization, CSL/65 usually generates from 20 to 70% more bytes of object code than an equivalent assembly language program prepared by an experienced programmer; however, its use increases programmer productivity from 200 to 400% over use of assembly language. Software optimizers allow direct enhancement of the assembly language code; however, although the optimizers are quite good, they rarely surpass the efficiency of assembly language produced by hand.

Itself written in a form of high level language, the CSL/65 compiler is generated through a semiautomatic process that will theoretically produce an assembly language version capable of running on virtually any host machine. The process begins by supplying a description of the compiler rules (its syntax) as input to a software compiler generator. Compiler generator output is assembly language code for the host machine on which the compiler will run; this need not be one of the 650x target machines that execute code generated during compilation. An assembly language driver is then combined with the output from the compiler generator to construct the complete compiler. For example, one version of the CSL/65 compiler runs on a PDP-11 host to generate 650x target machine code.

The compiler generator approach offers several advantages. Generated compilers are themselves easier to maintain and enhance than compilers written in a more conventional manner. Also, it is easier to create new versions of the compiler capable of running on different host machines since this requires only a new driver routine and a change to the semantics portion of the compiler generator. In fact, for the PDP-11 based compiler just mentioned, the driver was itself written in CSL/65. Although the process may seem circular, its ultimate flexibility and utility warrant the initial compiler development effort.

A brief description of 650x microprocessor characteristics demonstrates the potential of the CSL/65 statement repository. This microprocessor family is byte oriented: the arithmetic and logic section and the data registers are all 8 bits wide. Neither 16-bit registers nor double-register operations that might be equivalent to 16-bit registers are provided. However, the family does provide both pre- and post-indexing, which is constrained by the 8-bit index registers to a range of 256 bytes. Indirect addressing must be performed using a 16-bit pointer that resides in one of the lowest 128 pairs of bytes within the 64k-byte address space. 650x microprocessors are very popular for use in consumer products, industrial controllers, and intelligent peripherals. Various manufacturers offer 650x development tools and support components.

Table 1 lists a representative selection of CSL/65 language statements, and Table 2 shows representative forms of the versatile assignment statement. Fig 1 shows a complete, functional source program as a further means for evaluating the language, while Fig 2 presents the assembly language output produced by compiling the Fig 1 source, highlighting its potential for optimization at the assembly language level.

From a development strategy viewpoint, data structuring and register manipulation represent two extremes of a software design effort, one best suited to a high level language

TABLE 1

Partial List of CSL/65 Language Statements

Statement	Function
DECLARE	Reserve named locations or regions
DEFINE	Define external variables
DATA(W)	Define and initialize locations or regions
COMMENT	Format output
PAGE	
TAB	
SET BITS	
CLEAR BITS	Set specific bits
SHIFT BITS	Clear specific bits
ROTATE BITS	Logical shift left or right
PULSE	Rotate left or right
	Pulse designated location at specified polarity
CODE	Insert assembler language code
HALT	Jump to current location
WAIT ON BITS	Wait until designated bits have specified polarity
STACK	Push bytes or words (or both) onto stack
UNSTACK	Pop bytes or words (or both) from stack
ENTRY	Initialize machine state
CASE	Initialize for computed GOTO
CALL	Invoke subroutine
RETURN	Terminate subroutine
WHILE DO	Structured flow of control
FOR TO BY	
INC	Increment byte or word
DEC	Decrement byte or word
BEGIN END	Define procedure block
IFF	Test condition code bits or named register

TABLE 2

Typical Assignment Statements

Statement	Function
B = @C	Indirect source
@B = C	Indirect destination
B = #B	Immediate byte data
B = ##C	Immediate word data
B ← C	2-byte data
B = C[N]	Transfer Nth byte of array C
B.N = C	Transfer N bytes starting at C
B[J + 1].K - 1 = 'ABC'	Transfer K - bytes of literal data
B = A .AND C	Logical operators augment + and -
B[5] = C[4] - (F - D + 3)	Parentheses are allowed
B = B + 1	Can increment (or decrement) any variable


```

0001; PAGE '**SORT**';
0002; ;
0003; * ASCENDING ORDER SORT*;
0004; ;
0005; DEFINE * = $10; *PAGE ZERO*;
0006; DECLARE F,I,TMP;
0007; ENTRY $200;
0008; ;
0009; N=N-2; *SET TERMINAL VALUE FOR LOOP*;
0010; F = 1; *SET TERMINATED FLAG*;
0011; WHILE F=1
0012; DO;
0013; F=0;
0014; FOR I=0 TO N
0015; BEGIN;
0016; IF BCI > BCI+1 THEN
0017; BEGIN;
0018; F=1; TMP=BCI;
0019; BCI=BCI+1; BCI+1=TMP;
0020; END;
0021; END;
0022; END;
0023; ;
0024; N: DATA 10; *N IS NUMBER OF SORT ELEMENTS*;
0025; B: DATA 23,55,36,28,54,39,99,86,21,67;
0026; ;
0027; EXIT;

```

Fig 1 Typical source program. Familiar to every programmer, bubble sort algorithm, coded here in CSL/65 source language, illustrates complete and useful program

approach and the other demanding the flexibility formerly provided only in assembly language. Because it was designed to support a specific machine architecture, CSL/65 allows programmers to attack both ends of a software design task, using only one programming tool that combines the economy of a high level language with most of the versatility of assembly language.

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SORT.....PAGE 0001

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0004	0000		
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0020	0203	9A	
0021	0204		
0022	0204		
0023	0204	AD 70 02	
0024	0207	38	
0025	0208	E9 02	
0026	020A	8D 70 02	
0027	020D		
0028	020D	A9 01	
0029	020F	85 10	
0030	0211		
0031	0211	A5 10	
0032	0213	C9 01	
0033	0215	F0 03	
0034	0217	4C 70 02	
0035	021A		
0036	021A		
0037	021A	A9 00	
0038	021C	85 10	
0039	021E		
0040	021E	A9 00	
0041	0220	85 11	
0042	0222	CD 70 02	
0043	0225	F0 05	
0044	0227	90 03	
0045	0229	4C 6D 02	
0046	022C		
0047	022C		
0048	022C	A5 11	
0049	022E	A8	
0050	022F	A5 11	
0051	0231	18	
0052	0232	69 01	
0053	0234	AA	
0054	0235	BD 71 02	
0055	0238	D9 71 02	
0056	023B	90 03	
0057	023D	4C 66 02	

Fig 2 Typical compiler output. Comparison with Fig 1 shows how compiler produces fairly efficient and well

SORT.....PAGE 0002

LINE #	LOC	CODE	LINE
0058	0240		
0059	0240		
0060	0240	A9 01	
0061	0242	85 10	
0062	0244	A5 11	
0063	0246	AA	
0064	0247	BD 71 02	
0065	024A	85 12	
0066	024C		
0067	024C	A5 11	
0068	024E	A8	
0069	024F	A5 11	
0070	0251	18	
0071	0252	69 01	
0072	0254	AA	
0073	0255	BD 71 02	
0074	0258	99 71 02	
0075	025B	A5 11	
0076	025D	18	
0077	025E	69 01	
0078	0260	A8	
0079	0261	A5 12	
0080	0263	99 71 02	
0081	0266		
0082	0266		
0083	0266		
0084	0266	E6 11	
0085	0268	A5 11	
0086	026A	4C 22 02	
0087	026D		
0088	026D		
0089	026D	4C 11 02	
0090	0270		
0091	0270		
0092	0270		
0093	0270		
0094	0270	0A	
0095	0271		
0096	0271		
0097	0271	17	
0097	0272	37	
0097	0273	24	
0097	0274	1C	
0097	0275	36	
0097	0276	27	
0097	0277	63	
0097	0278	56	
0097	0279	15	
0097	027A	43	
0098	027B		
0099	027B		
0100	027B		

ERRORS = 0000 <0000>
END OF ASSEMBLY

formed assembly language code that is easy to modify or further optimize

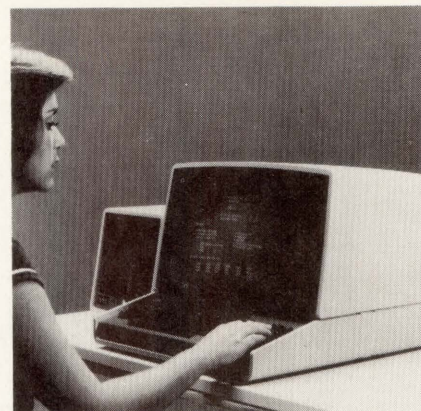
Single-Chip Microcomputer Family and Development System Offer Cost-Effective Sizing

Available in seven sizes, the S2200 family and Phoenix-1 development system are said to provide a mix of models and features that will aid in cost-effective selection of 8-bit microcomputer systems. The n-channel microcomputers, recently announced by American Microsystems, Inc., 3800 Homestead Rd., Santa Clara, CA 95051, include 5-Vdc operation, power-down RAM protection, onboard circuitry for keyboard decode, direct LED display drive, zero crossing detection, 8-bit programmable timer, two interrupts, and 50- or 60-Hz operation. ROM capacity ranges from 512 to 2048 bytes with table lookup capability.

From 32k to 128k of onchip RAM is available in 4-bit nibbles. All bits in RAM can be set, tested, or reset. There are three to five levels of subroutine depending on interrupt usage. A power fail interrupt is nonmaskable and of highest priority. Two maskable interrupts can be generated by the internal counter or by software.

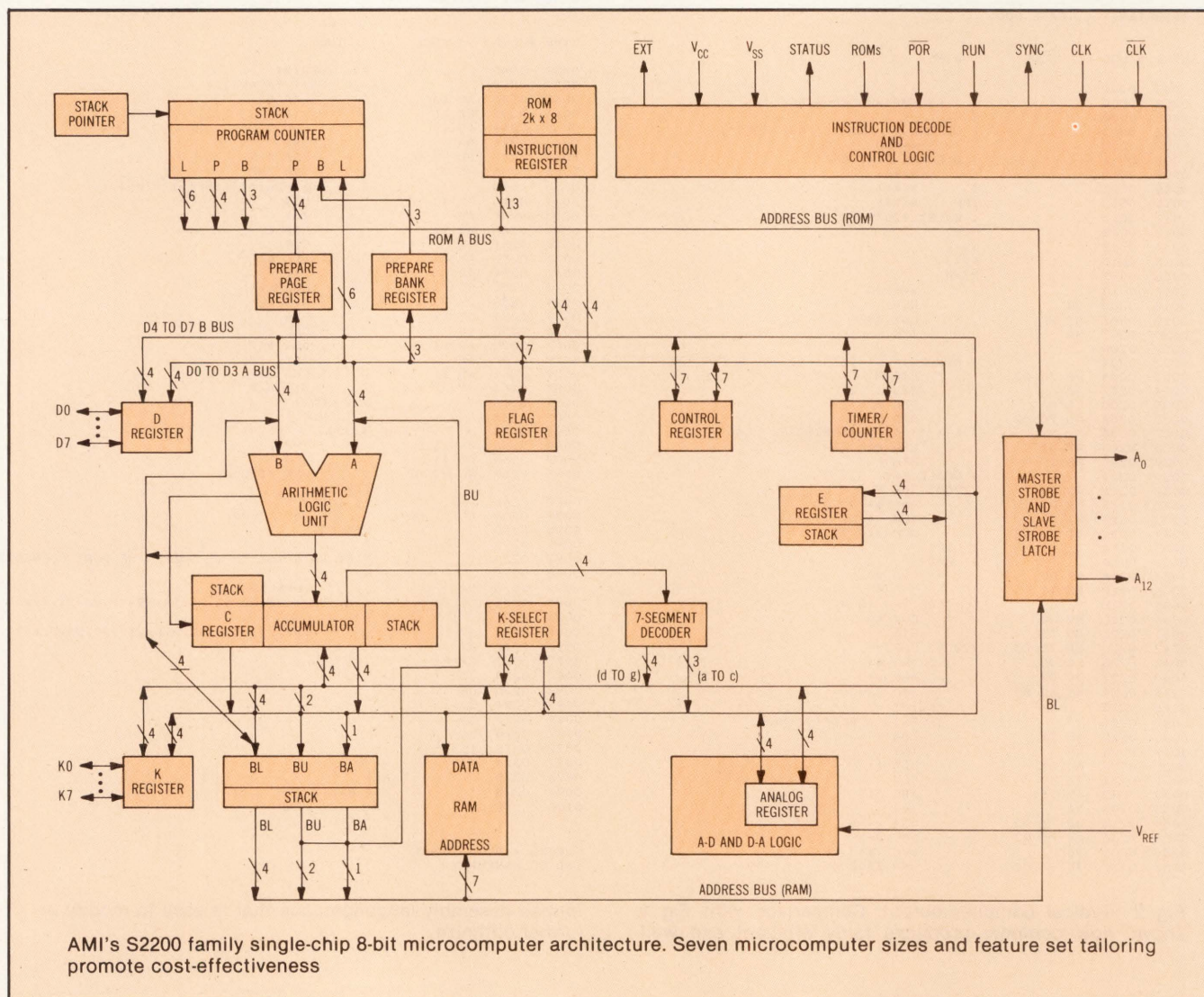
An inexpensive RC network is required for the internal oscillator; for critical timing applications a crystal may be used. Bit serial or byte parallel communication protocols can be implemented.

Development aids include a screen oriented editor for generating user



Phoenix-1 microprocessor development station. System supports 27 microcomputers and microprocessors. Software supplied includes a universal editor and assemblers with simulators for the AMI S2000 and S2200 microcomputers and assemblers for the AMI S6800 and S9900 microprocessors

source files and full macro capability. A software simulator allows software
(continued on page 214)



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A full-color video tape, demonstrating some of the many ILS capabilities and features, is available.

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A new set of mathematical operators has been added to ILS Version 3 to expand its signal processing capabilities. The software handles both real and complex data and supports functions such as: addition, multiplication, magnitude, hard and soft limiting, phase wrapping and unwrapping, FFT and inverse FFT, autocorrelation, crosscorrelation, convolution, spectral density, coherence, and moving or exponential averaging to reduce variance. New graphics programs have been added to display the results. Version 3 also supports an optional set of programs which enhance the performance of ILS for those who have an array processor made by Floating Point Systems, Inc.



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CIRCLE 108 ON INQUIRY CARD

Technological leadership.

New VLSI peripherals for the expand opportunities in

Motorola's MC6809 has been providing cost-effective solutions for advanced systems requiring a powerful 8-bit MPU for well over a year.

Now the M6809 Family of HMOS peripheral circuits allows users to make even more effective use of this advanced microprocessor, in systems from terminals and small business computers to process controllers.

No other 8-bit MPU combines so many outstanding features:

- 500 ns bus-cycle time
- Two million byte memory address capability (with the MC6829 MMU)
- Most complete combination of addressing modes
- Multiprocessing (with the MC6809E)
- Advanced software-oriented architecture with 16-bit registers
- Minimized code-space requirement
- Re-entrant and modular code support
- Four high-level languages, including Pascal, FORTRAN and MPL, plus assembly language
- Choice of EXORciser® or EXORset™ 30 development systems. M6809 USE available for in-circuit emulation with the EXORciser
- Lowest price of any 8-bit MPU with high-performance claims.

Lower software costs.

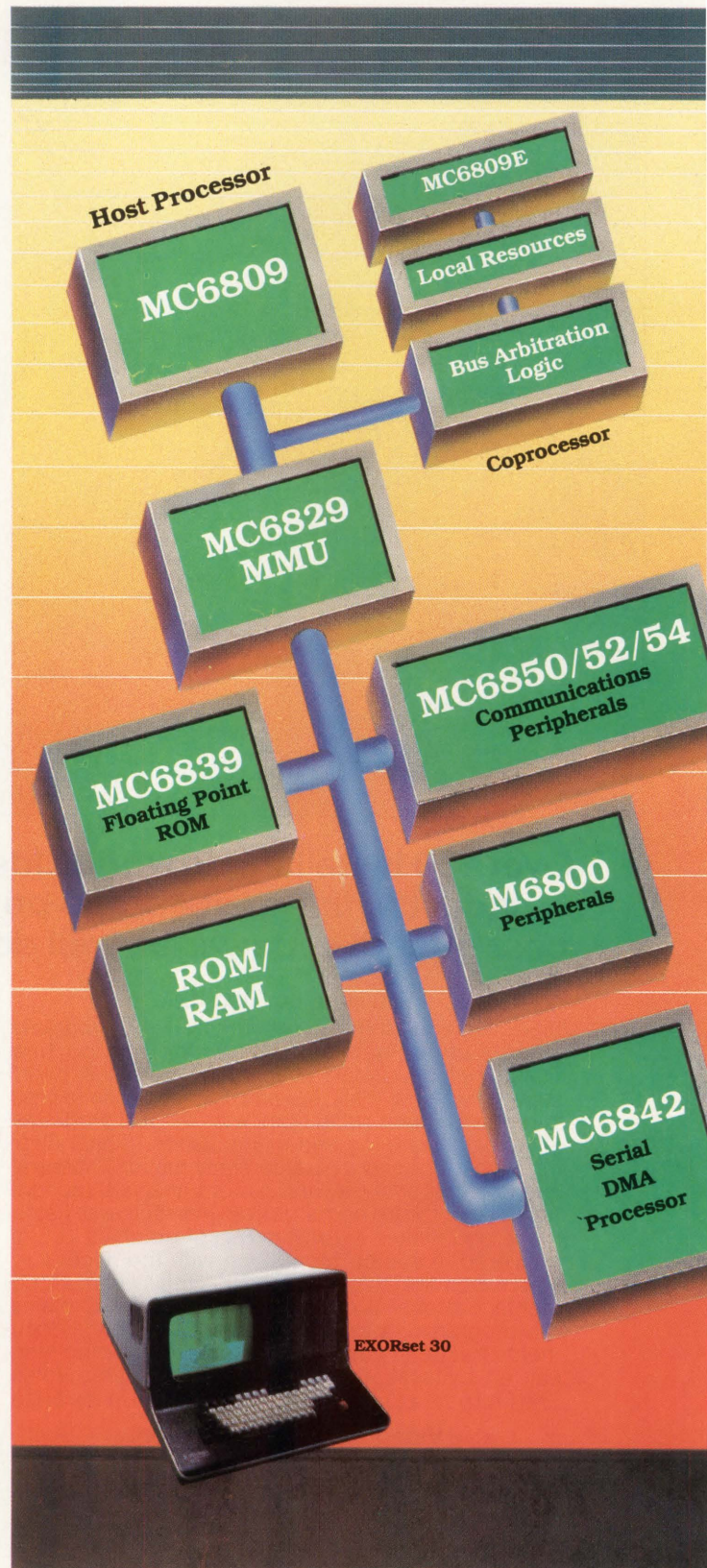
Helping keep software costs down must be counted as one of the MC6809's greatest assets. Its software-oriented architecture permits programmers to spend less time learning, more time programming. High-level languages like Pascal help keep costs down, too. And with the position independent addressing modes of the MC6809, standard "Software on Silicon" modules can be created to eliminate countless rewritings of commonly used codes.

Architectural advantages, beyond 16-bit registers and modern programming techniques, add to the versatility and cost-effectiveness of the MC6809. Auto-increment and auto-decrement addressing modes improve the efficiency of block moves and string handling, and extensive stack manipulation capabilities make block-structured high-level languages a natural.

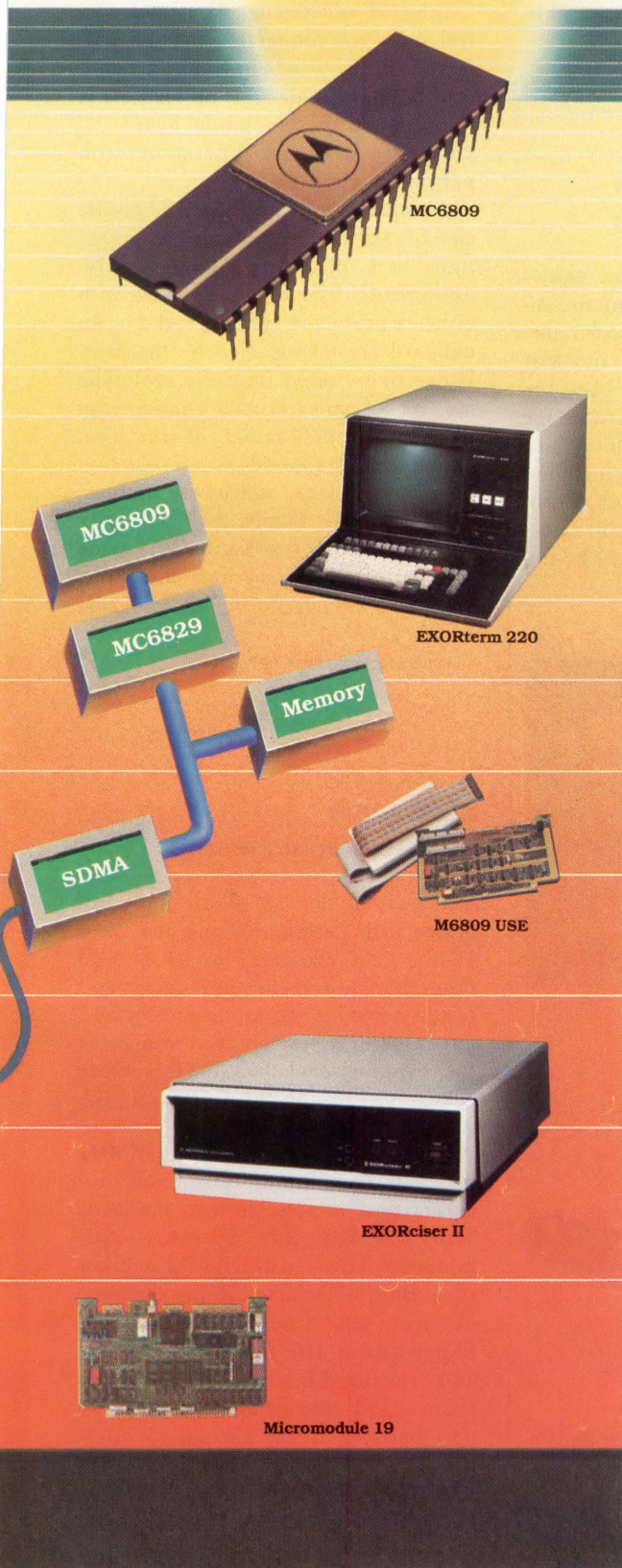
The M6809 Family plan for advanced systems.

A whole new family of VLSI peripherals has been designed to take advantage of the many powerful features of the MC6809, and in turn, to help users obtain its full potential in flexible, high-performance 8-bit and pseudo 16-bit systems.

System support for the MC6809 is still supplied by the entire complement of M6800 Family peripherals, and several of the high-performance VLSI peripherals of the 16-bit M68000 Family also are directly compatible.



high-performance MC6809 advanced 8-bit systems.



Coprocessing is easily accomplished with the M6809 Family. The new externally clocked MC6809E provides the flexibility required for multiprocessing: multiple processors operating in parallel on the same bus. Unlike some coprocessing schemes, with the MC6809E users are not limited only to floating point or string manipulations.

The MC6809 can **address** two million bytes of memory with the MC6829 Memory Management Unit, twice that of competing MPUs. And the MMU makes **multitasking** easy. It supports up to four tasks per chip, and it's cascadable for up to 32 tasks. System **reliability** is increased with the isolation, translation and protection of the MMU.

IEEE-standard floating point routines run on M6809 systems with the MC6839 Floating Point ROM. The floating point package is written with position independent code, and can be located anywhere in memory. It's re-entrant, so multiple tasks can share its routines.

The MC6842 Serial Direct Memory Access Processor is a family addition planned for next year to handle high-speed transfer of data and control between and among microprocessors and intelligent controllers in distributed processing systems.

The last word in support.

EXORset™ 30 is Motorola's latest MC6809-based development system: a compact, stand-alone unit that's the last word. EXORciser® and EXORterm™ systems, and the M6809 USE (User System Emulator) are available. And, many users find the MC6809-based Micromodule™ 19 monoboard microcomputer helpful for system prototyping.

In addition to assembly language, the MC6809 supports high-level languages including MPL, BASIC, and FORTRAN, with emphasis on Pascal, the structured language. Our symbolic debugger and a new Realtime Multitasking System (RMS09) will help speed the development cycle.

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through silicon.



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MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

package verification prior to hardware integration and an SES 2200 hardware simulator provides emulation capability.

Three models (designated SA22XX) perform 8-bit, multiplexed 8-channel A-D conversions. One mask optional D-A channel is available. A 48-pin package is standard for all models. For board sensitive applications, a lower cost 28-pin version is available.

The development system is equipped with a 12" (30-cm) scrolling CRT, ASCII keyboard, 48k RAM, three mini-disc drives, two RS-232-C ports, an AMIX™ fault tolerant operating system, a full screen oriented editor, and macro assemblers for the S2000, S2200 microcomputers, and S6800 and S9900 microprocessors. Available software includes Pascal and FORTRAN-77 and assemblers for the 8080A, 8085, Z80, 6502, 2650, 6801, 6805, and 6809.

For system checkout with any n-channel EPROM, the manufacturer supplies the ARIEL™, standalone or independent host computer controlled,

P/ROM programmer/ROM simulator. Realtime emulation with realtime trace is attained using DELPHI, the manufacturer's in-circuit emulator. Software and hardware additions can be used with other microprocessor development systems. The manufacturer claims that the development system is one-third the cost of most comparable systems.

Circle 320 on Inquiry Card

Emulation Board Allows Prototyping of EPROM Microcomputer

Functionally and electrically equivalent to the 8751 EPROM microcomputer, the EM-51 emulation board also can be used to develop 8051 and 8031 microcomputer prototypes. Sockets for 2716 or 2732 EPROMs that substitute for 8051/8751 onchip program memory and one 2732A 4k x 8 EPROM are included with the board from Intel Corp, Microcomputer Instrumentation Operation, 5200 NE Elam Young Pkwy, Hillsboro, OR 97123.

The 2.75 x 5.25" (6.99 x 13.34-cm) board plugs directly into 8751/8051/8031 sockets without a cable. It includes sockets for 2716 or 2732 EPROMs, which substitute for the 8051/8751 on-chip memory during prototype development. An Intel 2732A 4k x 8 EPROM is included with the board.

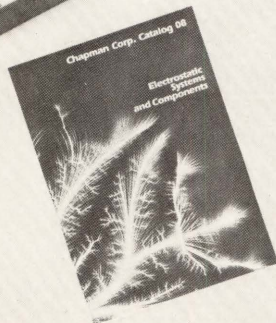
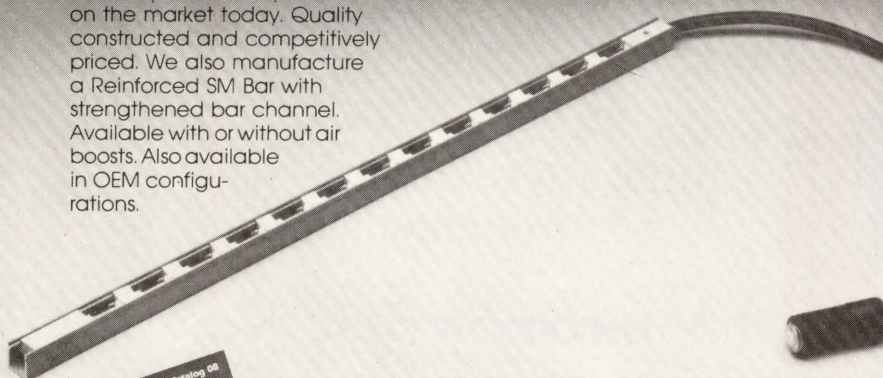
Internal addressing, data, and control lines are connected through buffers to the two sockets using a bond-out technique. Once onchip memory is replaced by the emulation board, I/O ports are free for operation with peripheral circuitry.

A single 4k x 8 or two 2k x 8 EPROMs can be selected depending on access time and operating frequency requirements. The board operates with either a prototype system crystal or an onboard crystal supplied by the user. It can be powered from the prototype 8051 socket, an external 5-V power supply, or a combination of the two. Jumpers on the board permit selection of memory, clock, and power options. Within the 8051 family, the 8751 has 4k bytes of EPROM, the 8051 has the same amount of mask programmable ROM, and the 8031 has no onchip program memory.

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CPUs Meet MIL-STD Requirements

Versions of the Z80 8-bit microprocessor with peripherals and the Z8000 16-bit CPU conform to MIL-STD-883 Class B requirements, processed and tested according to methods 5004 and 5005. Operating temperature range for the ceramic packaged devices from Zilog, 10340 Bubb Rd, Cupertino, CA 95014, is -55 to 125 °C.

Operation at a rate of up to 4 MHz with minimum 1.0-μs instruction execution time is possible with the Z80A. The 2.5-MHz Z80 operates with minimum 1.5-μs instruction execution time. Both CPUs have 158 instructions, duplicate sets of general purpose and flag registers (16 total), bus request and prioritized interrupt request daisy chains, and 8080 compatible, non-Z80 peripheral, and Z80 peripheral interrupt processing.

Z80 family peripherals available in MIL-STD versions include the Z8420

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dual-port parallel I/O controller. This device has interrupt driven handshake on both ports, four programmable operating modes, and programmable interrupts. Also available are the Z8430 4-channel counter/timer, Z8440 serial I/O controller with two 0- to 800k-bit/s full-duplex channels, 8470 dual asynchronous receiver/transmitter featuring programmable stop bit, parity, and clock mode options, and Z8410 direct memory access controller (DMA). The DMA manages CPU independent transfers between ports in systems using an 8- or 16-bit data bus and a 16-bit address bus.

Circle 322 on Inquiry Card

Multipurpose Bus Line System Analyzer

The AE-4100 series of microprocessor system analyzers feature a bus line switching system that displays several debug functions regardless of the hardware and software of the unit under test. System analyzers also serve as the operator panel of the microprocessor allowing read/write operations to/from all registers, memories, and I/O ports. From Inaba Corp, 11060B Artesia Blvd, Cerritos, CA 90701, the system analyzers are usable in research and development, product inspection, diagnosis, and maintenance on 8- and 16-bit systems.

Combinations of 16 function keys and 16 numeric keys perform required operations. To conduct detailed analyses, the analyzer connects to an oscilloscope, logic analyzer or other device. Waveforms are observable on an oscilloscope by REPEAT function and RUN, STOP, and STEP functions.

The series is also available with a built-in cassette MT to be used as an I/O interface for field testing and maintenance. Other options are an I/O interface, keyboard printer, and user mode RAM. The user mode RAM option can set 8k bytes of programmable random access memory into 64k bytes of any system address space.

Circle 323 on Inquiry Card

Microprocessor I/O Boards Offer SS50 and SS50C Bus Compatibility

An 8-port I/O interface board that occupies one slot of an SS50 or SS50C bus and a 2-port board were recently announced by Gimix Inc, 1337 West 37th Pl, Chicago, IL 60609. Both 6800/6809 microprocessor boards feature independent ports and RS-232 compatibility with handshaking.

The 8-port serial I/O board includes DIP switch selectable baud rates for each port, extended address decoding for the SS50C bus, selectable interrupts, and the versatile 6850 ACIA. It is available with an onboard baud rate generator for baud rates up to 38.4k baud.

Jumper programmable connector pinouts for easy cabling, independent baud rate, and interrupt jumpers for each port, as well as the 6850 ACIA, are standard on the 2-port serial I/O board. The board is compatible with both the SS50 (4 addresses per I/O slot) and SS50C (16 addresses per slot) bus configurations.

Circle 326 on Inquiry Card

Memory Boards Provide 64k Bytes of Dynamic RAM on S-100 Bus

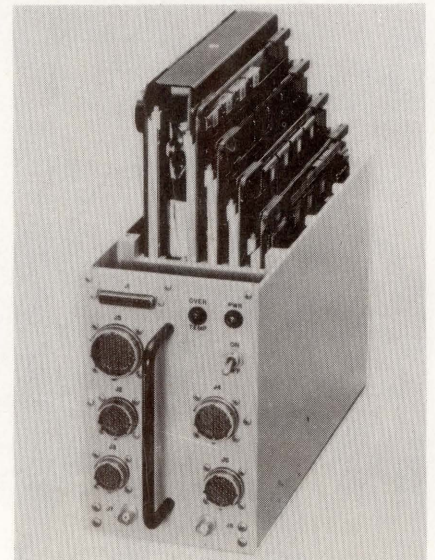
Memory boards provide 64k bytes of dynamic random access memory (memory refresh is transparent to the processor) for Z80A, 8080A, and 8085 microprocessors. Performance specifications are operating speed of 4 MHz (with no wait states), a 220-ns memory access time, and a 400-ns cycle time. The SUPERAM 4-Z family from Piiceon Inc, OEM Computer Products, 2350 Bering Dr, San Jose, CA 95112, is optimized for S-100 bus based systems.

Three versions are available: the 4-Z, which is the basic 64k-byte RAM board, the 4-ZB with memory selection, and the 4-ZBP with a parity bit option for error detection, which protects data by adding an extra bit to each byte. The option detects bit errors and alerts the CPU.

All three boards are organized in four 16k-byte blocks. Each block can be enabled or disabled by simple switch settings.

Circle 325 on Inquiry Card

Severe Environment Microcomputer Serves Industrial Applications



Offering all features of the MIL-STD model but with a narrower operating temperature range, industrial rated SECS 80/10I withstands severe shock and vibration and includes conformal coating of PCB components. The single-board system is a ruggedized counterpart of the Intel iSBC 80/10A and is fully compatible with Intel software and development systems.

Environmental operating characteristics include temperature range of -20 to 70 °C, vibration of 5 G, 5 Hz to 2 kHz, shock of 15 G, 11 ms, humidity range of 0 to 95% RH with condensation, and an altitude range of sea level to 70,000 ft (21.33 km). The board measures 9 x 6 x 0.5" (22.86 x 15.24 x 1.27 cm), and weighs 18 oz (0.48 kg).

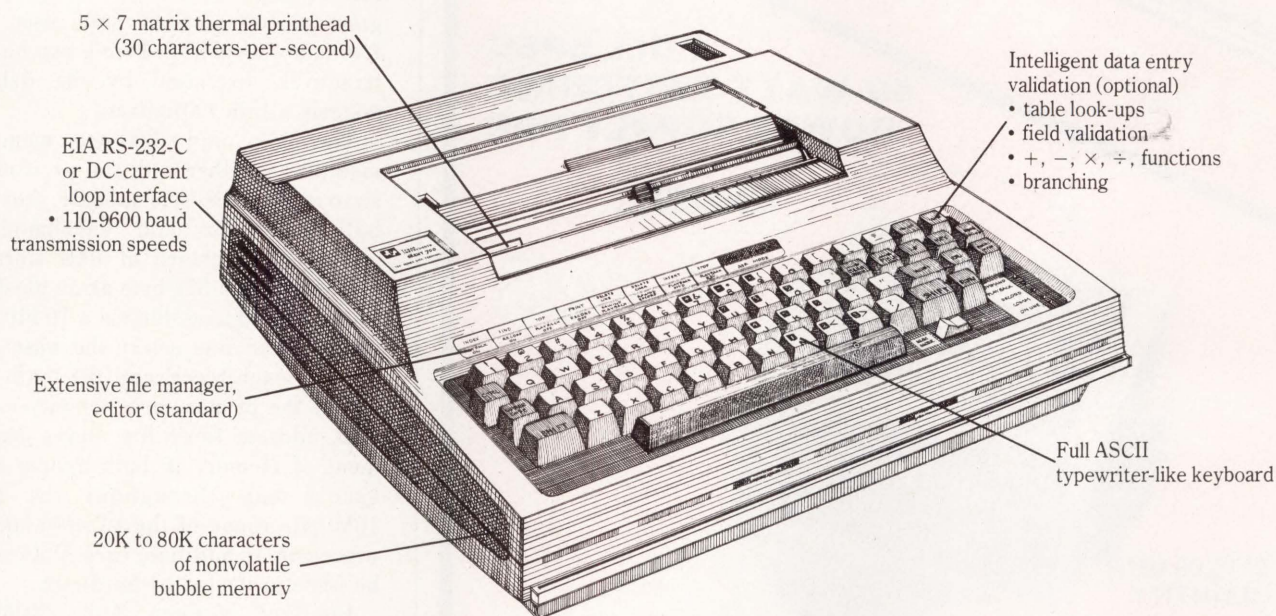
Produced by EMM Sesco, 20630 Plummer St, Chatsworth, CA 91311, the board offers up to 8k bytes of on-board ROM or P-ROM and 1k bytes of RAM. Expansion to up to 64k bytes of offboard combinations of RAM, ROM, and P-ROM is possible and ROM and P-ROM can be added in 1k-byte increments.

Circle 324 on Inquiry Card

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TI's *Silent 700** Model 763 Bubble Memory Data Terminal is ideal for remote data capture, and off-line data preparation and manipulation applications. Storing up to 20 typewritten pages of information in its built-in nonvolatile bubble memory, the 763 eliminates the need for more costly data storage devices and allows users to batch transmit data at their convenience. A Data Entry Validation option on the 763 provides program execution, file management interface, arithmetic operations

and data verification. The 763 with its other features and options, is a specialist when it comes to quick, accurate data entry and transmission.

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For more information on the 763 terminal, contact the TI sales office nearest you or write Texas Instruments Incorporated, P.O. Box 1444, M/S 7784, Houston, Texas 77001 or phone (713) 937-2016. In Europe, write Texas Instruments, M/S 74, B.P. 5, Villeneuve-Loubet, 06270, France.



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TEXAS INSTRUMENTS

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CIRCLE 111 ON INQUIRY CARD

Emulator/Memory Modules Extend Development System Capabilities

Four MC68000 microprocessor development modules, a user system emulator (USE), VERSAbus 32k- and 64k-byte

dynamic memory modules, and a VERSAbus adapter module extend capacity of the EXORmacs development system. Products of Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, the modules permit extension of development system resources to target system, increased memory flexibility, and interface between EXORbus modules and VERSAbus.

Consisting of control module, buffer box, and interface cable, the USE

emulator operates at 4 or 8 MHz or with an external clock and extends a user's target system. The extension provides necessary correction between the user's non-debugged hardware/software system and the diagnostic power of the EXORmacs. Debug functions of MACSbug and the symbolic debugger, SYMbug, are included along with file management and memory storage capability of EXORmacs.

Firmware on the USE control module sets up the external user system before and during a debug session. EXORmacs, through the MPU and DEbug modules, handles all terminal and printer I/O activity on the system during USE operation. Under command control from USE, the target program is downloaded into user or EXORmacs memory, where it can be interactively exercised by the debug systems within EXORmacs.

The 64k- and 32k-byte memory modules, together with the previously announced 128k-byte module provide both EXORmacs and VERSAmodule users with a choice of RAM storage elements. Each 32k-byte array block is separately addressable via a 10-bit DIP switch; nine bits select the base address of each block, and the tenth bit selects the primary or secondary map. This address flexibility allows placement of memory in both system and user's map throughout the full 16M-byte range of the MC68000 microprocessor. In addition, each block may be write protected by hardware.

Interface between 8-bit EXORbus modules and the 16-bit VERSAbus is provided by the VERSAbus adapter module (VAM). The VAM is provided as an option to enable use of various I/O modules, memory, and Micromodules designed for the EXORbus. Synchronous timing and control are available to the EXORbus module by use of the VAM.

Circle 327 on Inquiry Card

Interface Cards Extend Computer's Control Capabilities

Serial (RS-232-C), general purpose I/O (parallel), and BCD interface cards plug into slots in the back of the HP-85 desktop computer and provide full

(continued on page 223)

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Models Chart

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SD12-4.2	12V	4.2A
SD15-3.4	15V	3.4A
SD24-2.1	24V	2.1A
SD28-1.8	28V	1.8A



POWER-ONE D.C. POWER SUPPLIES

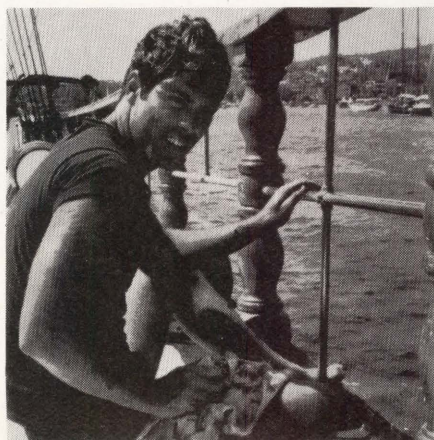
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8-Bit Champion

In price-performance, look to Intel's powerful iAPX 88 microprocessor to leave the pack behind. Both now and down the road.

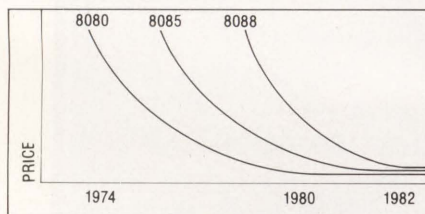
In price-performance races, the iAPX 88 is the one to beat. It's two times faster than the Z-80A and the MC6809. And recent benchmark tests* show that the iAPX 88, with its 8088 CPU, consistently outperforms its closest competitors in memory efficiency, ease of programming and throughput—by as much as 4 to 1. This is especially important in high-performance tasks such as block moves, character searches, word shifts, and 16-bit multiplies. All critical for applications like word processing, terminal control, scientific instrumentation and industrial control.

And because it's the only 8-bit microprocessor that addresses up to 1 million bytes of memory, the 8088 can take on large programs. Without having to slow down due to overlays or memory bank switching, like other 8-bit processors.

Tough price competitor

In price competition with other 8-bit microprocessors, the iAPX 88 has become the front runner.

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8-Bit Microprocessor Price Trends

memory chips, too. The iAPX 88 takes—on the average—30% less memory than competitors for the same programs. Then too, it allows you to use lower cost memory to get the same throughput as competitors. With a 5MHz 8088, you can use our 450ns memories and still outperform a 4MHz Z-80 requiring 250ns chips. Depending on

the application, your cost savings here can be substantial.

No contest now with new Intel software

To unleash the new power that the iAPX 88 puts in your hands, it takes more powerful software—

	iAPX 88	Z-80	MC6809	8085A
Relative performance	1 (5MHz)	0.4 (4MHz)	0.6 (2MHz)	0.3 (3MHz)
16-bit object code compatible	8086	NONE	NONE	NONE
Relative assembly language code required	1	1.5	1.4	1.5
Memory/I/O address space	1 Megabyte/64K	64K/256	64K/NONE	64K/256
Multi & co-processing	YES (with 8087, 8089)	NO	NO	NO
PASCAL, PL/M & FORTRAN	YES	NO	NO	YES
ICE symbolic debugging	YES	NO	NO	YES

the kind only Intel delivers today. Software that produces object code directly and gives you important extensions that allow you to fine-tune the software to your application.

Software such as PASCAL-88, the block-structured application language rapidly becoming the one most widely used. With our PASCAL-88, you can do direct port I/O and interrupt handling, as well as independent program module compilation. And produce code that runs faster than other, P-code interpreter versions.

Along with PASCAL-88, you get PL/M-88, our systems implementation language, our ANSI-compatible FORTRAN, and our ASM-88 macroassembler. So with more software capability than you've ever had before, now you

can choose the right language tool for each application—whatever it calls for.

Get out in front with complete development support

All the development support tools you need are ready to go today from Intel. Start with the Intellec® Microcomputer Development System. Add to that our ICE-88™ in-circuit emulator. Together they give you CPU emulation in real time, plus features like symbolic debugging, diagnostic commands and program trace capability. With these tools you'll get your products to market faster than by any other route.

Looking down the road

Best of all, with the iAPX 88, your investment in today's solution is protected. Since the 8088 is 100% object-code compatible with the 16-bit 8086—plus its future generations, the iAPX 186 and iAPX 286—you have the industry's only guaranteed headstart on the path to the future. Regardless of which language you're writing in.

So if you want to outdistance the pack, choose the iAPX 88—available today from your local Intel distributor. To get your copy of benchmark results, contact your local Intel sales office or distributor. For more information write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

*Benchmark studies were used comparing Intel's iAPX 88 with Motorola's MC68B09 and Zilog's Z-80B.

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feature I/O control functions. Products of Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, these cards expand I/O capabilities beyond those of the company's HP-IB interface, which implements the IEEE 488-1978 standard. All interface cards require installation of a ROM drawer and I/O ROM in the HP-85. The I/O ROM provides BASIC commands to access card capabilities. It snaps into a ROM drawer which plugs into the HP-85.

HP 82939A serial interface provides true full-duplex RS-232-C and 20-mA current loop communications at data rates of 50 to 9600 bits/s. Data formats available are 5, 6, 7, or 8 bits/character and 1 or 2 stop bits. Odd, even, one, zero, or no parity operation is selectable and a 1-bit switch enables or disables automatic handshaking on modem control lines. Two 20-mA sources are included. Interrupt response capabilities are break, framing or parity error, received data available, auto disconnect, and change of modem line configurations.

Circle 328 on Inquiry Card

Microcomputer Systems Expand Commercial Systems Family

Two microcomputer systems, consisting of entry level CS/10 models and full-feature CS/70 models, run an interactive version of ANSI-74 COBOL. Products of Data General Corp, Rte 9, Westboro, MA 01581, the systems can operate in order entry processing, inventory control, and general accounting applications, and are additions to the company's commercial systems family.

In the CS/10 system, two models are offered. Mod C1 has 64k bytes of MOS memory, one display terminal, and a choice of 2.4M-byte storage diskette system, or 12.5M- or 25M-byte Winchester disc with integral diskette. Hardcopy options include 60- or 180-char/s matrix printers, 55-char/s letter quality printer, or 300-line/min printer. The CS/10 Mod C3 has 128k bytes of MOS memory and can support up to three additional displays and two 25M-byte disc subsystems.

CS/70 system also offers two models. Mod C5 with 256k-byte MOS memory supports up to nine display terminals and up to four 20M-byte cartridge discs. Mod C6 has 512k bytes of MOS memory, and can support 17 display terminals and up to 250M bytes of disc storage. Both models support two system printers with speeds from 180 char/s to 900 lines/min, and both have optional 300-bit/in or dual-mode 800/1600-bit/in magnetic tape subsystems.

Circle 329 on Inquiry Card

Z80 Based Microcomputer, Expansion Cards Are Multibus Compatible

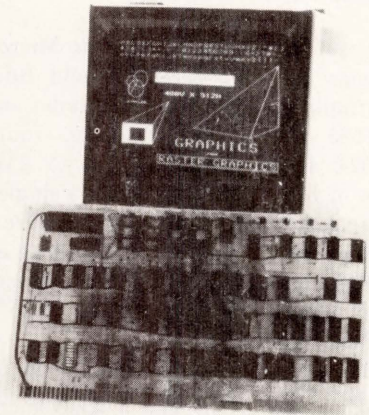
The MLZ-90 (2 MHz) and MLZ-90A (4 MHz) microcomputers and system expansion cards, from Heurikon Corp, 3001 Latham Dr, Madison, WI 53713, contain logic for the expanded Intel 20-bit SBC-80 Multibus. Z80 based, the MLZ-90 is a complete microcomputer system on a 6.75 x 12" (17.1 x 29.4-cm) 4-layer printed circuit card. An oncard floppy disc drive controller can regulate up to 16 single- or double-density drives with a direct interface to Shugart 801 and 850/851 drives. One ROM socket and eight ROM/RAM sockets will accommodate a variety of ROM and Mostek's byte wide RAM family.

Each of the nine memory sockets can contain up to 8192 bytes of storage. Write protection is provided by software control for all oncard RAM or ROM. Compatible memory types are Intel 2716, 2732, and 2764 (or equivalent) EPROM and Mostek 4118, 4801, 4816, 4802, and 4864 (or equivalent) byte wide RAM.

Memory addressing is software controlled by a memory mapping RAM which allows dynamic memory bank switching, greatly easing implementation of multitasking systems. Blocks of 4k bytes or more within 1M byte of off-card memory or 73k bytes of oncard memory may be relocated to any logical 4k-byte CPU address. Power-on jump is implemented using memory mapping logic. Jumpers are provided to enable users to select a variety of wait state conditions for oncard memory if slow memory devices are being used.

Circle 330 on Inquiry Card

Multibus Vector Generator Board Creates Text and Graphics



The RG-SBC-VG3 vector generator is designed for Multibus applications. Accepting high level commands from the system processor via the Multibus to draw vectors, circles, ASCII characters, graphic shapes, and fill and erase rectangles, it controls instructions such as jump, call, and repeat.

Point to point draw is provided allowing the user to specify end points of a line or to specify a string of coordinates which define a shape to be drawn. ASCII characters are generated from the ASCII code and may be specified as a string following the display ASCII opcode.

The vector generator, manufactured by Raster Graphics, PO Box 23334, Tigard, OR 97223, includes an 8085 microprocessor, 8k/16k of P/ROM address space, a hardware vector generator, and a 2k dual-port RAM to receive instructions from the Multibus system processor. The Multibus system processor acquires control of the dual-port RAM by issuing an I/O instruction to a user selected I/O page, and returns control to the vector generator when the dual-port RAM has been loaded.

Dual-port RAM resides in a user selected 4k address block of the Multibus system processor's address space as it is being updated by the processor. RAM and ROM inhibit signals are provided to allow the dual-port RAM to temporarily override system memory existing at the same address when the RAM is being updated.

Circle 331 on Inquiry Card

LSI-11/23 Based Computer Supports Floppy and Winchester Storage

Disc system 11X from Scientific Micro Systems Inc, 777 E Middlefield Rd, Mountain View, CA 94043, includes an LSI-11/23 CPU, 128k-byte RAM, four RS-232-C serial ports, and up to 2M bytes of floppy disc storage in a single 10.5" (26.7-cm) tabletop enclosure. Storage can be expanded by adding a 26.4M-byte 14" (36-cm) Winchester drive option in a matching 5.25" (13.3-cm) enclosure.

The disc system is compatible with the RT-11 and RSX-11M DEC operating systems. Adding dual-head floppies doubles the storage normally available when running the RT-11 operating system with DEC RX02 diskettes. 40% faster disc access improves performance.

A proprietary "Flinchester" controller is included to interface between the LSI-11 Q-Bus and both floppy and Winchester discs. Two modes of operation are possible. The compatible mode provides complete DEC RX02 hardware, software, and media compatibility. Standard DEC software will run without modification to device handlers. To access the Winchester disc and IBM compatible floppy discs, the controller employs an extended mode with appropriate device handler. Device handlers are available for RT-11 and RSX-11M operating systems.

Circle 332 on Inquiry Card

64k Tabletop Computer Includes High Speed 32M-Byte Disc

The 64k SD-700 computer system, manufactured by SD Systems, 3401 Kingsley, Garland, TX 75041, includes a 32M-byte fixed/removable disc with 30-ms average access time and 55-ms maximum access time. This disc expands to 96M bytes max. In multiuser configurations, the system supports up to five users with user partitions of 48k and a 16k-operating system with 256k maximum memory capacity.

The standard configuration provides two Z80 central microprocessors operating at a 4-MHz CPU speed and two I/O ports. Included with the system, the communications oriented multiuser operating system (COSMOS) supports CP/M compatibility, COBOL, MBASIC, CBASIC, and other compilers, as well as individual and shared files for multiuser applications.

Circle 333 on Inquiry Card

Miniature DPM Provides Microprocessor Data Bus Compatible Outputs



Circuitry required for direct 3-state gateable BCD data output, compatible with most 4-, 8-, 12-, or 16-bit microprocessors, is included in the 4½-digit DM-4100D DPM. Measuring 2.53 x 3.25 x 0.94" (6.43 x 8.26 x 2.39 cm), the 0.3" (0.762-cm) LED display indicates analog voltages from -1.9999 to 1.9999 Vdc. It is a product of Datal-Intersil, 11 Cabot Blvd, Mansfield, MA 02048.

BCD data outputs are 3-state gated out in 4-bit groups permitting compatibility with multiple-data bus widths. Impedance presented for single-ended analog inputs is 1000 MΩ with 5-pA bias current.

The meter is auto zeroed on each conversion cycle to reduce drift. An externally accessible reference voltage is provided to minimize error due to voltage drift in ratiometric or bridge type applications; blank circuit pads accept input attenuation resistors or current shunts. Temperature drift of the auto zeroed input amplifier is ± 1 count from 0 to 50 °C. Temperature drift of gain measures ± 50 ppm of FSR/°C (typ) and ± 100 ppm of FSR/°C max. Input to output conversion linearity is $\pm 0.02\%$ of reading, or ± 2 counts.

Circle 334 on Inquiry Card

Desktop Microcomputer Includes Built-in Impact Printer

Based on a 6809 microprocessor, the TX series includes built-in 26-col alphanumeric printer, 20-col alphanumeric display, and modem with RS-232-C ports. The units weigh 15 lb (6.8 kg) and are about the size of a portable typewriter. Included is extended BASIC and assembly language support.

Three models are available from Canon Inc, Systems Div, 10 Nevada Dr, Lake Success, NY 11042, with memory capabilities of 15k to 31k bytes. TX-25 is programmable with full typewriter keyboard and built-in microfloppy disc drive. TX-10 and TX-15 are nonprogrammable models, the TX-15 incorporating full typewriter keyboard while the TX-10 uses 26 labeled keys and a 10-key pad.

Circle 335 on Inquiry Card

Memory Card for EXORcisor Bus Incorporates Versatile Addressing

A memory card for EXORcisor bus microcomputer systems accommodates 32k or 64k of EPROM and allows a mix of triple- or single-supply devices throughout the 64k memory map. Each device is independently addressable on 2k or 4k boundaries with wirewrap jumpers. The EPROM memory can be divided into two separate blocks of eight devices with each block configured for a different type of EPROM (TMS2716, INT2716, and INT2732). 2k and 4k devices can be used together. The board accommodates 4k of 2114 static RAM and is addressable in 2k blocks throughout the memory map.

The EPROM/RAM board is available from TAK Components, 1307 N Carolan Ave, Burlingame, CA 99010. Measuring 6.06 x 9.75 x 0.062" (15.4 x 24.8 x 0.16 cm), the board can hold noncontiguous memory locations without wasting memory space. It operates at 1 to 2 MHz on a standard Motorola EXORcisor/Micromodule bus and is 6800, 6801, 6802, 6809, and 650X compatible.

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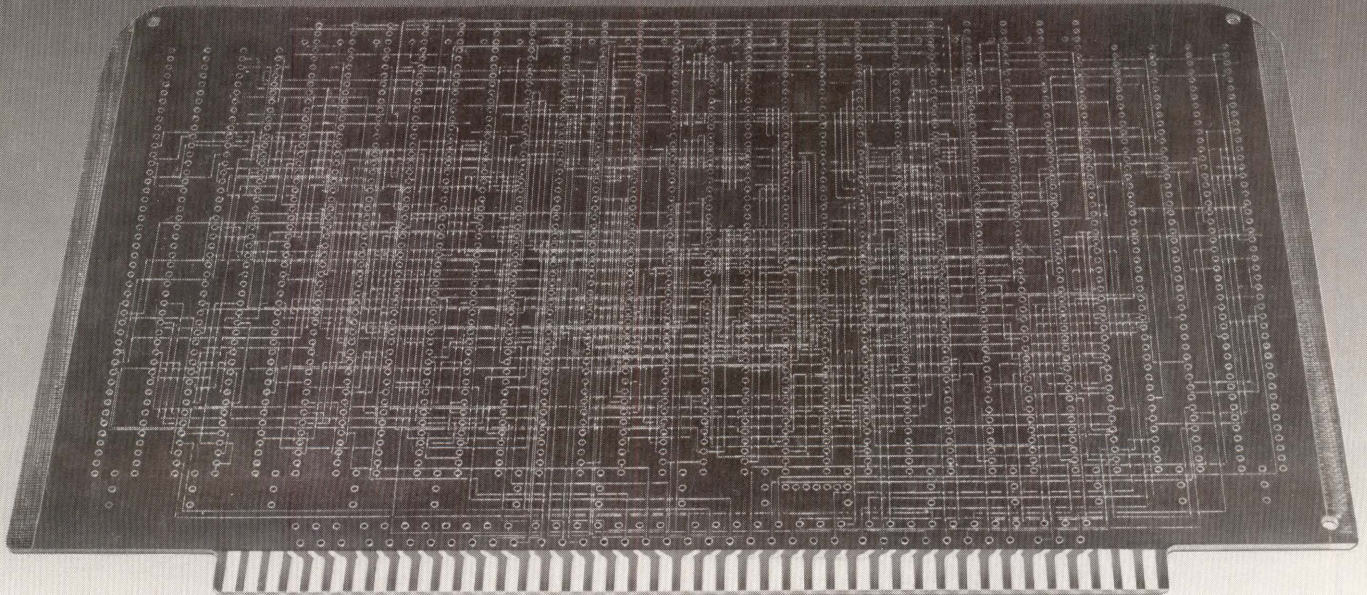
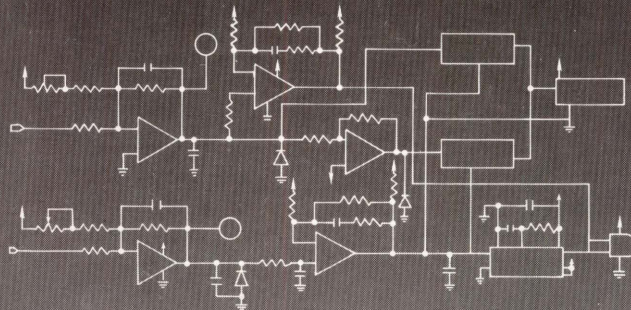
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**CIRCLE 118 ON
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Video Display Controller Card Plugs Into STD-BUS

Claimed to be the only fully programmable plug-in alphanumeric display controller card on the STD-BUS, the STD-ALPHA can display popular formats including 25 lines x 80 char, 24 x 80, 20 x 64, and 16 x 32. Other display formats having up to 128 characters per line or 44 lines per page (to a maximum of 2048 characters) can be obtained by replacing the onboard timing crystal with another of the appropriate frequency. Four character heights are available display.

The character set consists of 96 upper/lower-case alphanumeric ASCII characters and 32 graphics symbols. When user defined characters or symbols are required, the existing

character generator can be replaced with a custom programmed 2716 EPROM.

Depending on the display format selected, the card uses 1k or 2k bytes of memory address space; each character position on the CRT screen corresponds to a location in the display memory. When a character is to be displayed, its ASCII and attribute codes (normal, inverse or blinking) are written into the appropriate memory location. A cursor can be positioned anywhere on the display. With transparent memory, no glitches or snow appear on the display regardless of the rate at which the CPU writes to display memory.

This 4.48 x 6.50" (11.4 x 16.5 cm) card has a single 5-V power supply requirement. Outputs will drive any standard data display monitor having com-

posite video or direct drive inputs. American or European TV standard is selectable. The display controller card, along with a complete high speed lightpen interface, is available from Matrox Electronic Systems Ltd, 5800 Andover Ave, T.M.R. Quebec H4T 1H4, Canada.

Circle 337 on Inquiry Card

Interface for Microcomputer Drives Parallel ASCII Printer

A printed circuit board interface allows the Atari 400 or 800 to drive a parallel ASCII printer directly. Once a 15-s machine language program is loaded from cassette, all printed data are directed to the parallel printer interface instead of the serial port. For example, LIST"P:" will list a basic program on the printer; LPRINT in a basic program will direct output to the printer, and LIST#P will output assembler source listings on the printer. The program will remain in memory until the computer power is turned off.

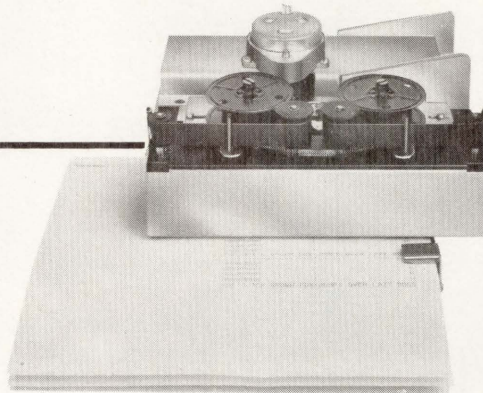
A disc booting version is included on the same cassette. DOS is modified by transferring the program from cassette to disc. From then on, each time DOS is booted, the parallel printer driver boots in. Disc system interface software is essentially invisible to the user.

The interface will drive most 7-bit ASCII parallel printers with handshaking (data strobe and busy signals). Connectors are available for popular printers, giving "plug-in" installation. Connection to almost any other parallel printer is possible.

Two versions of the parallel printer interface are available. The A4P fits the Atari 400 and the A8P fits the Atari 800. Both interfaces are manufactured by Macrotronics, Inc, 1125 N Golden State Blvd, Turlock, CA 95380.

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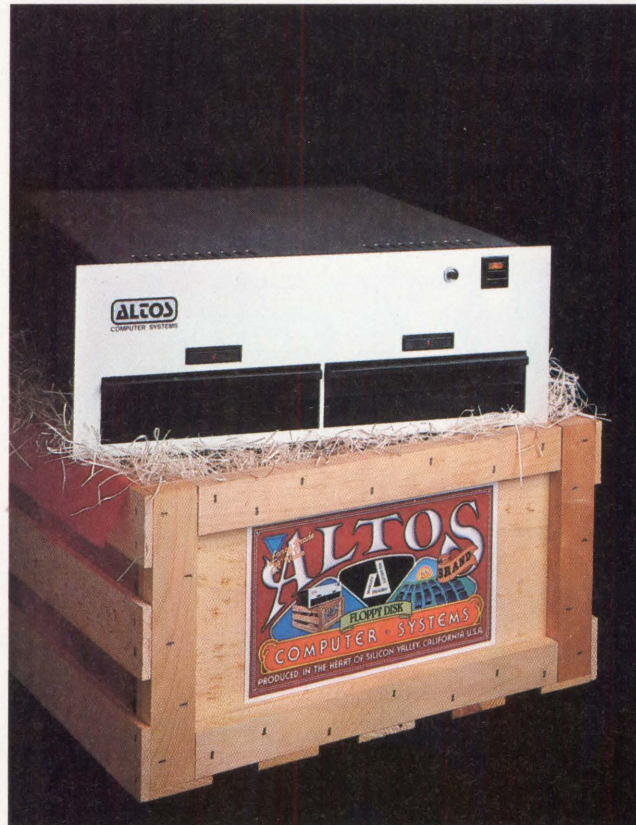
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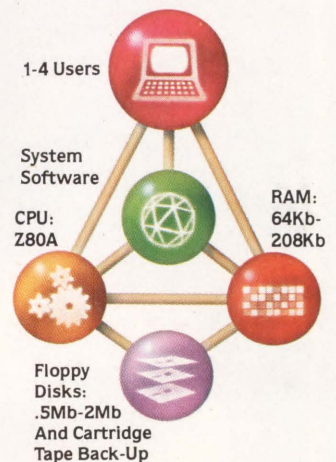


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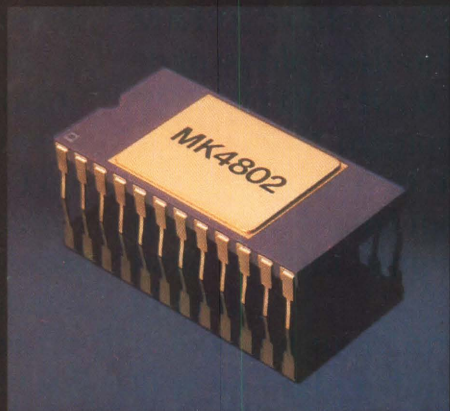
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16K

Static

CIRCLE 190 ON INQUIRY CARD

DS BRIEFS

LSI-11 Add-In Memory Detects and Corrects Single-Bit Errors—From 32k to 256k of memory, in 32k increments, with error checking and correcting is provided on the model MEccV11 from PEBX Inc, 501 D Vandell Way, Campbell, CA 95008. An LED error display flags RAMs with error conditions. The memory unit includes a controller, one or two array boards, and a 12-V battery backup for power outage protection. Circle 339 on Inquiry Card.

Multiprocessor System Adds Users with Single Cards—Built around a Z80A processor, the 1000-MP supports up to four Winchester 8" (20-cm) hard discs with 96M-byte storage, and file backup on cartridge tape drive. Announced by Computer Services Systems Network, 120 Boylston St, Boston, MA 02116, the expandable multiprocessor microsystem can accommodate up to 16 users on an S-100 bus. Circle 340 on Inquiry Card.

Advanced TRS-80 Level II Applications Covered in Interfacing Book—*TRS-80 Interfacing, Book 2*, by Jonathan A. Titus, Christopher A. Titus, and David G. Larsen, extends the interfacing techniques presented in Book 1 to include advanced applications of the TRS-80 level II. Using the TRS-80 breadboard developed by the authors, the reader is shown how to use the computer to drive loads with open collector chips, triacs, solid state relays, and other interface circuits. Available from Group Technology Ltd, PO Box 87, Check, VA 24072. Circle 341 on Inquiry Card.

Interface, Arithmetic Processing, and Clock Options for Microcomputer—Options for the Z80 based System 10, from GNAT Computers Inc, 7895 Convoy Court, Bldg 6, San Diego, CA 92111, add speed and flexibility. For high speed arithmetic calculations AM9511 or AM9512 arithmetic processing unit options are offered. Interface to the instrumentation world is made possible by the IEEE 488 general purpose interface bus. Circle 342 on Inquiry Card.

Timer/Counter Card Is STD BUS Compatible—A product of Circuits and Systems, Inc, 2 Main St, Hollis, NH 03049, the CS7650 series timer/counter and I/O card includes three software programmable 16-bit timer/counters and four 8-bit parallel I/O ports that can be used for input, output, or output with readback. Ports are hardware programmable. Circle 343 on Inquiry Card.

Microcomputer System Features Multiprocessor/Multiuser Architecture—Produced by Action Computer Enterprise, Inc, 75 W Green St, Pasadena, CA 91105, Discovery multiprocessor system uses independent Z80/8080 CPUs and up to 64k bytes for each user. Communication with up to 100 user processors is possible, each running independent CP/M programs. Circle 344 on Inquiry Card.

IEEE 488/Parallel Interface Enhances PET/CBM Flexibility—PIE-C permits use of Centronics or other parallel-input ASCII printers with PET/CBM computers. Included in the device from LemData Products, PO Box 1080, Columbia, MD 21044, are switch selectable conversion of nonstandard PET/CBM code to true ASCII and IEEE 488 primary address response capability. Circle 345 on Inquiry Card.

Expandable Dynamic RAM Board Meets S-100 Standards—dynamic RAM board conforming to the proposed IEEE S-100 bus standards is compatible with most S-100 systems. Model 2065 from California Computer Systems, 250 Caribbean Dr, Sunnyvale, CA 94086, is fast enough to require no wait states with a 4-MHz CPU. The bank selection system allows software enabling of a bank and memory expansion to 512k. Circle 346 on Inquiry Card.

Electrical Isolator Also Eliminates Equipment Interactions—Super Isolator is designed to control ac power line spikes, surges, noises, and hash, and to eliminate equipment interactions. It can accommodate an 1875-W load and each of the three individually dual-Pi filtered 3-prong ac sockets can handle 1000 W. Available from Electronic Specialists, Inc, 171 S Main St, Natick, MA 01760. Circle 347 on Inquiry Card.

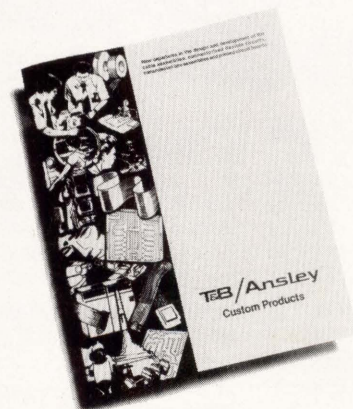
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SOFTWARE

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Modular Storage**

A compact Winchester system for the Q-bus provides 21M to 280M bytes of formatted storage to users of the LSI-11/2 and LSI-11/23. Designed around an 8" (20-cm) drive assembly, the interface electronics and microcomputer form factor allow users to easily add storage in 35- or 70M-byte increments. This modularity allows system growth without drastic increases in hardware and software complexity, since interfacing for all levels of storage is handled by one dual-height card in the computer backplane.

From Peritek Corp., Computer Technology Div, 3014 Lakeshore Ave, Oakland, CA 94610, the WINRS-11 F series floppy disc storage is integrated with the Winchester assembly to provide removable media for backup or transport needs.

R-series storage units are also available which provide fully redundant systems in a single enclosure. In 42M- and 70M-byte versions, these units comprise two independent storage systems in one package that includes two separate dual-height interface cards. The single, dual-height interface card contains a built-in bootstrap for 'hands-off' operation.

Circle 348 on Inquiry Card

**Portable Operating System
Places UNIX Software
On 16-Bit Microprocessors**

The full Version 7 UNIX operating system from Bell Laboratories has been modified by Microsoft, 10800 NE Eight, Suite 819, Bellevue, WA 98004, to run on advanced microcomputers including the 8086, Z8000, and M68000, as well as the PDP-11 series. All of Microsoft's existing system software including COBOL, Pascal, BASIC, and DBMS will be adapted to run under the XENIX system and software written for the UNIX operating system will also be

compatible. Library programs include a C compiler and several other high level languages, software development tools, function libraries, editors, text formatters, and other utilities.

Interactive, multiuser, multitasking design incorporates a tree structured directory hierarchy of files in mountable file systems, which allows identical handling of files, directories, and devices. XENIX also supports tree structured process hierarchies, providing simple system calls for a process to create offspring processes that then run in parallel. To support multitasking, there are interprocess communication features in the form of pipes, multiplexed pipes, and asynchronous software interrupts. Typical of the design philosophy is the interchangeability of the program elements. Files, devices, and interprocess pipes are read and written with identical system calls, and applications encompass several small general purpose tasks instead of one large special purpose task.

Circle 349 on Inquiry Card

**Pascal Compiler Expands
Programming Support**

A Pascal compiler for the iAPX-88/86 8-bit and 16-bit family of microprocessors will run on Intellec series III or any existing Intellec microcomputer development system (series II or model 800) with the model 556 upgrade package. Relocatable machine code is produced directly from a programmer's high level, English-like source code. Object code can be linked with other Pascal-88/86 object files, or the object files produced by PL/M-88/86 or ASM86.

The compiler, from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, is an integral part of the manufacturer's iAPX-88/86 support software. Modules compiled with Pascal-88/86 can be combined with other Pascal modules or with PL/M-88/86 or ASM86 modules by using the LINK86 and LOC86 system programs. These modules can be debugged with ICE-86 emulators and executed either on the series III or on an iSBC 86/12 board with RMX-86.

Pascal-86 programs outside the development system environment can be executed easily using the runtime support system. Programs compiled by the Pascal-88/86 compiler can be run on

any 8086/8087/8088/8089 system, provided that the operating system entry points required by the runtime system are linked in. These entries are part of the Series III operating system and the RMX-86 realtime executive. Pascal programs can be run under other operating systems when entry points required by the runtime system are supplied.

As implemented in the iAPX 86/20, the Realmath standard is supported by the inclusion of predefined data types and functions. Code produced by the Pascal-88/86 compiler can be executed on the iAPX 86/20 processor or on an iAPX-88/86 software emulator.

Circle 350 on Inquiry Card

**Analog and Digital
I/O Software For
DEC RT-11**

An analog and digital I/O subroutine software package that requires no knowledge of machine language has been released by ADAC, 70 Tower Office Pk, Woburn, MA 01801, to support their line of analog and digital I/O boards for use with DEC's RT-11 FORTRAN/BASIC operating system software for the LSI-11, -11/2, and -11/23 microcomputer series. The ADLIB package gives the user flexible realtime data acquisition and control software. It supports analog high level, low level and thermocouple inputs at high throughput rates.

Analog routines allow the user to select sequential or random access channels, programmable gain amplifier settings, internal or external triggering, and other parameters. Digital inputs and outputs, realtime clock functions, pulse counting and generation, applications requiring voltage or current loop outputs as well as the company's multiple interrupt controller are supported. The software will operate in a single job or a foreground/background environment and runs under program control, program interrupt, or in the direct memory access mode. The software package includes a user's manual with complete description of the various routines. Also included is the distribution media, a floppy diskette (RX01 or RX02 compatible) containing the source code, object code, and other library file information. □

Circle 351 on Inquiry Card

MNOS Devices Provide Flexibility in Nonvolatile Logic

Bob Greenwood

Plessey Semiconductors

1674 McGaw Ave, Irvine, CA 92714

One of the major difficulties facing the designer of digital systems is the loss of current data on the interruption of power. Traditionally, the problem has been overcome by using a CMOS memory and a battery, a solution that introduces problems associated with cost, size, weight, and shelf life of batteries. A more effective solution for many applications is the use of nonvolatile logic devices produced on a metal nitride oxide silicon process.

The metal nitride oxide silicon (MNOS) process is essentially a P-channel metal gate MOS process, with the additional feature that the nonvolatile memory transistors with electrically alterable threshold voltages can be fabricated on the same chip alongside conventional fixed threshold transistors. The MNOS memory transistors, therefore, enable nonvolatile data storage to be incorporated into standard MOS type circuits.

An MNOS memory transistor has a sandwich structure gate dielectric consisting of a very thin layer of silicon oxide under a thicker layer of silicon nitride (Fig 1). By applying suitable voltages to the terminals of the transistor, it is possible to inject a charge through the thin oxide layer. This charge subsequently becomes trapped at the oxide/

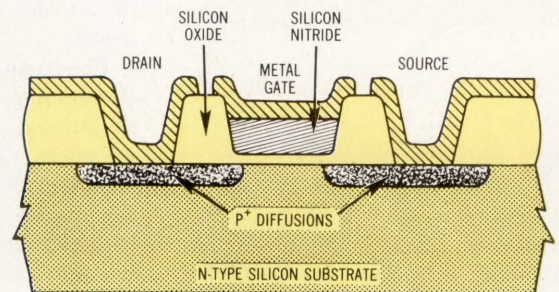


Fig 1 Simplified cross section of MNOS memory cell. Ability of MNOS transistors to be fabricated alongside fixed threshold transistors allows non-volatile storage to be incorporated into MOS circuits

ROMs

MOS STATIC ROMs (+ 5 Volts)

Character Generators³

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × (7 × 5)	MCM6670P	350	18
128 × (7 × 5)	MCM6674P	350	18
128 × (9 × 7)	MCM66700P	350	24
128 × (9 × 7)	MCM66710P	350	24
128 × (9 × 7)	MCM66714P	350	24
128 × (9 × 7)	MCM66720P	350	24
128 × (9 × 7)	MCM66730P	350	24
128 × (9 × 7)	MCM66734P	350	24
128 × (9 × 7)	MCM66740P	350	24
128 × (9 × 7)	MCM66750P	350	24
128 × (9 × 7)	MCM66760P	350	24
128 × (9 × 7)	MCM66770P	350	24
128 × (9 × 7)	MCM66780P	350	24
128 × (9 × 7)	MCM66790P	350	24

Binary ROMs (+ 5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
1024 × 8	MCM68A308P	350	24
1024 × 8	MCM68A308P7	350	24
1024 × 8	MCM68B308P	250	24
2048 × 8	MCM68A316AP	350	24
2048 × 8	MCM68A316EP	350	24
2048 × 8	MCM68A316P91	350	24
4096 × 8	MCM68A332P	350	24
4096 × 8	MCM68A332P2	350	24
8192 × 8	MCM68A364P	350	24
8192 × 8	MCM68A364P3	350	24
8192 × 8	MCM68B364P	250	24
8192 × 8	MCM68365P25	250	24
8192 × 8	MCM68365P35	350	24
8192 × 8	MCM68366P25	250	24
8192 × 8	MCM68366P35	350	24

CMOS ROMs (+ 5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 4	MCM14524	1200	16
2048 × 8	MCM65516C43	430	18
2048 × 8	MCM65516C55	550	18

Not all package options are listed.

Operating temperature ranges:

MOS — 0°C to 70°C

CMOS — 0°C to 70°C

ECL — Consult individual data sheets

TTL — Military —55°C to +125°C, Commercial 0°C to 70°C

³Character generators include shifted and unshifted characters, ASCII, alpha-numeric control, math, Japanese, British, German, European and French symbols.

PROMs

ECL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
32 × 8	MCM10139	20	ECL output	16
256 × 4	MCM10149	25	ECL output	16

TTL PROMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
1024 × 8	MCM7680	70	Open Collector	24
1024 × 8	MCM7681	70	3-State	24
2048 × 4	MCM7684	70	Open Collector	18
2048 × 4	MCM7685	70	3-State	18
2048 × 4	MCM7686	70	Open Collector with Latches	20
2048 × 4	MCM7687	70	3-State with Latches	20
2048 × 4	MCM7688	—	Open Collector with Registers	20
2048 × 4	MCM7689	—	3-State with Registers	20
1K × 8	MCM76LS81	175	3-State	24
1K × 8	MCM82708	70	3-State	24

MOTOROLA MEMORIES

Motorola has developed a very broad range of reliable MOS and bipolar memories for virtually any digital data processing system application. And for those whose requirements go beyond individual components, Motorola also supplies Memory Systems and Micromodules.

New Motorola memories are being introduced continually. **This selector guide lists all those available as of October 1980.** For later releases, additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

Data sheets may be obtained from your in-plant VSMF Data Center, distributors, Motorola sales offices or by writing to:

Literature Distribution Center

Motorola Semiconductor Products Inc.

P.O. Box 20912

Phoenix, AZ 85036.

MOTOROLA MEMORIES Selector Guide

RAMs ROMs PROMs EPROMs EEPROM

October 1980



MOTOROLA



RAMs

MOS DYNAMIC RAMs

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
4096 × 1	MCM4027AC-2	150	+12, ±5 V	16
4096 × 1	MCM4027AC-3	200	+12, ±5 V	16
4096 × 1	MCM4027AC-4	250	+12, ±5 V	16
16384 × 1	MCM4116BC15	150	+12, ±5 V	16
16384 × 1	MCM4116BC20	200	+12, ±5 V	16
16384 × 1	MCM4116BC25	250	+12, ±5 V	16
16384 × 1	MCM4116BC30	300	+12, ±5 V	16
16384 × 1	MCM4516C12* ¹	120	+5 V	16
16384 × 1	MCM4516C15* ¹	150	+5 V	16
16384 × 1	MCM4516C20* ¹	200	+5 V	16
16384 × 1	MCM4517C12	120	+5 V	16
16384 × 1	MCM4517C15	150	+5 V	16
16384 × 1	MCM4517C20	200	+5 V	16
32768 × 1	MCM4132L15	150	+12, ±5 V	18
32768 × 1	MCM4132L20	200	+12, ±5 V	18
32768 × 1	MCM4132L25	250	+12, ±5 V	18
32768 × 1	MCM4132L30	300	+12, ±5 V	18
32768 × 1	MCM6632L15 ¹	150	+5 V	16
32768 × 1	MCM6632L20 ¹	200	+5 V	16
32768 × 1	MCM6632L25 ¹	250	+5 V	16
32768 × 1	MCM6633L15	150	+5 V	16
32768 × 1	MCM6633L20	200	+5 V	16
32768 × 1	MCM6633L25	250	+5 V	16
65536 × 1	MCM6664L15 ¹	150	+5 V	16
65536 × 1	MCM6664L20 ¹	200	+5 V	16
65536 × 1	MCM6664L25 ¹	250	+5 V	16
65536 × 1	MCM6665L15	150	+5 V	16
65536 × 1	MCM6665L20	200	+5 V	16
65536 × 1	MCM6665L25	250	+5 V	16

TTL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
256 × 4	MCM93412	45	Open Collector	22
256 × 4	MCM93422	45	3-State	22
1024 × 1	MCM93415	45	Open Collector	16
1024 × 1	MCM93425	45	3-State	16

*To be introduced.

¹Motorola's innovative pin #1 refresh

²All MOS memory outputs are three-state except the open collector MCM2115A series.

MOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
128 × 8	MCM6810	450	24
128 × 8	MCM68A10	360	24
128 × 8	MCM68B10	250	24
1024 × 4	MCM2114P20	200	18
1024 × 4	MCM2114P25	250	18
1024 × 4	MCM2114P30	300	18
1024 × 4	MCM2114P45	450	18
1024 × 4	MCM2114P70	200	18
1024 × 4	MCM2114P25	250	18
1024 × 4	MCM2114P30	300	18
1024 × 4	MCM2114P45	450	18
1024 × 1	MCM2115AC45 ²	45	16
1024 × 1	MCM2115AC55 ²	55	16
1024 × 1	MCM2115AC70 ²	70	16
1024 × 1	MCM2115AC45 ²	45	16
1024 × 1	MCM2115AC70 ²	70	16
1024 × 1	MCM2125AC45	45	16
1024 × 1	MCM2125AC55	55	16
1024 × 1	MCM2125AC70	70	16
1024 × 1	MCM2125AC45	45	16
1024 × 1	MCM2125AC70	70	16
4096 × 1	MCM2147C55	55	18
4096 × 1	MCM2147C70	70	18
4096 × 1	MCM2147C85	85	18
1024 × 4	MCM2148C55*	55	18
1024 × 4	MCM2148C70*	70	18
1024 × 4	MCM2148C85*	85	18
1024 × 4	MCM2149C55*	55	18
1024 × 4	MCM2149C70*	70	18
1024 × 4	MCM2149C85*	85	18

CMOS STATIC RAMs (+5 Volts)

Organization	Part Number	Access Time (ns max)	No. of Pins
256 × 4	MCM5101P65	650	22
256 × 4	MCM5101P80	800	22
256 × 4	MCM51L01P45	450	22
256 × 4	MCM51L01P65	650	22
1024 × 1	MCM6508C30	300	16
1024 × 1	MCM6508C40	460	16
1024 × 1	MCM6518C30	300	18
1024 × 1	MCM6518C46	460	18

ECL BIPOLAR RAMs

Organization	Part Number	Access Time (ns max)	Output	No. of Pins
8 × 2	MCM10143	15	ECL output	24
256 × 1	MCM10144	26	ECL output	16
16 × 4	MCM10145	15	ECL output	16
1024 × 1	MCM10146	29	ECL output	16
128 × 1	MCM10147	15	ECL output	16
256 × 1	MCM10152	15	ECL output	16
256 × 4	MCM10422*	15	ECL output	24

EPROMs

MOS EPROMs

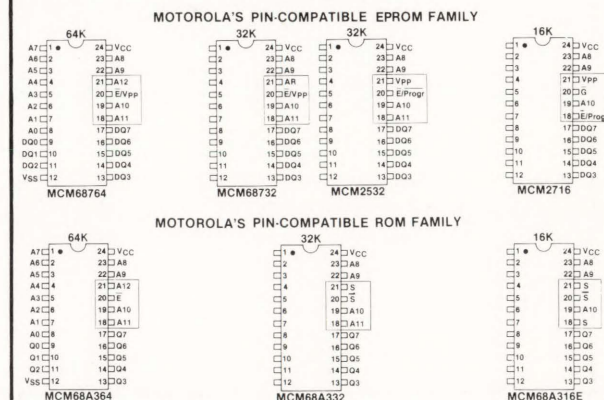
Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
1024 × 8	MCM2708C	450	+12, ±5 V	24
1024 × 8	MCM27A08C	300	+12, ±5 V	24
1024 × 8	MCM68708C	450	+12, ±5 V	24
1024 × 8	MCM68A708C	300	+12, ±5 V	24
2048 × 8	TMS2716C	450	+12, ±5 V	24
2048 × 8	TMS27A16C	300	+12, ±5 V	24
2048 × 8	MCM2716C	450	+5 V	24
2048 × 8	MCM2716C35	350	+5 V	24
2048 × 8	MCM27L16C	450	+5 V	24
2048 × 8	MCM27L16C35	350	+5 V	24
4096 × 8	MCM2532C	450	+5 V	24
4096 × 8	MCM2532C35	350	+5 V	24
4096 × 8	MCM25L32C	450	+5 V	24
4096 × 8	MCM25L32C35	350	+5 V	24
8192 × 8	MCM68764C	450	+5 V	24
8192 × 8	MCM68764C35	350	+5 V	24
8192 × 8	MCM68L764C	450	+5 V	24
8192 × 8	MCM68L764C35	350	+5 V	24
8192 × 8	MCM68766C	450	+5 V	24
8192 × 8	MCM68766C35	350	+5 V	24

EEPROM

MOS EEPROM

Organization	Part Number	Access Time (ns max)	Power Supplies	No. of Pins
16 × 16	MCM2801C*	10 μs	+5 V	14

EPROM/PROM COMPARISON



INDUSTRY STANDARD PINOUTS

nitride interface and modifies the threshold voltage of the transistor. Depending on the polarity of the injected charge, the threshold may be moved either to a low or high negative value.

Once the injected charge is trapped within the bulk of the gate dielectric, it is not affected by surface leakage, and the charge decays away only very slowly. It is, therefore, possible to distinguish between high and low threshold voltages for at least a year, in the absence of applied power, after they have been written, while retaining electrical alterability. All of this makes possible such varied applications as elapsed time metering for teleprinters and other types of devices, replacements for latching relays in all types of industrial equipment, electronic calculators and electronic games, automatic dialing devices for telephones, security systems such as electronic locks, and counters (automotive odometers, and text and measurement recorders).

One of the disadvantages of the MNOS transistor is the high voltage required across the transistor dielectric to inject the charge into the oxide/nitride interface traps. This has meant that programming pulses of 25 V or greater have had to be applied to the transistor. Bias considerations have precluded the use of MOS control logic for erase/write on the same chip.

However, the MN9000 series of nonvolatile (NOVOL) devices from Plessey Semiconductors (see Table) uses a modified form of erase and an internal dc-dc converter for generating high voltages. These characteristics have made it possible to include onchip sensing circuitry for retrieving data and drive circuitry for changing threshold voltage, while using standard MOS power supplies. Therefore, no additional external drive circuitry is required, and the transfer of data between the logic and the nonvolatile memory is achieved with simple control inputs using standard TTL/CMOS levels.

A 6-Decade Counter

A specific product will serve to illustrate the interaction between the logic and MNOS memory. The MN9106 (Fig 2) is a

6-decade up-counter in parallel with a 24-bit MNOS memory which can provide nonvolatile data storage of the current count status. An overflow latch and memory bit are also available to indicate a counter overflow condition. In addition to the conventional counter controls, recall and save inputs are provided to control the 2-way transfer of data between the counter and memory.

Output data are presented in the form of multiplexed 7-segment outputs and 6-digit strobes. The multiplexing sequence is controlled by an internal oscillator with a frequency that is either determined by a capacitor on the scan input or forced from an external source if control of the multiplexing sequence is required. Normal use of the device includes generating a $\overline{\text{save}}$ automatically on power-up. If the clock rate is sufficiently slow, however, a $\overline{\text{save}}$ could be generated every counter change.

Power-On/Power-Off Circuit

Systems that use NOVOL devices to provide nonvolatile data storage can be classified into two main operating modes. In one mode, data are transferred to and from the nonvolatile memory at times determined by the operating sequence of the system. Save and recall signals are generated, therefore, by logic or software that is an integral part of the whole system. The only additional requirement is to eliminate any unwanted save signals at power-on and power-off that could reduce the data retention time or possibly corrupt the stored data. Typical application areas in this operating mode include mainly those systems in which the data to be retained are changing relatively infrequently, such as in security code storage, programmable timers, and low frequency counting applications.

The second operating mode includes the majority of applications in which data are changing at relatively high frequencies. Nonvolatile memory is then used as a backup in the event of loss of power. Data are written into the nonvolatile memory only when power is removed from the system. When power is restored, the data are retrieved and

NOVOL Family Members

Type	Description	Supply Voltage	Features
MN9102	Quad Latch	5 V, - 12 V	Automatic data recall High impedance output state for multiplexed operation One year data retention at 70 °C
MN9105	4-Decade Up/Down-Counter	5 V, - 12 V	BCD outputs 250 kHz up/down counting Latched outputs facility One year data retention at 70 °C
MN9106	6-Decade Up-Counter (999999)	12 V	7-segment outputs
MN9107	6-Decade Timer (995959)	12 V	Full multiplexing
MN9108	6-Decade Timer (999959)	12 V	Counter overflow indicator 200-kHz count frequency One year data retention at 70 °C

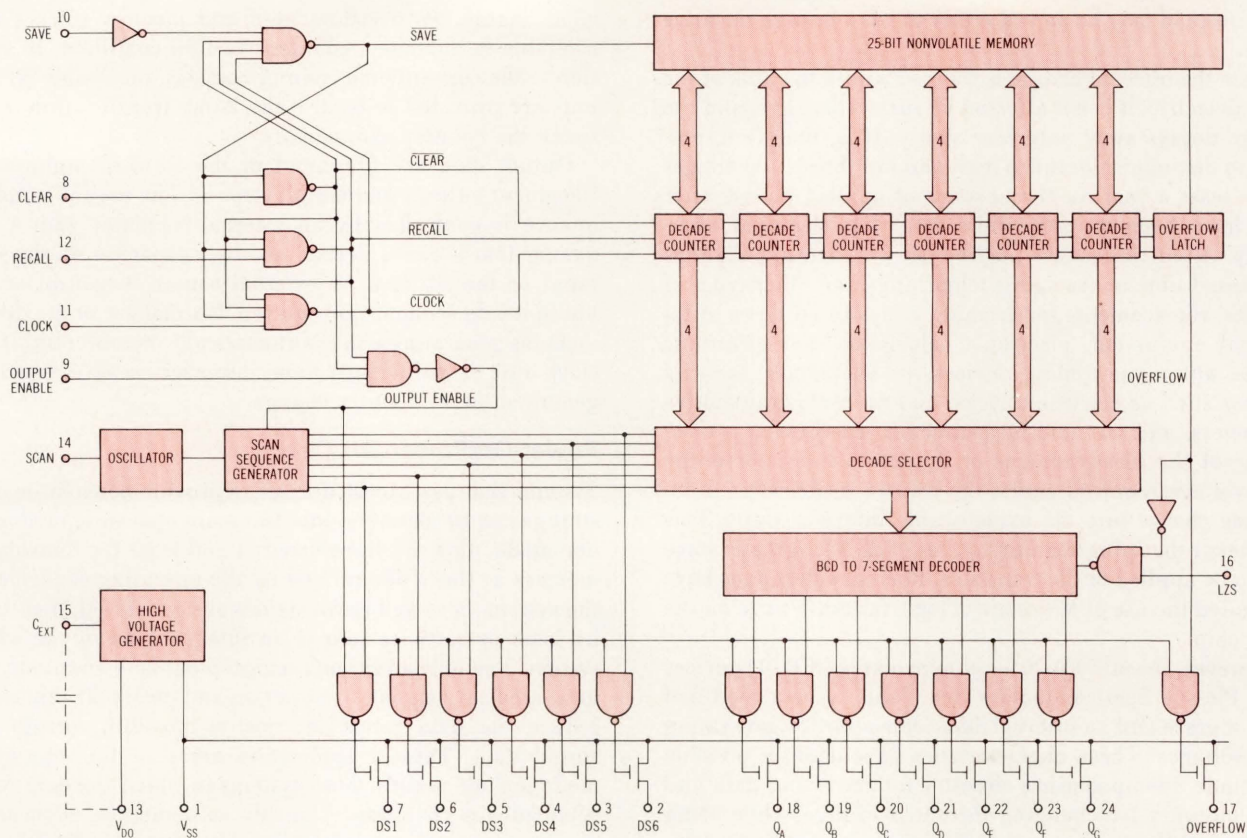


Fig 2 Nonvolatile data storage of count status. Function is provided by MN9106 from Plessey Semiconduc-

tors, which consists of 6-decade up-counter in parallel with 24-bit MNOS memory

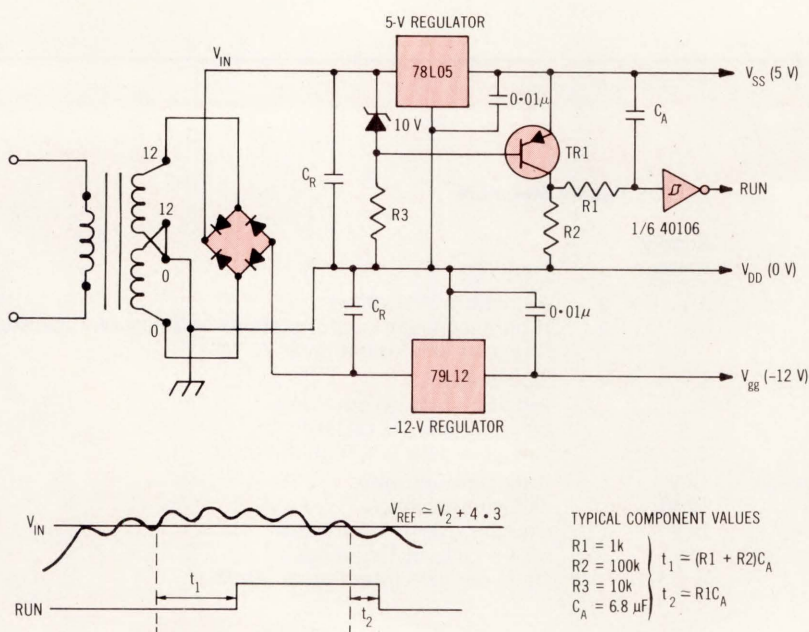


Fig 3 Power supply with power-on and power-off sensing circuitry. Voltage sensing is achieved by monitoring input to 5-V regulator

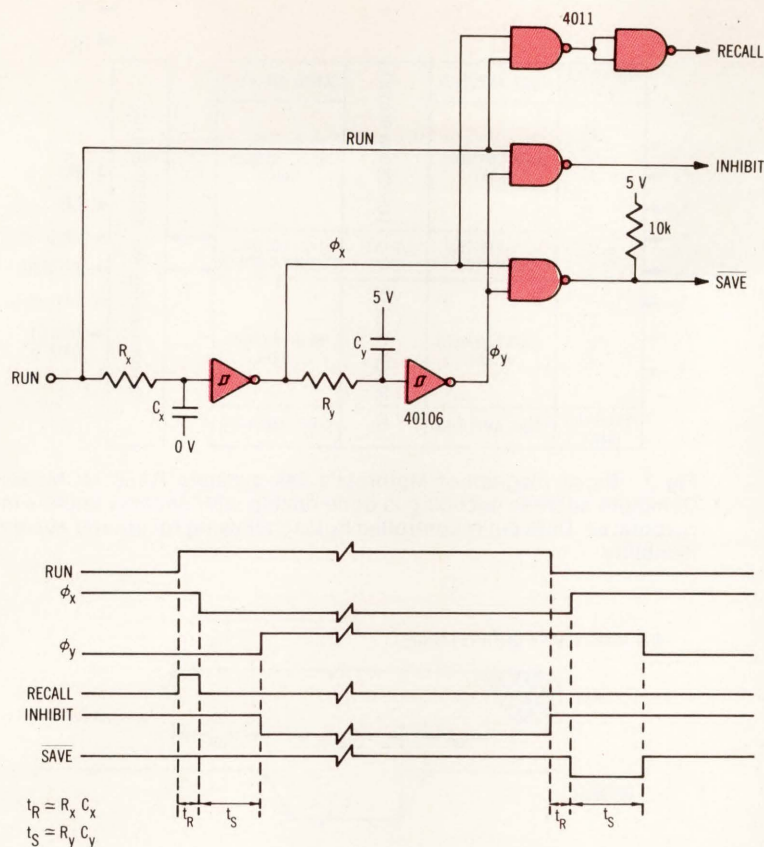


Fig 4 Power-on, power-off control. In conjunction with Fig 3 circuitry, this circuit provides control function for typical device of NOVOL family

the system then continues its normal operating sequence. Additional power supply sensing circuitry is, therefore, required to detect power-on and power-off conditions in order to generate the $\overline{\text{save}}$ and recall signals.

An example of a line powered 5- and -12-V supply with power-on and power-off sensing circuitry is shown in the circuit of Fig 3. Voltage sensing is achieved by monitoring the input to a 5-V regulator. When this voltage is less than V_{REF} (≈ 14.3 V), transistor TR1 is conducting, which holds the input of the Schmitt inverter close to V_{SS} and the output run signal remains low.

Once the input exceeds V_{REF} , sufficient voltage will be available for the 5-V supply to be within specification, and TR1 will be turned off. Provided this condition is maintained for a time period t_1 ($\approx [R1 + R2] C_A$), the input of the Schmitt inverter will have discharged to a sufficiently low level to take the run signal high, indicating a power-on condition. Time delay t_1 is included to give enough time for the high voltage levels within NOVOL devices to become fully charged.

Should the input voltage subsequently fall below V_{REF} , TR1 will turn on again and the input to the Schmitt inverter will charge through R1. After a time period t_2 ($\approx R1 \cdot C_A$), the run signal will return to a low level, indicating a power-off condition. The delay t_2 should generally be set longer than the time required to complete a recall command, although in certain applications it is permissible to set it to zero by removing R1.

A high level on the run signal gives a reliable indication that all power supplies are within specification and that high voltage levels are fully charged. The rising edge of the run signal can now be used to indicate a recall command

and the falling edge, a save command. Sufficient capacitance (C_R) should be included, however, to make certain that, when run returns to a low level, the output voltages will remain within specification until the save command is completed. Actual capacitance value will depend on the total current drain from the power supplies.

The save and recall signals can be generated from the run signal in a variety of ways, using delay circuits, monostables, or software design. Fig 4 illustrates a suitable delay circuit using Schmitt inverters which could be used with the above power sensing circuitry. Apart from the recall and $\overline{\text{save}}$ outputs, an inhibit signal is also provided which may be used to force the main system into a suitable state for recall and $\overline{\text{save}}$. In this particular example, it can be seen from the waveforms that a save command can occur only if ϕ_y is at a high level, which happens only after the recall command is finished. The minimum run period t_2 is, therefore, not needed, and R1 may be removed from Fig 3. Hysteresis of the Schmitt inverters is a requirement for maintaining minimum time periods t_R and t_S .

Conclusion

The MNOS devices provide logic with easily usable electrically programmable nonvolatile memory, capable of storing information for more than a year. Operating without external drive circuitry and characterized by simple TTL/CMOS compatible inputs, these devices find applications in both primary and backup memory roles. In applications that traditionally have used CMOS and a battery (or mechanical methods of nonvolatile storage), this technology should prove to be a cost-effective alternative.

64k Memory Heads 5-V Line of Dynamic RAMs

Based on HMOS N-channel silicon gate technology, and utilizing a single 5-V power supply, a family of dynamic RAMs from Motorola Semiconductors, 3501 Ed Bluestein Blvd, Austin, TX 78721, includes pin compatible 64k, 32k, and 16k devices. Multiplexing of row and column address inputs not only results in a requirement of eight address lines for each of these RAMs but also permits packaging in standard 16-pin dual inline packages.

The 65,536-bit memory, MCM6664, is organized as 64k x 1, with a refresh control function available on pin 1 to provide automatic and self-refresh modes. (See Fig 1.) Another 64k version, MCM6665, differs only in not providing the pin 1 refresh. Other characteristics shared by the two devices include 150-ns max access time from row address strobe, max power dissipation of 275 mW active and 30 mW on standby, 3-state data output, a 2-ms refresh of 128 cycles, and an early write common I/O capability. Complete address decoding is done onchip, with address latches incorporated. Refresh mode is RAS-only, while data out is controlled by CAS, allowing for greater system flexibility. (See Fig 2.) All inputs and outputs, including clocks, are fully TTL compatible.

Implemented on a 39,249-mil² (0.25-cm²) die, the RAMs utilize a folded bit line architecture, having 64 bits per line and a total of 512 sense amps. Benefits of folded bit lines include higher signal strength, noise insensitivity, and efficient access from data I/O to bit lines. Differential noise is further lowered through the use of array shielding. Bit line capacitance is lessened by reducing the number of cells per bit line, reducing capacitance per unit area using thick dielectric, and keeping bit lines physically short, not running across the column decoder.

Onchip back bias voltage generation is utilized to reduce bit line loading, increase data signal strength, and improve speed/power product. The back bias generator is powered up only during the active RAM cycle.

(continued on page 241)

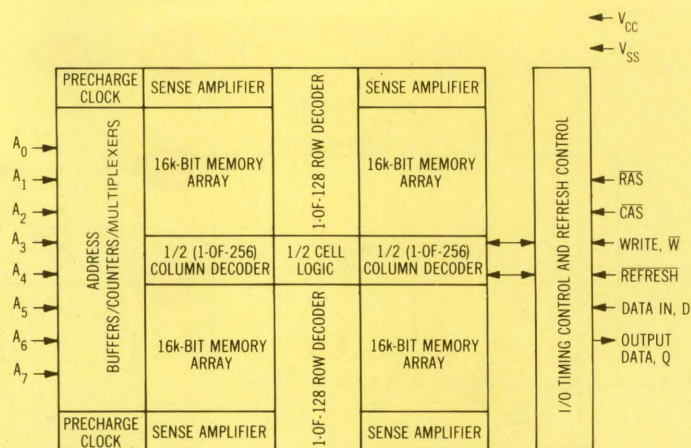
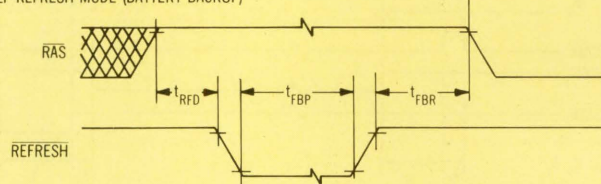
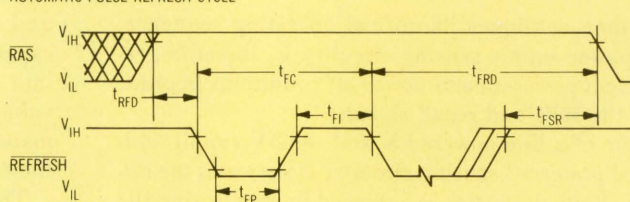


Fig 1 Block diagram of Motorola's 64k dynamic RAM, MCM6664. Complete address decoding is done onchip with address latches incorporated. Data out is controlled by CAS allowing for greater system flexibility

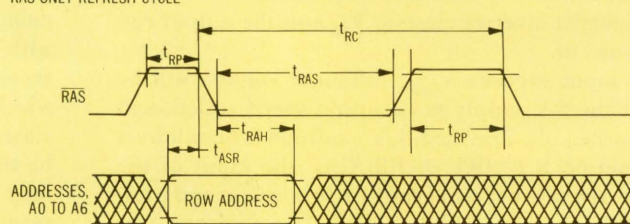
SELF-REFRESH MODE (BATTERY BACKUP)



AUTOMATIC PULSE REFRESH CYCLE



RAS-ONLY REFRESH CYCLE



- t_{RFD} — RAS to REFRESH delay
- t_{FBP} — REFRESH period
- t_{FBR} — REFRESH to RAS precharge time
- t_{FC} — REFRESH cycle time
- t_{FP} — REFRESH pulse period
- t_{FI} — REFRESH inactive time
- t_{FRD} — REFRESH to RAS delay time
- t_{FSR} — REFRESH to RAS setup time
- t_{RP} — Row address strobe precharge time
- t_{ASR} — Row address setup time
- t_{RC} — Random read or write cycle time
- t_{RAS} — Row address strobe pulse width
- t_{RAH} — Row address hold time

Fig 2 Refresh modes for 64k RAM. For self-refresh mode with battery backup (top) and automatic pulse refresh (center), CAS, addresses, data in, and WRITE are Don't Care. In RAS only mode (bottom), data in and WRITE are Don't Care; CAS is high

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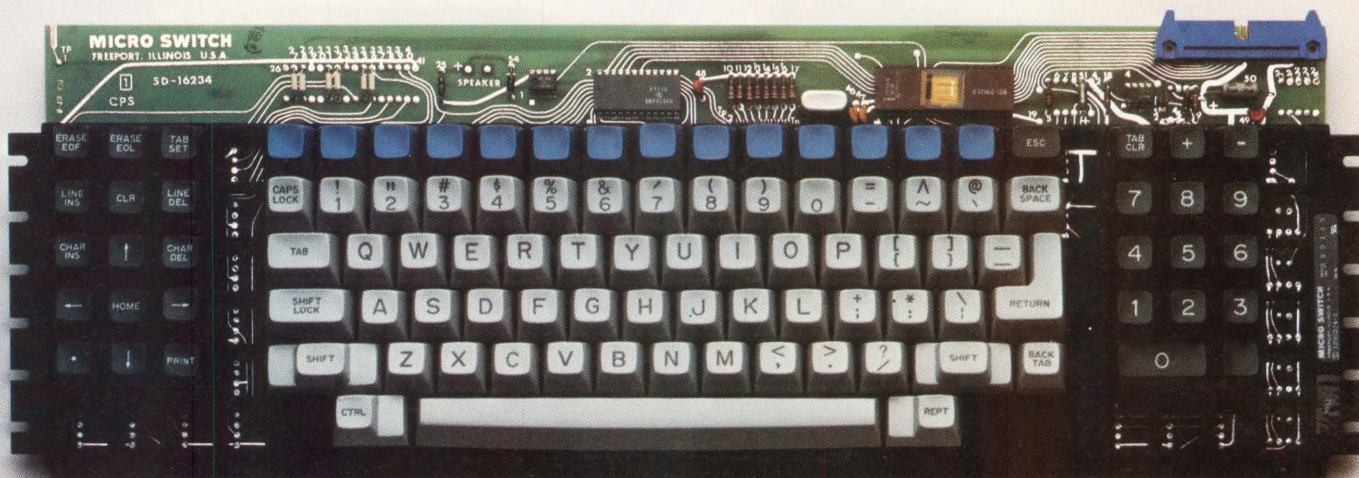
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CIRCLE 122 ON INQUIRY CARD



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That alone is probably good enough reason to specify a Hall effect solid state keyboard from MICRO SWITCH. It's the most reliable keyboard you can buy. From the beginning, it will help you and your customers save money on repairs.

As a result of design innovations, the Hall effect keyboard is competitively priced against lower-performance, less reliable keyboards. Innovations like the microcomputer that gave you the first "intelligent" keyboard, the three terminal keyswitch module and single-sided printed circuit boards.

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MICRO SWITCH
a Honeywell Division

AROUND THE IC LOOP

A 32,768-bit version, organized as 32k x 1, results from use of one-half of a 64k device, with all parameters other than bit capacity identical to those of the complete chip. With pin 1 refresh, the designation of the 32k RAM is MCM6632; without this feature, it is designated MCM6633.

The 16,384-bit members of the family are the MCM4516 (with pin 1 refresh) and MCM4517 (without). Organized as 16k x 1, these RAMs provide a max access time of 100 ns and max power dissipation of 150 mW active and 14 mW on standby, as well as a hidden refresh capability with output remaining valid from the previous cycle during refresh. Other characteristics of the 16k RAMs match those of the 64k and 32k members of the family.

Absolute maximum ratings for all of these RAMs require that voltage relative to V_{SS} stay between -1 and 7 V for V_{CC} and between -2 and 7 V for all other pins. Temperature must remain between 0 and 70 °C in operation and between -65 and 150 °C in storage. Power dissipation is limited to a max of 1 W and data out current to a max of 50 mA.

All of the memories are currently in production except for the 16k device with the pin 1 refresh option. This RAM is scheduled for availability later this year.

Circle 502 on Inquiry Card

Leadless Chip Carriers Provide Alternative to Conventional DIPs

According to an independent study, approximately 55% of all integrated circuits will be packaged in some form of leadless ceramic chip carrier (LCCC) by 1990. Chip carriers are said to be more reliable, easier to use, and more versatile, requiring less space and reducing system cost.

At 1/6 the surface area and 1/12 the weight of conventional dual inline package, a newly announced LCCC from Texas Instruments Inc, PO Box 225012, Dallas, TX 75265, has a single-level 100-mil thick structure consisting of a microelectronic chip mounted on a ceramic base and hot cap sealed for a hermetic ceramic-glass-ceramic struc-

ture. Several additional advantages relative to standard IC packages have been listed by the manufacturer. The ruggedness of the package facilitates its automatic placement on PCBs by magazine fed machines. Square shaped, flat, and thin, it can be readily flow soldered and mounted on different types of printed circuit board materials. During soldering, a chip carrier will properly align itself in place on a board, even if initially misaligned by as much as 25%.

Because an LCCC requires less board space, fewer boards are required in a system utilizing them and overall system cost is reduced. Furthermore, assembly is faster because fewer system assembly steps are required. It is said to provide a measurable improvement in high frequency and high speed switching performance, having a lower lead inductance, lower resistance, and significantly shorter signal paths. An LCCC finds application particularly in packaging VLSI circuits with more than 64 I/O counts.

Thermal properties are similar to those of a conventional DIP. The theta junction case (JC) is 26 °C/W typ, and the theta junction ambient (JA) is 63 °C/W typ.

Demands caused by improvements in electronic chip technology, such as increased complexity and size of circuits and a greater number of pinouts, led to the design of this package. Developed as part of a military contract program for the U.S. Air Force, this LCCC has been utilized for IC packaging as part of that program for the past two years. It is now available to military, commercial, and industrial systems designers, and, since it is a JEDEC standard part, it is expected to be available from multiple sources.

Although current packaging costs are slightly higher than conventional IC packaging, prices are expected to soon be comparable with other packaging. It is estimated that by 1982 LCCCs will cost less than flat packages, and that by 1984 they will cost about the same as dual inline packages. Furthermore, since LCCCs can reduce overall system costs, they can be used cost-effectively now.

Certain digital chip functions are available in LCCCs of two sizes, 20 contacts and 28 contacts. The 20-contact LCCC is 0.350" (8.9 mm) on each edge, while the 28-contact version is 0.450" (11.4 mm) per edge. All chip functions

requiring 20 pinouts or less are mounted in a 20-contact LCCC, and all chip functions which require 21 to 28 pinouts are mounted in a 28-contact LCCC. Both versions are 0.100" (2.54 mm) thick. LCCCs with 44, 68, and 84 contacts will be available within a few months.

The manufacturer presently offers 60 Schottky and low power Schottky digital functions in these packages, with off the shelf availability. Other digital, linear, and memory functions are supplyable subsequent to order. Devices are processed to MIL-STD 883 and are fully tested with guaranteed ac and dc characteristics.

Circle 503 on Inquiry Card

Mil Spec Chip Performs as Either Multiplier or Divider

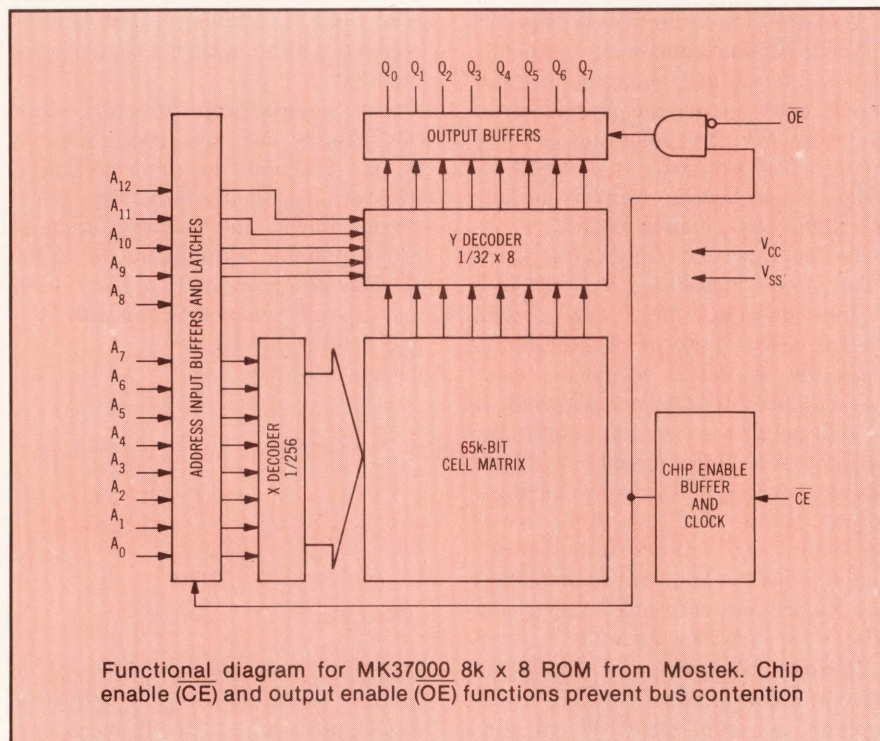
Designed to meet the requirements of military contractors and for industrial applications with critical, high reliability, high temperature requirements, the 4213VM/MIL is a precision 4-quadrant analog multiplier that can also function as a 2-quadrant analog divider. Produced by Burr-Brown, PO Box 11400, Tucson, AZ 85734, the device provides a 1% max total error, 50-mV max output offset voltage, and feedthrough of 100 mV max (pk-pk) at 25 °C. The IC is specified over the full MIL temp range of -55 °C to 125 °C. Offset drift is less than ± 1 mV/°C, and CMR is 60 dB min. Supply voltage range of the TO-100 packaged unit is ± 20 Vdc.

The chip is the latest addition to this manufacturer's /MIL program, which is designed to simplify nonstandard parts approval when MIL-M-38510 parts are unavailable. It is screened to MIL-STD-883 Class B, and qualification conformance inspection is performed on each lot. A qualification report for MIL-M-38510 inspection routine is available from the company.

Absolute maximum ratings require that supply voltage and input voltage remain in a range between ± 20 Vdc, with differential input voltage restricted to ± 40 Vdc. Temperature during storage must stay between -65 and 150 °C.

Circle 504 on Inquiry Card

64k Mask Programmable ROM Can Replace EPROM



A 65,536-bit mask programmable ROM, MK37000 from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, organized as 8k x 8, provides a pin and function compatible alternative to the similarly organized MK2764 EPROM. Its full compatibility extends to the entire family of N x 8 BYTEWYDE™ memories from the same manufacturer.

The ROM interfaces with all present generation 8- and 16-bit microprocessors. It features 250-ns access time, output enable (\overline{OE}) and chip enable (\overline{CE}) control functions that prevent bus contention problems, operation from a 5-V $\pm 10\%$ power supply, and power dissipation of 220 mW active (max) and 35 mW (typ) standby. Use of clocked control periphery and a standard static ROM cell are said to make this the lowest power 64k ROM available.

Onchip address latches are controlled by the \overline{CE} input. Once address hold time is met, new address data can be provided to the device in anticipation of a subsequent cycle. It is not necessary to maintain the address up to access time to access valid data. The output enable function controls only the outputs and is not latched by \overline{CE} . Therefore, the \overline{CE} input can be used for device selection and the \overline{OE} input used to avoid bus conflicts so that outputs can be ORed together when using multiple devices.

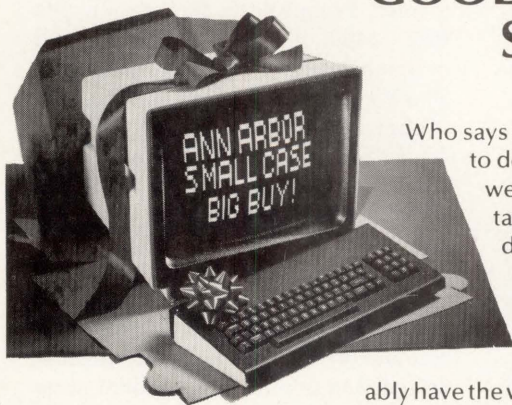
Other system oriented features include fully TTL compatible inputs and outputs. The 3-state outputs, controlled by the \overline{OE} input, will drive a minimum of two standard TTL loads.

Packaging is provided in a 28-pin DIP, with pin 20 handling the \overline{CE} and pin 22 the \overline{OE} function. Pins 1 and 26 are not connected, allowing easy upward compatibility with next generation higher density ROMs which will use these pins for addresses. Pin 27 is not connected in order to maintain compatibility with RAMs which use this pin as a write enable control function.

Absolute maximum ratings require that voltage on any terminal relative to V_{SS} lie between -1 and 7 V. Ambient temperature must remain between 0 and 70 °C during operation, between -65 and 150 °C during storage of the ceramic package, and between -55 and 125 °C during storage of the plastic package. Power dissipation must not exceed 1 W.

Circle 505 on Inquiry Card

GOOD CRT'S COME IN SMALL PACKAGES



Who says a CRT terminal has to be big and bulky to do a good job? At Ann Arbor Terminals, we offer a full 15-inch screen and detached keyboard as standard on all our desktop terminals. And the case is only 14" wide by 15" high by 13.6" deep.

We're known throughout the industry for our high quality and reliability. On top of this, we prob-

ably have the widest range of available options in the field. Display formats from 256 to 4800 characters. Foreign

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And if your application doesn't lend itself to a desktop terminal, we offer display controllers (especially good in industrial environments) for use with free-standing monitors. Or buy our terminal without the case and mount it in your own console.

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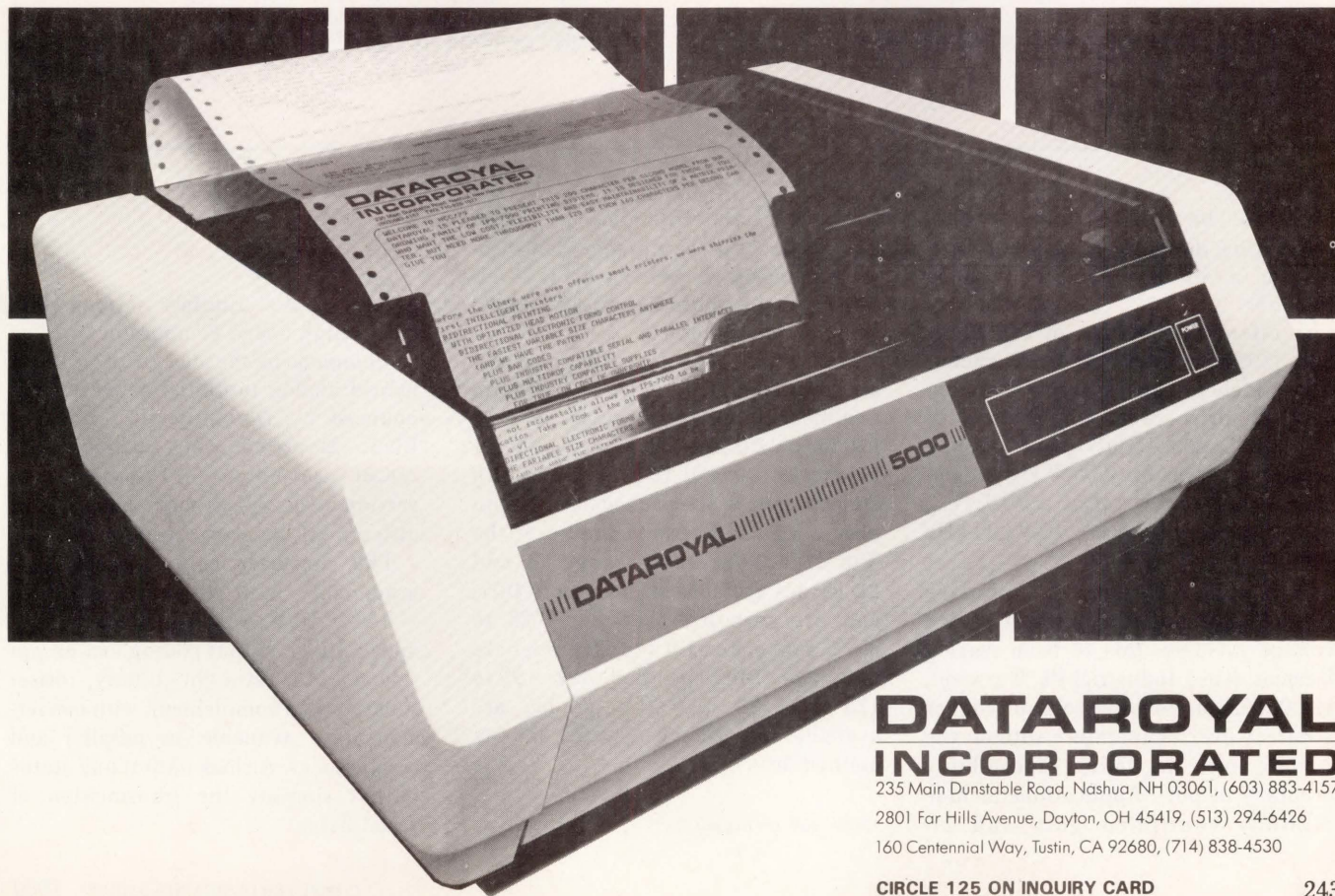
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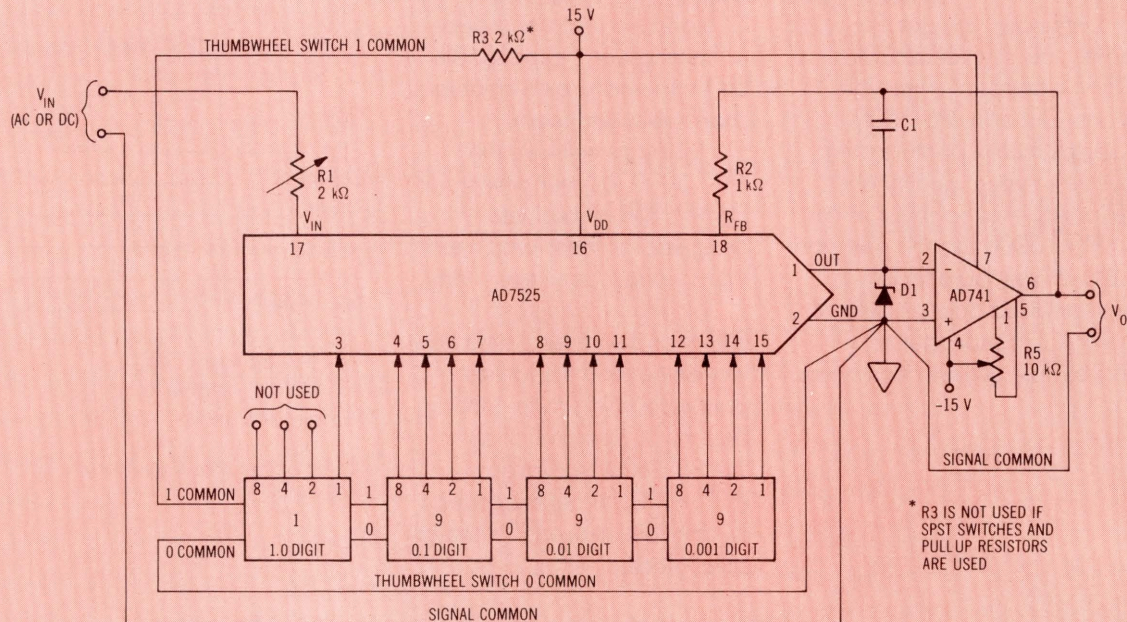
235 Main Dunstable Road, Nashua, NH 03061, (603) 883-4157

2801 Far Hills Avenue, Dayton, OH 45419, (513) 294-6426

160 Centennial Way, Tustin, CA 92680, (714) 838-4530

CIRCLE 125 ON INQUIRY CARD

Digital Pot Circuit Implemented on Single Chip



Application of digitally controlled potentiometer, AD7525, in thumbwheel switch attenuator. BCD-coded thumbwheel assembly applies BCD data to

IC's digital inputs. Switch assembly shown has single-pole double-throw action; thus BCD inputs are pulled either to 15 V or GND

Said to be the industry's first monolithic integrated circuit to function as a digitally controlled potentiometer, the AD7525 is a CMOS device that offers a resolution of $3\frac{1}{2}$ digits BCD (1999 counts). Other characteristics include guaranteed monotonicity, a drift over temperature of 25 ppm/°C max, 15-mW power dissipation, gain error of $\pm 0.05\%$ FS typ, and max feedthrough error of $\pm 0.1\%$ V_{IN} , with V_{IN} defined as a ± 10 -V, 20-kHz sine wave.

Designed to replace expensive 10-turn pots and thumbwheel switch voltage dividers, this IC from Analog Devices, Rte 1 Industrial Pk, Norwood, MA 02062, offers lower cost and higher accuracy over temperature without the contact noise and limited repeatability accuracy of pots. Applications include digitally controlled gain and at-

tenuator circuits in audio equipment, automatic test equipment, and instrumentation where dc voltage levels or ac signal amplitudes must be dialed from a front panel.

Six grades (plus four MIL versions) are available. Guaranteed maximum nonlinearity over temperature is $\pm 1/2$ LSB for LN, CD, and UD grades, and ± 1 LBS for KN, BD, and TD grades. Both KN and LN grades are packaged in 18-pin plastic DIPs and are specified over the 0 to 70 °C temperature range. CD and BD grades are housed in ceramic DIPs, and are specified over the -25 to 85 °C range, and UD and TD grades are in ceramic DIPs, specified over -55 to 125 °C. All D suffix grades are available fully screened to MIL-STD-883, method 5004, class B.

Circle 506 on Inquiry Card

12-Bit Hybrid ADC Converts in 2 μ s

A proprietary ultrafast settling DAC and a high speed comparator are key components in the design of a 12-bit hybrid analog to digital converter announced by Datal-Intersil, 11 Cabot Blvd, Mansfield, MA 02048. The ADC-817 accomplishes a 12-bit A-D conversion with 1/2-LSB max integral and differential linearity errors in 2 μ s.

This converter features six pin programmable input voltage ranges, 0 to -5 V , -10 V , -20 V , $\pm 2.5\text{ V}$, $\pm 5\text{ V}$, and $\pm 10\text{ V}$. Output coding can be pin selected for straight binary, offset binary or 2's complement, with conversion data available in parallel and serial modes. A clock output and status output simplify the transmission of serial data.

SYSTEM 19 NOW PROGRAMS MORE THAN 200 DIFFERENT PROMS WITH ONLY ONE SOFTWARE SELECTABLE MODULE.



Our new System 19/UniPak lets you program most MOS and bipolar PROM'S from AMD, Fairchild, Harris, Intel, MMI, Motorola, National, Raytheon, Signetics and Texas Instruments. UniPak's software assembles the programming algorithm and selects the correct socket for 16, 18, 20, 24 and 28-pin PROMS.

System 19/UniPak gives you design and purchasing freedom. This means you can select the best PROM for each application, and you can second-source for the best price and availability.

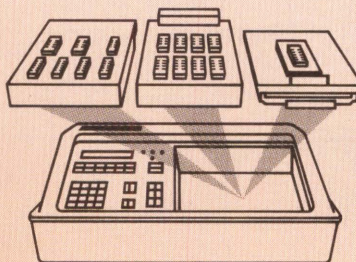
Semi-house approvals and easy calibration help maintain higher device yields.

UniPak has earned written approval from device manufacturers. And easy calibration lets you keep performance within PROM manufacturers' specifications.

UniPak algorithms shorten programming time enhancing System 19's use as a production tool. UniPak is the first module to use a newly developed algorithm which makes it possible to program a 64K EPROM in less than half the time it takes to program a 16K EPROM using standard methods.

And the System 19/UniPak is easy to operate, with a minimum of operator training.

New System 19 concept is open ended to keep it state of the art. The System 19 is designed around a standard main frame and plug-in modules.



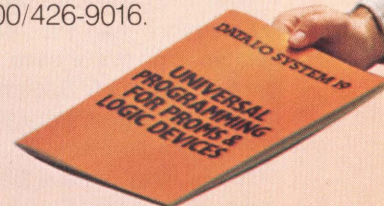
Modules available now include the UniPak, a gang programming pak for MOS devices, and a series of programming paks for logic devices and individual PROM families.

23 communication formats including six for development systems.

Development systems, computers, teletypes and CRT terminals interface easily with the System 19. The System 19 accepts micro-processor instruction codes from Motorola, Intel, Tektronix, Fairchild, FutureData and other development systems without intermediary equipment.

Let us show you the future.

The new Data I/O System 19/UniPak is available now. To make arrangements for a demonstration or to get your free copy of this valuable 32-page book, circle reader service number or contact Data I/O, P.O. Box 308, Issaquah, WA 98027. Phone 206/455-3990 or TOLL FREE: 800/426-9016.



DATA I/O

AROUND THE IC LOOP

Each unit is equipped with an internal high speed precision input buffer, allowing it to be driven directly from a high impedance source. The buffer may be bypassed for operation with a low impedance source such as a sample/hold. Inclusion of the buffer in the A-D package reduces the chance of noise being introduced to the system by external sources.

Maximum parameters include a gain tempo of 25 ppm/°C, a 0 drift of 150 μ V/°C, and an offset tempo of 15 ppm/°C. The ADC finds uses in a wide variety of data acquisition applications, such as fast signal processing, ultra sound imaging, and fast precision instrumentation, and is packaged in a 32-pin, hermetically sealed, ceramic triple-spaced DIP. Three models are available covering operating temperature ranges of 0 to 70 °C, -25 to 85 °C, and -55 to 125 °C. These converters operate from \pm 15- and 5-V supplies.

Circle 507 on Inquiry Card

ADC Chip Runs For a Year on Single 9-V Battery

A monolithic analog to digital converter, the ICL7126, can operate for 8000 h (nearly 1 yr) on a single 9-V battery. The 3½-digit ADC, produced by Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014, is described as a lower power version of the industry standard ICL7106, utilized in a wide variety of handheld DMMs, DVMs, digital thermometers, and other devices.

This single CMOS IC includes 7-segment decoders, display drivers, reference, and clock. It is designed to interface with a liquid crystal display (LCD) and includes a backplane drive.

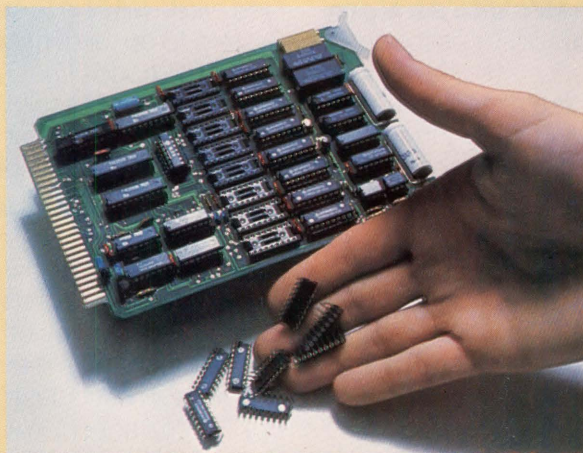
The high accuracy device features guaranteed 0 reading for 0 V on all scales and has true polarity at 0 for precise null detection. Auto 0 is less than 10 μ V, 0 drift is less than 1 μ V/°C, input bias current is 10 pA max, and

rollover error is less than one count. It also provides true differential input and reference, offering the designer a particular advantage when measuring load cells, strain gauges, and other bridge-type transducers. The single 9-V power supply operation allows a high performance handheld meter to be built with the addition of only seven passive components and a display. Other features include low noise (less than 15 μ A pk-pk), a 100- μ A supply current, and power dissipation guaranteed to be less than 0.9 mW.

These devices are provided in 40-pin plastic or ceramic dual inline packages. Maximum ratings limit supply voltage (V^+ to V^-) to 15 V or less, with analog input voltage and reference input voltage required to stay between V^+ and V^- . Power dissipation must not exceed 1000 mW for the ceramic nor 800 mW for the plastic package. Allowable temperature ranges are 0 to 70 °C in operation and -65 to 160 °C in storage.

Circle 508 on Inquiry Card

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Our STD Bus-compatible card saves more than your data. For a limited time it will save you money. Through December 1, 1980, we'll sell you our 8K version for the single-piece, 4K price.

We at Matrix have been producing the 7911/CRC card in both 8K and 4K versions for quite some time. Both have many

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Programmable IC Generates Clock Pulses At 64 Frequencies

Available in two models, a clock pulse generator integrated circuit from Epson America Inc, 23844 Hawthorne Blvd, Torrance, CA 90505, can generate 64 frequencies (57 unique) from the original frequency of its built-in crystal oscillator. This original frequency has a range from 30 to 130 kHz; the output frequencies are generated through setting six program leads. The 8650 model offers an accuracy of \pm 50 ppm in its output pulse frequency, while the corresponding parameter for model 8651 is \pm 5 ppm.

Programming of the hybrid IC is accomplished by means of a CMOS divider that offers ratios from 1/1 to 1/12 (10)⁻⁷. Other characteristics include a supply current of 0.5 mA max and 0.35 mA typ, operation from a 5-V power supply, and TTL compatibility.

The time accuracy of the IC makes it suitable for use as a clock generator in a wide range of applications, including clocks, instruments, computers, and automatic machines. Packaging is provided in a 16-pin DIP. □

Circle 509 on Inquiry Card

New iSBX™ Multimodule™ boards

Intel® introduces a whole new dimension in configuring single board computer systems.

Intel pioneered the concept of flexible microcomputer system design in 1976, with our family of iSBC™ single-board computers interfaced via the Multibus™ system bus—presently accepted as the industry standard.

Now we've extended this well-accepted concept to board-level design: A new generation of Multimodule boards interface to iSBCs via the new iSBX bus. So now you have a second design option. You can expand systems in large increments with Multibus boards. Or in smaller, more economical increments with Multimodules.

The key to configuration flexibility

The iSBX bus—the first physical/electrical interface for direct on-board expansion of iSBC systems—assures compatibility between these systems and the emerging Multimodule product line.

Present on all future Intel single-board computers, the iSBX bus saves design time and space, and facilitates fast, easy upgrading. System performance is

also improved because Multimodules tie directly to the iSBC internal bus. Connection to the iSBX bus is made with a set of rugged connectors—one on the iSBC board, the other on the Multimodule itself.

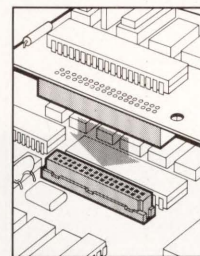
The new Multimodule family

Multimodules represent a whole new family of plug-in expansion boards. They allow you to add a variety of special performance features to your existing iSBC system. Currently available add-ons are shown below. Soon you'll also be able to add other Multimodules for D-to-A and A-to-D conversion, communications, peripheral interfaces—and more.

With those modules you can now respond

the more economical iSBX 331 or 332 math modules.

New Multimodule-compatible iSBC boards



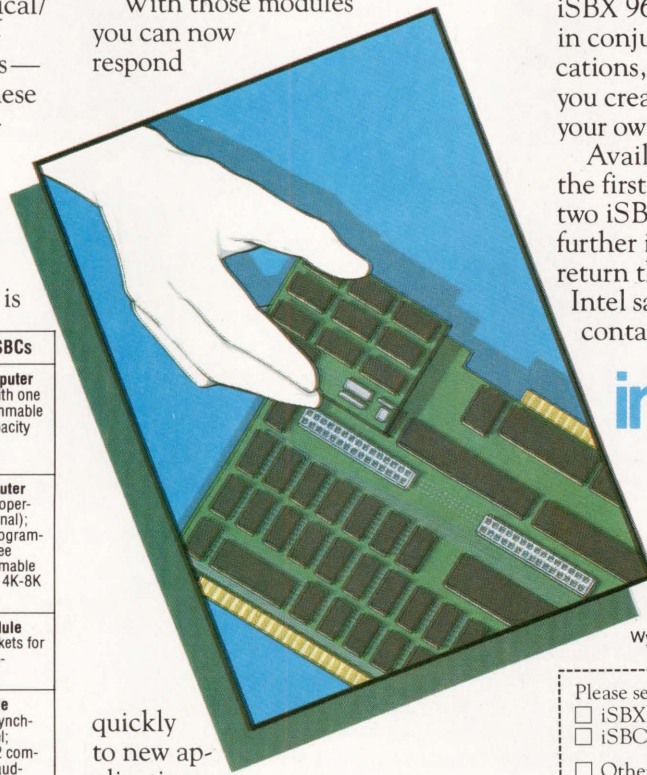
iSBX 960-5 Connector

Intel's new 8-bit iSBC 80/10B and 80/24 single-board computers are the first of many iSBCs to offer iSBX Multimodule expansion capabilities. Both are improved versions of widely used iSBC boards. (See table).

Custom tailoring, too

For users who want to design their own Multimodule boards, Intel offers iSBX 960-5 connectors. When used in conjunction with the iSBX specifications, this set of connectors lets you create modular boards that meet your own unique requirements.

Available from Intel today are the first four iSBX Multimodules and two iSBX-compatible iSBCs. For further information, or to order, return this coupon or call your local Intel sales office or distributor. Or contact Intel at the address below.



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New Multimodules and iSBX Bus-compatible iSBCs	
	iSBX 80/10B Single Board Computer 8080A-based microcomputer with one iSBX bus connector; 48 programmable I/O lines; one USART; timer; capacity for 1K-4K bytes RAM; up to 16K EPROM
	iSBX 80/24 Single Board Computer 8085A-2 based microcomputer operating at 4.8 MHz (2.4 MHz optional); two iSBX bus connectors; 48 programmable I/O lines; one USART; three programmable timers; programmable interrupt controller; capacity for 4K-8K bytes RAM; up to 16K EPROM
	iSBX 350 Parallel I/O Multimodule 24 programmable I/O lines; sockets for inverting and noninverting transceivers
	iSBX 351 Serial I/O Multimodule Programmable synchronous/asynchronous communications channel; standard RS232C or RS449/422 compatibility; software-selectable baud-rate generation; two programmable 16-bit BCD or binary timers/event counters
	iSBX 331 Fixed/Floating Point Math Multimodule Fixed point single- (16-bit) and double- (32-bit) precision arithmetic; floating point single- (32-bit) precision functions; floating-to-fixed and fixed-to-floating point conversions; transcendental functions
	iSBX 332 Floating Point Math Multimodule Single- (32-bit) and double- (64-bit) precision arithmetic; compatible with proposed IEEE format and existing Intel floating point standard.

quickly to new applications opportunities. Examples? Take data acquisition or industrial control: to add extensive I/O processing power, you simply plug in the iSBX 350 board. Or consider communications networks. Now there's no need to add entire USART boards; just use the iSBX 351 unit. In laboratory control applications, instead of an independent math processor, now you can choose

Please send information on:

- ☐ iSBX Multimodules ☐ iSBC 80/10B
☐ iSBC 80/24 ☐ Configuration Guide
☐ Other
☐ Please have a Sales Representative call.

Name _____

Title/Organization _____

Address _____

City/State/Zip _____

Phone _____

Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

THE HUGHES H800

The fastest route from concept to production...

From concept to design, from prototype to production no other development system can match the speed, the power, the flexibility and the capability of the new Hughes advanced microcomputer development system—the H800.



HUGHES

HUGHES AIRCRAFT COMPANY

Solid State Products Division
Semiconductor Product Line
500 Superior Avenue
Newport Beach, CA 92663
(800) 854-3515 or
(714) 759-2678

State-of-the-art multiprocessor architecture of the H800 includes intelligent peripheral controllers and memory management unit that's expandable to more than 128K. And the H800 is virtually universal, supporting the 1802, 1804, Z80, 8080, 8085, 8048, 6800, 6809, 6502, with additional microprocessor support now in design.

Cost-effective development software of the H800 includes high-level languages through CP/M, a convenient screen editor and a relocatable macroassembler. Additional software features include a library capability, linkage editor and symbolic debug.

The modular operating system of the H800 allows both multi tasking and multiusers, and includes a real-time clock and timer, background printing, logical I/Os, utilities and file management. And with the H800, you can software down load to and from any other system.

In-circuit-debug emulator of the H800 provides real-time execution, disassembler in trace, and patch assembler in debug. In addition there are

unlimited hardware, software and special conditional break points, single step/multiple steps, a powerful mapping facility, and a universal real-time Logic Analyzer.

The H800 Advanced Microcomputer Development System... another important addition to the Hughes microprocessor family.

The 1800 Microprocessor Family

(Available Now)

Number	Function
HCMP 1802	CPU
HCMP 1822	256 x 4 RAM
HCMP 1824	32 x 8 RAM
HCMP 1831/2	512 x 8 ROM
HCMP 1833/4	1024 x 8 ROM
HCMP 1835/6	2048 x 8 ROM
HCMP 1851	Prog. I/O
HCMP 1852	I/O Adapter
HCMP 1853	3 to 8 Decoder
HCMP 1854	UART
HCMP 1855	Mul./Div.
HCMP 1856/7	Bus Buffer/Separator
HCMP 1858/9	Memory Latch/Decoder
HCMP 1861	TV Interface

CIRCLE 193 ON INQUIRY CARD

DILOG INTERFACES DEC 11*

10 intelligent hard disc and magnetic tape controllers offer LSI-11*, 11/2, 11/23, and PDP-11* single quad slot compatibility with up to 60% power saving.

Only DILOG (Distributed Logic Corporation) exclusive automated design, common proprietary architecture and sophisticated bipolar μ Ps give you • all single board quad size products requiring no external power or chassis . . . just a cable to connect the drive . . . *you don't need anything else* • high reliability • automated self-test including data base protect feature and indicator. And at cost savings of 50% or more.

LSI-11 MAGNETIC TAPE CONTROLLER, Model DQ 120, interfaces 4 industry standard reel-to-reel drives • emulates TM11* • handles 7 and/or 9 track NRZI drives to 112.5 ips • selectable DEC or IBM byte order formatting • data error checking • RT-11/RSX-11* compatible • extended addressing to 128K words.

LSI-11 MAGNETIC TAPE COUPLER, Model DQ 130, interfaces dual density (NRZI/PE) formatted drives • emulates TM11 • handles up to eight 9 track 800/1600 bpi industry standard drives at speeds from 12.5 to 125 ips • "streamer" mode capability • software or switch selectable density • RT-11/RSX-11 software compatibility.

LSI-11 MASS STORAGE DISC CONTROLLER, Model DQ 200, interfaces any two SMD flat cable interface compatible hard disc drives for up to 500 MB on-line storage • mix or match compatible Winchester, SMD or CMD • variable sector size • automatic media flaw compensation with bad sector flagging • optimized logical to physical unit mapping • implements Winchester fixed head option.

NEW LSI-11 SHUGART SA4000 WINCHESTER DISC CONTROLLER, Model DQ 201, emulates DEC RK* • runs drivers under RT-11 and RSX-11M* systems • compatible with 14.5 MB SA4004 or 29 MB SA4008 drives • automatic media flaw compensation.

LSI-11 DISC CONTROLLER, Model DQ 100, interfaces 2.5, 5, 10 or 20 MB cartridge and fixed platter drives in combinations to 80 MB

• RKV-11/RKO5* emulator • handles front load (2315) and/or top load (5440) drives • automatic power fail/power down media protection • RT-11/RSX-11 compatible.

NEW LSI-11 EMULATING MASS STORAGE CONTROLLER, Model DQ 202. Cost effective interface of two 8 and/or 14-inch Winchesters, SMD or CMD hard disc drives without changing controller . . . 8 to 300 MB capacity • RP emulator • automatic media flaw compensation.

PDP-11 MAGNETIC TAPE CONTROLLER, Model DU 120, emulates TM-11 and has same features as Model DQ 120 (LSI unit) • software compatible with RT-11, RSX-11, RSTS, IAS and MUMPS.

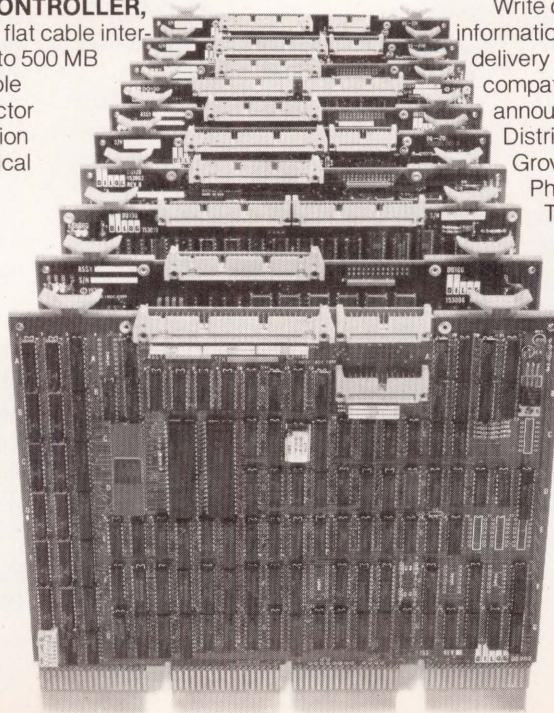
NEW PDP-11 MAGNETIC TAPE COUPLER, Model DU 130, offers features of Model DQ 130 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS software compatible.

PDP-11 DISC CONTROLLER, Model DU 100 includes features of Model DQ 100 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS compatible • emulates RK-11.

NEW PDP-11 EMULATING MASS STORAGE CONTROLLER, Model DU 202, offers same features as Model DQ 202 (LSI unit).

Write or call for detailed product performance information, OEM quantity pricing, stock to 30 day delivery or warranty data on these DEC 11 compatible products . . . or several soon to be announced new DILOG products.

Distributed Logic Corp., 12800-G Garden Grove Blvd., Garden Grove, CA 92643
Phone (714) 534-8950
Telex: 681399 DILOG GGVE



**DISTRIBUTED
LOGIC CORP.**
DILOG

CIRCLE 130 ON INQUIRY CARD

All DILOG μ P Products
are Low Power, Quad Size

PRODUCT FEATURE

Workstation Permits Designers to Configure Unique Computer Systems

By incorporating a choice of microprocessor compatible cards into a CD100 integrated workstation, an OEM designer is able to build the computer system that exactly meets a user's specific requirements. The compact, single-unit, Callan Data Systems workstation consists of an intelligent 12" (30-cm) CRT display, detachable keyboard with 82 keys and 7 LEDs, front panel control switches and display LEDs, card cage, and 200-W switching power supply. Two initial versions are available—for Intel Multibus or Digital Equipment Q-bus cards. (Both are sold without cards.) Dual 5.25" (13-cm) floppy disc drives or one floppy drive and one 5.25" Winchester disc drive are options.

Design Features

Once the customer's CPU (8080, 8085, 8086, Z80, Z8000 or LSI-11/2, LSI-11/23) is installed in the card cage, it interfaces with the system's terminal through a standard RS-232 interface at speeds up to 9600 baud. Communications protocol is in accordance with a subset of ANSI standard X3.64-1979. Terminal functions are controlled by a separate microprocessor.

Display features include 25 lines of 80 characters/line, split screen capability, separate scrolling regions within each screen, smooth scrolling, and forms drawing graphics. Among the "invisible" field attributes that do not use a character position are normal and half intensity, character blink, underline, reverse field, alternate character strike, and overstrike. Edit features consist of tabs, insert/delete character, insert/delete line, erase line up to cursor, erase line after cursor, erase entire line, erase screen, move cursor, and dump entire display

memory. Switch selectable features include 50- to 9600-baud rate, auto wraparound, auto line feed after carriage return, key click enable, monitor mode, cursor type, 115-V 60-Hz/230-V 50-Hz, local/self test mode, seven or eight data bits, parity enable, odd/even parity, intensity, and contrast.

As an option the Multibus backplane can be configured with power fail detection circuitry and provisions for battery backup. Address extension to 16M bytes is provided. The standard backplane provides interface to front panel interrupt and CPU reset momentary switches. Up to 12 LEDs are available.

This packaging technique allows the designer to place all system components in a single box. The Multibus version can hold up to six cards; the Q-bus version can be configured with as many as 12 double-height or 6 quad-height cards. Removal of a rear cover offers full access to the CPU card cage while maintaining full protection to

the remainder of the system. Cards can be on extenders during the development stage.

The switching power supply provides up to 25 A at 5 V, 4 A at ± 12 V, and 4 A at -5 V. Peripherals include various types of floppy discs, hard discs, printers, analog input/output, and industrial control interfaces.

A complete system measures 20" W x 25" D x 14" H (51 x 63.5 x 35.6 cm). Depth with keyboard separated is 19" (48 cm). UL and VDE standards are met.

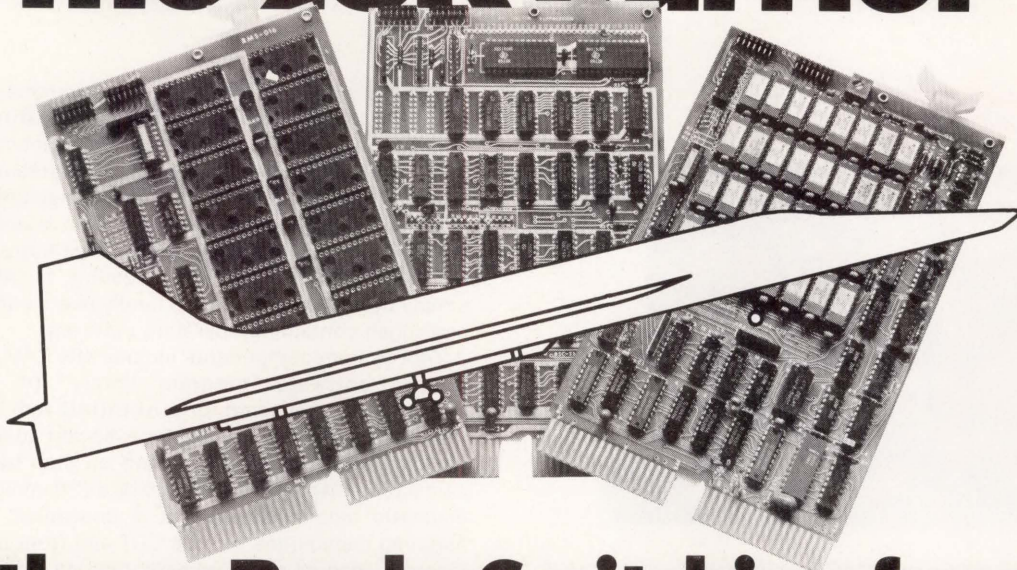
Price and Delivery

Unit price for the CD100 integrated workstation is \$3795 with, and \$3195 without, optional floppy disc drives. OEM discounts start at five units. Deliveries are 60 days ARO. Callan Data Systems, 2637 Townsgate Rd, Westlake Village, CA 91361. Tel: 805/497-6837.

**For additional information circle
199 on Inquiry Card.**



Let your LSI-11* break the 28K barrier



With our Bank-Switching family

In LOCAL mode our memory is functionally just like DEC memory. But when you run out of memory space you're not lost. Add an inexpensive Bank-Switch Controller (BSC-256) and you can go to **two megabytes**. Add another and go to **four megabytes**.

So don't get boxed in with other brands of LSI-11* memory. Break free. Join the family:

RMA-032	32K by 16 bit RAM. On-board refresh	\$990 (Single qty.)
RMS-016	16K by 16 bit ROM. (Intel 2716)	\$300 (Single qty.)
BSC-256	The Bank-Switch Controller	\$300 (Single qty.)

Substantial quantity discounts are available. The RMA-032 is also available without memory chips for \$450 (single quantity). For a free copy of our Bank-Switching manual, call or write on your company letterhead.

*Digital Pathways Inc.
1260 L'Avenida
Mountain View, CA 94043
(415) 969-7600*

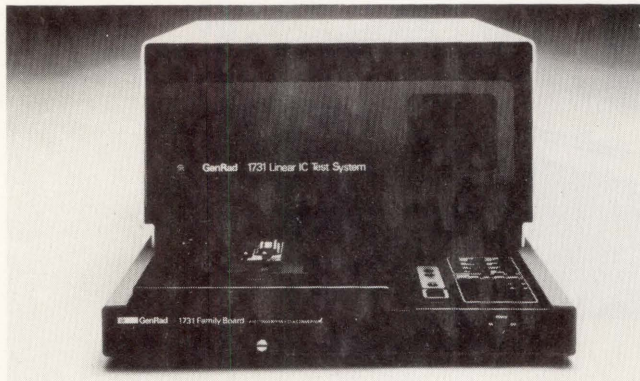
**Registered trademark of Digital Equipment Corporation*



DIGITAL PATHWAYS

PRODUCTS

Benchtop Tester Accepts Wide Range of ADCs and DACs

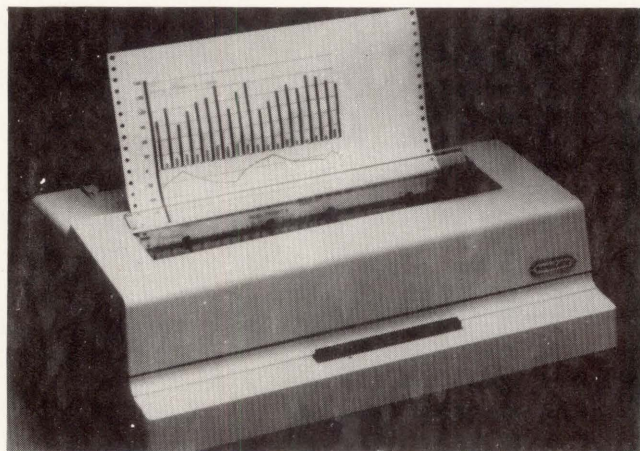


Most 4- to 12-bit ADCs and DACs—whether bipolar or MOS, monolithic or hybrid—can be tested on the benchtop 1731 test system without the need for special programming languages or operator programming skills. Step by step instructions displayed on the system's CRT allow the operator to describe the DUT and enter test conditions and limits in a fill-in-the-blanks procedure. As many ADC/DAC component parameters

can be tested as by most large scale systems—including gain, zero, and linearity errors; differential linearity; power supply; rejection ratio; and internal voltage reference accuracy for the DUT. Current force and voltage measurement capabilities enable performance of dc parametric measurements on digital I/O pins. Precise day to day calibration is ensured by voltage reference and software algorithms. Operators can switch from op amp/comparator/regulator testing to ADC/DAC testing simply by exchanging plug-in family boards and magnetic tape cartridges containing operating software.

Test system components include 48k RAM based operating system software, program library, 5" (12.7-cm) CRT, alphanumeric keyboard, and ADC/DAC family board. Among the options are handler interface, socket adapters for popular package styles and devices, and op amp family board. Test calculation display is controlled by a Z80 microprocessor while magnetic tape mass storage is controlled by a 6502. Data handling capabilities include CRT and front panel pass/fail indicators, manual and automatic binning, parametric measurement test results, and summary screens on the integral CRT. Hardcopy is available through a choice of IEEE-488 bus, 20-mA current loop, or optional RS-232 output. Statistical analysis can be performed by connecting I/O data ports to a computer or calculator. **GenRad, Inc.**, 300 Baker Ave, Concord, MA 01742. Circle 200 on Inquiry Card.

3-Color Ink Jet Printer Produces Graphic Output



By overlaying 3 ink colors (yellow, cyan, and magenta), the IS8001 printer terminal can provide a 7-color (yellow, cyan, green, magenta, brown, blue, and black) graphic output. Each

of the 3 basic colors is produced by 4 nozzles, for a total of 12 ink jet nozzles in the printhead. Resolution for the 6 x 8 dot font is 100 dots/in (39/cm) horizontally and vertically. Printing is bidirectional at 70 char/s. An 8080 microprocessor with 6k ROM and 16k RAM (as data buffer) controls printhead movement and color being printed. The standard RS-232-C interface has 7 baud rates from 110 to 9600; a 20-mA current loop interface is an option. Because it is a CRT page printer, it will print a full page (80 char x 48 lines) only when its buffer is full.

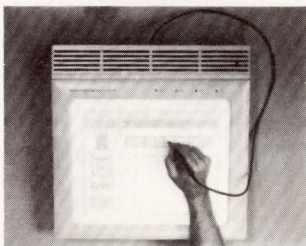
The terminal operates on an 8-bit USACII code; all Intelligent Systems Corp 8001 series control codes are recognized. Power requirements are 120/240 Vac, 50 to 60 Hz at 50 W in standby and 140 W max in operation. Op temp range is 20 to 40 °C at 30 to 90% RH. (Storage temp range is -25 to 70 °C at 55 to 95% RH.) Operating noise is no more than 50 dBA at 70 char/s. Printer line spacing at 80 char/line is 66 per 11" (28-cm) page. Characters are 0.1" (2.54 mm) normal, 0.125" (3.175 mm) elongated. Fanfold paper up to 15.7" (39.9 cm) wide can be used. Unit dimensions are 8.2" (20.8 cm) H, 22" (55.9 cm) W, 17.4" (44.2 cm) D; weight is 37.4 lb (17 kg). **Printacolor Corp.**, 5965 Peachtree Corners E, Norcross, GA 30071.

Circle 201 on Inquiry Card.

PRODUCTS

Graphics Input Tablet Enables Operator-Computer Interaction

Drawing on a CRT, tracing graphics documents, or picking from a menu can be accomplished through use of the HP 9111A graphics input tablet. A pen-shaped stylus provides a means for human interface with any HP-IB compatible host computer. Position of the stylus (fitted with either inking or noninking ballpoint pen refills) on the platen can be resolved to 0.1 mm. Data input and program control are provided by 16 softkeys. To select a menu item, the operator touches the stylus to a particular area of the platen and presses down. The tablet interprets which softkey was selected and notifies the host computer to branch to the appropriate application program segment. (The operator need not write program code to interpret softkey location.)



A programmable beeper for audio feedback spans 4 octaves of musical notes on an even-tempered scale. Duration and volume of each note are also programmable. Four LEDs indicate power is on, instrument ready to digitize, softkey operation selected, or error. Two built-in self-tests either provide verification that the unit is functional or aid in problem isolation. Graphics tablet utility software available as a separate product for use with the System 45B desktop computer includes a graphics editor to choose, place, delete, move, rotate, and rescale elements; a drawing utility to draw a picture, add text, create a data base, and plot; and a menu utility to create a program driver for interpreting a menu.

Data transfer rate is programmable from 1 to 60 points/s to match the CRT-refresh rate and provide smooth cursor movement. X/Y coordinate data can be transferred either in standard ASCII format or as binary information, and a hysteresis circuit provides exceptionally stable data. Artwork defining softkeys and borders is embedded in the ceramic platen and will not wear off. The active work area, including softkeys, is 9.3 x 11.8" (23.7 x 30.1 cm) and the area below the softkeys will accommodate an 8.5 x 11" (21.6 x 28-cm) document. (If necessary, the work area can be extended to the full area by turning off the softkey functions.) The tablet is fully compatible through HP-IB and HPGL with the HP-85 personal computer, the 9800 series of desktop computers, and the HP 1000 family of technical minicomputers. **Hewlett-Packard Co.**, 1507 Page Mill Rd., Palo Alto, CA 94304.

Circle 202 on Inquiry Card.

CIRCLE 132 ON INQUIRY CARD →

How to Display True Color Images With Just 10 Bits/Pixel



Do it with a Lexidata System 3400 Image and Graphics Processor.

If you want true color images but don't want to pay for the memory required by conventional 24 bit/pixel systems, Lexidata's System 3400 offers a practical alternative. Through a combination of software algorithms and versatile hardware color lookup tables, the 3400 can reduce memory cost by over 50% without significantly reducing image quality.

Look at the picture above. Like most true color images, it has a limited number of colors relative to the entire spectrum. This phenomenon makes it possible to program the 3400's color lookup tables so that a 24-bit output, high-fidelity color image can be generated with only 10 bits of input/pixel.

The 3400's color imaging versatility lets you use the same configuration to display pseudo-color, simply by reloading appropriate parameters into the lookup tables. The system also offers a wide range of application-oriented options such as separate simultaneous output for a B&W monitor and RGB-to-NTSC converter with color subcarrier regeneration.

GET MORE INFORMATION

Send today for literature that will help you evaluate how the Lexidata 3400 can improve your computer graphics image. For immediate response call (617) 273-2700.

LEXIDATA CORPORATION
37 NORTH AVENUE, BURLINGTON, MA 01803

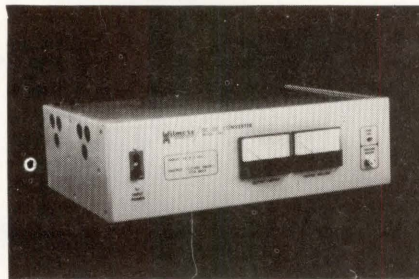
PRODUCTS

RASTER SCAN COMPUTER GRAPHIC SYSTEM

Operating standalone or as a terminal in distributed processing system, the 8600 is available in two 8-color models with resolution of 320 x 240 and 640 x 480. Insertion of additional frame buffer boards expands the 640 x 480 to 64 colors. The desktop system features multiple languages and operating systems, dual 16-bit processors, ACM Siggraph support, fill algorithms, zoning, smooth or line scrolling, zoom, simultaneous graphic/text display, and optional synchronization with external video signals. It also incorporates variable character generation and broad color selection. Number of color maps and colors in each are under software control. With a 6-plane memory, 64 colors may be displayed simultaneously; a 3-plane memory provides 8 simultaneous colors. Output of maps produces 8 levels each for red, green, and blue, resulting in 512 possible levels of intensity, saturation, and hue. **Terak Corp.**, 14151 N 76th St, Scottsdale, AZ 85260.

Circle 203 on Inquiry Card

400-W DC TO DC CONVERTERS



Series 1385 converters, capable of providing 400 W, are well regulated, feature efficiency to 85%, and are characterized by effective suppression of spikes and ripple on output voltage. Std inputs are 24, 48, 125, and 240 Vdc; std outputs include 13, 24, 48, and 125 Vdc. Converters have a no-load power requirement of < 5 W, making them efficient even at light loads, and adapting them for applications requiring standby service. They are designed to operate at full rated power throughout an ambient temp range of -30 to 65 °C, and are protected against overload, short circuit, and accidental reversal of input polarity. Measuring 5.25" high and 12" deep (13.3 x 30 cm), units are designed for std 19" (48-cm) rack mounting. **Wilmore Electronics Co, Inc.**, PO Box 1329, Hillsborough, NC 27278.

Circle 204 on Inquiry Card

MULTIPASS 300-LINE/MIN PRINTER

T-3000M high resolution printer operates in 3 printing modes: standard 300 lines/min, double-high character, and multipass. Any mode can be selected on a line by line basis by the host computer without operator intervention. Char sets can be downstream loaded and can be changed on the fly during printing. An asynchronous communications adapter for remote printing is optional. The printer does not require preventive maintenance. **Mannesmann Tally**, 8301 S 180th St, Kent, WA 98031.

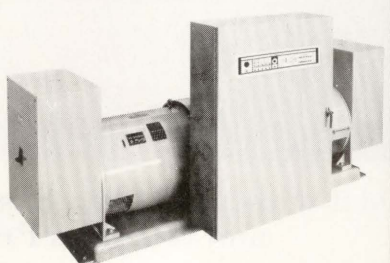
Circle 205 on Inquiry Card

SEMICONDUCTOR BULK STORAGE FOR PDP-11

ExpandaSTOR-11, configured as a hard disc, combines the access time and data transfer rate of main memory with the capacity of disc storage. The semiconductor bulk store is said to improve DEC PDP-11 throughput by 2X to 9X. Access time is 350 ns and transfer rate is 231 μ s/256-word sector (72M bytes/s). Built-in error correction, write protect, and maintenance capability are std. **Cambex Corp.**, 360 Second Ave, Waltham, MA 02154.

Circle 206 on Inquiry Card

THE ANSWER TO COMPUTER POWER PROBLEMS



The **POWER CONDITIONING SYSTEM** . . . An energy efficient synchronous motor generator system that eliminates power-related computer problems. The Computer Products Division offers a money-back guarantee against all power quality related problems such as sags, surges, transients, brown-outs, and up to 500 milliseconds of total black-outs!

Sweinhart offers the most technically advanced Power Conditioning System available . . . at any price! The System II, 15 to 219 KVA, utilizes a digital read-out system and a System Status Panel that provides a central location for essential read-out information . . . for both the status of the computer system's power and the facility's safety systems.

Outstanding Features:

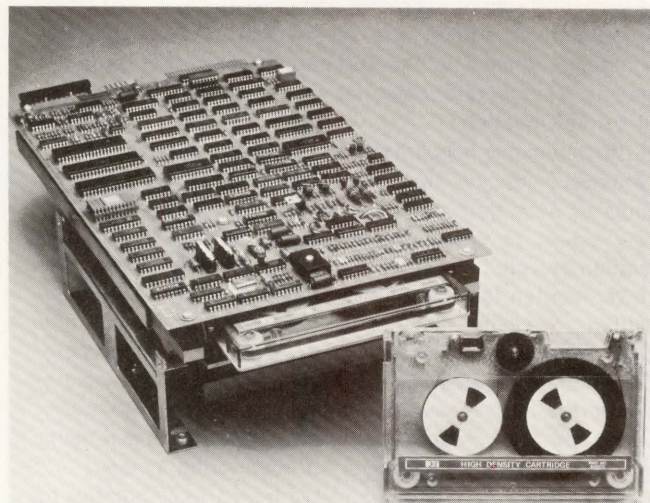
- A 5 year limited warranty on motor generator (an industry first).
- Digital Status Panel • Money-back guarantee • 6 to 8 weeks delivery • Priced at the lowest cost per KVA in the industry.

For complete information, call or write Richard N. Bowyer



COMPUTER PRODUCTS DIVISION

2900 East Olympic Blvd., Los Angeles, CA 90023
(213) 264-1521



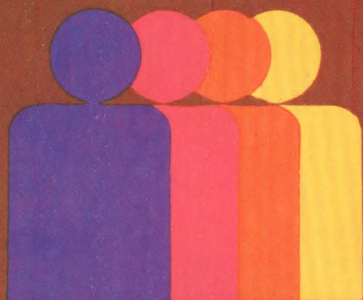
Multiple Interface Capability Announced for DEI Streaming Cartridge Tape Drives.

Data Electronics, Inc., has announced multiple interfaces for its new 10 and 20 MByte streaming $\frac{1}{4}$ " cartridge tape drives. The drives, which are specifically designed for Winchester disk backup, are now available with SMD, Priam and Shugart Associates interfaces.

With these available interfaces, systems designers and systems houses can greatly reduce costly design time. Only final packaging and power supply are needed to upgrade a floppy-based system to a 10 or 20 MByte Winchester/Streaming Cartridge Tape Drive unit.

DEI
Data Electronics Inc.
10150 Sorrento Valley Road
San Diego, California 92121
Telephone (714) 452-7840
Telex 69-7118

UnifLEX™



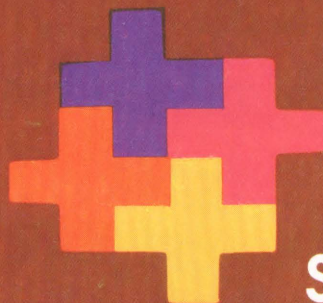
Multi-User

UnifLEX is the first full capability multi-user operating system available for microprocessors. Designed for the 6809 and 68000, it offers its users a very friendly computing environment. After a user 'logs-in' with his user name and password, any of the system programs may be run at will. One user may run the text editor while another runs BASIC and still another runs the C compiler. Each user operates in his own system environment, unaware of other user activity. The total number of users is only restricted by the resources and efficiency of the hardware in use.



Multi-Tasking

UnifLEX is a true multi-tasking operating system. Not only may several users run different programs, but one user may run several programs at a time. For example, a compilation of one file could be initiated while simultaneously making changes to another file using the text editor. New tasks are generated in the system by the 'fork' operation. Tasks may be run in the background or 'locked' in main memory to assist critical response times. Inter-task communication is also supported through the 'pipe' mechanism.



Support

The design of UnifLEX, with its hierarchical file system and device independent I/O, allows the creation of a variety of complex support programs. There is currently a wide variety of software available and under development. Included in this list is a Text Processing System for word processing functions, BASIC interpreter and precompiler for general programming and educational use, native C and Pascal compilers for more advanced programming, sort/merge for business applications, and a variety of debug packages. The standard system includes a text editor, assembler, and about forty utility programs. UnifLEX for 6809 is sold with a single CPU license and one years maintenance for \$450.00. Additional yearly maintenance is available for \$100.00. OEM licenses are also available.

FLEX™

UnifLEX is offered for the advanced microprocessor systems. FLEX, the industry standard for 6800 and 6809 systems, is offered for smaller, single user systems. A full line of FLEX support software and OEM licenses are also available.

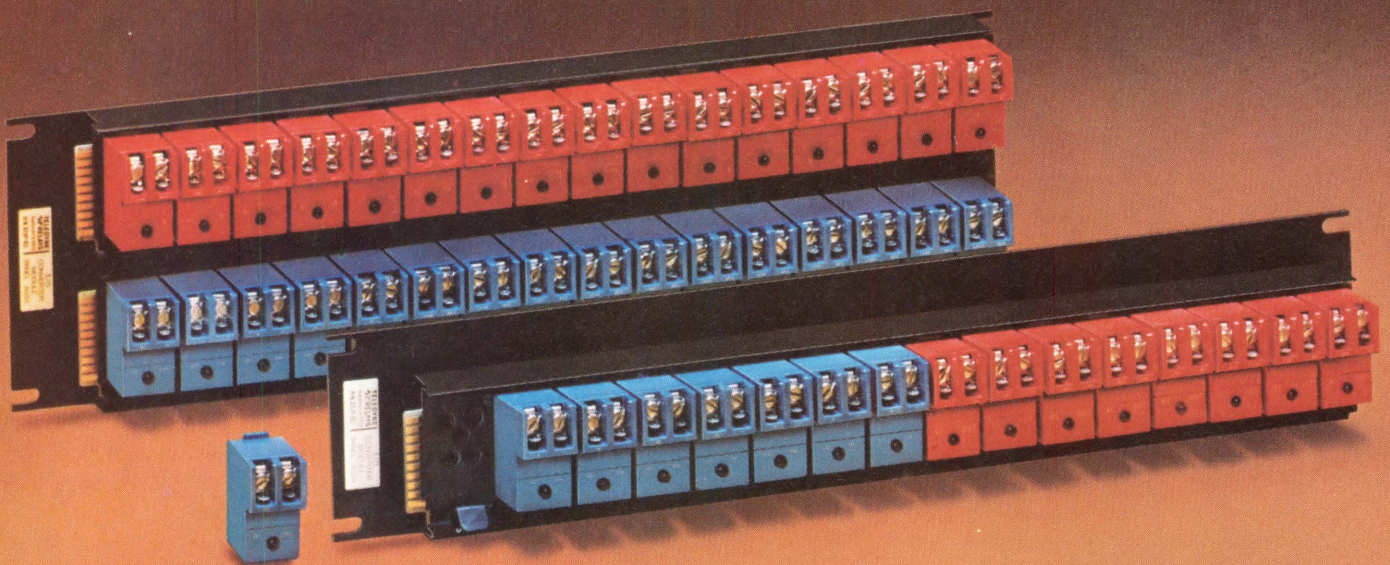


Box 2570, West Lafayette, IN 47906
(317) 463-2502 Telex 276143

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SSR UPDATE

We put a generation of know-how into this industrial I/O system



We brought you the first solid state I/O Interface modules for computerized industrial controls. With 5 years of experience to guide us, our 2nd generation I/O system (Teledyne 673 Series) features significant refinements in both modules and mounting panels.

The modules are smaller and more efficient. Transient and noise immunity so critical in industrial control applications are exceptionally high. Thermal ratings have been substantially improved. And the price is lower.

An all new mounting track design combines convenience, safety, appearance, and economy. Modules snap in and out, requiring no mounting screws. No exposed PC boards. AC and DC line voltages are kept off the board. Up to 16 modules fit on the single panel, 32 on the dual. Logic connections are made via a 20-pin edge connector or a rear-facing D connector. And again, the price is lower.

If you want the best in I/O systems compatible with today's microprocessor-based single board computers, call on the folks who started it all — Teledyne Relays.

 **TELEDYNE RELAYS**

12525 Daphne Avenue, Hawthorne, California 90250 • (213) 777-0077

CIRCLE 144 ON INQUIRY CARD

PRODUCTS

MICROPROCESSOR BASED PRINTER SYSTEMS

A microprocessor controlled printer system for Hewlett-Packard 300/3000 series 30/33 minicomputers offers speeds up to 1800 lines/min. The HPI-33 controller includes Z80 microprocessor, Intel 8291 talker/listener for interfacing with GPIB, along with associated memory and logic circuits. The 13 x 7.625 x 0.5" (33 x 19.36 x 1.27-cm) interface is installed within the printer cabinet and is daisy chained with other peripherals in std manner. Power is supplied by the printer. The program consists of 3 modes of operation: program control mode, transfer mode, and test mode. Printers available for use on the controller include band printers operating at from 300 to 600 lines/min, drum printers with speeds of 300, 600, 800, and 1800 lines/min; and a charaband printer running at 1250 lines/min. Printers use either 132- or 136-col line length and a std ASCII 64-char set with 96 char or other sets as options. All use a direct access vertical format unit for operation with std HP operating systems. **BDS Computer Corp.**, 1120 Crane St, Menlo Park, CA 94025.

Circle 207 on Inquiry Card

ALPHANUMERIC CRT DISPLAY TERMINAL

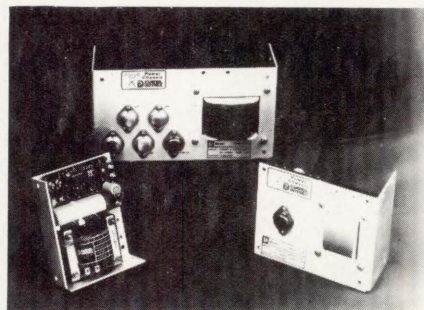


VC2100 is compatible with and includes all features of the DEC VT100, plus advanced video, key selectable jump, smooth scroll, double-size and double-width characters, status line, 8 programmable string keys, and host savable set-up control. It also includes home and clear keys, local or remote copy, stored set-up mode parameters, green or amber nonglare CRT, full- or half-duplex operation, and optional RS-449 interface accessory. **Volker-Craig Ltd.**, 266 Marsland Dr, Waterloo, Ontario N2J 3Z1, Canada.

Circle 208 on Inquiry Card

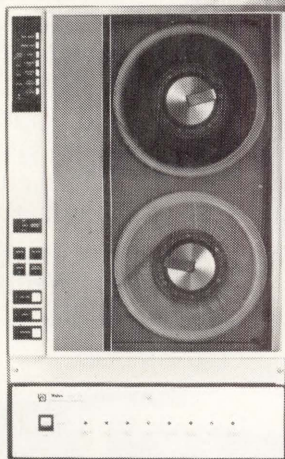
OPEN FRAME POWER SUPPLIES

Power Chassis series consists of 4 1-output models: 5 V at 3, 6, 12, and 18 A; 6 2-output models: ± 12 V at 1, 2, and 3 A; and ± 15 V at 1, 2, and 3 A; and 6 3-output models: 5 V, 3 A with ± 12 or ± 15 V at 2 A, and 5 V, 12 A with ± 12 or ± 15 V at 2 A. The units accept 115- or 230-Vac input at 48 to 440 Hz with voltage selection done by input connection. Input voltage tolerance is $\pm 10\%$. Line regulation is 0.05% and load regulation is 0.1% for 5-V outputs and 0.05% for ± 12 and ± 15 -V outputs. Outputs are protected by a foldback circuit for all 5-V outputs and current limiting for dual outputs. Output voltage tempco is 0.02%/°C max and output ripple voltage is 2 mV rms max. **Datel-Intersil**, 11 Cabot Blvd, Mansfield, MA 02048.



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The Dylon Corporation

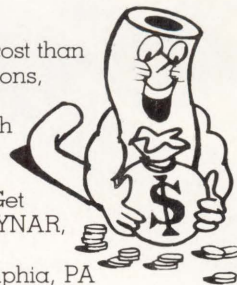
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Size

This is the ultimate version, the 8K cache with everything. You have never seen one like it before, and you may never see another. Designed for the 11/34, 11/35 and 11/40, it has byte and address parity, upper/lower limit switches, on-line/off-line manual switch control, activity indicator lights, 8K bytes of memory (4K words) providing a capacity four times that of competitive units and an interconnect board design which consumes no extra space in the computer.

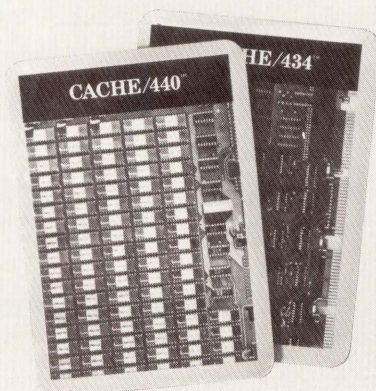
That's why there is always room in your computer for this incredible cache. You should put one there, especially if you are the kind of guy who likes to optimize his system for top performance. Our 8K super-charger lets you tailor performance to match your application and to establish hit-ratio optimization. It indicates hit rate and parity error immediately and, if errors are detected, shuts off automatically without ever interfering with system operation. It is, in fact, the only intelligent buffer memory turned out by an independent manufacturer.

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ABLE COMPUTER, 1751 Langley Avenue, Irvine, California 92714. (714) 979-7030. TWX 910-595-1729.

ABLE COMPUTER-EUROPE, 74/76 Northbrook Street, Newbury, Berkshire, England RG13 1AE. (0635) 32125. TELEX 848507 HJULPHG.

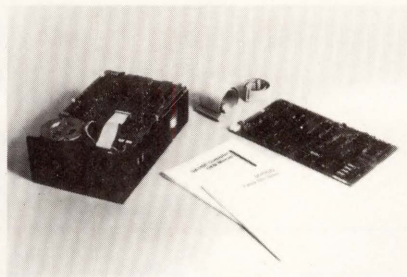


PRODUCTS

QUAD ALPHANUMERIC DISPLAY CONTROLLER

Multibus compatible MSBC-QV2 features 4 separate and independent video outputs on a single card. Permitting lower cost/display controller than was previously possible, the device is most cost effective in applications requiring terminal clusters, where a single card can replace 4 terminals. It also offers order of magnitude speed advantages because of video memory access instead of serial RS-232-C. The board uses the Synertek/Rockwell SY6545 CRT controller chip and advanced circuit design techniques to enable users to program the board's format and features through software. Programmable features include character cell sizes of from 6 to 11 dots horizontally and from 8 to 32 dots vertically; screen format of from 16 to 128 char/line on 8 to 25 lines (noninterlaced) or up to 50 lines with interlace; and character size of 1-16 clock times/char dot horizontally and 1, 2, or 4 scan lines/char dot vertically. **Matrox Electronic Systems, Ltd.**, 5800 Andover Ave, TMR, Quebec H4T 1H4, Canada. Circle 210 on Inquiry Card

WINCHESTER 8" DISC DRIVE EVALUATION KIT



Package, including SA1002 8" (20-cm) rigid disc drive, SA1400 intelligent fixed/floppy disc controller, interface cables, and support documentation, is intended as a low cost evaluation tool for those who have not previously designed systems using Winchester technology. The SA1002 drive features 5.3M bytes of fixed disc storage (unformatted), transfer rate of 4.34M bits/s, and average access time of 70 ms. The microprocessor based SA1400 controller handles up to 4 drives in any combination of fixed and floppy. It performs control functions and data transfers between host CPU and requires no additional data separator logic. The package operates on a 110-V power supply at a clock rate of 50 Hz. **Shugart Associates**, 475 Oakmead Pkwy, Sunnyvale, CA 94086. Circle 211 on Inquiry Card

10M-BYTE CARTRIDGE DISC DRIVE

Model 9310/9320 provides up to 40 times more storage than was available on the 1500 small business system and 10 times more than was available on the 1800. The 9310 consists of a disc drive and controller; the 9320 includes a disc drive, controller, and 4-terminal serial interface. A diskette drive is included as a backup for the cartridge. Both processors can support up to 4 9310/9320 drives for a total of 40M bytes of disc storage. **Datapoint Corp.**, 9725 Datapoint Dr, San Antonio, TX 78284. Circle 212 on Inquiry Card

ARRAY PROCESSOR FAMILY

With similar architecture and software support, the 460, 470, and 480 offer processing flexibility. The single-channel floating point 460 is designed for use with minicomputers. Midsize computers such as the DEC VAX-11/780 will interface with the 2-channel intermediate 470. Model 480 is a 4-channel high speed processor designed for use with large mainframe computers such as the Univac 1100/80 and the IBM 370. **Datawest Corp.**, 7333 E Helm Dr, Scottsdale, AZ 85260. Circle 213 on Inquiry Card

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translation tables, four independent alphanumeric overlays and dual cursor generators as well as high speed vector and special function generators.

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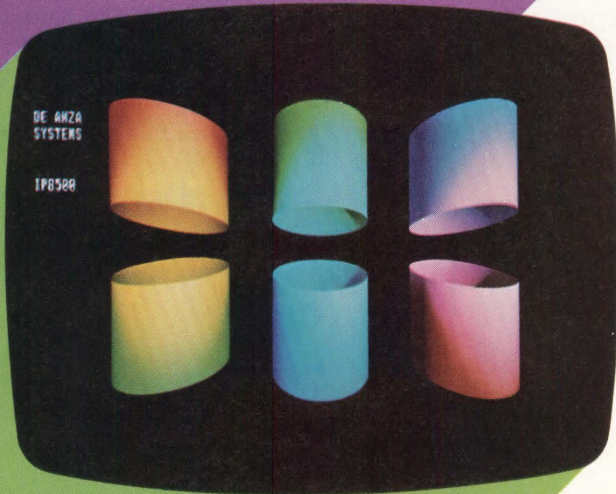
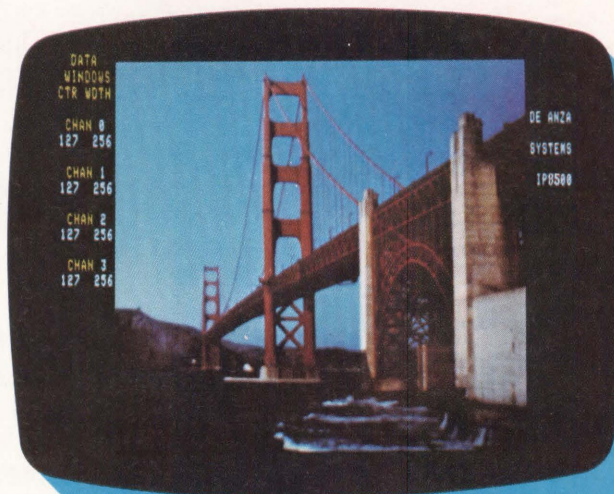
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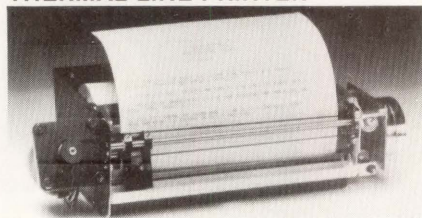
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GIVE YOURSELF A BETTER IMAGE



PRODUCTS

80-COL, 120-CHAR/s THERMAL LINE PRINTER



PL-80E head design features a 1 x 16 line of dots and a hard tooled printing mechanism. The printhead provides 7 x 11 dot matrix printing in a 9 x 16 field with all 96 ASCII characters printable. A compressed printing feature increases the number of columns from 80 to 132. High resolution graphics can be produced with the user able to define each dot. Up to 120 char/s can be printed. Five interfaces, self test, manual line feed, and a warning bell are standard. **Telpar Inc.**, 4132 Billy Mitchell Rd, Addison, TX 75001.

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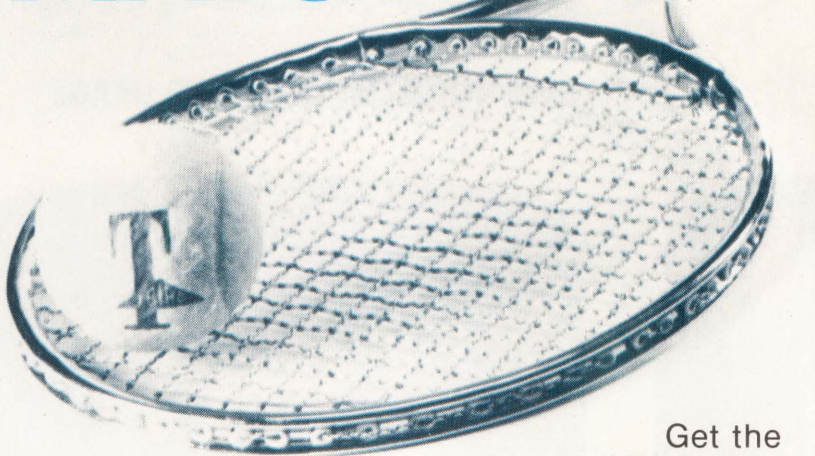
ENHANCED CAPABILITY INTELLIGENT TERMINAL



Enhanced version of ZMS-40 user programmable terminal incorporates an 8085A microprocessor, extended character generator, hidden attributes, up to 32k RAM, 8k ROM, full interlace, customized firmware and software, and a telecommunications interface that functions in both synchronous and asynchronous modes. Designed to provide performance and flexibility in word and data processing applications, the upgraded model features an attached 96-char keyboard, including 14-key numeric pad, 12 special purpose function keys, and 16 programmable function keys that operate in both shifted and nonshifted modes. The 12" (30-cm) nonglare video screen offers 24 lines of 80 char plus a 25th line for operator messages and status information. **Zentec Corp.**, 2400 Walsh Ave, Santa Clara, CA 95050.

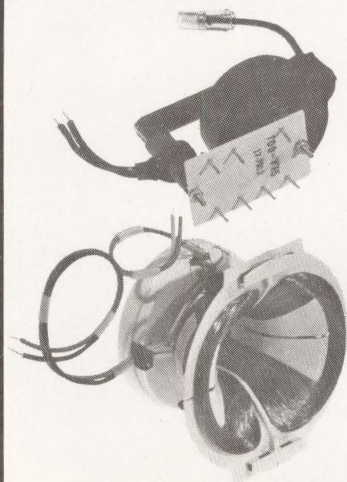
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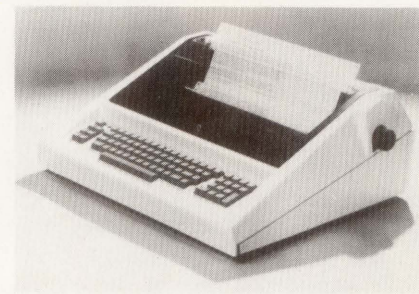


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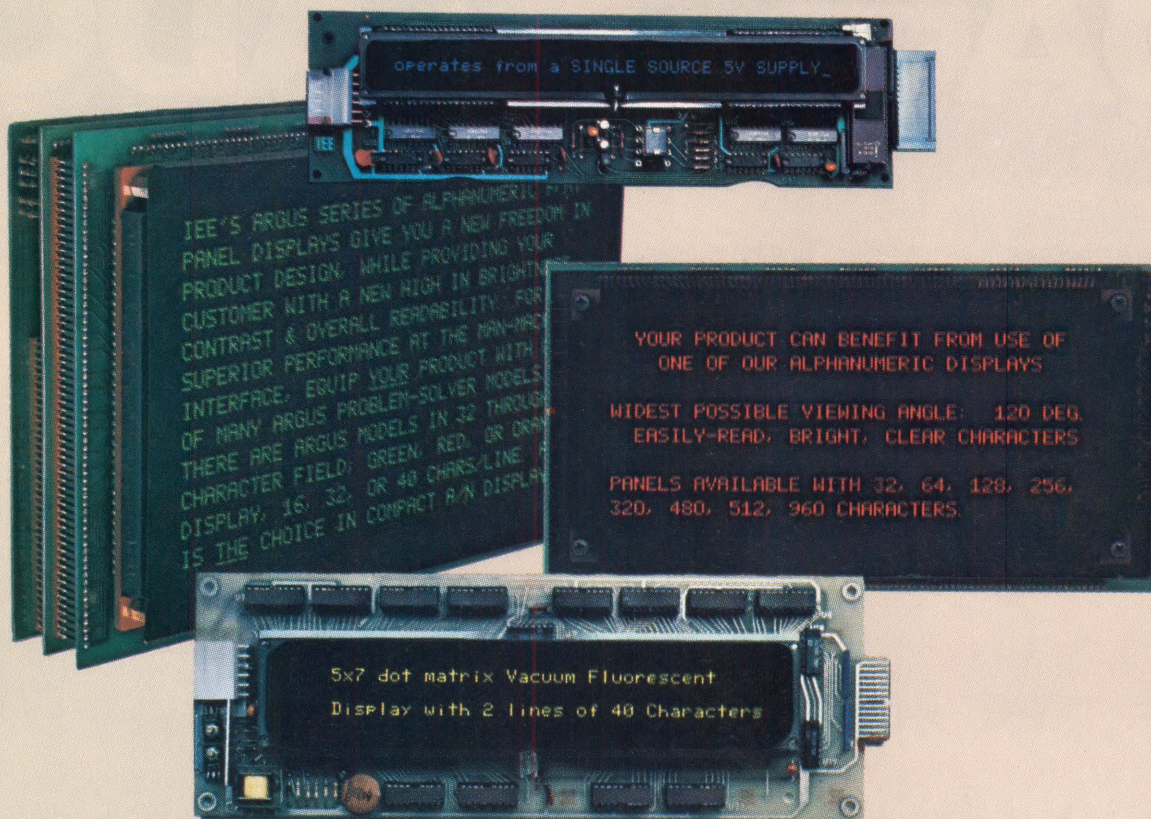
200-CHAR/s REMOTE PRINTER

Dual microprocessor control on 2510 series remote printing stations provides up to 200 char/s. A 9-pin matrix printhead is used for bidirectional printing with full underlining and true descenders. Model 2511 is an RO configuration, while 2516 is a KSR unit with full keyboard. A 1200-baud print rate can be sustained with bursts of 19.2k baud. A dc motor powered lead screw drives the printhead. The KSR version measures 21.9 x 18.5 x 8.5" (55.6 x 47 x 21.6 cm) and weighs 40 lb (18 kg). **Digi-Data Corp.**, 8580 Dorsey Run Rd, Jessup, MD 20794.



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We've designed a complete line of alphanumeric display modules so that you won't have to. Many of them simply require +5VDC and TTL level ASCII data from your host system to operate. What could be easier?

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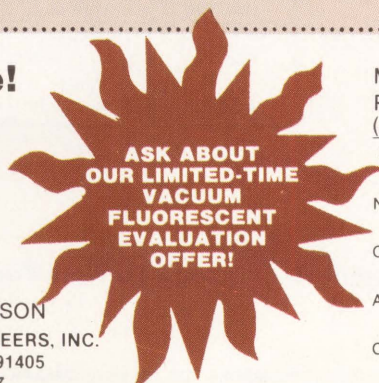
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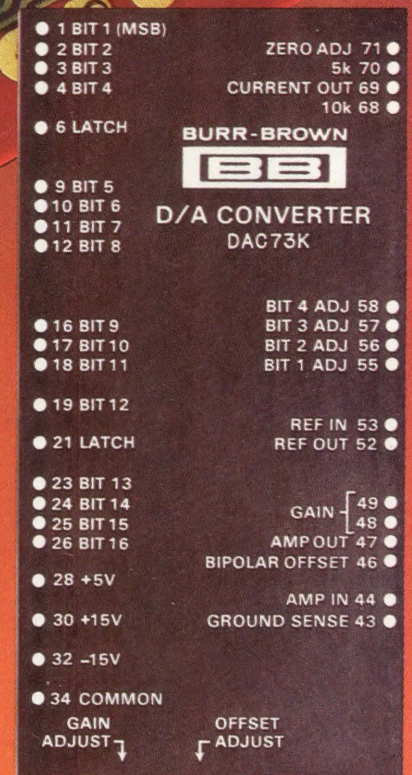
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Looking for realistically priced 16-bit converters? DAC71 is priced from \$45.70 in 100's. Burr-Brown, P.O. Box 11400, Tucson, Arizona 85734.

Burr-Brown Model	Package	Speed (max)	Non-linearity (max)	Total Accuracy Drift (max)
DAC70	Metal Dual-In Line	100μsec	±0.003%	±10ppm/°C
DAC71	Ceramic Dual-In Line	10μsec	±0.003%	±15ppm/°C
DAC72	Metal Dual-In Line	10μsec	±0.003%	±8ppm/°C
DAC73	2" x 4" x 0.4" Module	50μsec	±0.0007%	±22ppm/°C
DAC736	2" x 4" x 0.4" Module	50μsec	±0.0007%	±22ppm/°C
ADC71	Ceramic Dual-In Line	50μsec	±0.003%	±20ppm/°C
ADC72	Metal Dual-In Line	50μsec	±0.003%	±15ppm/°C



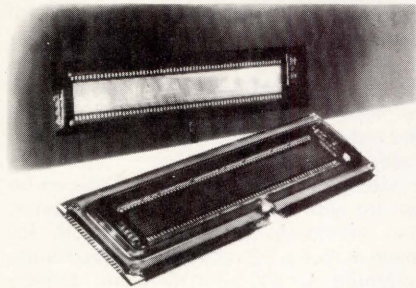
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PRODUCTS

256 x 26-DOT MATRIX ARRAY FLAT FLUORESCENT PANEL

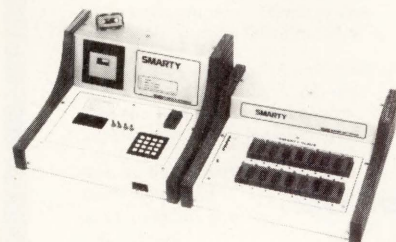


The randomly addressable "itron" DM256X26B, a 256-dot long x 26-dot wide flat vacuum fluorescent panel provides a continuous closely spaced dot pattern that emits high luminance and uniform blue-green display over a wide viewing area. It can display side to side scrolled messages, expanding or contracting dot matrix graphics, symbols, hieroglyphics, multisize alphanumerics, and varied pattern thicknesses and shapes. Phosphor dot pattern array measures 16.65-mm wide and 166.15-mm long. Each bright output dot is 0.4-mm square aligned between dots spaced on 0.65-mm centers in both X and Y directions. Complete panel size is 60 x 226 x 12 mm. Luminance is 200 ft-L typ, while luminance efficiency is 5.2 L/W. **Noritake Electronics, Inc.**, 22410 Hawthorne Blvd, Torrance, CA 90505.

Circle 217 on Inquiry Card

GANG EPROM PROGRAMMER

An addition to the Smarty P/ROM programmer, the 16-socket programming slave Sweet 16 allows 16 EPROMs of up to 32k bits to be programmed. Fifteen units can be daisy-chained for programming of 240 EPROMs simultaneously. A software intensive architecture makes it unnecessary to use pinout adapters when changing from one device type to another. A 2-char device selection and command code selects a device, lights an LED to confirm selection, and then initiates programming. **Sunrise Electronics**, 524 S Vermont Ave, Glendora, CA 91740.



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CIRCLE 146 ON INQUIRY CARD

BICOLOR DISCRETE LED INDICATORS

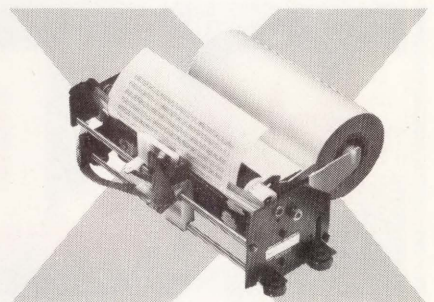
Discrete LED indicator lamps 521-9177 and -9178 are intended for high density packaging applications; -9177 is a 2-leaded device with red and green GaP chips mounted in parallel (with polarities reversed); -9178 is a 3-leaded device with red and green chips operating independently. Luminous intensities are 1.8 and 1.5 mcd, respectively, at 10 mA max. Both devices are available in T-1 3/4 packages with diffused dome lenses. **Dialight**, 203 Harrison Pl, Brooklyn, NY 11237.

Circle 219 on Inquiry Card.

900-LINE/MIN BAND PRINTER

B-900 includes interchangeable 48-, 64-, and 96-char set bands as well as specialized and foreign char sets. Print speed is 1100 lines/min at 48 char, 900 lines/min at 64, and 600 lines/min at 96. A diagnostic display monitors printing status at all times and a self-test feature allows performance monitoring independent of the computer. Parallel interface is std, but synchronous and asynchronous serial interfacing is available for remote operation. **Southern Systems Inc.**, 2841 Cypress Creek Rd, Ft Lauderdale, FL 33309.

Circle 220 on Inquiry Card



Fast, low cost printer.

This DC-4004A discharge printer prints 48 columns at 144 cps. Printing alphanumerics in 5 x 7 matrix format on 4.72" paper, its MTBF is 144 million characters. Just 2.6" H x 6.7" W x 5.9" D, it's only \$127 in 100 quantity. Other printers with interface electronics available.

Call or write **HYCOM**, 16841 Armstrong Ave., Irvine, CA 92714 — (714) 557-5252

HYCOM

CIRCLE 129 ON INQUIRY CARD

PRODUCTS

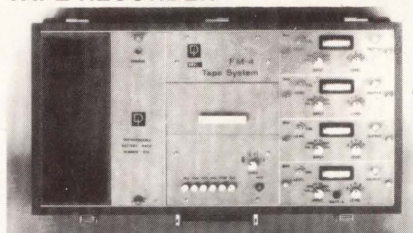
23M-BIT MILITARIZED TAPE SYSTEM

SETS-1 is a high performance storage unit for severe applications. A compact drive module is coupled to a sealed removable tape module with a 23M-bit capacity at 1600 bits/in (630/cm). The unit has bidirectional R/W capability on 4 tracks with a 192k-bit/s transfer rate and hermetically sealed media to prevent contamination. It has an operating temperature range of -40 to 71 °C and meets MIL-E-16400, 5400, and 4158. **EMM Sesco**, 20630 Plummer St, Chatsworth, CA 91311.



Circle 221 on Inquiry Card

INSTRUMENTATION TAPE RECORDER

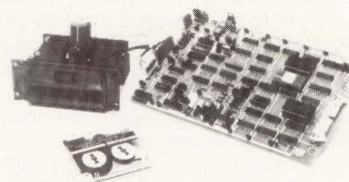


Model FM-4-4 offers 4 channels (record/reproduce) in a lightweight, battery powered package. Multispeed feature allows 8 to 1 time expansion/contraction capability along with a dc to 4-kHz frequency response. Voice comments (data interrupt channel 1), rechargeable battery pack, and remote control operation are all std. Ac or dc input coupling is provided and signals of 100 mV to 5 V peak may be recorded. Peak signal levels in record or reproduce modes may be monitored on separate channel meters. Input signals are amplified and buffered and are available at output BNC connector when record push button is depressed. Buffered output is amplified to provide 1.0 V zero to peak for full scale input signal, regardless of sensitivity range selected. **Dallas Instruments, Inc**, PO Box 38189, Dallas, TX 75238.

Circle 222 on Inquiry Card

MINICARTRIDGE RECORDER COMPUTER SYSTEM

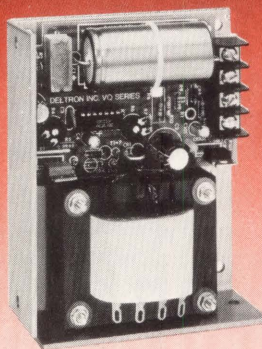
Designed for low cost and compactness, the STR-610 uses std 3M DC-100A minicartridges, and interfaces with mini/microcomputer systems using std programmable peripheral interface (PPI) devices, peripheral interface adapter (PIA) devices, or parallel interface controllers (PIO). Alternately, interface can be hooked directly into the system via the bidirectional address/data bus. Interface rate is 1.8k bytes/s. Within a system, strings of up to 4 drives can be set up with one drive acting as master, and providing formatting network for slave devices. PE recording is used while retaining an 800-bit/in (314/cm) density for data reliability via Speed-Tolerant Phase Encoded Recording decoding technique. Overall capacity is 168k bytes/track giving a 2-track total of 336k bytes. **Electronic Processors, Inc**, 1265 W Dartmouth Ave, Englewood, CO 80110.



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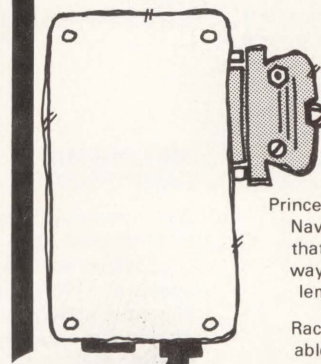
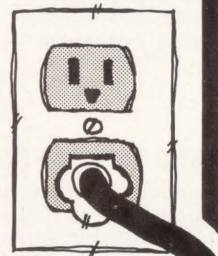
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AC 32

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THE \$99 MODEM*



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Write or call us now for a data sheet and complete price information.

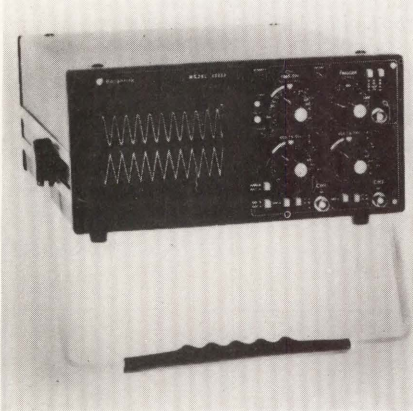
*100 Quantity

CIRCLE 148 ON INQUIRY CARD

PRODUCTS

UPDATED PORTABLE DUAL-CHANNEL OSCILLOSCOPE

Modifications to the 1032A bench/portable oscilloscope include increasing the range to 25 MHz, as well as pushbutton selection of ac/dc input coupling and a full and active TV sync stripper. Filters in the latter circuit are selected by switching logic on the sweep range control to provide automatic sync on either TV line or frame, depending on sweep speed range selected by the operator. **Ballantine Laboratories, Inc.**, PO Box 97, Boonton, NJ 07005.



Circle 224 on Inquiry Card

VIDEO INTERFACES FOR Q-BUS/UNIBUS SYSTEMS

Direct access alphanumeric and graphic video display interfaces for the Q-Bus and Unibus systems are available for use where serial display terminals are inadequate. Applications combining interactive portions of the monitor screen with realtime background display in split screen formats, such as in control room settings, are an example. The VIURAM interfaces employ onboard memory in a dual-port transparent design, thereby eliminating CPU contention problems. **Peritek Corp.**, 3014 Lakeshore Ave., Oakland, CA 94610.
Circle 225 on Inquiry Card

VARIABLE RELUCTANCE STEPPING MOTORS

Size 20 MR 209 and 206 stepping motors have a 15-deg (0.26-rad) step angle, step error of 0.5% of step angle with no load, and holding torque of 42 oz-in (0.294 N-m), and operate at 24 steps/r in temp range of -20 to 170 °C. Nom current is 1.4 A, rotor inertia is 12 g.cm² with stiffness at 2-deg (0.0349-rad) deflection. The 206 also includes integral lead screw. **Muirhead Vactric**, 1101 Bristol Rd, Mountainside, NJ 07092.
Circle 226 on Inquiry Card

LOGIC PROBE AND KIT

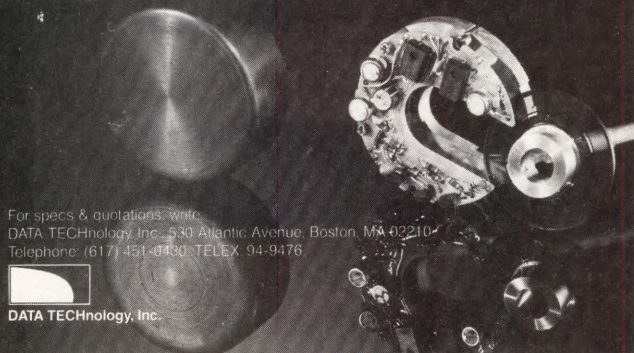


Model 205 "Catch-A-Pulse" handheld logic probe and model 205-K kit analyze and troubleshoot logic gates and sequential circuits. The probe, similar in size to a felt tip marker pen, has LED display for Hi, Lo, pulsing, or open circuit logic states. It automatically adjusts to the proper DTL, TTL, MOS, CMOS, or microprocessor circuit thresholds when its leads are connected to the IC circuit power supply. **Triplet Corp.**, 1 Triplett Dr, Bluffton, OH 45817.
Circle 227 on Inquiry Card

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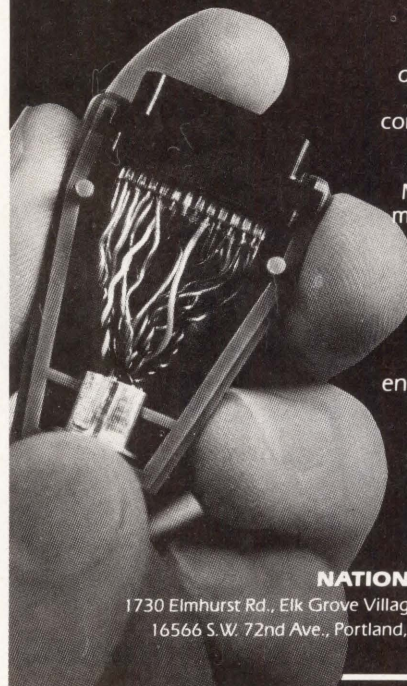


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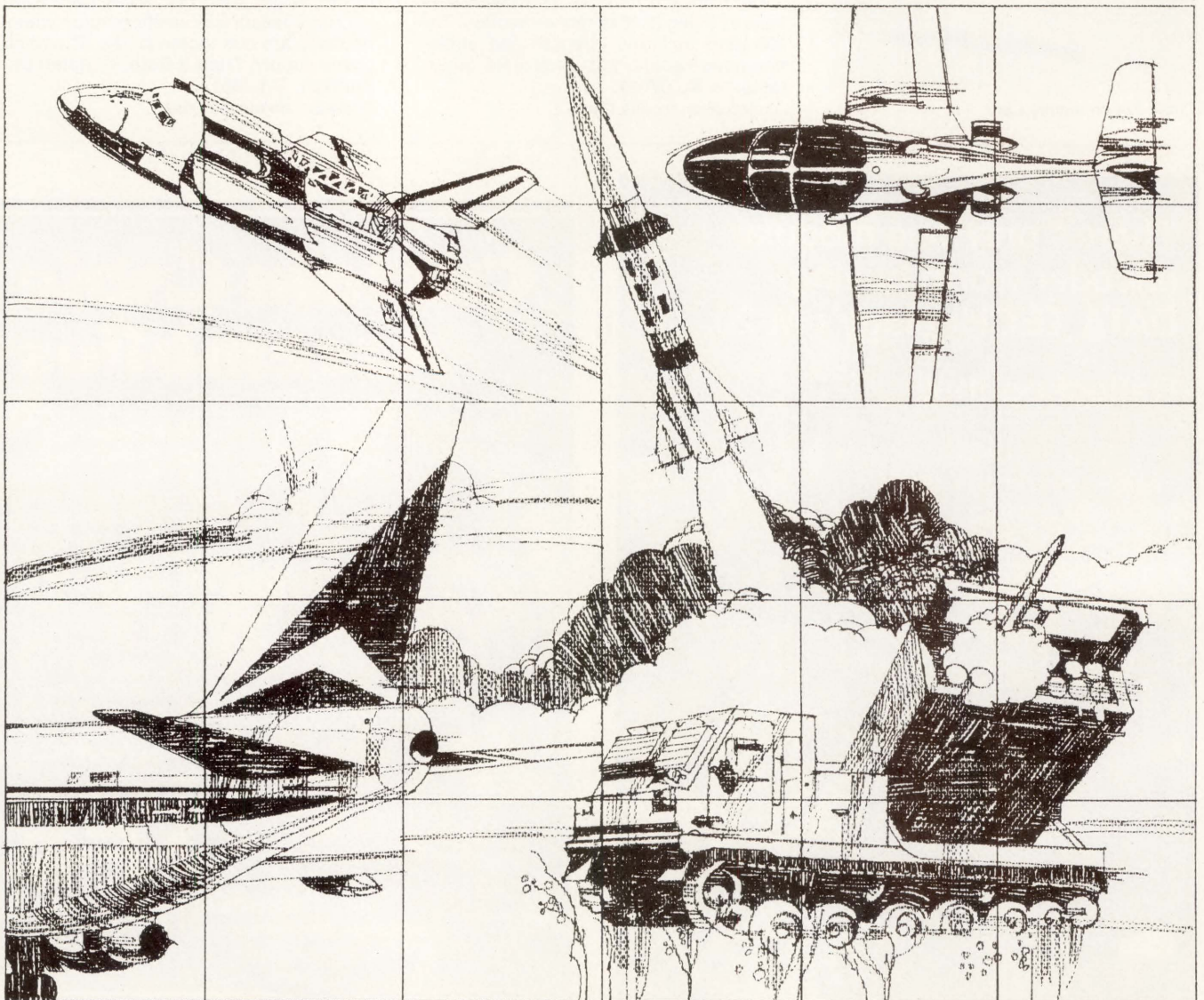
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PRODUCTS

DOCUMENT PRINTER FOR IBM 3270



Model 2120 demand document printer, developed for use with the IBM 3270, provides immediate access to the last printed document, and a tear-off bar provides clean cut-off just below the last printed line to avoid wasting forms. It is available in type B (3271/72) or type A (3274/76) compatibility (including SDLC), and in all buffer sizes. **Interface Systems, Inc.**, 462 Jackson Plaza, Ann Arbor, MI 48103.

Circle 228 on Inquiry Card

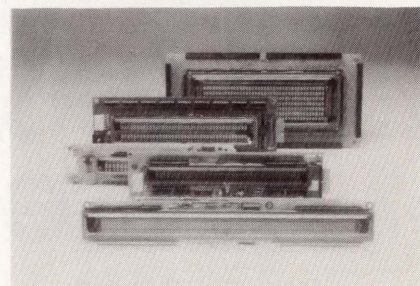
FIXTURE CARDS FOR BACKPLANE TESTER

NF600 series features design improvements that make it easier for users to manufacture extender boards which adapt std modules to backplane shelves and connectors of various sizes. Gold fingers on the card mate with std card edge connectors. User supplied card edge connectors fit extender boards of various thicknesses for flexibility. Plated-through holes spaced for ribbon cable headers are also provided. Containing solid state switching and logic necessary for continuity testing, the cards are electrically compatible with the company's other fixturing methods for interconnect verification. Custom ICs on the cards carry out addressing and testing functions directly at the unit being tested. Each fixture card has a pair of flexible 14-wire daisy chain cables which connect it to other cards in series. Units come in 64-, 88-, and 128-pin sizes to accommodate a range of backplane connectors. **Teradyne, Inc.**, 183 Essex St, Boston, MA 02111.

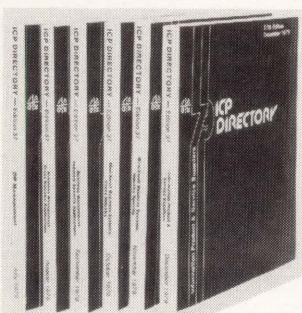
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VACUUM FLUORESCENT DISPLAY MODULES

Vacuum fluorescent 14-segment type display modules require ASCII serial or parallel data and 5 Vdc. The Flip 3700 series of 7 displays includes some that are less than 1" (2.54 cm) deep and some that are "drop-in" replacements for modules previously offered by only one supplier. Modules will display upper case letters, numbers, symbols, and punctuation. **Industrial Electronic Engineers, Inc.**, 7740 Lemona Ave, Van Nuys, CA 91405.



Circle 230 on Inquiry Card



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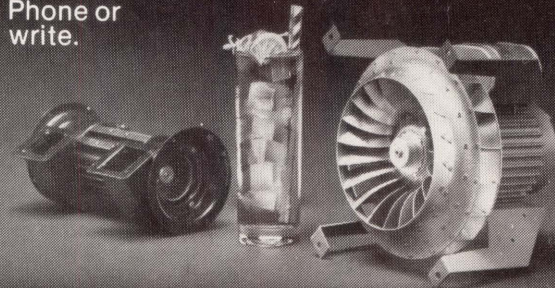
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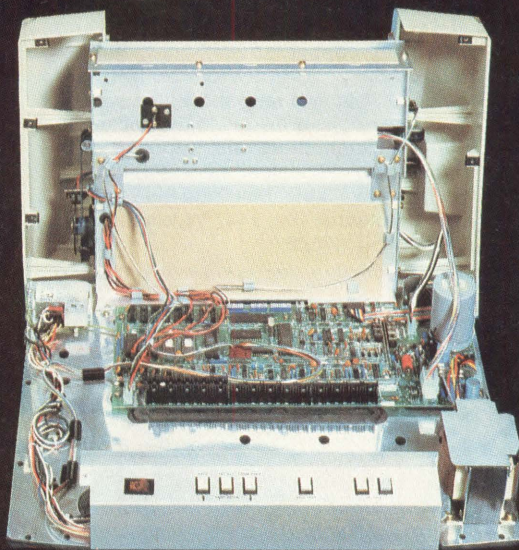


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The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

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The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-

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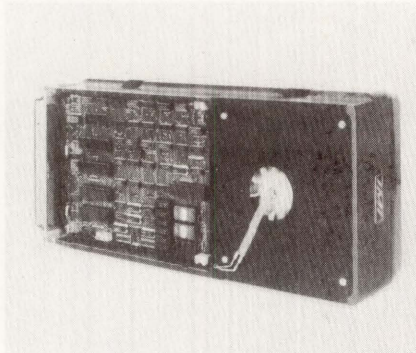
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CIRCLE 155 ON INQUIRY CARD

PRODUCTS

8" WINCHESTER DRIVES WITH SINGLE BOARD CONTROLLER



An embedded controller provides an asynchronous parallel interface between 8" (20-cm) Winchester drive and CPU; software routines previously executed by the CPU can be handled by controller firmware. For example, the embedded controller performs diagnostics from servo tests to media verification. The controller fits within the company's 10M- and 20M-byte models. Access time is 35 ms and power required is 75 W. **International Memories Inc.**, 10381 Bandley Dr, Cupertino, CA 95014.

Circle 231 on Inquiry Card

2-PIECE PCB CONNECTOR

191/192 series connectors with 107 contacts on 3 rows of 0.050" (1.27-mm) staggered centers have diallyl phthalate MIL-M-14F type SDG-F insulators and beryllium copper socket contacts per MIL-C-55302. Connector bodies are polarized both visually and with pins. Optional keying is provided in the socket insulator. Connectors are supplied with right angle dip solder tails. Plating options are available. **Method Electronics, Inc.**, Connector Div, 7447 W Wilson Ave, Chicago, IL 60656.



Circle 232 on Inquiry Card

CONTROL CABLES

Suitable for interconnection of instrumentation and control system components, Dataflex™ cables are insulated and jacketed with an irradiation cross linked thermoset polyolefin that resists melting and flowing when exposed to heat. They contain no PVC, asbestos, or fibrous material, meet VW-1 flame tests, and have 125 °C UL listing. Completed cables, specified for 600-, 300-, or 150-V ratings, will pass an IEEE 383 vertical tray fire test at 70k Btu (73.85M J)/h. **ITT Surprenant**, 172 Sterling St, Clinton, MA 01510.

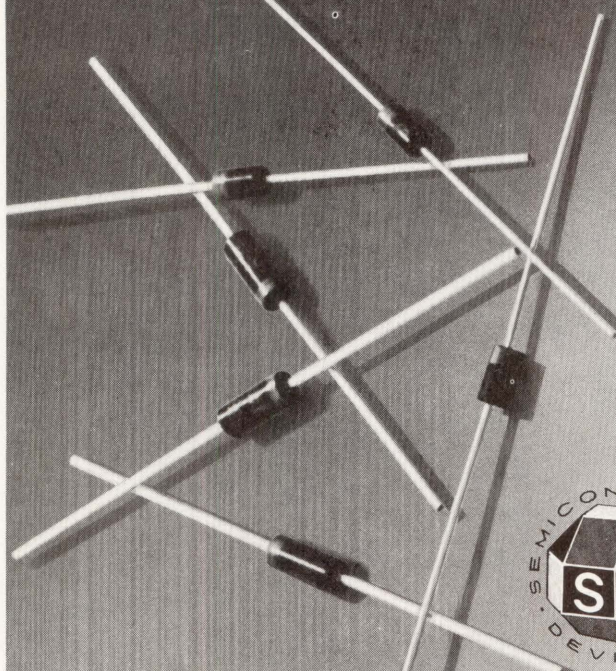
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SWITCHING POWER SUPPLY TESTER

JADEC J 500 tester consists of a sequence control unit, 4 load control units, 4 load power units, input ac power variac, and ammeters and voltmeters to test a supply with positive and negative outputs. Five digital voltmeters are provided, 1 for each voltage output and 1 for dc current. The unit will test power supplies up to 300 W and is capable of short circuit testing and interlocking power-up for operator protection. **Jadec**, PO Box 2241, Sunnyvale, CA 94807.

Circle 234 on Inquiry Card

New ultra high speed Silicon Rectifiers in epoxy cases.



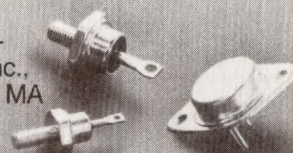
Axial lead Silicon Rectifiers with very fast recovery characteristics are now available in low cost epoxy case styles. An ideal alternative to high priced glass units, these high surge devices give unsurpassed performance through 400 volts.

Field proven in countless industrial and computer applications, these units are especially attractive for high efficiency switching power supplies.

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You can choose from the industry's widest range of very fast rectifiers with recovery times from 30 to 50 nsec max. Features include 20 to 70 amp ratings, low V_F , high surge and low leakage.

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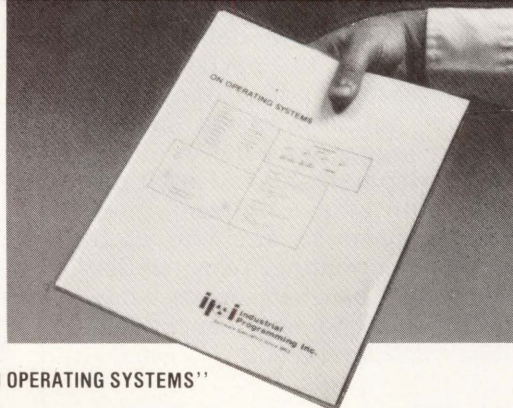
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PRODUCTS

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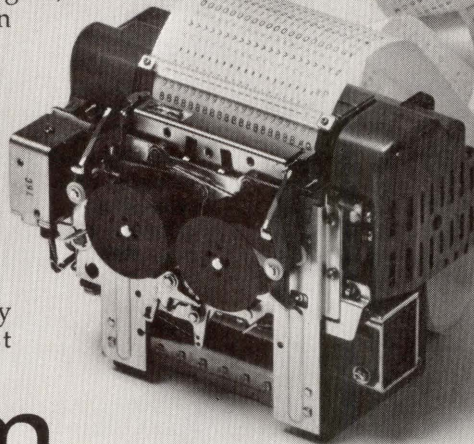
516M-BYTE REMOVABLE DISC DRIVES



T-600/602 achieve increased capacity by using narrower heads of manganese zinc ferrite core, which increase output by 25% and resolution by 5%. Other enhancements include rewriting the servo surface of conventional 3330 II-type media to provide 1349 cylinders, maximizing servo electronics to control positioning, optimizing read/write electronics to meet performance specs, tightening mechanical tolerances, and modifying logic to address additional cylinders. T-600 has std Trident TTL/DTL interface, and T-602 has SMD (differential) interface compatible with range of independently available controllers. TTL/DTL interface drives have capacity for 27M, 54M, 82M, 208M, 312M, and 516M bytes of unformatted data; SMD drives hold 83M, 210M, 315M, and 516M bytes. **Century Data Systems, A Xerox Co.**, 1270 N Kraemer Blvd, Anaheim, CA 92803. Circle 236 on Inquiry Card

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Sometimes you need a dependable workhorse that will do the job efficiently, reliably, day after day. Like the compact drum printers from C. Itoh. Our Model 102 18-column digital, for example, weighs in at only 3.3 lbs., but it's more dependable than many units costing far more. Or our Model EP-101: it's at home in a lot of applications, but, like all our drum printers, it doesn't take much power—only 17 VDC. Or our most



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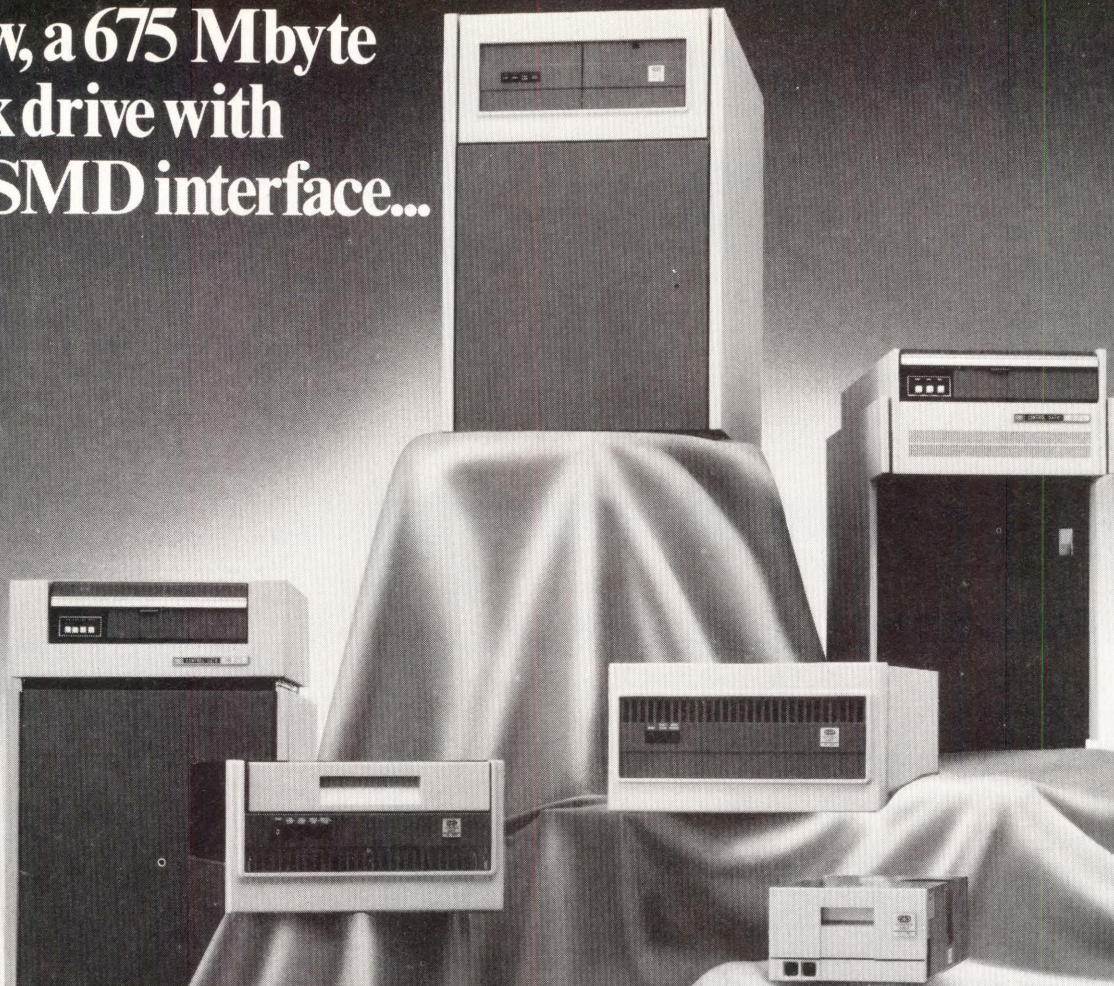
19-mm 1-W OUTPUT MOTOR

Employing a Faulhaber skew-wound rotor system, the 12 x 19-mm series 1219 micromotors are available in 4.5-, 6-, 9-, 12-, 15-, and 18-Vdc models. Capable of operating at up to 21,500 r/min with efficiencies to 85%, the motors fit standard 12/1 screw-on gearheads, providing ratios of 6:1 to 1M:1. Low starting voltage and armature inertia, short time constants, and linear voltage-speed and speed-torque characteristics are featured. Mounting flanges are optional. **Micro Mo Electronics**, 3691 Lee Rd, Cleveland, OH 44120.



Circle 237 on Inquiry Card

Now, a 675 Mbyte
disk drive with
an SMD interface...



...from the people who invented the SMD.

Control Data's new 9775 Fixed Module Drive is at the peak of today's capacity range — 675 Mbytes plus an optional 1.9 Mbytes of fixed-head-per-track storage for fast access.

And better yet, it comes with our popular SMD interface. So it can be attached to the same controller that you probably are using already. That means you don't have to change your basic system design every time your storage requirements change. That means easier system integration and simple field upgrades.

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CIRCLE 159 ON INQUIRY CARD

PRODUCTS

HANDHELD COMPUTER TERMINAL

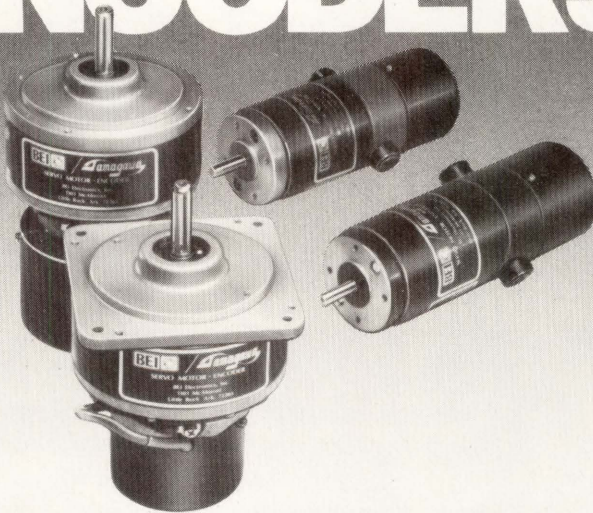
Portable terminal based on LK-300 personal computer, LK-2010 communicates with host by means of std RS-232 telecommunications interface. Plc telephone receiver on acoustic coupling and plugging in computer with communication module allows user to enter data, review it on 16-char scrolling LED



display, and transmit it to host computer. Similarly, user can access host to receive stored data. The RS-232 compatible unit operates at rates from 110 to 300 bits/s, asynchronous half- or full-duplex. Terminal display is a 16-char, 16-segment alphanumeric LED with integrated MOS LSI display controller. It uses 8-bit word length including parity, 3 stop bits, and 80-char display buffer. Other modules transform unit into language translator, filing system, calculator, or programmable note pad. **Nixdorf Computer Personal Systems, Inc.**, 168 Middlesex Tpk, Burlington, MA 01803.

Circle 238 on Inquiry Card

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PROGRAMMABLE TRANSIENT RECORDER




A microprocessor based 2-channel recorder, DL1080 may be controlled automatically by a computer or used in freestanding operator controlled environment. A waveform acquisition and measurement instrument for one-shot and low repetition events, it offers an integral minicassette backup store and full compatibility with GPIB interface protocol. It can simultaneously digitize and store waveforms at sample rates up to 20 MHz/channel in each of 2 static RAMs having 4k x 8-bit capacity. Selection of recording parameters is done by means of single control knob. Recording modes include delayed sweep, dual speed timebase, and pretrigger modes, as well as zoom sweep recording, which allows one channel to zoom in at a high sample rate on an interesting region of the other channel. **Kontron Electronic Inc.**, 630 Price Ave, Redwood City, CA 94063.

Circle 239 on Inquiry Card

HORIZONTAL CARD CAGE

A single enclosure that allows users to combine analog and digital PC cards also allows combining wirewrap with stitch weld and stitch wire boards. Optional guide separator locations permit mixing of single-, double-, and triple-width boards. Cages are available with either continuous backplane or 3 separate backplanes to accommodate different voltages and grounds. **Augat Inc., Interconnection Systems Div.**, 40 Perry Ave, Attleboro, MA 02703.

Circle 240 on Inquiry Card



UDS technology

accelerates to 9600 bps

The accelerating growth in modem technology at Universal Data Systems has now produced the Company's first 9600 bps unit on a super-compact OEM board. Occupying about 100 square inches of PCB space, this microprocessor LSI modem offers dramatic space savings for designers who wish to package data sets internally in microcomputers, minicomputers or interactive terminals. The traditional UDS economy and reliability are inherent in the new 9600 bps modem.

Contact UDS for complete technical details, or phone your UDS representative. Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone: 205/837-8100.

"Confidence in Communications"

Universal Data Systems



Member
IDCMA

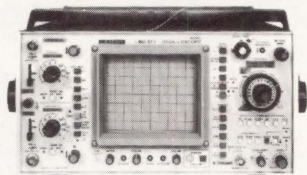
DISTRICT OFFICES: Summit, NJ, 201/522-0025 • Blue Bell, PA, 215/643-2336 • Atlanta, 404/952-3463 • Chicago, 312/441-7450 • Dallas, 214/385-0426 • Santa Ana, 714/972-4619 • Sunnyvale, 408/738-0433 • Boston, 617/875-8868.

CIRCLE 161 ON INQUIRY CARD

Created by Dayner/Hall, Inc., Winter Park, Florida

PRODUCTS

50-MHz DUAL-TRACE PORTABLE OSCILLOSCOPE



Features and capabilities previously available only on expensive laboratory instruments, including a calibrated time base for accurate measurements and observations of complex waveforms or long pulse trains, are incorporated in the LBO-517 50-MHz dual-trace portable oscilloscope. Main and delayed time bases can be displayed simultaneously for both input channels. An alternate triggering mode allows comparison and measurement of 2 frequency unrelated signals. **Leader Instruments Corp.**, 380 Oser Ave, Hauppauge, NY 11787.

Circle 241 on Inquiry Card

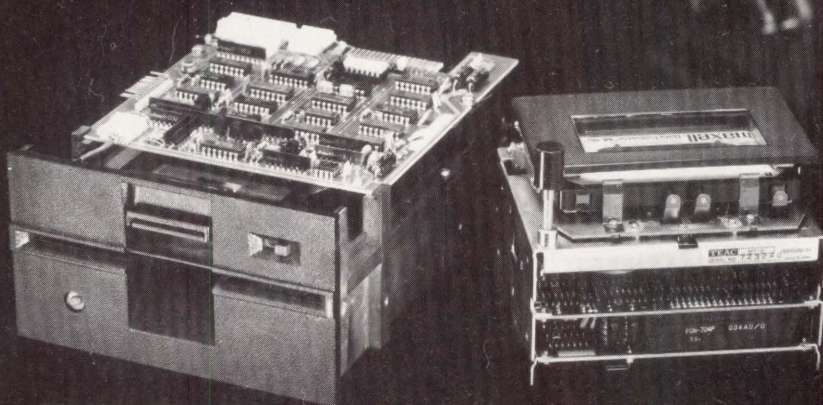
LOW COST CRT TERMINAL



Model 550B incorporates proprietary LSI controller chip that allows a fully featured design with only 19 ICs and gives it a calculated MTBF of 5 yrs in an office environment. Std features are audible alarm (bell); switchable new line wraparound, allowing multiple-line display of data formatted for more than 80 columns; extended numeric mode including +, -, *, and / keys; and support for dual character sets. Easy to read characters, including lower case letters with true descenders, are formed on a 7 x 10-dot matrix. Keyboard includes an embedded numeric pad and dedicated keys for repeat, on/offline, print, tab, shift lock, and backspace; an all-case DEL key; and a control protected clear. Transparent mode displays all 128 ASCII char. The screen is switchable between black on white or white on black. **Perkin-Elmer Terminals Div.**, 360 Rt 206 S, Flanders, NJ 07836.

Circle 242 on Inquiry Card

TEAC. A newcomer?



Well, Yes and No.

YES, we are introducing 5 1/4" floppy disk drives.

NO, we are not new in the digital recording field; in fact we are a leader in digital cassette recorders with over 200,000 units already sold.

And with a solid 25 years of expertise in magnetic recording technologies—digital, analog, video, and of course our popular stereo tape decks—we *know* how to design and build recorders (to put it modestly).

Now you can have a reliable
Floppy Disk Drive or
Digital Cassette Recorder—
when it bears the name TEAC.

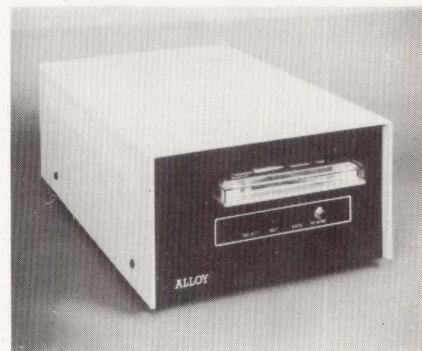
TEAC

TEAC Corporation of America
Industrial Products Division

7733 Telegraph Road Montebello, California 90640 (213) 726-0303

CARTRIDGE TAPE SUBSYSTEM FOR WINCHESTER DISC BACKUP

TIP (tape interchange package), an S-100 compatible subsystem with comprehensive menu driven software, allows transfer of program and data files from a Winchester disc to a 13.4M-byte 0.25" (6.35-mm) cartridge tape. It is comprised of a DS-100 controller, 6400-bit/in (2520/cm) tape drive, and power supply, and installs by plugging into an S-100 computer system. Software is distributed on a single-sided, double-density 8" (20-cm) floppy disc in CP/M format. **Alloy Engineering Co., Inc.**, Computer Products Div, 85 Speen St, Framingham, MA 01701.



Circle 243 on Inquiry Card

STR® technology for high data integrity. Three major tape formats for design flexibility.



We don't forget the OEM's needs.

The **STR-810** digital recorder is designed for data logging, data acquisition and as a system loader. Using either the 3M DC-300A or DC-300XL cartridges, packing density is 1600 bpi, for respective data capacities of 2.3M bytes and 3.4M bytes per cartridge, using four tracks. Features include microprocessor-controlled tape movement and read/write electronics. For maximum versatility, interfaces include RS-232 and IEEE-488. Or, using control and status lines available, you can interface to specific microcomputers such as LSI-11 and 8080. EPI's optional ANSI X3.56 formatter, with NRZI or phase-encoded personality cards, turns the 810 into a plug-in component for industrial instrumentation and mini/microcomputer-interfaced peripheral markets. Price: \$756 in quantities of 100. **STR-STREAM** is a high-speed, high-capacity version of the 810 designed for Winchester disc backup. Density is 6400 bpi for 17M bytes capacity per cartridge. Features include advanced head design, MFM formatting and compatibility with 8" or 14" discs.

EPI's STR-610 is a compact, low cost digital recorder that's ideal for use with POS terminals, smart CRT terminals and as a general peripheral for mini/microcomputer-based systems. The 610's recording density is 800 bpi for a capacity of 168K bytes/track, using a two-track 3M DC-100 mini-cartridge. Formatting is ANSI Standard and interfacing is parallel, with a variety of options. Price: \$280 in quantities of 1,000. **The STR-LINK III** is a high-speed (9600 baud), portable program loader that uses the STR-610's drive system and shares the same specifications. It is used as a field service tool for diagnostic work or as a peripheral in a mini/microcomputer system. STR-LINK III uses a serial RS-232 interface for data communications or data terminal applications, and it can be controlled through RS-232, ASCII control codes, or manually. Price: \$1,561 in single quantity.

STR-LINK II is EPI's proven medium-speed (1200 baud) universal portable program loader for programmable controllers and process control systems. Using a standard cassette, it features switch-selectable transmission modes for maximum flexibility. Price: \$1,735 in single quantity.

For maximum design freedom, proven reliability and high data integrity through Speed Tolerant Recording technology, remember EPI—the company that doesn't forget the OEM's needs. For more information, contact Electronic Processors Inc., P.O. Box 569, Englewood, Colorado 80110. Phone (303) 761-8540.

E0/3

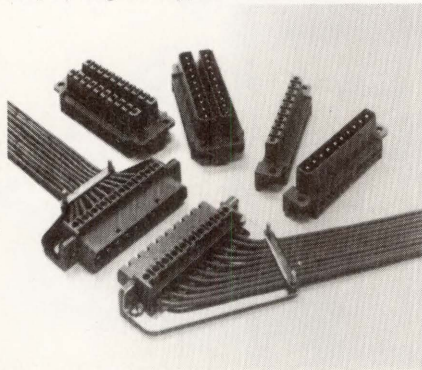
Let EPI remember for you.

**ELECTRONIC PROCESSORS
INCORPORATED**

PRODUCTS

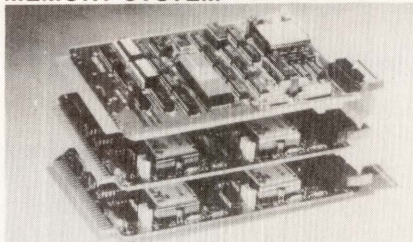
20-A SOLDERLESS CABLE CONNECTOR

Quick-Connect 10-pin solderless cable connectors combine screw clamp wire termination with the ability to be mounted in several ways on flat surfaces or through panels. They can be mounted in pairs to provide 20 contacts/set, or side by side without interference when disconnecting, have 300-V UL rating at 20 A/contact, and accept wire up to 12 AWG. The molded nylon connector body fully encloses screws and clamps. **Cogenel, Inc./Entrelec Div.**, 2 Ram Ridge Rd, Spring Valley, NY 10977.



Circle 244 on Inquiry Card

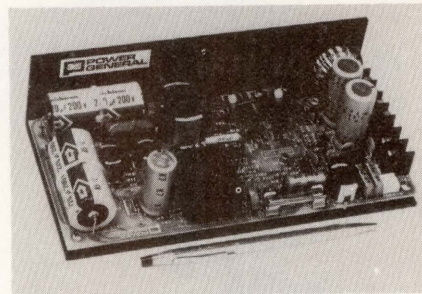
MAGNETIC BUBBLE MEMORY SYSTEM



TBB7090 and TBB8091 are completely assembled and tested memory systems that are supplied with 1, 2, 3, or 4 92k-bit TIB0203 bubble memories for 11.5k, 23k, 34.5k or 46k bytes of storage, respectively, on a single board. The -7090 is a complete system containing 11.5k bytes of nonvolatile memory storage and all necessary support circuits, including custom controller. The -7091 expansion system, designed for use with the -7090 to provide system storage capacity of 104k bytes, contains up to 46k bytes of memory; two -7091 boards can be used with one -7090 board. Both are available in 0 to 50 °C and 0 to 70 °C temperature ranges, and are bus and timing compatible with Pro-Log and Mostek STD-BUS series microcomputers. They feature low power operation, 4-ms access time, 50k-bit/s data transfer rate, and use 5- and ± 12 -V power supplies. **Texas Instruments Inc.**, PO Box 225012, Dallas, TX 75265. Circle 245 on Inquiry Card

60-W SWITCHING POWER SUPPLY

Series 1060 switchers provide output power of 5 Vdc at 12 A and may be adjusted from 4.5 to 5 Vdc. Full rated output is provided over an ambient temperature range of 0 to 50 °C with 2%/°C derating to 70 °C. Power supply input offers pin strappable voltage ranges of either 85 to 130 Vac or 170 to 260 Vac at 47 to 470 Hz for European applications. An rfi input line filter is std. All ac line filter capacitors are high quality and have VDE, S, N, D, OVE, and other European approvals. Half-bridge configuration, used to do the switching, achieves efficiency of 80%, ripple and noise of 50 mV pk-pk or 10 mV rms. Line and load regulation is $\pm 0.1\%$, tempco is $\pm 0.02\%/^{\circ}\text{C}$, and transient response is 200 μs to 1% of final value. **Power General**, 152 Will Dr, Canton, MA 02021.



Circle 246 on Inquiry Card

Model EP-2A-88 EPROM Programmer



Fast as Jackrabbits . . . Well, almost!

In Australia, two rabbits can reproduce over 13 million offspring in 3 years . . . at 105 seconds per 2716, the EP-2A-88 can reproduce 1,892,160 EPROMS in 3 years. Single push button control, the EP-2A-88 checks if EPROMS are erased, programs and verifies. It also checks for defective EPROMS.

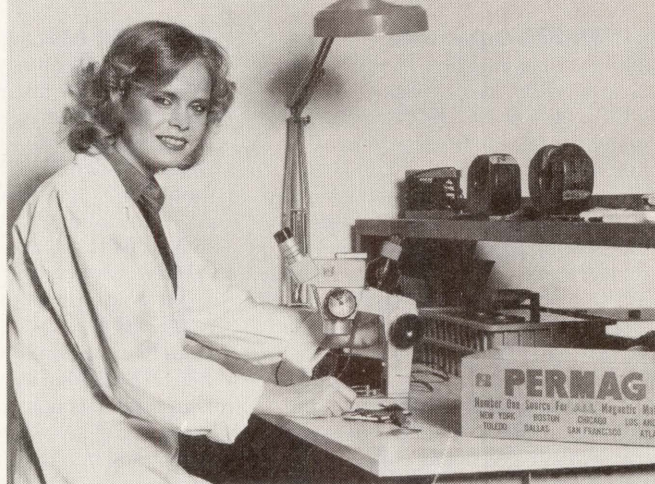
Two basic models are available, The EP-2A-88-1 will accept Copy (CM) modules for the 2758, and 2716 EPROMS. The EP-2A-88-2 will accept copy modules for the 2716, 2732 and TMS 2532 EPROMS. Power requirements are 115 VAC 50/60 Hertz at 15 watts.

Part No.	Description	Price
EP-2A-88-1	EPROM Programmer	\$450.00
EP-2A-88-2	EPROM Programmer	450.00
CM-50	Copy Module for 2716, TMS 2516 EPROMS	25.00
CM-70	Copy Module for 2758 EPROMS	25.00
CM-20	Copy Module for 2732 EPROMS	25.00
CM-40	Copy Module for TMS-2532 EPROMS	25.00
	Non-Standard Voltage Option (220 v, 240 v, 100 v)	15.00

Optimal Technology, Inc.
Blue Wood 127, Earlysville, Virginia 22936
Phone (804) 973-5482

CIRCLE 164 ON INQUIRY CARD

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...PERMAG's materials are subjected to quality control requirements that are the standard of the industry. When it comes to magnetic measuring, magnetizing and calibrating and magnetic testing, PERMAG has the skilled engineers and technicians to assure you of consistently superior results. Each of our 9 modern plants is stocked, staffed and equipped to meet your every need.

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CIRCLE 165 ON INQUIRY CARD



**Remember When We Had To Go To Different Stores
for Math Processors, Industrial I/O and Sensor Conditioning.**

Your challenges are too complex to depend on modules that come from different sources -- especially modules that were not designed for hostile plant environments. We now have a broad line of modules that covers virtually all industrial applications.

But modules are only part of our story. XYCOM offers a broad line of packages, modules and software designed specifically for industrial applications. We even have analog subsystems that interface directly to a broad range of primary sensors. Our growth in the highly specialized

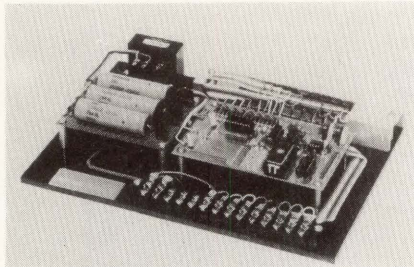
industrial microcomputer field has caused us to be referred to as 'The Hardhat Computer People'—and with good reason. The trend today is to put the control or target computer out on the plant floor with the operator. To do so, you've got to have equipment that is designed, built and tested specially for the hostile plant environment. Simply adapting general purpose hardware isn't the answer.

So, to get the real answers call your local XYCOM office or call XYCOM World Headquarters-(313)429-4970

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The Hardhat Computer People®
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PRODUCTS

P/ROM BASED SOLID STATE TIMERS

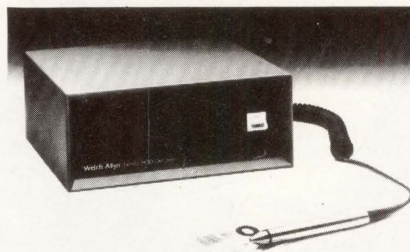


PROM-8 handles complex sequences of on/off steps using 8 load circuits, with up to 256 steps/complete cycle. The basic solid state timer is fully programmed to customer specifications when shipped. Almost any degree of timing precision can be set up by the manufacturer through substitution of special time bases. Optional use of line current counters provides interval durations of any length up to several hours. **Bayside Timers, Inc.**, 43-69 162nd St, Flushing, NY 11358.

Circle 247 on Inquiry Card

DATA ENTRY TERMINAL FOR BAR CODE SYSTEMS

HBD series terminal provides bar code reading capability to existing computer based data collection systems but also functions independently as a bar code decoder with a std 120-Vac power source and a compatible data display unit. Data communication uses a serial ASCII format and RS-232-C compatible signal levels. Included are A-D signal conditioner, digital date mixer, and signal interface unit. **Welch Allyn, Inc., Industrial Products Div.**, Skaneateles Falls, NY 13153.



Circle 248 on Inquiry Card

675M-BYTE DISC DRIVE SUBSYSTEM

A Winchester disc drive with 675M bytes of random access storage in a fixed, sealed media drive operates with other members of the company's storage module drive family but has twice the capacity. Features include light load, contact start/stop head designs, and microprocessor control of the servo. Avg seek time is 25 ms and avg latency time is 8.3 ms, for a total avg access time of 33.3 ms. Transfer rate is 9.67 MHz. **Harris Corp., Computer Systems Div.**, 2101 W Cypress Creek Rd, Ft Lauderdale, FL 33309.

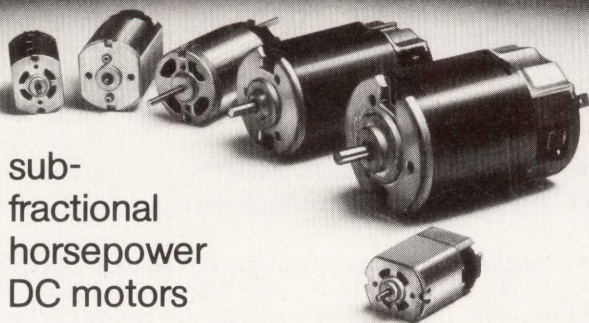
Circle 249 on Inquiry Card

VIDEO TERMINAL EMULATORS

Capable of emulating Lear Siegler ADM 3A, Hazeltine 1410 and 1500, and DEC VT52 and VT100, 3 video terminals provide alphanumeric asynchronous ASCII capabilities. 4410, 4420, and 4430 terminals feature green, non-glare display and operate in individual enhanced modes to increase flexibility; 4420 and 4430 have detached, low profile keyboards, tiltable screens, and smooth scrolling. **Facit AB Data Products**, 105 45 Stockholm, Sweden.

Circle 250 on Inquiry Card

Customized



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fractional
horsepower
DC motors

Buehler Products, Inc. offers a complete line of permanent magnet DC motors that are performance rated to your specific application for maximum cost effectiveness. These customized, long life Buehler motors are available with a wide variety of options in voltage, current, torque, speed, electrical connections, and frame size. They're used worldwide in office products, business machines, cameras, computer peripherals, tape recorders, marine and automotive applications. Write for full details on the Buehler FHP motor line.

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Precision Mount,
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Industrial mount,
Exceptionally versatile.

Three typical Vikron magnetic heads that come equipped with total service. That simply means we're not done helping you until you're done needing help.

We deliver much more than quality magnetic heads!

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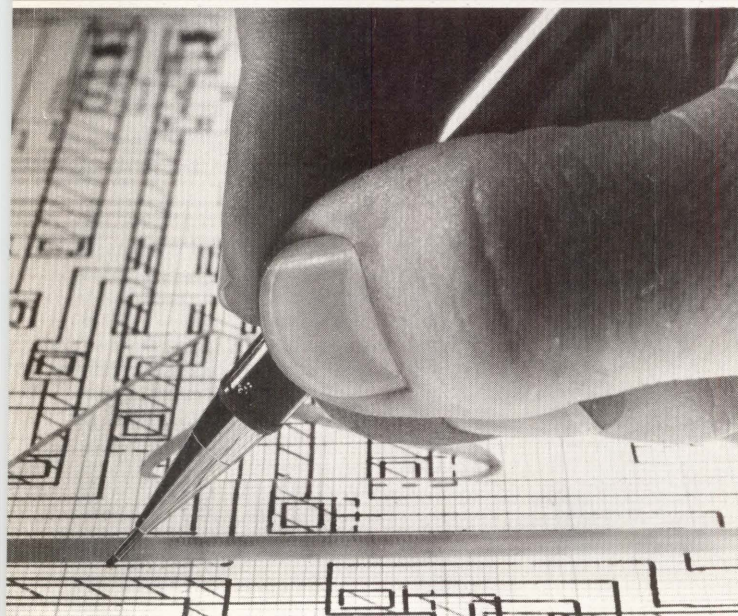


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"Every time we ask a MOS/LSI company about their custom experience, they change the subject."



That's no surprise. Most MOS/LSI companies take on custom work only when market conditions force them to. And, no matter how big they may seem, they're usually only willing to handle a few limited jobs. So they really don't have much custom experience worth talking about.

AMI does. As the leader in the field, we have 14 years of successful custom work behind us. Since we opened for business in 1966, our engineers have designed over 1,300 LSI circuits. And for the entire period of time, custom has been the major — and most important part — of what we do.

We've designed circuits for appliance and consumer electronics companies, the telecommunications and EDP fields, the automotive industry and the military. In fact, we've created custom solutions for virtually every kind of company.

Which means that whatever business you're in, you can be just about certain that we'll understand your problems. And that we'll be able to offer you a MOS system solution tailored to the exact needs of your application.

We can design a MOS peripheral circuit for you that will interface with any standard micro-power memory and 4-, 8- or 16-bit microprocessor (ours or someone else's). Or we can offer you one of our own standard circuits customized to your specific requirements.

We've also designed complete systems on a chip with as many as 60,000 devices, and we're able to combine both linear and digital circuitry on the same piece of silicon. So if you need a chip with

switched capacitor filters, A/D and D/A converters and other linear type circuits, we can give it to you.

What's more, our SIDS (Symbolic Interactive Design System) is the world's most advanced design system. It's the reason we've been able to cut design time while producing increasingly more complex circuits.

We're very flexible. AMI's engineers work in 14 variations of the three major MOS processes: the very mature P-channel, high speed, state-of-the-art N-channel and CMOS. So when the time comes for you to choose the process you want, unlike other companies, we have no limitations to impose on you.

But AMI's flexibility doesn't end there.

If you want to design your own LSI circuits, we make it easy for you to work with us. We can interface with you at any stage of chip development, and we have the industry's only group specially organized to handle customer designed circuits. In six years, they've managed the production of over 750 of these circuits.

You'll be in good company. AMI's list of satisfied customers includes some of Fortune 500's biggest companies. But we work for a lot of small and medium size companies, too. That's another part of our flexibility. We're set up so that we can provide cost-effective, state-of-the-art results for just about any size company — and just about any size job.

If what AMI has to offer sounds like what you've been looking for, mail in the coupon. We'll send you two books that will help you decide if custom MOS is right for your application and tell you everything you should know about AMI's custom capability.

It's really the quickest way for you to start taking advantage of our experience.

I want to know more about AMI's custom LSI capabilities.

☐ Send me the books. ☐ Have your applications engineer contact me.

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Company _____

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Phone _____

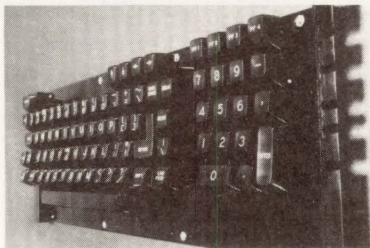
What is your application? _____

Send to: American Microsystems, Inc.,
3800 Homestead Road,
Santa Clara CA 95051.

AMI
AMERICAN MICROSYSTEMS, INC.

PRODUCTS

VT100-TYPE KEYBOARD

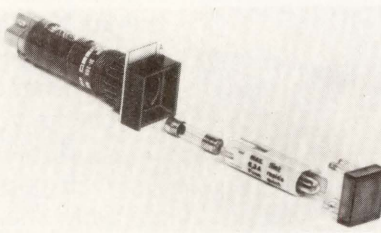


Layout and legends of the Fasttype[®] AN26394 keyboard are identical to the VT100, and a simplified keystation scanning scheme permits microprocessors to take data at their own rate. Included is a 4-wire serial interface, 7 LEDs, and key click and bell capabilities. With key travel of 0.015" (0.0381 cm) with a life rating of greater than 50M operations, the alphanumeric keyboard is designed for VT100 emulator manufacturers and users requiring a VT100 type arrangement. **Chomerics, Inc.**, 77 Dragon Ct, Woburn, MA 01888.

Circle 251 on Inquiry Card

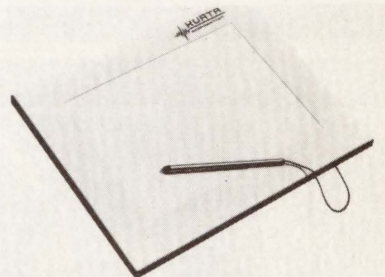
FUSED PUSHBUTTON SWITCHES

An integrated adapter equipped with a lamp and fuse can be locked onto and removed from a series 31 switch housing, converting that switch to a fused series 31 switch. A T-1 $\frac{3}{4}$ groove base lamp (6, 14, 28, and 48 V) and 6.3 A (max) 250-V fuse can be wired to produce separate circuits for lamp and fuse, or an operation or interruption indicator. Switch ratings are 250 Vac at 5 A at an operating temp range of -25 to 45 °C. Snap acting, Hall effect, or low level switch elements also are standard for the fused series. **EAO Switch Corp.**, 255 Cherry St, Milford, CT 06460.



Circle 252 on Inquiry Card

GRAPHIC TABLET



Designed for small computers, these graphic tablets are directly compatible with standard 7 x 9" (17.8 x 22.9-cm) display screens. Standard 8.5 x 11" (21.6 x 28-cm) paper pad exactly fits tablet surface. Output directly matches computer capabilities minimizing interface and software requirements. Resolution is 100/200 points/in (39.4/78.7 points/cm), and conversion rate is 100 coordinate pairs/s. Bisequential output is std, with full parallel output as option. Tablet measures 13 x 15.5 x 0.75" (33 x 39.3 x 1.9 cm). **Kurta Corp.**, 206 S River Dr, Tempe, AZ 85281.

Circle 253 on Inquiry Card

DCS/80 Multibus[®] Development/ Control System \$3595



The DCS/80 is a low cost, industrial quality rack-mountable Multibus[®] compatible development/control system. This compact unit was designed for high reliability, easy maintenance and includes dual 8" floppy disks, DCS8010A CPU, 5-slot (optional 9-slot) backplane and power supply. A 16k byte system costs \$3595. Complete systems with in-circuit emulation (8080/8085/Z80/6800) include DCS/80, PROM programmer, printer and CRT for less than \$12,000.

MULTIBUS HARDWARE — DCS designs and manufactures a complete line of Multibus compatible boards including the DCS8010A CPU that can contain up to 4k RAM, 16k PROM/ROM, 48 Bits parallel I/O, and 2 serial I/O ports.

SOFTWARE — The DCS/80 is CP/M[®] compatible and the software available includes Fortran, Pascal, Process Control Basic, "C" Programming Language, cross-assemblers and a PL/M[®] compatible compiler.

* Multibus, PL/M Trademark of Intel
**CP/M Trademark of Digital Research

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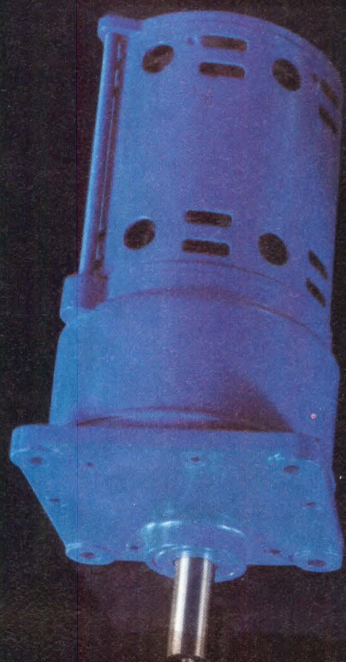
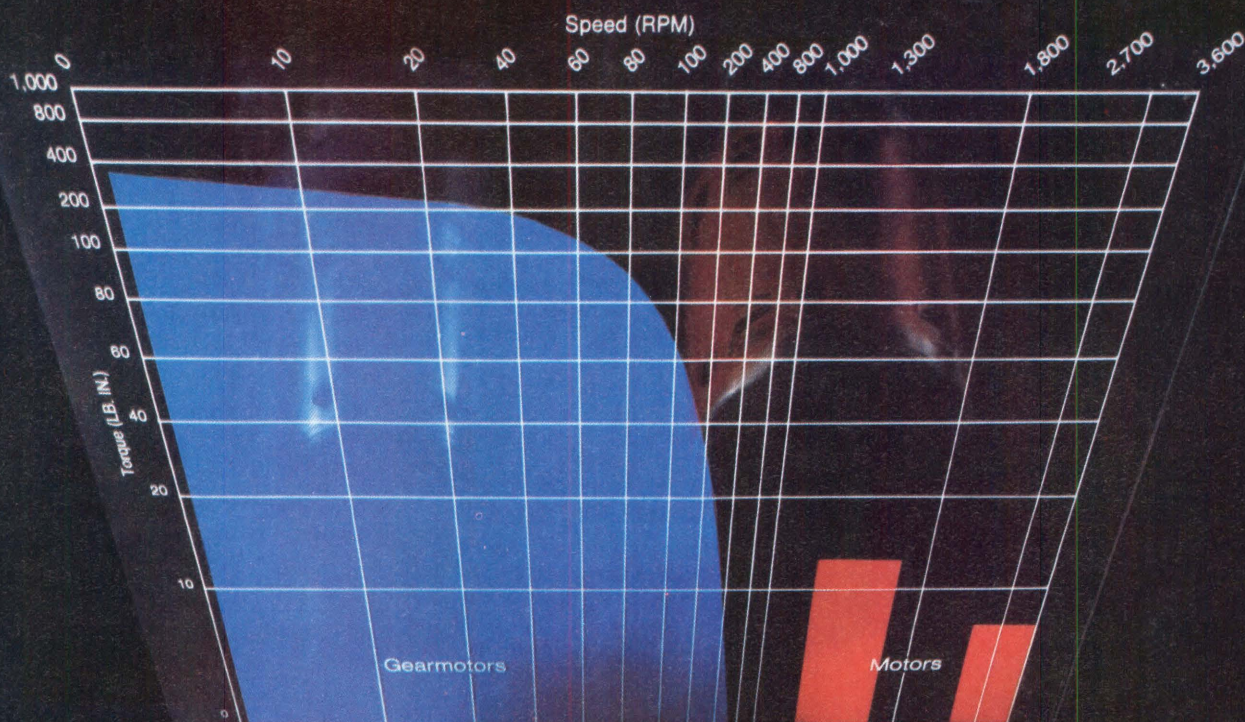
CAMBION'S LOW PROFILE



Cambion's low profile sockets feature inverted contact design, dual face wipe contacts, Kapton[®] coverage for antiwicking protection, and wide-area contact openings for easy IC insertion. Available in a wide range of 8- to 64-pin position sizes, some socket models also provide beneficial center space to carry an electrolytic capacitor. Get very useful low-profile socket low-down in our Catalog 121, and get evaluation samples from Your Cambion Connection at over 100 distributor locations! Cambridge Thermionic Corp., 445 Concord Avenue, Cambridge, MA 02238, Tel: (617) 491-5400, Telex: 92-1480, TWX: (710) 320-6399.



CAMBION[®]
The Right Connection.



Drive at the right speed

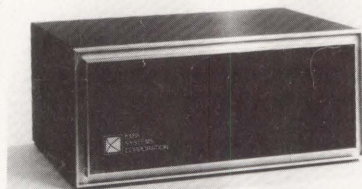
If your speed-torque need falls within the blue or red areas of the chart, Robbins & Myers can get you the gearmotors or speed reducers, motors, and controls to give you the exact output that's right for your application. No compromise. Request Catalog D-1120 for full details on: **Gearmotors**. Comprehensive line of face and foot mounted spur gearmotors rated to 1/6 HP. **Speed reducers**. Three basic spur gearheads with 226 standard ratios from 3.5:1 to 2544:1, with output torques from 16 to 176 in. lb. **A.C. Subfractional HP motors**. Specially sized for OEM needs up to 1/2 HP with millions of standard design variations in diameters from 3 1/8" to 4 11/16". **Variable speed control**. SCR controls for DC gearmotors give constant torque performance from near zero to rated rpm. Get expert help! Electric Motor Division, Robbins & Myers, Inc., 1949 Lagonda Ave., Springfield, OH 45501. Tel. 513-327-3329.

**ROBBINS
MYERS**

CIRCLE 172 ON INQUIRY CARD

PRODUCTS

DATA CONVERTER FOR SYSTEM/34 COMPUTER



BAC-34 sends and receives EBCDIC data via IBM sync protocol, performs error checking, translates data to ASCII, and outputs data in serial asynchronous ASCII format to and from user attached devices. It allows the user to attach peripheral equipment, such as CRTs and line printers, to an IBM System/34 computer at high data rates. Data may be deferred and transmitted at user selected rates of 75 Hz to 19.2 kHz. **KMW Systems Corp.**, 8307 Highway 71 W, Austin, TX 78735.

Circle 254 on Inquiry Card

TO-3-STYLE HEAT SINK

Designed to provide efficient cooling in minimum board space, the heat sink is fabricated from 0.090" (0.23-cm) Al and is available in plain or black anodized finishes. Model 3-1307-001 measures 1.81 x 1.81 x 1.25" (4.59 x 4.59 x 3.18 cm). Finned design produces temperature rises of 43 °C at 8 W, 56 °C at 12 W, and 70 °C at 16 W, following an approximately linear power-temperature rise from 43 °C. **Tran-Tec Corp.**, PO Box 1044, Columbus, NE 68601.

Circle 255 on Inquiry Card

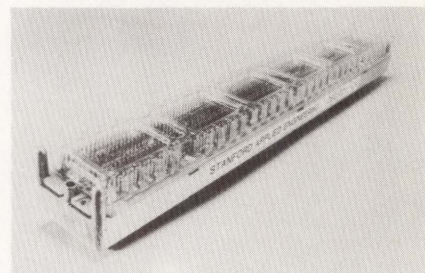
UNIVERSAL COMPUTER SWITCHING MATRIX

Digital Micro-Matrix™ is an 8-port universal crosspoint switching matrix that permits direct data transfer between any combination of computers and peripherals. Up to 8 RS-232-C and/or current loop devices in any combination can be interconnected without software modification, providing 2⁶⁴ possible paths. Sixteen key-selectable connection combinations are stored in non-volatile memory. The device handles baud rates up to 9600 and measures 8.25 x 7.25 x 3" (20.9 x 18.4 x 7.62 cm). **Digital Laboratories, Inc.**, 600 Pleasant St, Watertown, MA 02172.

Circle 256 on Inquiry Card

DEC COMPATIBLE PRESS-FIT BACKPLANES

PDQ/DSC backplanes feature automatic insertion of pins for precision alignment and gas tight connections. Press-fit technology ensures reliable connections. The prewired and pretested unit is available in 4- and 9-slot systems. A plastic protective cover allows entry, yet prevents disturbance of pins or wirewrap. Options include contact plating to customer specifications, a fast-on terminal, and special modifications. **Stanford Applied Engineering, Inc.**, 340 Martin Ave, Santa Clara, CA 95050.



Circle 257 on Inquiry Card



NEW FN 30 SERIES OF POWERFUL LOW NOISE 30 mm DC MOTORS

Available in nine different combinations of motor length (41, 48 and 55 mm) and voltage (6, 12, 24 V) this new series features extremely low electrical noise, very high efficiency, long service life, smooth operation and low mechanical noise.

- Starting torques from 280 to 500 g-cm
- Maximum efficiency as high as 65% at 24 Volts.
- Varistor ring and high quality brush material.
- 7 bar armature for smooth operation.
- Available with AC tach, gearheads and AMP 110 terminals

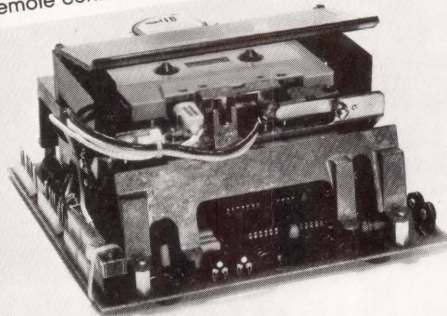
For complete technical information:

Canon

Canon U.S.A., Inc.
Electronic Components Division
10 Nevada Drive,
Lake Success, L.I., N.Y. 11042
Tel. (516) 488-6700
Telex 96-1222
Cable - Canon USA LAKS

PHI-DECK® Cassette Transports

- Fully remote controllable
- Four-motor design
- Cast chassis



New Phi-Deck Electronics

- Motion Control ... Minimum complexity, Maximum performance.
- Digital ... Read/Write and Motion Control on one board. Recording density to 1600 FRPI.
- Analog ... Two channel Record/Play and Motion Control on one board.

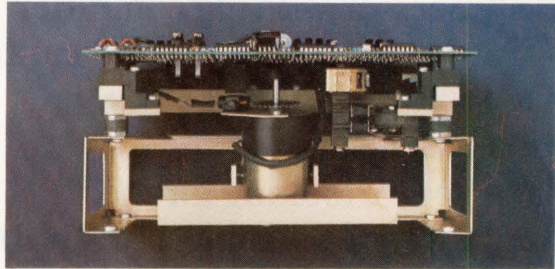
Write or call for information on our specially priced Design Kits and OEM Modules featuring PHI-DECK electronics.

4605 N. Stiles P.O. Box 18209 (405) 521-9000
Oklahoma City, OK 73154 TWX: 910-831-3286

Phi
Incorporated

There are many good reasons to backup Winchester Disks with Cartridge Tape.

The Streamer is all of them.



20 MByte Streaming Cartridge Tape Drive.

Meet the Streamer, a product that makes sense every way you look at it. Designed specifically for Winchester disk backup, DEI's new 10 and 20 MByte high density, microprocessor controlled, $\frac{1}{4}$ " streaming cartridge tape drives have impressive advantages over other backup methods.

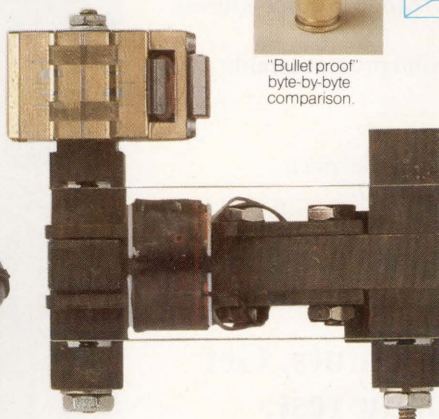
LOW COST

Streaming drives do not require rapid stop/start tape drive electronics and mechanics, resulting in a lower cost servo system, lower power requirements and lower heat dissipation. A unique bi-directional two track head with digital positioner that provides low cost four track operation is also new. What does this all cost? About $\frac{1}{3}$ rd the price of a Winchester disk for OEM's.



Digital magnetic tach and motor

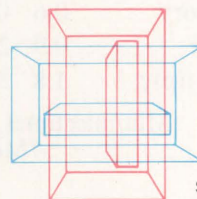
and data resynchronization provides less than 1 error in 10^{10} bits. That boils down to about one error in three years of normal usage! In addition cartridge certification is built into the Streamer, because the data cartridge is calibrated during operation. The improvements don't end here. Our new digital magnetic tachometer increases mechanical reliability because it's operation is not susceptible to dust and dirt problems.



Unique 2-track head with digital positioner



"Bullet proof" byte-by-byte comparison.



Same space requirement as diskette.

EASE OF INSTALLATION

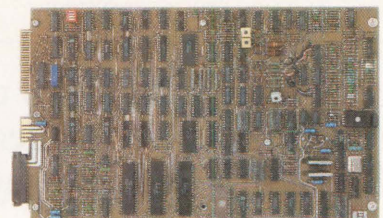
The Streamer is configured to fit the same size enclosure as a conventional 8 inch flexible disk drive. If you have a dual floppy system now, you can upgrade to a Winchester/Streamer 10 or 20 MByte system without additional space requirements.

TRANSFER RATE

The nominal rate is 5 MBytes per minute at a tape speed of 90 ips.

SIMPLE INTERFACING

The drive appears to the host as one of the most familiar interfaces in the industry, a FIFO memory chip.



Streaming electronics.

RELIABILITY AND INTEGRITY

The read-while-write capability allows for 'bullet proof' byte-by-byte comparison. Consequently error detection, correction

The tape is protected against abuse, since it is totally contained within the cartridge. On insertion into the drive, a small door is opened which allows contact with the recording head.

We believe that the Streamer is easy to install, easy to interface, easy to use and easy to afford. Call Whitney Lynn and ask about the Streamer. You'll be in the mainstream of things to come.



DATA ELECTRONICS INC.

10150 Sorrento Valley Road
San Diego, California 92121
Call (714) 452-7840. Telex 69-7118

DEI is a registered trademark of Data Electronics Inc.

Miproc processor speed is industry's right arm

The little processor with big computer power – that's Miproc, for process control, industrial robots, signal analysis, simulation and research.

When you're looking for the computer power of a big microcomputer like the DEC* PDP-11/70* but can't afford the size and price, you should think seriously about Miproc 16. Check out the facts and see why Miproc 16 is probably the computer you need.



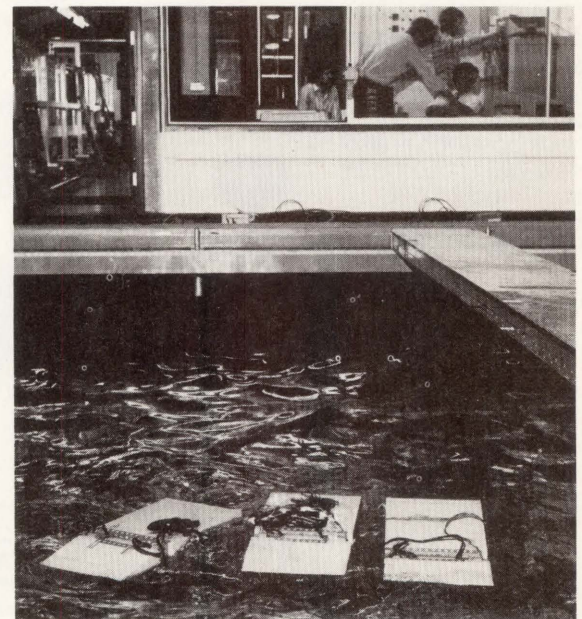
In advanced industrial robotics, high speed processing with floating point accuracy is spot-on with Miproc 16.

	PDP-11/70*		Miproc 16	
	Min	Max	Min	Max
● Integer Add, from memory	0.6	0.6†	.25	.25
● 32 bit floating point Add	0.9	2.52	1.25	3.50
● 32 bit floating point Multiply	1.8	3.44	2.50	2.75

Min/max times, all in microseconds.

†Mode 1 source address.

- **Incredible I/O power**
10 megawords DMA or 1 megaword/second programmable
- **Memory up to 128k word of 16 bits**
- **Price**
Typical small system: CPU, 16k words, 2 parallel ports, 1 serial port, chassis and power, less than £6500.
- **Size**
480×460×220mm. And there's room for lots of expansion, or even a second processor system.



The high-speed data acquisition and signal processing capabilities of Miproc provide wavepower energy researchers on-the-spot results. Fast.

Photograph courtesy Wavepower Limited/Dept of Energy

Get ahead of your competitors. Get the computer that's ahead of the rest. Miproc 16. From Plessey Microsystems, staying up front.

*Digital Equipment Corporation trademarks



PLESSEY
MICROSYSTEMS

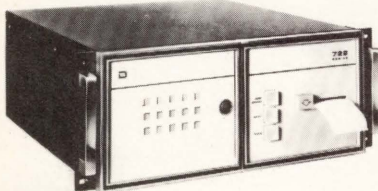
Plessey Microsystems, Water Lane, Towcester, Northants NN12 7JN.
Telephone: Towcester (0327) 50312 Telex: 31628

France: Paris (01) 776 43 34. Holland: Noordwijk 01719 19207. Germany: Munich (089) 23621.

Japan: Eiji Kitahara, Tokyo 244 3782. USA: Gaithersburg, Maryland (301) 948 2791, Irvine, California (714) 540 9931.

PRODUCTS

UNIVERSAL INTERFACE 22-CHAR LINE PRINTER

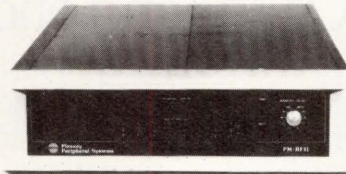


Model 722UA accepts 20-mA loop, RS-232, ANSI/IEEE 488, and BCD inputs via a universal computer interface. The line printer allows for device select through either a single line or a BCD decoder. Interface lines are 3-state, hard-wired active high or low. Solid chars are printed at up to 2400 lines/min. Max line length is 22 char. Available in either rack or table mounting, the unit measures 19"W x 7"H x 18"D (48 x 18 x 46 cm) and weighs 73 lb (33 kg). **Datadyne Corp.**, PO Box 247, King of Prussia, PA 19406.

Circle 258 on Inquiry Card

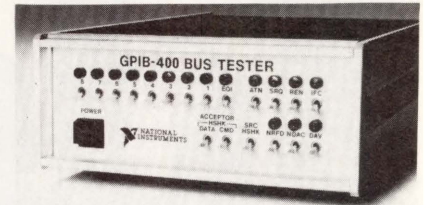
FIXED DISC EMULATOR FOR PDP-11

PM-RF11 emulates the DEC RF11-A system by using dynamic MOS memory as the storage medium. It is claimed to provide increases of 10 to 1 in transfer rate and 1700 to 1 in access time. One version supplies 512k bytes of MOS memory in a 5.25" (13.33-cm) chassis with room for expansion to 1.5M bytes. The other model, in a 10.5" (26.7-cm) chassis, is expandable to 4M bytes. **Plessey Peripheral Systems**, 17466 Daimler Ave, Irvine, CA 92714.



Circle 261 on Inquiry Card

IEEE 488 BUS TESTER



GPIB-400 bus tester, applicable to any IEEE 488-1978 instrumentation system, includes LEDs and switches for monitoring and controlling all bus lines. Automatic source handshake mode allows an RS-232 or current loop terminal to generate IEEE 488 commands or data from the keyboard. Automatic acceptor handshake mode permits the terminal to receive IEEE 488 commands or data and display or print their ASCII equivalent on the terminal. **National Instruments**, 8900 Shoal Creek, Austin, TX 78758.

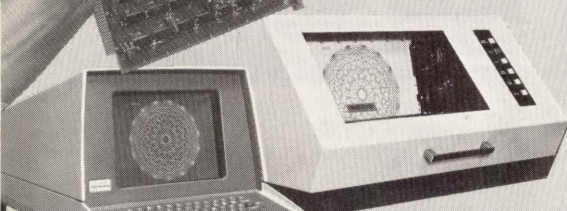
Circle 260 on Inquiry Card

PRINTRONIX+TEKTRONIX the perfect match!

Now Tektronix Graphic CRT's can be happily wedded to your Printronix printer/plotter — P150, P300 or P600. TRILOG's efficient little matchmaker, the Graphics Adapter Board — GAB for short — plugs right into the spare card slot in your Printronix unit. In seconds you'll get hard copies of the images from one or two

Tektronix Graphic CRT's while retaining all the Printronix normal printing/plotting functions. And GAB's special switch-selectable mode reduces the image size to fit on 8½" x 11" paper — for a beautiful reflection of their love's affection!

Contact your Printronix/TRILOG distributor or call TRILOG direct at (714) 549-4079.



TRILOG

17391 Murphy Avenue, Irvine, CA 92714

CIRCLE 176 ON INQUIRY CARD

D100

Availability.
Compatibility.
Reliability.
Disk to disk
back up.



Cii Honeywell Bull

Bull Corporation of America

Mail station 430-200 Smith Street - Waltham Mass 02154.
Tel: (617) 895.6020.

801 Mahler Road - Suite D - Burlingame CA 94010.
Tel: (415) 692.5724.

CIRCLE 177 ON INQUIRY CARD

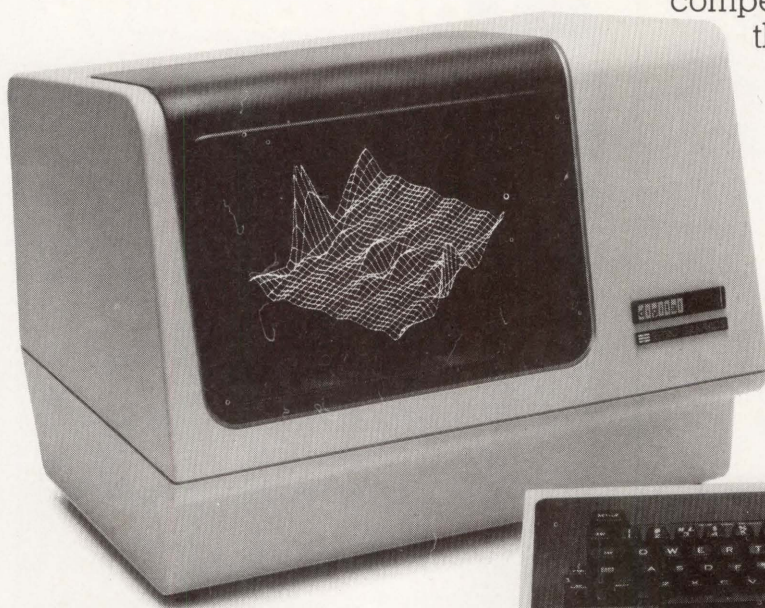
The Idea:

To take the Digital VT100 and make it both graphical and economical for OEMs and end-users.

Digital Engineering, the pioneers in retro-fit graphics, has done it again. This time, we've turned DEC's VT100 alphanumerics terminal into a sophisticated graphics terminal that features multiple character sizes, dot-dash lines, point plotting, vector drawing and selective erase for quick, easy updating of the graphics display.

But complete emulation of Tektronix® 4010 Series terminals—and compatibility with most existing graphics software, including Tektronix Plot 10™ and ISSCO's® DISSPLA® and TELLAGRAF®—is just the beginning of the Retro-Graphics™ VT100 story. Graphics are displayed on a 12" (diagonal) green-toned screen at 640 x 480 resolution. Refresh raster scan technology insures a bright, easy-to-read display. And all of the features that DEC's VT100 begins with remain intact, including 96 upper/lower case ASCII characters, up to 132 characters per line, numeric and function keypads, detachable keyboard and a wide variety of screen customizing features.

The Retro-Graphics VT100. Whether you are looking for continuity with existing DEC products, or for a high-quality graphics terminal at hundreds less than the competition, the Retro-Graphics VT100 is the right idea. An idea proven on thousands of Lear Siegler ADM-3A and 3A+ Dumb Terminals®. And an idea taken another step further, once again by Digital Engineering. For more information, write or call.



**DIGITAL
ENGINEERING**

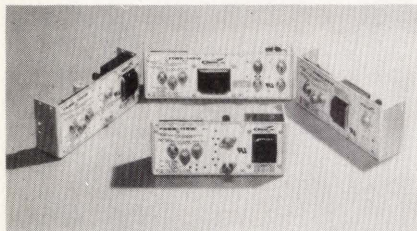
630 Bercut Drive
Sacramento, CA 95814
(916) 447-7600
TWX: 910-367-2009

Retro-Graphics™ is a trademark of Digital Engineering, Inc.
DumbTerminal® is a registered trademark of Lear Siegler, Inc.
Tektronix® and Plot 10™ are trademarks of Tektronix, Inc.
ISSCO® DISSPLA® and TELLAGRAF® are registered trademarks of
Integrated Software Systems Corporation.

CIRCLE 178 ON INQUIRY CARD

PRODUCTS

FIXED DISC MEMORY POWER SUPPLIES



Intended for Winchester, Shugart, Micropolis, and other fixed disc memories, power supply line includes 3 models with 5 outputs (5, 12, 24, -5, and -12 V) and 4 models with 3 outputs (5, 24, and -5 or -12 V). These are said to be the only fixed disc memory power supplies with an international transformer as standard equipment. Line regulation for a 10% line change is $\pm 0.02\%$. For a 50% load change, load regulation is $\pm 0.02\%$. **Condor, Inc.**, 4880 Adohr Ln, Camarillo, CA 93010.

Circle 259 on Inquiry Card

1-PIECE CARD CONNECTOR

Series HPF 1-piece card connectors eliminate need for motherboards in most applications. A single body serves for all connections, allowing PC cards to connect to one another directly. Benefits include faster signal access time, elimination of tolerance buildup between connectors, 0.25" (6.35-mm) board spacing, shock and vibration resistance, positive alignment, contact resistance of $< 5 \text{ m}\Omega$, and continuous performance of $< 10 \text{ ns}$ at 20 G rms. **Smith Industries, Inc., Connector Div**, PO Box 5389, Clearwater, FL 33518.

Circle 262 on Inquiry Card

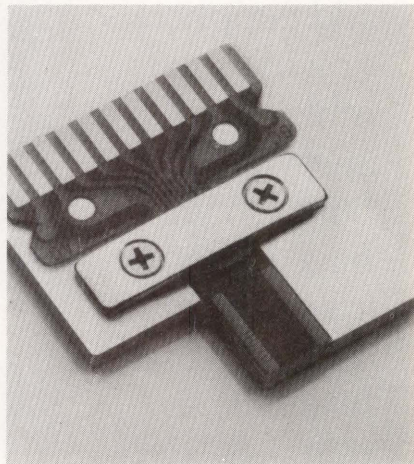
SONIC DIGITIZERS WITH RS-232 AND IEEE-488 INTERFACES

Capable of providing digital coordinates for any point on a plane, GP-6-25 (with integral RS-232 interface) and GP-6-26 (IEEE-488) digitizers produce a standard parallel 14-bit output. Active areas of the models range from 18 x 18" (45.7 x 45.7 cm) to 60 x 72" (1.52 x 1.83 m). Digitizers produce digital values for display, data processing, storage, or transmission. L-frame sensor borders active work area, and sensors can be used with light table, rear projection setups, or with opaque surfaces. **Science Accessories Corp.**, 970 Kings Hwy W, Southport, CT 06490.

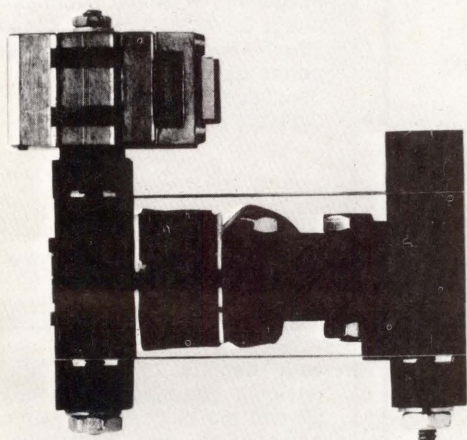
Circle 263 on Inquiry Card

HIGH SPEED THERMAL PRINTHEAD

Designed for alphanumeric applications, the KH319 high speed 1 x 7-dot thin film thermal printhead is intended for applications where continuous bidirectional printhead movement is required. At 10 char/in, (3.9/cm) print speeds of up to 120 char/s can be attained. The head is designed for low wear; a secondary glazed area positioned parallel to the heat elements ensures flat travel. Head alone and head mounted on a heat sink are 2 of the versions available. **R.ohm Corp.**, PO Box 19515, Irvine, CA 92713.



Circle 264 on Inquiry Card



Two Track Moving Head Featured On New DEI Streaming Cartridge Drives.

The heart of Data Electronics' new 10 and 20 MByte streaming cartridge tape drives is a unique 2-track head. The new head is bi-directional and uses a simple digital positioner on the 20 MByte drive to provide 4-track operation. Because of the overall simplicity of these drives, OEM prices start at about 1/3rd the cost of the Winchester drives they are designed to backup. A further benefit of the drives' design is small size; they fit in the same space as floppy drives. Designers can easily upgrade a floppy-based system to 10 or 20 MByte capacity using a Winchester/Streaming® cartridge tape drive combination.



10150 Sorrento Valley Road
San Diego, California 92121
Telephone (714) 452-7840
Telex 69-7118

Data Electronics Inc.

CIRCLE 179 ON INQUIRY CARD

D100

A family of compact, fixed and removable disk drives. 10 to 120 Mb.

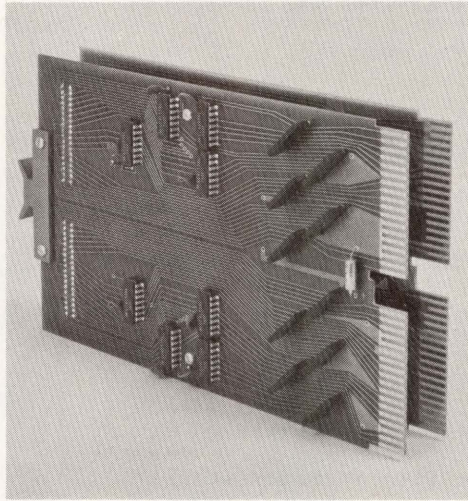


Cii Honeywell Bull

CIRCLE 180 ON INQUIRY CARD

Unibus* repeater for PDP11 series systems.

Do you need to add peripherals or additional cable lengths to an overloaded bus? Do you have unknown system crashes such as caused by a type 4 trap — delayed response from a slave sync? Is your current repeater too slow for your current system?



If these questions are relevant, then Datafusion Corporation has a device that can answer your needs, the OSB11-A Bus Repeater. It is a functional equivalent of DEC's* DB11-A, and is designed to drive at least 19 bus loads and 50 foot of bus cables.

Ultra Fast: 80 nanoseconds MSYNC to return SSYNC maximum (40 nsec one way). This is due, primarily, to the specially designed patented integrated circuit employed by the OSB11-A.

Reliable: Only 34 operational circuit components. Tested in environments from 0° to 70°C with virtually no degradation of signal quality.

Easy to Install: Remove a M920 Jumper and replace it with a OSB11-A. No extra system unit is needed; no wires or plugs to connect (or disconnect); no lost time in reconfiguration.

Available: Off-the-shelf. And, it's fully supported and warranted.

Cost: About 25% below DEC.* Quantity discounts are available.

Other PDP11 products available are a Busrouter (a Unibus* Switch) to reconnect multiple peripherals to one or more PDP11 cpu's, a Unibus* Cable Tester, and an Associative File Processor for high speed text search — a hardware approach.

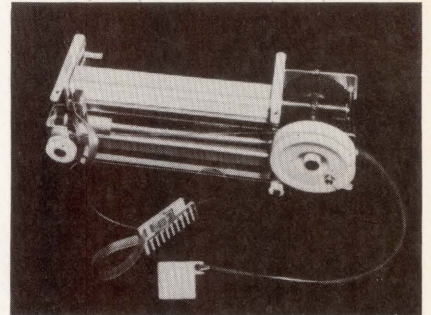
We also have some ideas for the application of our products which might not have occurred to you. If you can't get the performance that you would like from your PDP11 system, maybe we can help. Telephone our marketing Manager at (213) 887-9523 or write to Datafusion Corporation, 5115 Douglas Fir Road, Calabasas, California 91302.



*TRADEMARK OF DIGITAL EQUIPMENT CORPORATION

PRODUCTS

80-COL MINIATURE ALPHANUMERIC PRINTERS

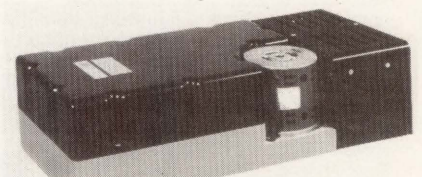


EUY-5E and -5T print 32, 40, 64, or 80 char/line on electrosensitive or thermally sensitive paper at 2 and 0.8 lines/s, respectively. Characters are 2.7 mm high, formed by a 7 x 5 dot matrix. Measuring 195 mm wide, 65 mm high, and 70 mm deep, both units print on 127-mm wide paper with expected life of 1×10^6 lines. Long life and small size make the 5" (12.7-cm) printers suitable for applications requiring inexpensive hard copy. Units come without a case, ready to be mounted into user's equipment and connected through ribbon cables and PC connectors. The electrosensitive model requires two ± 24 -Vdc sources at 100 mA each and a 5-Vdc supply at 30 mA. The thermal unit needs one ± 24 -Vdc supply at 100 mA, one ± 24 -Vdc source at 1 A, and 5-Vdc at 30 mA. **Panasonic Co, Electronic Components Div, One Panasonic Way, Secaucus, NJ 07094.**

Circle 265 on Inquiry Card

8" SEALED DISC MEMORY

Cheyenne series fixed media sealed disc systems have available capacities from 7.35M (1 disc) to 51.4M (4 discs) bytes with density of 6409 bits/in (2523 bits/cm), recording 478 tracks on 7.874" (20-cm) dia discs; 8.268" (21-cm) discs can also be used. Electronics package allows daisy chaining up to 8 drives with microbus, SMD, or ANSI interfaces. P/ROM control provides write compensation, servo functions, and interface control, with microprocessor control for self-diagnostics and status reports. **SLI Industries, 21040 Victory Blvd, Woodland Hills, CA 91367.**



Circle 266 on Inquiry Card

PRODUCTS

FLOPPY DISC LOADER

Eliminating operator intervention, the Media Loader is software driven and has a stacking capacity of up to 50 5.25" (13.3-cm) or 8" (20-cm) single- or double-sided floppy discs. The automatic floppy disc loader is designed for data certification, initialization, batch terminal data storage, error logging, and program spooling from tape or disc. A loader is capable of processing 80 floppy discs/hour. Discs are automatically fed through an input hopper and accepted or rejected. **Media Systems Technology, Inc.**, 1616 S Lyon, Santa Ana, CA 92705. Circle 267 on Inquiry Card

UNIVERSAL NMOS EPROM PROGRAMMER



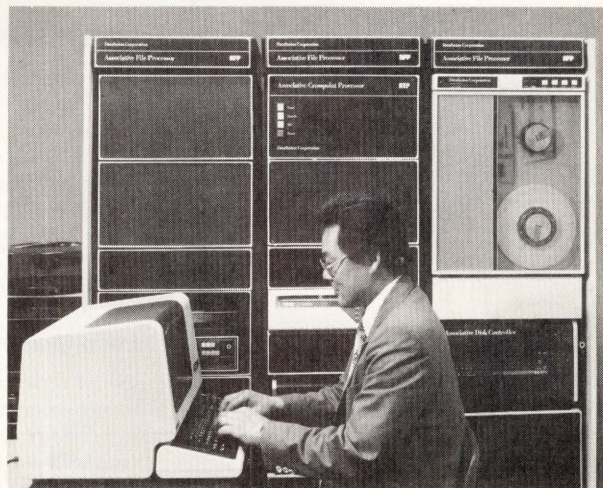
MOS Pak, with a System 19 programmer, will program all 2704, 2708, 2758, 2716, 1732, 2732A, 2532, 2564, 2764, 68764, and 4716 EPROMs, as well as the Hitachi 48016 EEPROM. The unit makes the System 19 a universal NMOS programmer without changes in hardware. Keying in a 4-digit code customizes the programmer, which assembles the correct programming algorithm and lights the LED for its appropriate 24- or 28-pin socket. The algorithm saves programming time for 64k or larger EPROMs. An 8k x 8 unit can be programmed in 2 min. **Data I/O**, PO Box 308, 1297 NW Mall, Issaquah, WA 98027. Circle 268 on Inquiry Card

10 AND 19" CARD CAGES

Designated the CCK Vector-Pak™ "S" series, 4 card cages are available in 5.25 x 9" (13.33 x 22.85-cm) or 10 x 19" (25.4 x 48.26-cm) configurations. Slotted side walls and brackets permit cross members to be adjusted both laterally and vertically to accommodate card sizes from 3.0 to 4.5" (7.62 to 11.43 cm) wide and 4.5 to 6.5" (7.62 to 16.51 cm) long. UL rated nylon snap-in card guides are included. Ruled scales on both connector mounting struts allow fast, accurate connector positioning. **Vector Electronic Co, Inc.**, 12460 Gladstone Ave, Sylmar, CA 91342. Circle 269 on Inquiry Card

The Associative File Processor. AFP.

A Special Purpose Hardware System for Retrieving Textual Information.



Full Text Retrieval. Finds relevant information in large free text files (typically 300 million characters or more) that match queries.

Unrestricted Queries. Unrestricted query vocabulary with boolean AND, OR, NOT and proximity key word logic.

Simple Configuration. AFP® runs on a PDP11 host mini-computer and includes all necessary user software.

Real Time Data Input. New data may be input and searched as it is received, if necessary.

Special Associative Hardware. The processing power is made possible by the special AXP® hardware effectively having the capability of 1200 cpu's.

Affordable. Now you can afford full text retrieval costing only a few pennies per search.

Available in Three Configurations. The **AXP100** attaches to an existing PDP11 computer; the **AXP200** is self contained with a communication interface to a network or another host computer; the **AXP300** is a turn key system including CRT terminals and a line printer.

Application Areas Include:

Military and Intelligence
Law Enforcement
Library Search
Word Processing Support
Abstract Search
Title and Property Search
Trial Transcripts
Patent Search
Litigation Support

Technical Report Retrieval
Generic Record Keeping
Current Awareness Bulletin
Laboratory Testing and Retrieval
Journal Abstracting and Control
Pharmaceutical Literature Retrieval
Product Bibliographies
Chemical Compound Retrieval
Historical Records and Archives



Call (213) 887-9523 or write for a detailed brochure.

Datafusion Corporation

5115 Douglas Fir Road, Calabasas, California 91302

RS232C Paper Tape Transmitter



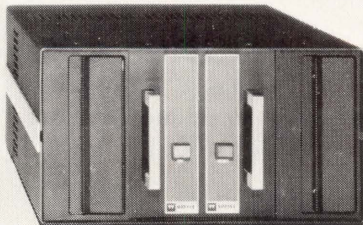
Computer entry, numerical control and data transmission. Includes X-on, X-off and parallel output, current loop optional. Desk top or rack mount. OEM model and spooler also available.



ADDMASTER
CORPORATION
416 Junipero Serra Drive
San Gabriel, California 91776
(213) 285-1121

CIRCLE 103 ON INQUIRY CARD

Sprint 68 Microcomputer



CONTROL COMPUTER DEVELOPMENT SYSTEM

6800 MPU, serial I/O, 48K RAM, dual 8" drives, WIZRD[®] multi-tasking DOS, editor, assembler, 12K BASIC, all for \$3995.

OPTIONS

C, PL/W, PASCAL, FORTRAN, EROM programmer, analog I/O, parallel I/O, 488 GPIB interface, CMOS RAM/battery, power fail detect/power on reset.



Wintek Corp.
1801 South Street
Lafayette, IN 47904
317-742-8428

294 CIRCLE 104 ON INQUIRY CARD

LITERATURE

Bit and Sleeve Selector

Pocket-size device provides users of Wire-Wrap[®] tools with readout of bit and sleeve part numbers, max terminal diagonal, effective radius, and max insulation. **Gardner-Denver, Pneutronics Div**, Grand Haven, Mich.

Circle 300 on Inquiry Card

Loop Modems

Use of series 12 LMS and 24 LMS in IBM 3600 finance communications systems is detailed in brochure that also describes function of loop modems in network management control systems. **Racal-Milgo, Inc**, Miami, Fla.

Circle 301 on Inquiry Card

Handheld Logic Probes

Brochure furnishes descriptions, photos, and technical specs for 700 series and LP-450 logic probes as well as HL-480 universal pulser, which can be used with any probe. **Kurz-Kasch, Inc**, Dayton, Ohio.

Circle 302 on Inquiry Card

Matrix Boards and Applications

Boards in 3 different sizes and those with 1- and 2-layer and multideck construction are detailed along with programming pins in brochure. **Programming Devices Div, Sealectro Corp**, Mamaroneck, NY.

Circle 303 on Inquiry Card

Data Communications Systems

Illustrated booklet describes applications in manufacturing, chemicals, international affairs, drugs, food distribution, law enforcement, and securities. **Data General Corp**, Westboro, Mass.

Circle 304 on Inquiry Card

Power Semiconductor Devices

Specs and drawings are supplied by catalog describing ion implanted semiconductors, high voltage transistors and rectifiers, ultra fast recovery rectifiers, power hybrids, and bridge assemblies. **Solid State Devices, Inc**, La Mirada, Calif.

Circle 305 on Inquiry Card

Pen Plotting Media

Users' guide/catalog describes 11 different plotting media, includes compatibility data and cross-reference, and discusses solutions to problems and economical usage. Request on company letterhead from Catalog, **Graphic Resources Corp**, 5442 Research Dr, Huntington Beach, CA 92549.

Printed Circuit Connectors

Dimensional drawings, specs, and photos are included in catalog describing dip-solder, wirewrap, round-tail, and 2-piece connectors, connector blocks, and AnTac[®] selective gold plating process. **Viking Connectors, Inc**, Chatsworth, Calif.

Circle 306 on Inquiry Card

Touch Screen Digitizers

Given in illustrated brochure are features, applications, functional descriptions, and specs for 12- and 15-in models 12A/15A and retrofit kits 12B/15B. **TSD Display Products, Inc**, Bohemia, NY.

Circle 307 on Inquiry Card

Pushbutton, Key, Rotary, and Slide Switches

Photos, drawings, mechanical and electrical data, option guide glossary of terms, and suggested cleaning procedures are presented in catalog. **ITT Shadow Inc**, Eden Prairie, Minn.

Circle 308 on Inquiry Card

LEDs

Illustrated catalog provides selector guide, applications section, and mechanical data for 2-pin midget flanged, 2-color, discrete, PCB, and telephone slide-base models. **Data Display Products**, Inglewood, Calif.

Circle 309 on Inquiry Card

Printers and Paper Tape Readers

Catalog details numeric/limited alpha printers for data logging and readers of tape prepared to ANSI standards for computer entry, numerical control, data transmission, and P-ROM programmers. **Addmaster Corp**, San Gabriel, Calif.

Circle 310 on Inquiry Card

THERE IS ONLY ONE 32-BIT COMPUTER WHOSE LOGIC DOESN'T DEFY LOGIC.

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GENERAL ECLIPSE MV/8000.

Apparently, our competitors are operating under the premise that there is no need to make their new computers compatible with their older ones. And have no qualms about rendering obsolete the years of man-hours and the hundreds of thousands of dollars you've invested in software.

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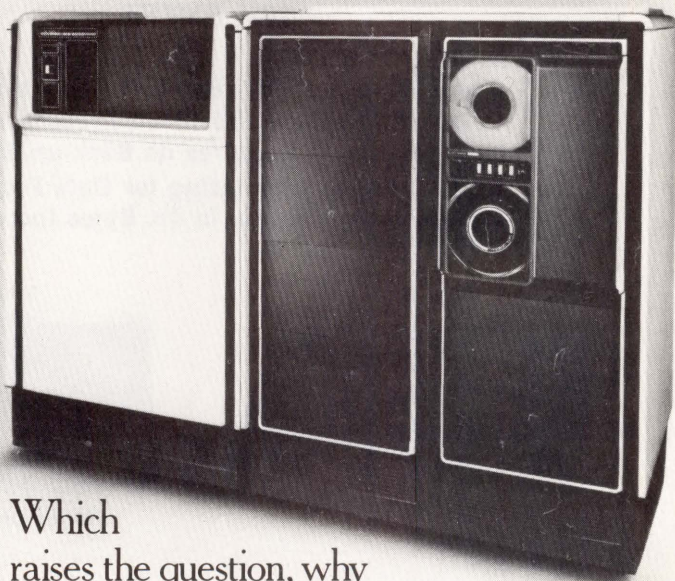
Not destroy it.

However, the MV/8000's software compatibility is only part of what places it in a class by itself. Another factor is speed. It's the fastest computer of its size on the market.

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☐ Please have a sales representative call on me immediately.

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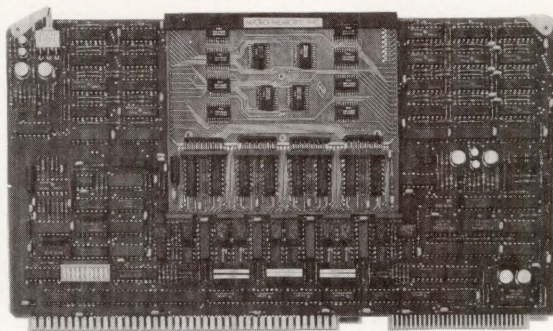
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*Fortran 77, Cobol, Basic, PL/I and RPG II

MULTIBUS^{*} CORE MEMORIES

*NON-VOLATILE *WRITE-PROTECT *POWER-FAIL INTERRUPT

MM-8086/16

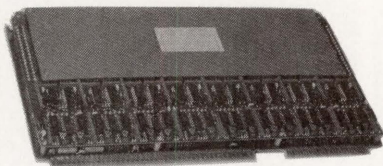


NEW
\$875

16K BYTES

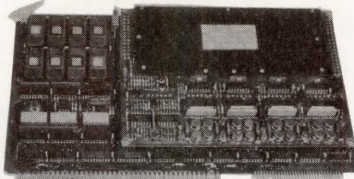
- * Single Card Slot 16K Bytes of Read/Write Memory
- * Compatible with 8 and 16 Bit Processors
- * Non-Volatile — Requires no Back-up Battery
- * AC/DC Power Monitoring for Data Protection
- * Write-Protect Control in 4K Bytes Increments

MM-8086



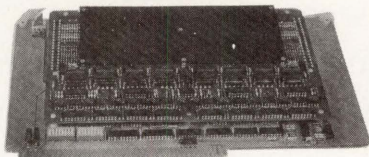
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MM-8080B



16K EROM & 8K CORE

MM-8080/16



16K BYTES

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*Multibus is a trademark of the Intel Corp.

LITERATURE

17M-Byte High Density Digital Cartridge Tape Drive

Data sheet provides photo, general description, options available, and complete specs for "The Funnel." **Data Electronics, Inc.**, San Diego, Calif.

Circle 311 on Inquiry Card

Power Sources

Dimensional drawings, specs, and selection guide are provided in catalog along with specific application for each power source and general applications for all ac-dc and dc-dc supplies. **Reliability, Inc.**, Houston, Tex.

Circle 312 on Inquiry Card

Ac Line Voltage Regulators

Graphs, photos, specs, dimensional drawings, and selection guide for portable and handwired micro/minicomputer regulators and constant voltage transformers are found in catalog. **Sola Electric**, Elk Grove Village, Ill.

Circle 313 on Inquiry Card

Production Monitoring System

Brochure discusses Loginet system employed in discrete part manufacturing control, depicts configuration of standard modules, and explains function of each. **Logicon, Process Systems Div**, Fairfax, Va.

Circle 314 on Inquiry Card

Readout Enhancement

Technical bulletin with graphs and photos supplies features, description, and specs for Chromafilter^R sheet materials for improving readability of optoelectronic and video displays. **Panelgraphic Corp.**, West Caldwell, NJ.

Circle 315 on Inquiry Card

Modems, Multiplexers, and Network Processors

Set of data sheets presents photos, features, and specs for M900 Intertran^R data sets, M1308 and M1318 Multitran^R multiplexers, M3201 network processors, M3212 network access concentrators, and XPRTTM X.25 tester. **Tran Telecommunications Corp.**, Marina del Rey, Calif.

Circle 316 on Inquiry Card

ADVERTISERS' INDEX

Able Computer	258
ADAC Corp	4
Addmaster Corp	294
ADE Corp	138
Advanced Electronics Design	115
Advanced Micro Devices	184, 185
Air Land Systems	98
Altos Computer Systems	227
American Microsystems Inc	283
AMP	204, 205
Ampex Memory Products	119
Anadex	271
Ann Arbor Terminals	242
Associated Computer Consultants	153
Atlantic Research Corp	76
Audiotronics	107
Aydin Controls	206
Beehive International	91
BEI Electronics	276
Belden Corp	196, 197, 230
Bell & Howell/CEC Div	42
Bizcomp	84
Bo-sherral Co	266
Buehler Products	282
Burr-Brown Research	264
Cambion	284
Canon USA	286
Cermetek	66
Chapman Corp	214
Charles River Data Systems	139
Chromatics	158
Columbia Data Products	123, 136
Compas Microsystems	106
Computer Sciences Corp	260
Control Data Corp	275
Converter Concepts	182
C&TE	259
Custom Systems	94
Data Electronics	187, 254, 287, 291
Datafusion Corp	292, 293
Data General	295
Datagraphix	54
Data I/O	245
Dataram Corp	5, 170
Dataroyal	243
Data Systems Design	124, 125
Data Technology	267
Data Translation	137
DeAnza Systems	261
Deltron	266
Diablo, a Xerox Co	127
Dialight	140, 141
Digi-Data Corp	70
Digital Engineering	290
Digital Pathways	251
Distributed Computer Systems	284
Distributed Logic Corp	249
The Dylon Corp	257
Eastern Air Devices	270
Electronic Processors	279
Facit	65
Fairchild Semiconductor	18, 19, 174, 175, 188, 189
Floating Point Systems	203
France Telecom	50
Gandalf	24
GAW Control Corp, TDX Peripherals Div	86
General Electric Co, Terminet Div	43
Gould Inc	90
Biomation Div	8, 9, 179
Foil Div	298
Greenray Industries	112
Grinnell Systems	239
GTCO Corp	201
Hazeltine Corp	100, 101
Hitachi America Ltd	180, 181
Cii Honeywell Bull Int'l	289, 291
Houston Instrument	Cover III
Hughes	248
Hycam	248
IEE (Industrial Electronic Engineers)	263
ILC Data Device Corp	134
Industrial Programming	273
Innovative Data Technology	113
Integral Data Systems	269
Intel Corp	132, 133, 220, 221, 247

Intelligent Systems Corp	194, 195
International Computer Programs	270
International Electronic Machinery	64
International Microcircuits	14, 15
Intersil Systems	120, 121
C Itoh Electronics	103, 274
ITT Datanetics Corp	215
Kapusi Labs	99
Kennedy Co	1
Laser Diode Laboratories	96
Lear Siegler	20, 21
Lenco	114
Lexidata Corp	253
Mannesmann Tally Corp	2
Matrix Corp	246
MDB Systems	95
Megatek Corp	Cover II
MFE Corp	35
Micom Systems	44
Micro Memory	296
Micropolis	168
MicroSwitch	240
Mitsubishi	118
Monolithic Memories	12, 13
Monolithic Systems	146
Morrow Designs	16, 17
Mostek	228
Motorola Inc	212, 213, 233, 234
National Electric Cable	267
NEC Information Systems	28
Norm DeNardi Enterprises	144
North Star Computers	145
OK Machine & Tool	222
Ontel Corp	89
Optelecom	48
Optical Information Systems	38
Optimal Technology	280
Opto 22	131
Paratronics	10
PCK Technology	225
PEBX	202
Pennwalt Corp	257, 259
Penril Corp	83
Permag Corp	280
Pertec Computer Corp, Peripherals Div	177
Plessey Microsystems	288
Power General	265
Power-One	218
Practical Automation	226
Printer Systems Corp	81
Qantex, Div NOAT	183
Qume	109
Racal Vadic	87
Ramtek	Cover IV
Robbins & Myers	285
Robinson Nugent	6, 7
Rockwell International	93, 126
Semicon	272
Shugart Associates	142, 155, 156, 157
Signal Technology	211
Signetics	36, 37, 49, 97
The Singer Co, Librascope Div	191
Spectronics	110, 111
Storage Technology	116, 117
Sweinhart Electric Co	254
T&B/Ansley	229
TEAC	278
Technical Systems Consultants	255
Tektronix, Inc	104, 105
Teledyne Relays	256
Teletype Corp	22
TEXAS INSTRUMENTS	26, 217
3M Co	198, 199
Toshiba America	193
Triad-Utrad	262
Trilog	289
Triple I	286
Universal Data Systems	277
Vermont Research Corp	154
Versitron	58
Vikron	282
Visual Technology	129
Vought Corp	268
Westrex OEM Products	298
Windjammer Barefoot Cruises	219
Wintek	294
Xycom	281
Zilog	172, 173

PRINTERS

slip and two station

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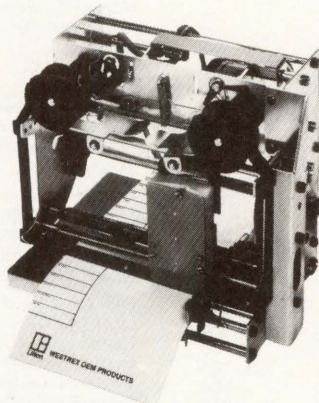
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Model MR-1824

Two Station
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Model MS-4000

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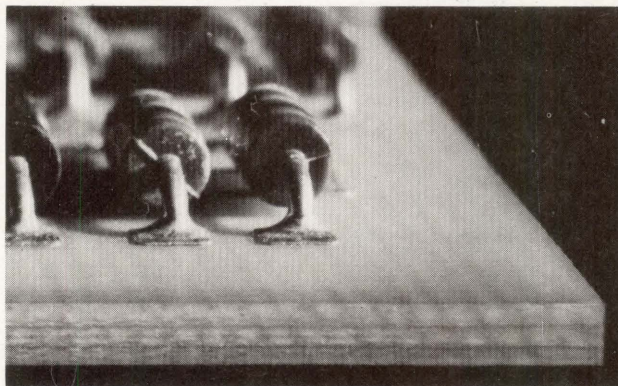


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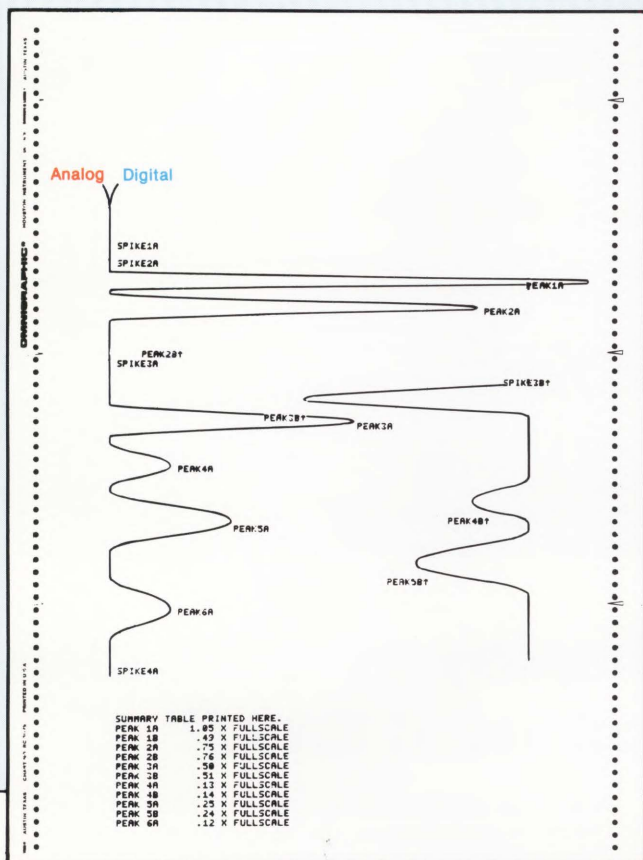
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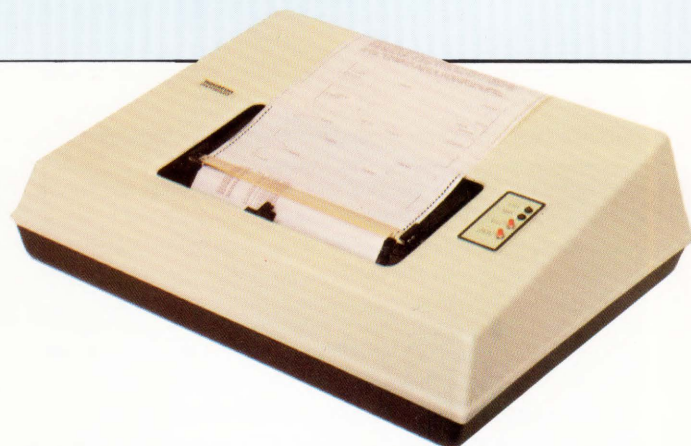


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