KONTRON
LOGIC ANALYZER
DIAGNOSTIC PROGRAM
(LDP)

SMK-LA-1010-01

NOVEMBER 1985

KONTRON ELECTRONICS
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MOUNTAIN VIEW, CA 94039-7230
The Kontron Logic Analyzer Diagnostic Program (LDP) is primarily intended to be used by engineers and technicians to test the high-speed component boards (TBQ, SEQ, DMB) of the logic analyzer. To test the KDT6 and LA INT boards, see the Service Manual: Kontron LA, Volume 1 (SMK-LA-1001). The basic operating text is the Kontron Logic Analyzer Series III Operations (LA-5000).

This manual contains the following chapters and appendices:

Chapter 1 - Introduction
Chapter 2 - Test Setup
Chapter 3 - Memory Tests
Chapter 4 - TBQ Tests
Chapter 5 - SEQ Tests
Chapter 6 - DMB Tests
Appendix A - LDP Menu Input Fields
Appendix B - LDP Test Failures

For easy reference, additional schematics are provided at the end of this manual that are also duplicated in SMK-LA-1001 and LA-5000.
### REVISION HISTORY

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<td>SMK-LA-1010-01</td>
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### RELATED PUBLICATIONS

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WARNING

This equipment generates, uses and can radiate radio frequency energy. If it is not installed and used in accordance with this instruction manual, it may cause interference to radio communications. Kontron has constructed this equipment in accordance with good engineering design and practice, in order to minimize such interference. Because it is classified as "commercial test equipment", the equipment is exempt from the current FCC rules. Therefore, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of the FCC rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area may cause interference, in which case the user will be required, at his own expense, to take whatever measures may be required to correct the interference.
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1.1 PURPOSE

Because of the complex architecture of the equipment, the Kontron Logic Analyzer (LA) is difficult to test. A special program, the Logic Analyzer Diagnostic Program (LDP), has been developed to conduct appropriate tests and report the results. The purpose of this manual is to acquaint you with the LDP tests and how to perform them.

1.2 CONTENTS

This manual contains the following chapters and appendices:

- Chapter 1 - Introduction
- Chapter 2 - Test Setup
- Chapter 3 - Memory Tests
- Chapter 4 - TBQ Tests
- Chapter 5 - SEQ Tests
- Chapter 6 - DMB Tests
- Appendix A - LDP Menu Input Fields
- Appendix B - LDP Test Failures

Information on the CPU and I/O boards (KDT6, LA INT) is found in the Kontron_LA_Service_Manual_Volume_1 (SMK-LA-1001). The basic text for operating the LA is the Kontron_Lcngic_Analyzer_Series III_Operations (LA-5000) manual. There is also a Customer Application Note (CAN-175) that explains how the Universal Probe Rack (UPR) operates and specifies pinout connections.
1.2.1 ORGANIZATION OF THIS MANUAL

The LDP tests are grouped in the order the hardware is configured (i.e., TBQ, SEQ, DMB), therefore, you should follow that sequence in testing.

To enhance readability, the test material in Chapters 4 through 6 is presented as follows: flowchart (if applicable), description of test, and schematics for the board. The flowcharts describe the principle underlying each test. They are intended to help the user follow the step-by-step operation, and thus enable him to find the point where the error occurred. The test descriptions suggest the cause of possible errors.

Appendix A explains what each LDP menu does and shows the associated LA sample screen shots. Appendix B describes some possible reasons for LDP test failures and also includes sample screen shots. There are additional schematics at the end of this manual pertaining to the motherboard and the KDT6 and LA INT boards (see section 1.3).

1.2.2 QUICK REFERENCE GUIDE

This subsection is designed to give you a "hands-on" approach to locating information relevant to testing the LA. The items are listed alphabetically with the corresponding manual and chapter numbers:

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<td>Universal Probe Rack connection</td>
<td>CAN-175</td>
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1.3 HARDWARE DESCRIPTION

Each Kontron LA has the following board configuration (see Figure 1-1):

- KDT6 is the Z80-based, general-purpose computer board that has 256K of memory with two serial ports, one parallel port, and a floppy disk controller.

- LA INT is the I/O board that controls the reset logic, serial/parallel ports, GPIB/RS-232 connections, interface to the front panel keyboard, and the CPU-driven TTL connection.

- TBQ is the Time Base and Clock Qualifier board that controls clock generation.

- SEQ is the Trigger Sequencer Controller board that handles triggering.

- DMB is the Data Memory Board (0 to 4) that maintains data recording. Each board supports two probes and has its own clock, either external or internal.

- TMB is the Time Measurement Board, which is an optional component that records time information during Data Qualified and Transition Recording.
The boards are all plugged into the LA's motherboard, which has a double Eurocard bus. There are seven pairs of 64-pin connectors; each connector pair is assigned to one of two buses:

- **A-Bus**

  This is a slower TTL bus used for memory access by the CPU as well as for managing other computer components.

- **B-Bus**

  This is a high-speed ECL bus used for communication between boards during a recording or trigger search.

See Figure 1-2 for a functional block diagram of the LA hardware.
Figure 1-2. LA Hardware Functional Block Diagram
CHAPTER 2
TEST SETUP

2.1 PRE-TEST INSTRUCTIONS

Including this manual, we recommend that you have the following assembled prior to testing:

Documentation: See publications listed in section 1.2

Disks: Computer Test, SMK-LA-1001-01
KLA/KSA Diagnostic Program (LDP), SMK-LA-1010-01

Equipment: LA-32, LA-48 or LA-64

Probes (LA-SPDA):

- 32 channels = 6
- 48 channels = 8
- 64 channels = 10

Universal Probe Rack (LA-UPR-10)

LA test configurator with flat ribbon cables

We also suggest that you review the Quick Reference Guide in subsection 1.2.2, which identifies where supplemental testing information is located.

2.2 TEST RUN PROCEDURES

Again, we advise you to conduct your testing according to the board configuration (see section 1.3). To test the KDT6 and LA INT boards, insert the Computer Test disk into drive A, press the RESET button to automatically load the program, and follow the prompts to complete testing.

The two methods for using the LDP software to test the TBQ, SEQ and DMB boards are:

- Self-Test (with UPR and test configurator)
- Manual (without UPR and test configurator)
2.2.1 SELF-TEST METHOD

For the self-test method, perform the following steps:

1. Connect all probes into the LA-UPR-10.

2. Connect all probes to their respective positions in the rear of the LA.

3. Connect one ribbon cable of the test configurator to the front of the LA-UPR-10. Next, connect the other ribbon cable to the Data Probe/Clock Probe test terminals on the LA's back panel. These test terminals are controlled by the pattern generator circuit on the SEQ board.

4. Insert the LDP disk into drive A, press RESET to load the program, and press key 1 to start the test; follow the LDP prompts to complete testing. NOTE: If you want the test to run automatically without stopping, press the "+" key before pressing key 1, which toggles to OFF (default is ON).

2.2.2 MANUAL METHOD

If no Universal Probe Rack is available, connect the probes to the Data Probe test terminal on the LA's back panel according to the LDP operating instruction prompts. For the manual method, perform the following steps:

1. Insert LDP disk into drive A and press RESET to load the program.

2. After the Main Menu (see Figure A-1) has appeared on the screen, you can press the "+" key, which eliminates test interruption after each screen.

3. Press key 1 to start the test.

4. If the screen shows "No defective board detected", the test is finished and the equipment is in perfect working condition.

5. If, however, errors are detected and there is no indication as to which test recognizes the error, follow steps 6 through 8.

6. Push the "+" key to follow the test run on the screen.

7. Resume the test run by pressing key 1.
8. If the test indicating the presence of an error is found, press the RUBOUT key (external keyboard) or the F1 key (KLA keyboard) to get back to the Main Menu.

9. Press the "+" key again, which indicates "stop after each screen is off".

10. Press key 2 to get into the Single-Test Menu.

11. In the Single-Test Menu if you want the test to run continuously, set the flag ON by pressing key C (see Figure A-2).

12. Using the menu, select a test and then start the test by pressing the RUN/STOP key.

13. Because the audible error detection is switched ON, a "beep" will sound off during each test run when it identifies which board has an error.

   WARNING: Exchanging boards is not recommended while the power is on.

It is important to note that all data lines must go across the TBQ board and to the data bus. If one of the lines is defective, almost all tests are going to yield a negative result.
In order to test the various functions of the LA boards, all RAMs located on the boards have to be in excellent working condition. Therefore, software diagnosis starts out with memory tests, followed by an operation check of the interface with the TBQ, SEQ and DMB boards. These memory tests are subdivided into data tests and address tests, which are described in the following sections.

3.1 DATA TESTS

In data tests, the same data pattern is laid down in all memory elements in order to ignore possible addressing mistakes. The data pattern itself is constructed in such a way that every bit at one point has a low and a high state. Moreover, the layout of the data pattern can indicate faulty connections between the data bits.

This kind of data test can be conducted with the following memories:

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<th>Specific RAM</th>
<th>Addresses*Data</th>
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<td>256*8 (exists 2x)</td>
</tr>
<tr>
<td>SEQ Level Address RAM</td>
<td>16*4</td>
</tr>
<tr>
<td>SEQ Occurrence Counter RAM low byte</td>
<td>16*8</td>
</tr>
<tr>
<td>SEQ Occurrence Counter RAM high byte</td>
<td>16*8</td>
</tr>
<tr>
<td>SEQ Level Status RAM</td>
<td>16*8</td>
</tr>
<tr>
<td>SEQ Trigger Filter RAM</td>
<td>16*4</td>
</tr>
<tr>
<td>DMB Condition RAM</td>
<td>256*8 (exists 4x)</td>
</tr>
</tbody>
</table>
Reasons for negative test results:
- Defective RAM
- Defective buffer
- Errors in the data logger

In the case of DMB Data RAM and TMB Data RAM, data cannot be written in from the computer directly; however, it is generated and written in by the DMB and TMB, respectively. The computer's task is to read the data and check it for accuracy of information.

3.2 ADDRESS TESTS

In order to find addressing errors, the RAMs are loaded with a non-repetitive pattern. This assures that each pattern is only laid down at one distinctive point in the RAM. The computer reads this pattern and checks it for accuracy of information.

Reasons for negative test results:
- Defective RAM
- Defective address counter
- Error in address logger

On the SEQ, the address counter is tested for the level address (Register 60H) in addition to the tests mentioned above. In order to yield a positive result in the test, it is not absolutely necessary that the RAMs are in perfect working condition.

Address counters located on the DMBs are also tested for data RAMs. According to the selected memory depth (2K, 4K, 8K), it is determined if the address counter can count properly all the way through the entire depth of memory. If another test is conducted, it shows whether the address counter can be precharged with any permissible value.
CHAPTER 4
TBQ TESTS

This chapter contains the tests listed below for the Time Base and Clock Qualifier (TBQ) board. The flowchart for each test (if applicable) precedes the description of the test. Schematics for the TBQ board are at the end of the chapter.

4.1 Time Base Test
4.2 All Clocks Triggered by Divider Chain Test
4.3 Slow-Clock-Detection and Probe ID Test
4.4 Qualifier Inputs Test
4.5 Interlace Clocks ILA1, ILB1, ILA2 and ILB2 Test
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4.1 TIME BASE TEST

Name of the test in the source listing: CLOKTS
In the Single-Test Menu of the LDP: Special Test 01

Purpose: CLOKTS determines if the time base works properly.

Reasons for negative test results:
- CL 1000 does not show up (error in clock generator or in divider chain).
- Error in the slow-clock-detection (check by means of Special Test 03, see section 4.3).

Description of the test:

The different clockings are generated in a divider chain (see page 2 of the TBQ schematics). If the slowest clocking is operating (i.e., 1000ms; hereafter referred to as CL 1000), it can safely be assumed that the divider chain is in perfect working condition.

Because CL 1000 is used in the slow-clock-detection, it is possible to test its operation via software.

The signal ENEX/ is induced and reinduced in Coil 1 (no more than 65,535 times). Thus, an external clocking rhythm is stimulated because the signals TJ0, TJ1, TK0 and TK1 toggle in the clocking rhythm of ENEX/ (see page 4 of the TBQ schematics).

Moreover, Coil 1 reads Register 73H until the date 0FH changes into 00H, which should occur when the next SYNC signal comes on. (The FLIP-FLOPs L6, K6, J5 and K5 are induced as variable cycle operations.) If the date 00H is not found within 65,535 cycles, the test result is negative.
4.2 ALL CLOCKS TRIGGERED BY DIVIDER CHAIN TEST

Name of the test in the source listing: CLOKT2
In the Single-Test Menu of the LDP: Special Test 02

Purpose: CLOKT2 determines if the adjustable frequencies have the proper value, and if they have been selected and processed properly.

Reasons for negative test results:

- Error detection (too fast or too slow) in all frequencies indicates a missing condition increment (Cause: DMB(s) or SEQ).

- Error detection in some frequencies indicates that there are either errors in the occurrence counter (SEQ) or in the time base (TBQ).
Description of the test:

A 16-bit wide occurrence counter is located on the SEQ. The counter uses a clock that has been selected by the TBQ. If this counter is asked to count for a specific period of time, an exactly defined counter reading has to be reached when given a precise frequency of counting. This enables the user to determine whether or not the counter readings and clockings are correct.

NOTE: A prerequisite for this test is that the counter must be in excellent working condition. Experience with this test has shown that the counter itself is imperfect rather than the clocking.

In order for the occurrence counter to work, three conditions have to be met:

1. Condition 0 (increment) has to be active. To achieve an active Condition 0, the Condition RAMs on the DMBs have to be filled with 11H. In addition, the Condition RAMs have to be enabled accordingly (load Register n2 with 30H).

2. No final trigger should have been found yet. By filling the Level Status RAMs of the sequencer with 1BH, the result is that no final trigger can be found. (Bit 4 is high at all times.)

3. The LA has to be "armed". The "arming" of the LAs is done via Register 72 on the TBQ.
Tell the user to attach a data probe and to restart the test by pressing RETURN.

Set all data probes for ECL Threshold (Register 76/77 with 72H)
Enable all external clocks (Register 72 with 0FH)
Enable -J0, +J0, -K0, and +K1
Load Qualifier RAM Register 74 with 66H
Arm the LA

Is an existing clock recognized? (Reg. 73H: XXXXXX11B Probe J, XXXX11XXB Probe K)
- Yes
  - Test okay
- No
  - Test faulty

Figure 4-2. TBQ72 Flowchart
4.3 SLOW-CLOCK-DETECTION AND PROBE ID TEST

Name of the test in the source listing: TBQ72
In the Single-Test Menu of the LDP: Special Test 03

Purpose: TBQ72 determines if

a. An attached data probe is recognized properly.

b. The slow-clock-detection works properly.

Reasons for negative test results:

As per a:

- Route-marking characteristic on the probe was improperly wired or not wired at all.

- Error in the data line of Register 72.

As per b:

- Probe is not properly attached to the SEQ.

- Probe or test configurator wire defective (test has to be conducted).

- Slow-clock-detection defective (see section 4.1).
Tell the user to attach a data probe and to start the test once again by pressing the RETURN key.

Set all probes for ECL Threshold (Register 76/77 with 72H)

Enable all external clocks (Register 72 with 0FH)

Enable -J0, +J0, -K0, and +K1
Load Qualifier RAM from Register 74 for the Qualifier to be tested

Arm the LA

Error in Qualifier

Is the Qualifier recognized?

Have all Qualifiers been tested?

START

Is probe attached?
Reg 72H: XXXXXX1118 Probe J
XX111XXXXE Probe K

no

yes

yes

no

Was RETURN key pressed?

no

yes

no

yes

END

Figure 4-3. QUALTS Flowchart
4.4 **QUALIFIER INPUTS TEST**

Name of the test in the source listing: QUALTS
In the Single-Test Menu of the LDP: Input Tests 09 and 10

**Purpose:** QUALTS checks the data line from the pattern generator on the SEQ up to the Qualifier RAM on the TBQ.

**Reasons for negative test results:**
- Probe is not correctly attached to the SEQ.
- Probe or test configurator wire is defective (test has to be conducted).
- Pattern generator on the SEQ does not supply the right pattern.
- Input buffer on the TBQ is defective.
The Condition RAMs of the DMBs will be loaded with 11H: for Address starting at 00H up to 7FH
00H: for Address starting at 80H up to FFH

All interface clocks will be enabled with
0CH: for Register 75H
Test frequency is 1 MHz (1 megacycle/s) and with
35H: for Register 70H

Conditions will be enabled on the DMB0 with
39H: for Register 02H

LA will be armed

Read Register 02 and retain value

Read Register 02.
Does new value equal old value?

yes

Is loop finished?

no

ILA and ILB okay

yes

ILA is defective

no

ILA and ILB okay

yes

ILA and ILB okay

no

ILA is defective

Is loop finished?

yes

ILA is defective

yes

ILA is defective

Figure 4-4. ILAB12 Flowchart
4.5 **INTERLACE CLOCKS ILA1, ILB1, ILA2 AND ILB2 TEST**

Name of the test in the source listing: **ILAB12**
In the Single-Test Menu of the LDP: **Special Test 06**

**Purpose:** ILAB12 determines if the interlace clocks are present, if they are selected properly, and indicates whether they are processed.

**Reasons for negative test results:**
- Control error on the TBQ (Register 75H, bits 2 and 3).
- Errors in the interlace clocks themselves.
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This chapter contains the tests listed below for the Trigger Sequencer Controller (SEQ) board. The flowchart for each test (if applicable) precedes the description of the test. Schematics for the SEQ board are at the end of the chapter.

5.1 Level Counter and Occurrence Counter Test
5.2 Trigger Filter 0 Test
5.3 Trigger Filter 1 Test
Initialize the LA such that the occurrence counter will do the counting (compare CLOKT2)

Load test frequency

Has end-mark been reached?

Increment the reference counter

Has maximum value been exceeded?

Has last level been reached? Register 60 = 1FH

Actual value = Rated value?

Actual value < Rated value?

Actual value > Rated value?

ERROR 1

okay

ERROR 2

ERROR 3

Figure 5-1. LEVINC Flowchart
5.1 LEVEL COUNTER AND OCCURRENCE COUNTER TEST

Name of the test in the source listing: LEVINc
In the Single-Test Menu of the LDP: Special Test 04

Purpose: LEVINc determines if the occurrence counter is loaded properly at every level, if it counts properly, and if the passage through all trigger levels takes place at the right time.

Description of errors:

Error 1:
The reference counter has reached a value of 8,000H; thus, it is safe to assume that the last level is not reached.

Possible causes:
- It is unlikely that the occurrence counter "got stuck" in one of the levels.
- The occurrence counter probably does not work at all.

Error message in the program:
"Last level was not reached"

Error 2:
The last level was reached, but too late.

Possible causes:
- The level counter does not increment.
- The occurrence counter is loaded improperly.
- The occurrence counter counts improperly.
- Errors in the data line of Register 60H.

Error message in the program:
"Last level was reached too late"

Error 3:
The last level was reached, but too early.

Same causes as in Error 2

Error message in the program:
"Last level was reached too early"
5.2 **TRIGGER FILTER 0 TEST**

Name of the test in the source listing: TRGFL0

In the Single-Test Menu of the LDP: Special Test 07

**Purpose:** TRGFL0 determines if the trigger filter for Condition 0 (increment) is in proper working condition.

**Reasons for negative test results:**
- Trigger filter is loaded improperly.
- Trigger filter does not operate properly.
- Error in the logic (which is influenced by the trigger filter).

In principle, the sequence of operation in this test is the same as in LEVINC. The differences between the two tests are:
- Only one test frequency of 100 kHz (100 kilocycles/s)
- In Level Status RAM, trigger filter 0 is enabled (1 AH)
5.3 **TRIGGER FILTER 1 TEST**

Name of the test in the source listing: **TRGFL1**

In the Single-Test Menu of the LDP: **Special Test 08**

**Purpose:** TRGFL1 determines if the trigger filter for Condition 1 (JUMP) is in proper working condition.

**Reasons for negative test results:**

- Trigger filter is loaded improperly.
- Trigger filter does not operate properly.
- Error in Condition 1 (JUMP).
- Error in the logic (which is influenced by the trigger filter).

In contrast to TRGFL0, the Level Status RAM is loaded with 19H (enable trigger filter 1) and the Condition RAMs are loaded with EEH (Condition 0 is not active; Condition 1 is active). Otherwise, Special Test 08 is conducted in the same way as Special Test 07.

**NOTE:** This is the only test that uses the condition JUMP. It checks to see that the JUMP to every level is conducted properly.
Kontron LA Diagnostic Program (SMK-LA-1010-01)

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This chapter contains the tests listed below for the Data Memory Board (DMB). There can be up to four of these boards, which are numbered 0 through 3. The flowchart for each test (if applicable) precedes the description of the test. Schematics for the DMB board are at the end of the chapter.

6.1 Condition GLIT Test
6.2 All Trigger-Delay-Counters Test
6.3 Glitch-Latch Test
6.4 Transitional Clocking Signal (TCLK) Test
6.5 Conditions 2 and 3 (Data Qualified Recording) Test
6.6 Probe Test
6.7 DMB Inputs and Additional Data RAM Test
Enable Glitch-trigger on the SEO Level Status RAM with 13H

Arm the LA

Increment counter

Has rated value been reached?

Has Level 2 been reached?
Register 61H = EDH

yes

no

ERROR 1

Stop LA

Enable GLA (Register n2 with 78H) or enable GLB (Register n2 with B8H) on DMBn

Arm the LA

Increment counter

Has maximum value been exceeded?

Has last level been reached:
Register 61 = 0FH?

yes

no

ERROR 2

Test okay

END

Figure 6-1. GLAGLB Flowchart
6.1 **CONDITION GLIT TEST**

**Name of the test in the source listing:** GLAGLB

**In the Single-Test Menu of the LDP:** Glitch Tests Condition

**Purpose:** GLAGLB determines if Condition GLIT is selected properly by each DMB, if Condition GLIT is received properly by the SEQ, and if it is processed.

**Description of errors:**

**Error 1:**

Although glitch was not enabled on the DMBs, Level 2 was reached on the SEQ. As a result, Condition GLIT is always active.

**Possible causes:**

- If errors occur in all eight tests, the cause for the errors is probably found on the SEQ.
  
  Example: Line GLIT, short circuit on low

- If errors occur only in some of the tests, the cause for the errors is probably found on the respective DMB.
  
  Example: Control error in Register 2 on the respective DMB

**Error message in the program:**

"Condition glit error"

**Error 2:**

The last level was not reached, probably due to a missing Condition GLIT.

**Possible causes:**

- If errors occur in all eight tests, the cause for errors is probably found on the SEQ.
  
  Examples: Line GLIT, short circuit on high
  Line GLIT interrupted
Possible causes (continued):

- If errors occur in only some of the tests, the cause for the errors is probably found on the respective DMB.

Example: Control error in Register 2 on the respective DMB

Error message in the program:
"Condition glit is missing"
Kontron LA Diagnostic Program (SMK-LA-1010-01)

START

Initialize the LA such that the trigger-delay-counter will do the counting

Load test frequency

Has end-mark been reached?

yes END

no Load rated value for reference counter

Arm the LA

Increment reference counter

Has maximum rating been exceeded?

yes ERROR 1

no

no Has counter run out? 60H = D0000000H

yes

yes Have all four counters run out? Register 60H = 11111111B

no ERROR 2

Increment reference counter

Has maximum value been exceeded?

yes ERROR 1

no

no Have all other counters run out?

yes

Compare actual value with expected value
actual value > rated value = ERROR 3
actual value < rated value = ERROR 4
actual value = rated value = okay

Figure 6-2. DELCNT Flowchart
6.2 **ALL TRIGGER-DELAY-COUNTERS TEST**

Name of the test in the source listing: DELCNT
In the Single-Test Menu of the LDP: Special Test 05

**Description of errors:**

**Error 1:**
The maximum value (8,000H loops) of the reference counter was reached. As a result, no trigger-delay-counter ran out.

**Error 2:**
At least one trigger-delay-counter has run out. However, not all four trigger-delay-counters have completed the run.

By now, all trigger-delay-counters have run out, but the timing of the work cycle was wrong.

**Error 3:**
Trigger-delay-counter ran out too late.

**Error 4:**
Trigger-delay-counter ran out too early.
Test for incorrect glitches
Test frequency: 50 MHz (50 megacycles/s)

Arm the LA

Increment the counter

Has counter reached rated value?

yes

no

Read data (Register 2) masked with 10101010B

Glitch present?

yes

ERROR 1

no

Load next test frequency

Last test frequency?

yes

END

no

Arm the LA

Increment the counter

Has maximum value been exceeded?

yes

ERROR 2

no

Read data (Register 2) Mask the glitch

Glitch present?

yes

Figure 6-3. GLIT Flowchart
6.3 **GLITCH-LATCH TEST**

Name of the test in the source listing: **GLIT**
In the Single-Test Menu of the LDP: **Glitch-Latch Tests**

**Purpose:** GLIT determines if all glitch-latches on the DMBs are working properly.

**Description of errors:**

**Error 1:** Glitches were detected, although no glitches should appear at a test frequency of 50 MHz (50 megacycles/s).

**Possible causes:**

- Defective FLIP-FLOP at respective input.
- Control error in Register 2 on the respective DMB.

**Error message in the program:**

"Test of false occurring glitches":

<table>
<thead>
<tr>
<th>Glitch-latch</th>
<th>status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glitch-latch 01</td>
<td>error/ok</td>
</tr>
<tr>
<td>Glitch-latch 03</td>
<td>error/ok</td>
</tr>
<tr>
<td>Glitch-latch 05</td>
<td>error/ok</td>
</tr>
<tr>
<td>Glitch-latch 07</td>
<td>error/ok</td>
</tr>
</tbody>
</table>

**Error 2:** No glitch appeared, although the respective glitch-latch at this particular test frequency should recognize the input signals as glitches.

**Possible causes:**

- Defective FLIP-FLOP at respective input.
- Control error in Register 2 on the respective DMB.

**Error message in the program:**

"Test of false missing glitches":

<table>
<thead>
<tr>
<th>Glitch-latch</th>
<th>status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glitch-latch 01</td>
<td>error/ok</td>
</tr>
<tr>
<td>Glitch-latch 03</td>
<td>error/ok</td>
</tr>
<tr>
<td>Glitch-latch 05</td>
<td>error/ok</td>
</tr>
<tr>
<td>Glitch-latch 07</td>
<td>error/ok</td>
</tr>
</tbody>
</table>
Figure 6-4. TRANS Flowchart
6.4 TRANSITIONAL CLOCKING SIGNAL (TCLK) TEST

Names of the test in the source listing: TRANS
In the Single-Test Menu of the LDP: Transition Tests

Purpose: TRANS determines if the transitional clocking signal (TCLK) is triggered by the DMBs and processed by the SEQ.

Description of errors:

Error 1:
The trigger-delay-counters on the SEQ have run out, although the TRANSITION DETECTION command on the DMBs was disabled. As a result, the transitional clocking signal (TCLK) is permanently active.

Possible causes:
- TCLK short circuit on high.
- Control error in Register 2 on the respective DMB (TRANSITION DETECTION cannot be disabled).

Error message in the program:
"Test of false occurring transitions error"

Error 2:
Trigger-delay-counters on the SEQ did not run out within the maximum time allowed for testing, although TRANSITION DETECTION command on the respective DMB was enabled.

Possible causes:
- If errors occur in all eight tests, the cause for the errors is probably found on the SEQ.
  Example: Conductor TCLK, short circuit on low
- If errors occur only in some of the tests, the cause for the errors is probably found on the respective DMB.
  Example: Control error in Register 2 on the respective DMB

Error message in the program:
"Transitional clocking signal (TCLK) error"
Stop the LA and read the data
Wait some milliseconds
Stop the LA and read the data

Actual value = Rated value?

no → ERROR 1

yes →

Enable condition 3
Address 0 = 86H
Arm the LA
Wait some milliseconds
Stop the LA and read the data

Actual value = Rated value?

no → ERROR 2

yes → Test okay

END

Figure 6-5. DATAQUAL Flowchart
6.5 CONDITIONS 2 AND 3 (DATA QUALIFIED RECORDING) TEST

Name of the test in the source listing:  DATAQUAL
In the Single-Test Menu of the LDP:  Qualified Recording Test

Purpose:  DATAQUAL determines if Conditions 2 and 3 are generated properly by the DMBs and if they are properly processed by the SEQ.

Description of errors:

Error 1:
The data measured does not correspond with the rated values (01, 02, 03, 04, 05, 06, 07, 08, 09, 00, 01, etc.). Condition 2 was set for this data.

Possible cause:
- Errors on the conductor CND2.

Error message in the program:
"Condition 2 error"

Error 2:
The data measured does not correspond with the rated values (01, 02, 03, 04, 05, 06, 07, 08, 09, 00, 01, etc.). Condition 3 was set for this data.

Possible cause:
- Errors on the conductor CND3.

Error message in the program:
"Condition 3 error"
Kontron LA Diagnostic Program (SMK-LA-1010-01)

Figure 6-6. PROBETS Flowchart
6.6 PROBE TEST

Name of the test in the source listing: PROBETS

In the Single-Test Menu of the LDP: Probe Tests

Purpose: PROBETS determines if all data probes are working properly.

Description of errors:

Error 1:
In the first and second tests results all bits have the same value, although the threshold is adjusted to -12 volts for the first test and to +12 volts for the second test.

Possible causes:
- Errors in the data transfer from the TBQ to the probe.
- Errors in threshold hardware of the probe.

Error 2:
The first and second tests results showed that not all bits differed.

Possible causes:
- Amplifier in the probe is defective.
- ECL compactor in the probe is defective.

Error message in the program for Test 2:
"Test of all channels via changing threshold voltage"
(Error message is indicated separately for each channel.)

Error 3:
Although the threshold is adjusted to -1.3 volts (ECL threshold), some of the bits never alternate their polarity.

Possible causes:
- Test configurator wire or UPR is defective.
- Amplifier in the probe is defective.

Error message in the program for Test 3:
"Test of all channels via ECL input signal"
(Error message is indicated separately for each channel.)
Error 4:
Although the threshold is adjusted to -2.0 volts, not all data was FFH. If Error 3 did not occur, Error 4 indicates an undershoot or a negative offset.

Possible cause:
- Amplifier in the probe is defective or misaligned.

Error message in the program for Test 4:
"Test of overshoot respectively positive offset voltage" (Error message is indicated separately for each channel.)

Error 5:
Although the threshold is adjusted to -0.5 volts, not all data is 00H. If Error 3 did not occur, Error 5 indicates an overshoot or a positive offset.

Possible cause:
- Amplifier in the probe is defective or misaligned.

Error message in the program for Test 5:
"Test of undershoot respectively negative offset voltage" (Error message is indicated separately for each channel.)
6.7 DMB INPUTS AND ADDITIONAL DATA RAM TEST

Name of the test in the source listing: PODTS
In the Single-Test Menu of the LDP: Input Tests

Purpose: PODTS determines if all memory data on the DMBs supplied by the pattern generator is recorded. Possible addressing errors in the DMB Data RAMs are recognized, because the recorded pattern is induced by a decimal counter.

The pattern generator on the SEQ is tested.

The entire data line (starting from the input buffer up to and including the Data RAM) is tested.

Reasons for negative test results:
- Defective probe
- Pattern generator on the SEQ board is defective
- Test configurator wire or UPR is defective
- Error in the DMB data line
- Data RAM on the DMB is defective
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This appendix contains a list of the LDP Main Menu input fields as shown in Figure A-1 and a brief description of each. The Single-Test Menu is illustrated in subsequent pages.

**Commands**

1. Start complete test-sequence
2. Go to single-test menu
3. Print a detailed error-description
4. Print suspected defective boards
5. Exit

**Switches**

1. Stop after each screen is on
2. Akustik error message is on
3. User guidance for pod-tests is on

**Information**

You can always come back to this menu with \( \text{F1} \) or \( \text{F1} \),

You can always leave the program with \( \text{ESC} \) or \( \text{F2} \).

Please select your input:

```
Figure A-1. LDP Main Menu
```
Kontron LA Diagnostic Program (SMK-LA-1010-01)

(1) **start complete test-sequence**
Runs through all diagnostic tests (see "+" below).

(2) **user guidance for pod-test on**
Displays backplane diagram, showing unconnected probes as blinking fields. If all probes are connected, this screen does not appear.

(3) **go to single-test menu**
If you see an error during the first run of diagnostic tests, you can choose to run individual tests. The types of tests are highlighted in reverse video; the list below allows you to select where to run that test. Individual tests are activated with the RUN/STOP key.

(4) **print a detailed error-description**
Displays final diagnostic test results. You must run the diagnostic tests first in order to get an accurate summary on this screen.

(5) **print suspected defective boards**
Displays list of suspected defective boards. You must run the diagnostic tests first in order to get an accurate summary on this screen.

(6) **exit**
Returns you to the Main Menu.

(+) **stop after each screen is on**
The LA stops after each diagnostic test. If you enter "+" in the input field, this line reads "stop after each screen is off". The LA then runs through all diagnostic tests without stopping.

(-) **akustik error message is on**
The LA "beeps" at every error. If you enter "-" in the input field, this line reads "akustik error message if off". Then the LA does not "beep" at every error.
The tests in the Single-Test Menu are represented in Figure A-2, which is followed by a list of test names and corresponding page numbers of the sample screen shots.

<table>
<thead>
<tr>
<th>Test Code</th>
<th>Test Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(G1)</td>
<td>Test of data bus and rams</td>
</tr>
<tr>
<td>(G2)</td>
<td>Memory tests of DMB(s)</td>
</tr>
<tr>
<td>(G3)</td>
<td>Memory tests of TBQ, SEQ, TMB</td>
</tr>
<tr>
<td>(G4)</td>
<td>Address-counter-tests</td>
</tr>
<tr>
<td>(G5)</td>
<td>Glitch-tests CONDITION 1</td>
</tr>
<tr>
<td>(G6)</td>
<td>Glitch-latch-tests</td>
</tr>
<tr>
<td>(G7)</td>
<td>Transition-tests</td>
</tr>
<tr>
<td>(G8)</td>
<td>Qualified-recording-tests</td>
</tr>
<tr>
<td>(G9)</td>
<td>Probe-tests</td>
</tr>
<tr>
<td>(GA)</td>
<td>Input-tests</td>
</tr>
<tr>
<td>(GB)</td>
<td>Special tests</td>
</tr>
<tr>
<td>(X)</td>
<td>Back to main menu</td>
</tr>
<tr>
<td>(F)</td>
<td>Forward</td>
</tr>
<tr>
<td>(B)</td>
<td>Backward</td>
</tr>
<tr>
<td>(C)</td>
<td>Continuous flag</td>
</tr>
<tr>
<td>(E)</td>
<td>Stop on error</td>
</tr>
</tbody>
</table>

Test of data bus and rams

- (00) - Memory test (data bus) of condition ram on DMB0
- (01) - Memory test (data bus) of condition ram on DMB1
- (02) - Memory test (data bus) of condition ram on DMB2
- (03) - Memory test (data bus) of condition ram on DMB3
- (04) - Memory test (data bus) of TBQ qualifier ram
- (05) - Memory test (data bus) of SEQ level address ram
- (06) - Memory test (data bus) of SEQ occurrence counter ram LO
- (07) - Memory test (data bus) of SEQ occurrence counter ram HI
- (08) - Memory test (data bus) of SEQ level status ram
- (09) - Memory test (data bus) of SEQ trigger filter ram

Please select your input:

Figure A-2. Single-Test Menu
### Test Name

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data test, address test</td>
<td>1</td>
</tr>
<tr>
<td>Clock test of the TBQ board</td>
<td>2</td>
</tr>
<tr>
<td>Test of the following clocks via occurrence counter of SEQ</td>
<td>3</td>
</tr>
<tr>
<td>Probe identification for connector C - probe J</td>
<td>4</td>
</tr>
<tr>
<td>Probe identification for connector C - probe K</td>
<td>5</td>
</tr>
<tr>
<td>Qualifier input test of pod J</td>
<td>6</td>
</tr>
<tr>
<td>Qualifier input test of pod K</td>
<td>7</td>
</tr>
<tr>
<td>Level increment test</td>
<td>8</td>
</tr>
<tr>
<td>Trigger-delay-counter test</td>
<td>9</td>
</tr>
<tr>
<td>Test of trigger filter 0 on SEQ (via condition 0)</td>
<td>10</td>
</tr>
<tr>
<td>Test of trigger filter 1 on SEQ (via condition 1)</td>
<td>11</td>
</tr>
<tr>
<td>Test of GLA on DMB0 via condition GLIT on SEQ</td>
<td>12</td>
</tr>
<tr>
<td>Test of GLB on DMB0 via condition GLIT on SEQ</td>
<td></td>
</tr>
<tr>
<td>Test of GLA on DMB1 via condition GLIT on SEQ</td>
<td></td>
</tr>
<tr>
<td>Test of GLB on DMB1 via condition GLIT on SEQ</td>
<td></td>
</tr>
<tr>
<td>Test of GLA on DMB2 via condition GLIT on SEQ</td>
<td></td>
</tr>
<tr>
<td>Test of GLB on DMB2 via condition GLIT on SEQ</td>
<td></td>
</tr>
<tr>
<td>Test of GLA on DMB3 via condition GLIT on SEQ</td>
<td></td>
</tr>
<tr>
<td>Test of GLB on DMB3 via condition GLIT on SEQ</td>
<td></td>
</tr>
<tr>
<td>Glitch-latch test of pods 1-8</td>
<td></td>
</tr>
<tr>
<td>Test of false occurring transitions</td>
<td></td>
</tr>
<tr>
<td>Transition recording test of pods 1-8</td>
<td></td>
</tr>
<tr>
<td>Data qualified recording test pods 1-8</td>
<td></td>
</tr>
<tr>
<td>Test of interlace clocks ILA1, ILB1, ILA2, ILB2 (ILAC)</td>
<td></td>
</tr>
<tr>
<td>Probe test pods 1-8</td>
<td></td>
</tr>
<tr>
<td>Probe test probes 1-8</td>
<td></td>
</tr>
<tr>
<td>Board(s) suspected to be defective</td>
<td></td>
</tr>
<tr>
<td>Board</td>
<td>Specific: RAM</td>
</tr>
<tr>
<td>-------</td>
<td>--------------</td>
</tr>
<tr>
<td>TBQ</td>
<td>Qualifier RAM ok</td>
</tr>
<tr>
<td>TBQ</td>
<td>Qualifier RAM ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Level Address ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Occurrence CNT ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Occurrence CNT ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Status ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Trigger filter ok</td>
</tr>
<tr>
<td>DMB 3</td>
<td>Condition RAM ok</td>
</tr>
<tr>
<td>DMB 3</td>
<td>Data RAM ok</td>
</tr>
<tr>
<td>DMB 2</td>
<td>Condition RAM ok</td>
</tr>
<tr>
<td>DMB 2</td>
<td>Data RAM ok</td>
</tr>
<tr>
<td>DMB 1</td>
<td>Condition RAM ok</td>
</tr>
<tr>
<td>DMB 1</td>
<td>Data RAM ok</td>
</tr>
<tr>
<td>DMB 0</td>
<td>Condition RAM ok</td>
</tr>
<tr>
<td>DMB 0</td>
<td>Data RAM ok</td>
</tr>
<tr>
<td>TMB</td>
<td>Data RAM ok</td>
</tr>
</tbody>
</table>

test is in hold, type any key to continue
test of the 100ms via slow-clock-detection  

ok

test is in hold, type any key to continue
test of the following clocks
via occurrence-counter of SEQ

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Jitter (Samples)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>+ 0006 Samples</td>
</tr>
<tr>
<td>50</td>
<td>- 0001 Samples</td>
</tr>
<tr>
<td>20</td>
<td>- 0001 Samples</td>
</tr>
<tr>
<td>10</td>
<td>- 0000 Samples</td>
</tr>
<tr>
<td>1</td>
<td>+ 0001 Samples</td>
</tr>
<tr>
<td>100 KHz</td>
<td>+ 0001 Samples</td>
</tr>
<tr>
<td>1 KHz</td>
<td>- 0000 Samples</td>
</tr>
<tr>
<td>100 Hz</td>
<td>- 0000 Samples</td>
</tr>
<tr>
<td>10 Hz</td>
<td>- 0000 Samples</td>
</tr>
</tbody>
</table>

test is in hold, type any key to continue
probe-identifikation for Connector C (PROBE J) ok
slow-clock-detection for Connector C (PROBE J) ok

test is in hold, type any key to continue
probe-identifikation for Connector D (PROBE K) ok
slow-clock-detection for Connector D (PROBE K) ok

test is in hold, type any key to continue
Qualifier input test of pod J  ok

(also runs QUALIFIER INPUT TEST OF POD K)

test is in hold, type any key to continue
level-increment-test

100 MHz = 10 ns  jitter = + 0000 Samples  ok
50 MHz = 20 ns  jitter = + 0000 Samples  ok
20 MHz = 50 ns  jitter = + 0000 Samples  ok
10 MHz = 100 ns  jitter = + 0000 Samples  ok

test is in hold, type any key to continue
trigger-delay-counter-test

50 MHz = 20 ns
- Trigger-delay-counter 0 ok
- Trigger-delay-counter 1 ok
- Trigger-delay-counter 2 ok
- Trigger-delay-counter 3 ok

10 MHz = 100 ns
- Trigger-delay-counter 0 ok
- Trigger-delay-counter 1 ok
- Trigger-delay-counter 2 ok
- Trigger-delay-counter 3 ok

1 MHz = 1 us
- Trigger-delay-counter 0 ok
- Trigger-delay-counter 1 ok
- Trigger-delay-counter 2 ok
- Trigger-delay-counter 3 ok

100 KHz = 10 us
- Trigger-delay-counter 0 ok
- Trigger-delay-counter 1 ok
- Trigger-delay-counter 2 ok
- Trigger-delay-counter 3 ok

Test is in hold, type any key to continue
Test of trigger filter 0 on SEQ (via condition 0)

last level was reached in time jitter = + 0000 Samples ok

test is in hold, type any key to continue
Test of trigger filter 1 on SEQ (via condition 1) 
last level was reached in time jitter = + 0000 Samples ok 

test is in hold, type any key to continue
Test of GLA on DMB0 via condition GLIT on SEQ

condition GLITCH ok

(also runs Test of GLB on DMB0 via condition GLIT on SEQ
Test of GLA on DMB1 via condition GLIT on SEQ
Test of GLB on DMB1 via condition GLIT on SEQ
Test of GLA on DMB2 via condition GLIT on SEQ
Test of GLB on DMB2 via condition GLIT on SEQ
Test of GLA on DMB3 via condition GLIT on SEQ
Test of GLB on DMB3 via condition GLIT on SEQ)

test is in hold, type any key to continue
glitch-latch-test of pod 1

test of false occurring glitches  
test of missing glitches

Glitch-latch 01 ok
Glitch-latch 03 ok
Glitch-latch 05 ok
Glitch-latch 07 ok

Glitch-latch 01 ok
Glitch-latch 03 ok
Glitch-latch 05 ok
Glitch-latch 07 ok

(also runs glitch-latch-test of pods 2 - 8)

test is in hold, type any key to continue
test of false occurring transitions ok

test is in hold, type any key to continue
transition recording test of pod 1

Transitional clocking signal (TCLK) ok

(also runs transition recording test of pods 2 - 8)

test is in hold, type any key to continue
data qualified recording test pod 1  ok

(also runs data qualified recording test of pods 2 - 8)

test is in hold, type any key to continue  

Test of interlace clocks ILA1, ILB1, ILA2, ILB2, (ILAC)

ILA1  ok
ILB1  ok
ILA2  ok
ILB2  ok

test is in hold, type any key to continue
Probe-test probe 1

Test 1: Threshold hardware or all Inputs on Probe or OMS ok
Test 2: Test of all channels via changing Threshold voltage (no input necessary)
Test 3: Test of all channels via ECL-input-signal (Threshold is fixed)
Test 4: Test of overshoot respectively positive offset voltage
Test 5: Test of undershoot respectively negative offset voltage

<table>
<thead>
<tr>
<th>Channel</th>
<th>Test 2</th>
<th>Test 3</th>
<th>Test 4</th>
<th>Test 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 00</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>Channel 01</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>Channel 02</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>Channel 03</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>Channel 04</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>Channel 05</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>Channel 06</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>Channel 07</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
</tbody>
</table>

Test is in hold, type any key to continue

(also runs probe-test on pods 2 - 8)
Probe-test probe 1

(Also runs probe-test probe 2 - 8)

test is in hold, type any key to continue
board(s) suspected to be defective:

No defective board detected

Press [RETURN] or [RUN/STOP] to continue.
This appendix describes the possible board-specific LDP test failures and includes sample screen shots.
Simulated error on: TBQ board

Possible errors detected in the following tests:

- Data test, address test
- Test of the following clocks via occurrence counter on SEQ
- Probe identification for connector D (probe K)
- Qualifier input test of pod K
- Level increment test
- Trigger-delay-counter test
- Transition recording test of pods 1-8

Boards(s) suspected to be defective:

- TBQ - Time Base and Clock Qualifier
- SEQ - Trigger Sequencer Controller
- DMB0 - Data Memory Board 0
- DMB1 - Data Memory Board 1
- DMB2 - Data Memory Board 2
- DMB3 - Data Memory Board 3

Suggested correction: TBQ board replacement
<table>
<thead>
<tr>
<th>Board</th>
<th>Specific-RAM</th>
<th>Data-test</th>
<th>Address-test</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBQ</td>
<td>Qualifier RAM</td>
<td>special Address-test</td>
<td>Error</td>
</tr>
<tr>
<td>SEQ</td>
<td>Level Address</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Occurence CNT</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Occurence CNT</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Status</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Trigger filter</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 3</td>
<td>Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 3</td>
<td>Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 2</td>
<td>Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 2</td>
<td>Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 1</td>
<td>Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 1</td>
<td>Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 0</td>
<td>Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 0</td>
<td>Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>TMB</td>
<td>Data RAM</td>
<td>ok</td>
<td></td>
</tr>
</tbody>
</table>

test is in hold, type any key to continue
test of the following clocks
via occurrence-counter of SEQ

100 MHz = 10 ns jitter = + 0006 Samples     ok
50 MHz = 20 ns jitter = + 19E3 Samples     *too-fast*
20 MHz = 50 ns jitter = - 0001 Samples      ok
10 MHz = 100 ns jitter = - 0000 Samples     ok
1 MHz = 1 us jitter = - 0000 Samples        ok
100 KHz = 10 us jitter = + 0002 Samples     ok
10 KHz = 100 us jitter = + 0001 Samples     ok
1 KHz = 1 ms jitter = + 0000 Samples        ok
100 Hz = 10 ms jitter = - 0000 Samples      ok
10 Hz = 100 ms jitter = - 0001 Samples      ok

test is in hold, type any key to continue
probe-identifikation for Connector D (PROBE K) ok
slow-clock-detection for Connector D (PROBE K) ok

Test is in hold, type any key to continue.
Qualifier input test of pod K

Qualifier input 00 error
Qualifier input 01 error
Qualifier input 02 error
Qualifier input 03 error
Qualifier input 04 error
Qualifier input 05 error

test is in hold, type any key to continue
level-increment-test

100 MHz = 10 ns  jitter = + 0000 Samples  ok
50 MHz = 20 ns  jitter = - 00A1 Samples  too fast
20 MHz = 50 ns  jitter = + 0000 Samples  ok
10 MHz = 100 ns  jitter = + 0000 Samples  ok

test is in hold, type any key to continue
<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>Delay (ns)</th>
<th>Trigger-Delay-Counter 0</th>
<th>Trigger-Delay-Counter 1</th>
<th>Trigger-Delay-Counter 2</th>
<th>Trigger-Delay-Counter 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>20</td>
<td>ok</td>
<td>too early</td>
<td>too early</td>
<td>too early</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>100</td>
<td>10</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
<td>ok</td>
</tr>
</tbody>
</table>

- probably error on preset lines
- test is in hold, type any key to continue
transition recording test of pod 1
Transitional clocking signal (TCLK) -error-

test is in hold, type any key to continue
board(s) suspected to be defective:

TBQ  time-base and qualifier board
SEQ  sequence and control board
DMB0 data-memory-board 0
DMB1 data-memory-board 1
DMB2 data-memory-board 2
DMB3 data-memory-board 3

Press RETURN or RUN/STOP to continue
Simulated error on: SEQ board

Possible errors detected in the following tests:

- Data test, address test
- Test of the following clocks via occurrence counter on SEQ
- Level increment test
- Trigger-delay-counter test
- Test of trigger filter 0 on SEQ (via condition 0)
- Test of trigger filter 1 on SEQ (via condition 1)
- Test of GLA and GLB on DMB0 via condition GLIT on SEQ
- Data qualified recording test of pods 1-8

Boards(s) suspected to be defective:

- TBQ - Time Base and Clock Qualifier
- SEQ - Trigger Sequencer Controller
- DMB0 - Data Memory Board 0
- DMB1 - Data Memory Board 1
- DMB2 - Data Memory Board 2
- DMB3 - Data Memory Board 3

Suggested correction: SEQ board replacement
<table>
<thead>
<tr>
<th>Board</th>
<th>Specific RAM</th>
<th>Data-test</th>
<th>Address Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBQ</td>
<td>Qualifier RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>TBQ</td>
<td>Qualifier RAM</td>
<td>special Address-test</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ</td>
<td>Level Address</td>
<td>error</td>
<td>error</td>
</tr>
<tr>
<td>SEQ</td>
<td>Occurrence CNT</td>
<td>error</td>
<td>error</td>
</tr>
<tr>
<td>SEQ</td>
<td>Occurrence CNT</td>
<td>error</td>
<td>error</td>
</tr>
<tr>
<td>SEQ</td>
<td>Status</td>
<td>error</td>
<td>error</td>
</tr>
<tr>
<td>SEQ</td>
<td>Trigger filter</td>
<td>error</td>
<td>error</td>
</tr>
<tr>
<td>DMB 3</td>
<td>Condition RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 3</td>
<td>Data RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 2</td>
<td>Condition RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 2</td>
<td>Data RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 1</td>
<td>Condition RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 1</td>
<td>Data RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 0</td>
<td>Condition RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>DMB 0</td>
<td>Data RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>TMB</td>
<td>Data RAM ok</td>
<td>ok</td>
<td>ok</td>
</tr>
</tbody>
</table>

Test is in hold, type any key to continue.
test of the following clocks
via occurrence-counter of SEQ

100 MHz = 10 ns  jitter = - 01FD Samples  too slow
50 MHz = 20 ns  jitter = - 0000 Samples  ok
20 MHz = 50 ns  jitter = - 0201 Samples  too slow
10 MHz = 100 ns  jitter = - 0000 Samples  ok
1 MHz = 1 us  jitter = + 0001 Samples  ok
100 KHz = 10 us  jitter = - 0001 Samples  ok
10 KHz = 100 us  jitter = - 0001 Samples  ok
1 KHz = 1 ms  jitter = - 0200 Samples  too slow
100 Hz = 10 ms  jitter = - 0000 Samples  ok
10 Hz = 100 ms  jitter = - 0003 Samples  ok

test is in hold, type any key to continue

-2-
level-increment-test

100 MHz = 10 ns  jitter = - 008C Samples  too fast
50 MHz = 20 ns  jitter = - 0118 Samples  too fast
20 MHz = 50 ns  jitter = - 02BA Samples  too fast
10 MHz = 100 ns  jitter = - 0575 Samples  too fast

test is in hold, type any key to continue
### trigger-delay-counter-test

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Delay (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 MHz</td>
<td>20 ns</td>
</tr>
<tr>
<td>10 MHz</td>
<td>100 ns</td>
</tr>
<tr>
<td>1 MHz</td>
<td>1 us</td>
</tr>
<tr>
<td>100 KHz</td>
<td>10 us</td>
</tr>
</tbody>
</table>

**Note:**
- Probably error on preset lines
- Test is in hold, type any key to continue
Test of trigger filter 0 on SEQ (via condition 0)

last level was [not reached]; jitter = -0001 Samples [error]

test is in hold, type any key to continue
Test of trigger filter 1 on SEQ (via condition 1)

last level was not reached: jitter = - 0001 Samples error

test is in hold, type any key to continue •
Test of GLA on DMB0 via condition GLIT on SEQ
condition GLITCH is missing

test is in hold, type any key to continue.
Test of GLB on DMB0 via condition GLIT on SEQ

condition GLITCH [error]

condition GLICHT is missing

test is in hold, type any key to continue
data qualified recording test pod 1

Condition 2
Condition 3

Test is in hold, type any key to continue
board(s) suspected to be defective:

TBQ  time-base and qualifier board
SEQ  sequence and control board
DMB0 data-memory-board 0
DMB1 data-memory-board 1
DMB2 data-memory-board 2
DMB3 data-memory-board 3
TMB  time-measurement-board

Press #RETURN# or #RUN/STOP# to continue.
Simulated error on: DMB0 board*

Possible errors detected in the following tests:

Data test, address test
Data qualified recording test of pod 1
Probe test probe 1

Boards(s) suspected to be defective:

DMB0 - Data Memory Board 0

Suggested correction: DMB0 board replacement

* All four DMBs (DMB0 to DMB3) are identical and therefore interchangeable. The eight pods or probes, which are also interchangeable, are divided among these four boards in the following arrangement:

DMB0 = pods 1 and 2
DMB1 = pods 3 and 4
DMB2 = pods 5 and 6
DMB3 = pods 7 and 8
<table>
<thead>
<tr>
<th>Board Specific RAM</th>
<th>Data-test</th>
<th>Address-Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>TBQ Qualifier RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>TBQ Qualifier RAM</td>
<td>special Address-test</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ Level Address</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ Occurrence CNT</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ Occurrence CNT</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ Status</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>SEQ Trigger filter</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 3 Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 3 Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 2 Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 2 Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 1 Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 1 Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 8 Condition RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
<tr>
<td>OMB 8 Data RAM</td>
<td>error</td>
<td>ok</td>
</tr>
<tr>
<td>TMB Data RAM</td>
<td>ok</td>
<td>ok</td>
</tr>
</tbody>
</table>

test is in hold, type any key to continue
data qualified recording test pod 1  ERROR

Condition 2  ERROR
Condition 3  ERROR

Test is in hold, type any key to continue
Probe-test probe 1
Error on Address : 0004

test is in hold, type any key to continue ■
board(s) suspected to be defective:

OM80 data-memory-board 0

Press RETURN or RUN/STOP to continue.
ADDITIONAL SCHEMATICs

Note: These schematics are duplicates of those found in the Service Manual: Kontron LA, Volume 1 and the Kontron Logic Analyzer Series III Operations manual; they are provided here for easy reference.
14 STÜCK VG-EINH. EINLEITUNG 4-LAGIG

LAG 1 LÄTZEITE
LAG 2
ISOLIERFOLIE
LAG 3
LAG 4 BESTUCKUNGSSEITE

RÜCKVERDRÄHTUNG 4-LAGIG.

KLA MOTHERBOARD
Ax = unbuffered CPU address
BAx = buffered CPU address
MBAx = mapped address from MMU
XAx = buffered ECB address (external address)