FIG. 6-1
V COUNTER
FIG 6-2
V COUNTER DECODER
FIG. 6-3
SUB-BIT TIMING
FIG. 6-4

BIT COUNTER
FIG. 6-5
BIT COUNT DECODER
(SHT. 1 OF 2)
FIG. 6-5
BIT COUNT DECODER

(SHT 2 OF 2)
FIG. 6-6
BIT TIMING
FIG. 6-7
DIGIT COUNTER
FIG. 6-8
DIGIT COUNT DECODER

(SHEET 1 OF 2)
DIGIT COUNT DECODER

Fig. 6-8
Fig. 6-9
Digit Timing
* INPUTS FROM DECIMAL POINT SWITCH. SELECTED POSITION IS AT LOW LEVEL OTHER POSITIONS ARE OPEN CIRCUITED

NOTE:
0 POSITION INPUT OF DECIMAL POINT SWITCH IS NOT CONNECTED

FIG. 6-10
KP LOGIC
FIG. 6-12
$K_{DC}, K'_{DC}$ LOGIC
FIG. 6-13
WORD COUNTER
FIG. 6-14: A COUNTER AND M-COUNTER AC IN, AC IN AND MC IN GATES
FIG. 6-16
M COUNTER
FIG.6-18: C COUNTER INPUT GATES
FIG. 6-20
CYCLE COUNTER
FIG. 6-21: CYCLE COUNT DECODER AND INHIBIT LOGIC
FIG. 6-22: $\Delta B^2$ GENERATOR
FIG. 6-24
OF LOGIC
FIG. 6-25: CLEAR LOGIC
FIG 6-2G
DEMULTIPLEXER LOGIC
FIG. 6-27: R SW LOGIC
FUNCTION CONTROL LOGIC

FIG 6-30
FIG. G-31
"TO-" FROM STORAGE AND CONTROL LOGIC
FIG. 6-32: NC INPUT, "TO" BRIGHTENER, "FROM" BRIGHTENER LOGIC
FIG. 6-33: CHARACTER (N) COUNTER STORAGE (Q) REGISTER, AND DECODER LOGIC
FIG 6-34  OPTICAL CODER