SPIRAS-65 is a General Purpose Stored Program Controller/Processor expandable to 65 K of memory, representing unprecedented PERFORMANCE PER DOLLAR. SPIRAS-65 may be efficiently applied as a Data Processor or Real-Time Controller in either a dedicated and/or satellite environment.

FOR
Industrial/Manufacturing Processes
Numerical Machine Tools
Data Acquisition and Analysis
Automatic Test and Instrumentation
Function Generation
CRT Display Graphics
Generation
Communications Data Concentration and Distribution
Scientific Data Processing
Business Data Processing

ITS CREATOR
To understand the product you should know about its creator, about our fresh overview philosophy and system experience, our unique combination of talent, our total customer-service attitude, and why we designed the SPIRAS-65 to meet your needs.

Among the important commandments in our philosophy are:

- Communicate honestly and directly with the user in his own language without buzz words.
- Offer the total solution to the problem in terms of hardware and software, standard and custom.
- Provide supporting consultation, training, maintenance and a life line of information flow after the sale.

After a broad experience with available "mini-computers", we concluded that we could indeed offer dramatically improved utility, reliability and value. The approach was apparent - Build one machine without major options which includes as standard all of the performance characteristics afforded by the eclectic state of the art and realize the economy derived from large volume "one of a kind" production.
ARCHITECTURE - NVP

The SPIRAS-65 commits to hardware in the IDEAL instruction repertoire to solve the broadest base system problems. The design utilizes NVP “non-volatile program” which is, in essence, a computer controlling a computer. This multigeneration system architecture also allows for customized instruction sets tailored to specific applications. NVP is a 512-word Read-Only-Memory, 32 bits long and expandable to 1024 words.

MAN/MACHINE

The SPIRAS-65 control panel is an I/O device allowing 90% of the main frame to be easily checked out by an operator. All register information is displayed on NIXIE® tubes in octal, decimal, or engineering units under program control. The data entry is via a NORMAL-WAY electronic keyset.

INDUSTRIAL DESIGN

Small LOW INERTIA circuit boards are used to reduce susceptibility to shock and vibration and minimize cost of spares.

EVALUATION

A Measurement of Computer Power - can only be made on a per application basis in terms of STORAGE/TIME/DOLLAR economy by evaluating the:

Instruction Set —
Index & Addressing Modes —
Input/Output Modes —
Software — Reliability —
Human Interface — Training —
Maintenance — Systems Support —

The specifications listed are STANDARD.

SPECIFICATIONS

GENERAL

16 Bit Parallel Binary
Two’s Complement Arithmetic
Four Hardware Registers For Programmers Use
A Accumulator
B Extended Accumulator
X Index
P Program Counter

HARDWARE FUNCTIONS

Bootstrap Loader
Add/Subtract 3.6 μsec
Multiply 17. μsec
Divide 30. μsec
Normalize
Double Precision Add 9.0 μsec
Double Precision Subtract 10.8 μsec
Floating Point Add, Subtract, Multiply, Divide
Priority Interrupt
Block Transfer Cycle Stealing I/O
Extended Conditional Instructions

ADDRESSING MODES

Indexing with A and X Registers
Direct Addressing to
Relative Addressing with P Register
Multi-level Indirect Addressing up to
Immediate Operations

MEMORY

4096 to 65,536 words of Ferrite Core
Cycle Time 1.8 μsec

INPUT/OUTPUT CHARACTERISTICS

UP TO 64 DEVICE CHANNELS
16 BIT TRANSFER
PARTY LINE - Parallel or buffered parallel
DIRECT MEMORY CHANNEL
(Block Transfer)
DIRECT MEMORY ACCESS

CONTROL/INDICATOR PANEL

(REMOTABLE I/O DEVICE)

DISPLAY (NIXIE) - Four Registers,
Instruction Words
Memory, Memory Address (in Octal,
Decimal or under Program Control)
CONSOLE STATUS INDICATOR
DATA ENTRY - Octal Keystop
PROGRAM SENSE - 4 Push Buttons
MODE SWITCHES - Variable Speed

CONSTRUCTION

MAIN FRAME COMPLEMENT: CPU
with 21 IC/MSI
GLASS EPOXY BOARDS: Up to 8K
of core memory, 3 external device
controllers, 10 channel I/O Bus, NVP
Power Supply

LOGIC LEVELS

DTL/TTL - 0 Volts, +5 Volts (0 Volts
+3.5 Volts on I/O Busses)

DIMENSIONS

Rack Mount with Slides 14” H x 19” W
x 23” D
Desk Top - 14” H x 19” W x 25” D

WEIGHT - 100 Pounds
HUMIDITY - 0 to 95% Relative
TEMPERATURE 10°C to 35°C

SOFTWARE

See Price List and “Excellence in Software”

PERIPHERALS

INTERFACES

OPTIONS

See Price List

ADDRESSING

A1

XXX a(D) e = a
XXX a a = (a)
XXX a(X) e = a + (X)
XXX a(Y) e = (a + (X))
XXX a(A) e = a + (A)
XXX a(P) e = a + (P)
XXXI a operand = a

A2

XXX a(D) e = a
XXX a a = (a)
XXX a(X) e = a + (X)
XXX a(Y) e = (a + (X))
XXX a(A) e = a + (A)
XXX a(P) e = a + (P)

A3

XXXS a(D) e = a
XXXS a a = (a)
XXXS a(X) e = a + (X)
XXXS a(Y) e = (a + (X))
XXXS a(A) e = a + (A)
XXXS a(P) e = a + (P)

[b = 0 → 65535]
### SPIRAS-65 INSTRUCTIONS

#### LOAD/STORE

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>TIMING</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDA</td>
<td>(e) → (A)</td>
<td>[3]</td>
</tr>
<tr>
<td>LDAS</td>
<td>a2 (e) → (A)</td>
<td>[2]</td>
</tr>
<tr>
<td>LDB</td>
<td>a1 (e) → (B)</td>
<td>[3]</td>
</tr>
<tr>
<td>LDBS</td>
<td>a2 (e) → (B)</td>
<td>[2]</td>
</tr>
<tr>
<td>LDX</td>
<td>a1 (e) → X</td>
<td>[3]</td>
</tr>
<tr>
<td>LDXS</td>
<td>a2 (e) → X</td>
<td>[2]</td>
</tr>
<tr>
<td>STA</td>
<td>a1 (A) → e</td>
<td>[3]</td>
</tr>
<tr>
<td>STAS</td>
<td>a1 (A) → e</td>
<td>[2]</td>
</tr>
<tr>
<td>STB</td>
<td>a1 (B) → e</td>
<td>[3]</td>
</tr>
<tr>
<td>STBS</td>
<td>a2 (B) → e</td>
<td>[2]</td>
</tr>
<tr>
<td>STX</td>
<td>a1 (X) → e</td>
<td>[3]</td>
</tr>
<tr>
<td>STXS</td>
<td>a2 (X) → e</td>
<td>[2]</td>
</tr>
<tr>
<td>DLD</td>
<td>a1 (e), (e+1) → (A), (B)</td>
<td>[4]</td>
</tr>
<tr>
<td>DST</td>
<td>a1 (A), (B) → (e), (e+1)</td>
<td>[5]</td>
</tr>
<tr>
<td>LEA</td>
<td>a1 e → (X)</td>
<td>[4]</td>
</tr>
</tbody>
</table>

#### JUMP/CALL INSTRUCTIONS

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>TIMING</th>
</tr>
</thead>
<tbody>
<tr>
<td>JMP</td>
<td>a1 (e) → (P)</td>
<td>[3]</td>
</tr>
<tr>
<td>JMP_S</td>
<td>a2 (e) → (P)</td>
<td>[2]</td>
</tr>
<tr>
<td>CALL</td>
<td>a1 *(e+1) + (P) → (P)</td>
<td>[3]</td>
</tr>
<tr>
<td>CALS</td>
<td>a2 *(e+1) + (P) → (P)</td>
<td>[2]</td>
</tr>
</tbody>
</table>

#### LOGICAL/CONTROL

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>TIMING</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND</td>
<td>a1 (e) and (A) → (A)</td>
<td>[3]</td>
</tr>
<tr>
<td>ANDS</td>
<td>a2 (e) and (A) → (A)</td>
<td>[2]</td>
</tr>
<tr>
<td>XOR</td>
<td>a1 (e) or (A) → (A)</td>
<td>[3]</td>
</tr>
<tr>
<td>XORS</td>
<td>a2 (e) or (A) → (A)</td>
<td>[2]</td>
</tr>
<tr>
<td>ORA</td>
<td>a1 (e) or (A) → (A)</td>
<td>[3]</td>
</tr>
<tr>
<td>ORAS</td>
<td>a2 (e) or (A) → (A)</td>
<td>[2]</td>
</tr>
<tr>
<td>HLT</td>
<td></td>
<td>[-]</td>
</tr>
<tr>
<td>NOP</td>
<td></td>
<td>[14]</td>
</tr>
<tr>
<td>OVF</td>
<td>n → OV</td>
<td>[1]</td>
</tr>
<tr>
<td>SPF</td>
<td>1 → Protect Flag</td>
<td>[1]</td>
</tr>
</tbody>
</table>

#### DATA WORD FORMATS

**1-Word instruction**

<table>
<thead>
<tr>
<th>I</th>
<th>M</th>
<th>A</th>
</tr>
</thead>
</table>

**2-Word instruction**

<table>
<thead>
<tr>
<th>C</th>
<th>I</th>
<th>M</th>
</tr>
</thead>
</table>

**Indirect Address**

<table>
<thead>
<tr>
<th>A</th>
</tr>
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</table>

#### JUMP/CALL INSTRUCTIONS

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>TIMING</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASLA</td>
<td>n Arithmetic left shift</td>
<td>[1.2n]</td>
</tr>
<tr>
<td>ASLB</td>
<td>n 0 V →</td>
<td>[0]</td>
</tr>
<tr>
<td>ASRA</td>
<td>n Arithmetic right shift</td>
<td>[1.2n]</td>
</tr>
<tr>
<td>ASRB</td>
<td>n</td>
<td>[0]</td>
</tr>
<tr>
<td>LSLA</td>
<td>n Logical left shift</td>
<td>[1.2n]</td>
</tr>
<tr>
<td>LSLB</td>
<td>n 0 V →</td>
<td>[0]</td>
</tr>
<tr>
<td>LSRA</td>
<td>n Logical right shift</td>
<td>[1.2n]</td>
</tr>
<tr>
<td>LSRB</td>
<td>n 0 →</td>
<td>[0]</td>
</tr>
<tr>
<td>LRLA</td>
<td>n Logical shift rotate</td>
<td>[1.2n]</td>
</tr>
<tr>
<td>LRLB</td>
<td>n</td>
<td>[0]</td>
</tr>
<tr>
<td>ASLD</td>
<td>n 0 V →</td>
<td>[0]</td>
</tr>
<tr>
<td>ASRD</td>
<td>n</td>
<td>[0]</td>
</tr>
<tr>
<td>LSDD</td>
<td>n</td>
<td>[0]</td>
</tr>
<tr>
<td>LSRD</td>
<td>n</td>
<td>[0]</td>
</tr>
<tr>
<td>LSDD</td>
<td>n</td>
<td>[0]</td>
</tr>
<tr>
<td>LRRD</td>
<td>n</td>
<td>[0]</td>
</tr>
</tbody>
</table>

#### REGISTER TRANSFER

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>TIMING</th>
</tr>
</thead>
<tbody>
<tr>
<td>CP</td>
<td>s,d [CPF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>CPI</td>
<td>s,d [CPIF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>CPD</td>
<td>s,d [CPDF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>CPC</td>
<td>s,d [CPCF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>CPN</td>
<td>s,d [CPNF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>CAB</td>
<td>s,d [CABF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>CAX</td>
<td>s,d [CAXF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>CBX</td>
<td>s,d [CBXF] (s) → (d)</td>
<td>[1.4]</td>
</tr>
<tr>
<td>RGC</td>
<td>nnn Operation depends on bits nnn</td>
<td>[1.4]</td>
</tr>
</tbody>
</table>

s = Zero, A, B or X
d = Zero, A, B, X, AX, AB, AXB or ABX

#### OUTPUT

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>TIMING</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXCA</td>
<td>n (A) → device n control</td>
<td>[1]</td>
</tr>
<tr>
<td>EXCB</td>
<td>n (B) → device n control</td>
<td>[1]</td>
</tr>
<tr>
<td>EXCO</td>
<td>n (C) → device n control</td>
<td>[1]</td>
</tr>
<tr>
<td>EXCM</td>
<td>na3 (e) → device n control</td>
<td>[3]</td>
</tr>
<tr>
<td>EXCI</td>
<td>nv → device n control</td>
<td>[2]</td>
</tr>
<tr>
<td>OTA</td>
<td>n (A) → device n data</td>
<td>[1]</td>
</tr>
<tr>
<td>OTB</td>
<td>n (B) → device n data</td>
<td>[1]</td>
</tr>
<tr>
<td>OTX</td>
<td>n (X) → device n data</td>
<td>[1]</td>
</tr>
<tr>
<td>OTM</td>
<td>na3 (e) → device n data</td>
<td>[2]</td>
</tr>
<tr>
<td>OTI</td>
<td>nv → device n data</td>
<td>[3]</td>
</tr>
<tr>
<td>ARM</td>
<td>arm interrupts, 0 → OV</td>
<td>[1]</td>
</tr>
<tr>
<td>DRM</td>
<td>disarm interrupts, 0 → OV</td>
<td>[1]</td>
</tr>
<tr>
<td>ARMF</td>
<td>arm interrupts, 1 → OV</td>
<td>[1]</td>
</tr>
<tr>
<td>DRMF</td>
<td>disarm interrupts, 1 → OV</td>
<td>[1]</td>
</tr>
</tbody>
</table>

#### INPUT

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>TIMING</th>
</tr>
</thead>
<tbody>
<tr>
<td>SENA</td>
<td>n device n status → (A)</td>
<td>[1]</td>
</tr>
<tr>
<td>SENC</td>
<td>n device n status → (B)</td>
<td>[1]</td>
</tr>
<tr>
<td>SENX</td>
<td>n device n status → (X)</td>
<td>[1]</td>
</tr>
<tr>
<td>SENM</td>
<td>na3 device n status → (e)</td>
<td>[3]</td>
</tr>
<tr>
<td>SENS</td>
<td>nm skip if device n status (masked by m)</td>
<td>[2]</td>
</tr>
<tr>
<td>CIA</td>
<td>n device n data → (A)</td>
<td>[1]</td>
</tr>
<tr>
<td>CIB</td>
<td>n device n data → (B)</td>
<td>[1]</td>
</tr>
<tr>
<td>CIX</td>
<td>n device n data → (X)</td>
<td>[1]</td>
</tr>
<tr>
<td>CIM</td>
<td>na3 device n data → (e)</td>
<td>[3]</td>
</tr>
<tr>
<td>INAC</td>
<td>n device n data OR (A) → (A)</td>
<td>[1]</td>
</tr>
<tr>
<td>INB</td>
<td>n device n data OR (B) → (B)</td>
<td>[1]</td>
</tr>
<tr>
<td>INX</td>
<td>n device n data OR (X) → (X)</td>
<td>[1]</td>
</tr>
</tbody>
</table>

**S Single Precision**

**S Most significant data**

**S Least significant data**

**S Fraction**

**S Fraction-2**

**S Exponent**

**S Fraction-1**

**S Fraction-2**

**S Exponent**

**S Fraction-1**

**S Exponent**

**S Fraction-2**

**S Exponent**
excellence in software

We can provide complete systems to the customer because of the extensive software package offered with each SPIRAS-65 unit. In addition to the programs described below, our staff of engineers and programmers can provide applications programs to fit customer requirements.

SYMBOLIC MACRO ASSEMBLER PROGRAM
Free format input.
Macro capability with noise words allowed in the argument list (8K required).
Listing includes octal value generated, relative assignment address, sequential line number, detailed error diagnostics, and a symbol table cross-reference listing (concordance).
Listing control pseudo-ops provided.
Absolute or relocatable object output fully compatible with FORTRAN object output.
System provides capability for sharing literals between sub-programs, and allows page-free addressing (system creates indirect address links automatically if needed).
Operates in as little as 4K of memory (no macros).

FULL ASA FORTRAN-IV COMPILER
Operates in one pass in as little as 8K of memory.
High level of expression, subscript and register optimization.
I/O device independent.
Comprehensive error diagnostic logic.
Symbolic output listing provided with side-by-side octal output data.
Relocatable object output, fully compatible with assembly output.
(continued)
EXCELLENCE IN SOFTWARE

LINKING LOADER PROGRAM
Loads absolute or relocatable programs.
Device independent operation.
Provides memory map.
Manages literal and indirect pointer pool.
Generates indirect addresses, if required.
Searches library tapes, if necessary.

DEBUG PROGRAM
Type memory in octal.
Memory modifications in octal.
Display and modify live registers.
Masked memory search within limits.
Enter break point and start compute.
Makes self loading tapes.

SOURCE PROGRAM EDITOR
Permits modification of source tapes (or disks).
Insertions and deletions by line number.

OBJECT PROGRAM EDITOR
Subroutines can be inserted, deleted or replaced in library tapes (or from disk).

INPUT/OUTPUT LIBRARY
ASCII to/from Binary Conversion
  Fixed point single precision.
  Fixed point double precision.
  Floating point single precision.
  Floating point double precision.
  Integer.
Device Drivers for All I/O Devices
  Open device.
  Read/write data record.
  Close-out device.
  Provide special I/O function.

MATH LIBRARY
Single precision fixed point functions.
Double precision fixed point functions.
Single precision floating point functions.
Double precision floating point functions.
Complex functions.
Complete FORTRAN IV function library.

DIAGNOSTICS
CPU diagnostic.
Memory diagnostic.
Peripheral test programs.

OPERATING SYSTEM
Allows operator assignment of I/O devices.
Controls loading and operating of programs in batch mode.
Operates with basic computer system, a mag-tape system, or with a disk system.

CONVERSATION LANGUAGE*
Includes BASIC as a subset.
Allows macros to be defined and called.
Free-format including noise words and macros allows custom, user-oriented "languages" to be easily generated and used.

360-ASSEMBLER*
Allows assembly of SPIRAS-65 programs on the IBM 360 computer (Model 30 and above).
Available also on most other large computers.
Object output compatible with SPIRAS-65 assembly program object output.

360-SIMULATOR*
Allows simulation of SPIRAS-65 programs on the IBM computer (Model 30 and above).
Detailed trace listings and memory dumps available.
Available also on most other large computers.

*May be purchased. Not included with standard software package.

SPIRAS-65 has a twin called the IRASCOPE which is a DATA BASE EDITING DISPLAY.
Consider it as a peripheral to your SPIRAS-65.

Spiras Systems, Inc.
affiliate of
USM Corporation

332 Second Avenue
Waltham, Massachusetts 02154
617-891-7300  TWX 710-324-6699

USM is a world-wide 400 million dollar designer and manufacturer of systems, aimed at improving the productivity of manufacturing and service industries.

Spiras Systems Inc.,
formerly I.R.A. Systems, Inc.
SPIRAS-65 CONFIGURATOR/PRICE LIST

The purpose of this configurator/price list is to allow Spiras Systems, Inc. sales personnel or customers to accurately define his system configuration and cost. More complex systems which cannot be defined by this document should be referred to the factory for quotation. All final pricing must be confirmed by the factory. These prices do not include OEM or quantity discounts. All pricing is for single-lot quantities. Systems houses wishing to buy peripheral controllers only are urged to request for quotation. All pricing is F.O.B. Whitinsville, Massachusetts.

SPIRAS-65 MAIN FRAME CONFIGURATIONS

There are three basic main frame types, each of which may contain up to 8K, 16-bit words of memory in modulo 4K increments. In addition, the main frame has the optional capability of containing a real-time clock, power fail module, and controllers for teletype, perforated tape equipments, an analog expansion chassis interface, and IRASCOPE CRT display interface.

Each of the main frame types includes the following hardware as standard items:

- Central Processing Unit (CPU)
- Memory — 4096 (16-bit) Words
- Input/Output/DMC Bus — 10 Devices
- Direct Memory Access Bus (DMA)
- Power Supply — With Cooling
- Front Control Panel
- Enclosure

Read-Only Memory — Microprocessor (ROM), Contains:
- Bootstrap Loader
- Add/Subtract
- Multiply
- Divide
- Normalize
- Double Precision Add/Subtract
- Floating Point Add, Subtract, Multiply, Divide
- Priority Interrupt
- Block Transfer Cycle Stealing I/O
- Extensive Conditional Instructions

Each of the main frame types includes the following standard software packages:

- Symbolic Macro Assembler Program (8K Only)
- Basic Assembler Program (4K)
- ASA Fortran IV Compiler (8K Only)
- Linking Loader
- Debug Program
- Source Program Editor
- Object Program Editor
- Input/Output Library
- Math Library
- Diagnostics
- Operating System

Operator training for one man-week is provided in the basic price. A two-week maintenance course for one person is also provided in the basic price. All peripheral prices include driver software. The main frame prices include a one-year warranty.

MAIN FRAME CONFIGURATOR

The configuration for the main frame complement is specified by an eight-part, two-digit number as follows:

SP-65-A-B-C-D-E-F-G-H

where,

- A = Main Frame Type Designator
- B = Main Frame Memory Size Designator
- C = Real-Time Clock Designator
- D = Power Fail Safe Designator
- E = Teletype Designator (Includes Teletype Unit)
- F = Perforated Tape Equipment Designator (Includes Paper Tape Equipment)
- G = CRT IRASCOPE Data Base Editing/Communications Console Designator
- H = Analog Expansion Chassis Interface Designator

The price for each part is as follows:

<table>
<thead>
<tr>
<th>Designator</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = 00</td>
<td>4,400</td>
</tr>
<tr>
<td>A = 01</td>
<td>14,900</td>
</tr>
<tr>
<td>A = 02</td>
<td>15,400</td>
</tr>
<tr>
<td>B = 10</td>
<td>4,800</td>
</tr>
<tr>
<td>B = 11</td>
<td>4,800</td>
</tr>
<tr>
<td>B = 12</td>
<td>4,800</td>
</tr>
<tr>
<td>C = 21</td>
<td>900</td>
</tr>
<tr>
<td>C = 22</td>
<td>1,025</td>
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<tr>
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<td>E = 42</td>
<td>3,100</td>
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<td>E = 43</td>
<td>3,100</td>
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<tr>
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<td>F = 51</td>
<td>3,500</td>
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<tr>
<td>F = 52</td>
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<tr>
<td>F = 53</td>
<td>3,950</td>
</tr>
<tr>
<td>F = 54</td>
<td>6,950</td>
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<tr>
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<tr>
<td>F = 56</td>
<td>4,900</td>
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<td>G = 60</td>
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<tr>
<td>G = 61</td>
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<tr>
<td>G = 62</td>
<td>6,525</td>
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<tr>
<td>G = 63</td>
<td>6,700</td>
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<tr>
<td>H = 70</td>
<td>—</td>
</tr>
<tr>
<td>H = 71</td>
<td>—</td>
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</tbody>
</table>

EXAMPLE: A rack mount main frame with 8K memory, an ASR-33, a reader with reeling, and a parallel-interfaced IRASCOPE would be denoted as follows:

SP-65-00-11-20-30-41-51-63-70
MEMORY EXPANSION CHASSIS WITH POWER SUPPLY

If the system requires more memory than 8K words, a memory expansion chassis would be required. Each memory expansion chassis has an 8K memory capacity and occupies 8.75 inches of rack space.

Price
SP-65-101 Expansion Chassis with 4K Memory $ 6,800
SP-65-102 Expansion Chassis with 8K Memory $11,600

PERIPHERAL CONTROLLER EXPANSION CHASSIS WITH POWER SUPPLY

The peripheral controller expansion chassis with power supply has a 30-card capacity. The number of card slots required for a given controller is indicated in parenthesis. In ordering peripherals, simply add the number of cards per controller to obtain the number of expansion chassis required for the entire system. This unit occupies 5.25 inches of rack space.

Card Price
SP-65-150 Peripheral Expansion Chassis $ 910
SP-65-151 I/O Bus Repeater – 10 Devices (3) $ 1,000
(An I/O bus repeater is required for every 10 device controllers, including those contained in the main frame.)

Magnetic Tape Units (In Cabinet)

All units contain controllers and read/write electronic. All units are 9-track, 556 or 800 BPI, and are IBM compatible. Seven-track or 200 BPI units are available on special factory quote.

Card Price
SP-65-200 24 ips (10) $12,900
SP-65-201 45 ips (10) $22,000
SP-65-202 75 ips (10) $24,500
SP-65-203 DMA Device Controller for 200, 201, 202, Add $ 2,500

Magnetic Tape Cassettes

Magnetic tape cassettes provide 180,000, 8-bit characters, 800 characters per second read/write, 75 millisecond start/stop time. Prices include controllers. All units are rack mountable.

Card Price
SP-65-205 Single Cassette (6) $ 1,995
SP-65-206 Dual Cassette (6) $ 2,950
SP-65-207 Triple Cassette (6) $ 3,900

Line Printer

Card Price
SP-65-210 132-column, 450 alpha-numeric lines per minute (self contained controller) $22,500
SP-65-211 132-column (25 characters/second), 11 alpha-numeric lines/minute for 132-column $ 5,995

Card Systems (In Cabinet)

Card Price
SP-65-220 Reader (300 Cards/Minute) (10) $ 3,950

Disc Packs (In Cabinet)

The Removable Disc Pack is IBM compatible, having 640,000 16-bit words per disc. The average head access time is 60 milliseconds, and the average latency time is 20 milliseconds. The combination disc pack and disc has 640,000 words of pack removable storage and 640,000 words of permanent disc storage with identical access times.

Card Price
SP-65-230 640K Words (6) $20,900
SP-65-231 1.28 million words, 640K of which is on fixed disc (6) $23,500
SP-65-232 Dual, with 1.28 million words (6) $32,133
SP-65-233 Dual, with 2.56 million words, 1.28 million of which is on fixed disc (6) $37,450
SP-65-234 DMA Device Controller for 230, 231, 232, 233, Add (6) $ 2,500

Disc Files

The fixed head disc files have 8 records per track, each record having 256 words. The access time is 16.7 milliseconds, and the data rate is 75 KC.

<table>
<thead>
<tr>
<th>Card</th>
<th>Slots</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP-65-240</td>
<td>8K Words</td>
<td>(5) $ 6,295</td>
</tr>
<tr>
<td>SP-65-241</td>
<td>16K Words</td>
<td>(5) $ 7,182</td>
</tr>
<tr>
<td>SP-65-242</td>
<td>32K Words</td>
<td>(5) $ 8,500</td>
</tr>
<tr>
<td>SP-65-243</td>
<td>64K Words</td>
<td>(5) $ 9,810</td>
</tr>
<tr>
<td>SP-65-244</td>
<td>DMA Device Controller for 240 through 244, Add</td>
<td>(5) $ 2,500</td>
</tr>
</tbody>
</table>

Digital Plotters

Card Price
SP-65-250 300 Steps/Second (4) $ 8,500

Modem Interfaces

Card Price
SP-65-300 Half Duplex Asynchronous, Up to 1800 Baud (4) $ 1,250
SP-65-301 Full Duplex Asynchronous, Up to 1800 Baud (5) $ 1,500

General-Purpose Modules Interfaced

Card Price
SP-65-400 8-Bit Register with Latch (1) $ 224
SP-65-401 8-Bit Register without Latch (1) $ 169
SP-65-402 I/O Control with Interrupt & Trap (1) $ 230
SP-65-403 16-Bit Sense Status Module (3) $ 600
SP-65-404 Universal Interceptor Interface (3) $ 1,000

General-Purpose Programmable Factory Instrument Module, Interfaces to Digital Quote Instrumentation

ANALOG EXPANSION CHASSIS WITH POWER SUPPLY

The analog expansion chassis has 16-card capacity. The number of card slots required for a given analog device are indicated in parenthesis. In ordering analog devices, add the number of cards per device to determine how many analog expansion chassis are needed for the system. This unit occupies 7 inches of rack space.

Card Price
SP-65-500 Analog Expansion Chassis with Power Supply $ 1,300

Analog-to-Digital Converters

Card Price
SP-65-501 12-Bit, including sign, 0-10 volt, 12 bit word conversion (2) $ 1,500

Digital-to-Analog Converters

Card Price
SP-65-510 9-Bit with Sign (3) $ 1,550
SP-65-511 12-Bit with Sign (3) $ 1,600
SP-65-512 15-Bit with Sign (3) $ 1,650
SP-65-513 Dual 9-Bit with Sign (3) $ 1,950
SP-65-514 Dual 12-Bit with Sign (3) $ 2,060
SP-65-515 Dual 15-Bit with Sign (3) $ 2,150

Amplifiers

Card Price
SP-65-520 Differential (1) $ 400
SP-65-521 Sample and Hold (1) $ 450

Multiplexers

Card Price
SP-65-525 High level 16-channel one-wire, or 8-channel two-wire (2) $ 1,300

SP-65-526 Additional 16-channel one-wire, or 8-channel two-wire module – up to 7 $ 500 ea.

SP-65-527 Special Multiplexer Configurations Factory Quote
<table>
<thead>
<tr>
<th>Accessories</th>
<th>Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>SP-65-600 System Cabinet with AC Service (70” x 25” x 30”)</td>
<td>$750.00</td>
</tr>
<tr>
<td>SP-65-601 Dual System Cabinet with AC Service (70” x 50” x 30”)</td>
<td>$1,300.00</td>
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<tr>
<td>SP-65-602 Maintenance Test Set with Readout on all Registers</td>
<td>$2,500.00</td>
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<tr>
<td>SP-65-603 Motor Generator/Line Isolator, .5 KVA</td>
<td>$1,475.00</td>
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<tr>
<td>SP-65-604 Motor Generator/Line Isolator, 1 KVA</td>
<td>$1,798.00</td>
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<tr>
<td>SP-65-606 Spare Card Parts Kit</td>
<td>$3,995.00</td>
</tr>
<tr>
<td>SP-65-607 Special Paint (two-tone)</td>
<td>$195.00</td>
</tr>
<tr>
<td>SP-65-608 Desk Enclosure Unit</td>
<td>$300.00</td>
</tr>
<tr>
<td>SP-65-609 Instruction Manuals (Additional)</td>
<td>$3.00</td>
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<table>
<thead>
<tr>
<th>Software</th>
<th></th>
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<tbody>
<tr>
<td>SP-65-700 IBM 360 Assembler</td>
<td>$2,500.00</td>
</tr>
<tr>
<td>SP-65-701 IBM 360 Assembler &amp; Simulator</td>
<td>$3,500.00</td>
</tr>
<tr>
<td>SP-65-702 Autoscan/Log</td>
<td>Factory Quote</td>
</tr>
<tr>
<td>SP-65-703 Control Output</td>
<td>Factory Quote</td>
</tr>
<tr>
<td>SP-65-704 Gas Chromatograph Control</td>
<td>Factory Quote</td>
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<tr>
<td>SP-65-705 Nonlinear Optimizer</td>
<td>Factory Quote</td>
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<tr>
<td>SP-65-706 Data Acquisition</td>
<td>Factory Quote</td>
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<tr>
<td>SP-65-707 Custom Application Packages</td>
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</table>

<table>
<thead>
<tr>
<th>Other Support Services</th>
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<tbody>
<tr>
<td>SP-65-800 Installation (two man-days and expenses)</td>
<td>$500.00</td>
</tr>
<tr>
<td>SP-65-801 Additional Operator Training (For Programmers) — Per Man</td>
<td>$300.00</td>
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<tr>
<td>SP-65-802 Additional Two-Week Maintenance Training (For Technicians)</td>
<td>$600.00</td>
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<tr>
<td>SP-65-803 Systems Analysis Consulting</td>
<td>Factory Quote</td>
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<tr>
<td>SP-65-804 Maintenance Contracts</td>
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<tr>
<td>SP-65-805 Special Computer-Centered Systems</td>
<td>Factory Quote</td>
</tr>
</tbody>
</table>

NOTES:
1. All prices are subject to change without notice.
2. This price list supercedes all prior price lists.
3. Leasing is available upon request.

Spiras Systems, Inc.
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USM is a world-wide 400 million dollar
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and service industries.

Spiras Systems Inc.,
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