SCD–DLV11J/8P
8–Channel Programmable Interface
Manual
SCD-DLV11J/8P

8-Channel Programmable Interface

Manual

CORRECTIONS

<table>
<thead>
<tr>
<th>NAME</th>
<th>DATE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gary</td>
<td>26-Feb-87</td>
<td>4</td>
</tr>
<tr>
<td>Gary</td>
<td>4-Jan-91</td>
<td>9</td>
</tr>
</tbody>
</table>

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Contents

SECTION 1 - GENERAL INFORMATION

1.1 INTRODUCTION ........................................... 1
1.2 GENERAL DESCRIPTION .................................... 2
1.3 FEATURES .................................................. 2
1.4 SPECIFICATIONS .......................................... 3

SECTION 2 - INSTALLATION

2.1 UNPACKING AND INSPECTION .............................. 5
2.3 ADDRESS SELECTION ....................................... 7
2.4 VECTOR SWITCH SELECTION ............................... 8
2.5 BAUD RATE SELECTION .................................... 9
2.6 LINE PARAMETERS SWITCH SELECTION ................... 10
2.7 CONSOLE SELECTION ...................................... 10
2.8 BREAK RESPONSE ......................................... 11
2.10 CABLING .................................................. 11
2.11 MODULE INSTALLATION .................................. 12
2.12 RACKMOUNT PANEL (OPTION) ........................... 13

SECTION 3 - PROGRAMMING CONSIDERATIONS

3.1 INTRODUCTION ............................................. 15
3.2 DEVICE ADDRESS FORMAT ................................ 17
3.3 VECTOR INTERRUPT FORMAT .............................. 18
3.4 WORD FORMATS ........................................... 19
  3.4.1 Receive Control/Status Register (RCSR) ............ 19
  3.4.2 Receiver Buffer (RBUF) ............................. 20
  3.4.3 Transmit Control/Status Register (XCSR) .......... 21
  3.4.4 Transmit Buffer (XBUF) ............................. 21

APPENDIX A Q BUS PIN ASSIGNMENTS ........................ A-1
APPENDIX B ADDRESS AND VECTOR SWITCH SETTINGS .......... B-1
# Examples/Figures/Tables

<table>
<thead>
<tr>
<th>Example/Table/Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXAMPLE 2-1</td>
<td>ADDRESS SELECTION</td>
<td>7</td>
</tr>
<tr>
<td>EXAMPLE 2-2</td>
<td>VECTOR INTERRUPT SELECTION</td>
<td>8</td>
</tr>
<tr>
<td>FIGURE 2-1</td>
<td>FACTORY CONFIGURATIONS</td>
<td>6</td>
</tr>
<tr>
<td>FIGURE 2-2</td>
<td>RACKMOUNT CONNECTOR PANEL</td>
<td>13</td>
</tr>
<tr>
<td>TABLE 2-1</td>
<td>FACTORY-SET PARAMETERS</td>
<td>6</td>
</tr>
<tr>
<td>TABLE 2-2</td>
<td>BAUD RATE SELECTION</td>
<td>9</td>
</tr>
<tr>
<td>TABLE 2-3</td>
<td>LINE PARAMETERS SWITCH SELECTION</td>
<td>10</td>
</tr>
<tr>
<td>TABLE 2-4</td>
<td>CONSOLE ENABLE</td>
<td>10</td>
</tr>
<tr>
<td>TABLE 2-5</td>
<td>BREAK CONFIGURATIONS</td>
<td>11</td>
</tr>
<tr>
<td>TABLE 2-6</td>
<td>CTS BIAS CONFIGURATION</td>
<td>11</td>
</tr>
<tr>
<td>TABLE 2-7</td>
<td>CABLE PIN ASSIGNMENTS</td>
<td>12</td>
</tr>
<tr>
<td>TABLE 3-1</td>
<td>STANDARD ADDRESS AND VECTOR ASSIGNMENTS</td>
<td>16</td>
</tr>
</tbody>
</table>
Section 1 - General Information

1.1 INTRODUCTION

This manual supplies the information needed to install and operate the SCD-DLV11J/8P 8-channel serial line interface module manufactured by Sigma Information Systems, Anaheim, California. The material is arranged into the following sections:

SECTION 1 - GENERAL INFORMATION. This section contains a general description of the interface module, along with features. Specifications are included.

SECTION 2 - INSTALLATION. This section contains the switch selection and associated register formats for device and vector address assignments, baud rates and line parameters. Cabling and backplane installation is included.

SECTION 3 - PROGRAMMING CONSIDERATIONS. This section contains the address/vector formats and register formats for transmit and receive control/status and buffer registers.

APPENDIX A - The appendix lists the bus signals and their associated pin assignments.

APPENDIX B - This appendix contains a complete list of address and vector switch settings for address/vector assignments.
1.2 GENERAL DESCRIPTION

The SCD-DLV11J/8P is a dual-wide asynchronous interface between the LSI-11 bus and up to eight standard serial I/O devices. It is software compatible with DEC* operating systems and diagnostics designed for the DLV11J. It plugs directly into any dual Q bus* slot.

Sigma's SCD-DLV11J/8P has switch selectable address (160000 to 177776) and vector (000 to 776) assignments. Once the initial address and vector are assigned, all eight channels are contiguous except the console channel which, if selected, resides at 177560 with vector at 60.

All channels share a programmable baud rate with a switch selectable default value. Baud rates range from 50 to 19.2K baud. The SCD-DLV11J/8P supports only RS-232C devices with all channels sharing switch selectable line parameters.

The interface module requires two 12-foot, 4-channel cables, each terminating with four DB25P connectors. An optional rackmount panel provides convenient mounting for the eight DB25P connectors.

1.3 FEATURES

The following are some of the features of the SCD-DLV11J/8P.

- Eight asynchronous serial lines can be supported on one dual-wide module.
- The module is plug compatible with LSI-11 backplanes and plugs directly into any Q bus slot without backplane modification.
- The interface is software compatible with operating systems and diagnostics designed for the DLV11J.
- Baud rate is programmable with a switch selectable default value.
- Device address and vector assignments are switch selectable.
- Line parameters are switch selectable.

*DEC and Q bus are registered trademarks of Digital Equipment Corporation.
1.4 SPECIFICATIONS

Power Requirements: +5VDC AT 2.0A
+12VDC at 0.2A

Device Address: Switch selectable 160000-177776 (Console = 177560)

Vector: Switch selectable 000-776 (console = 60)

Baud Rate: Programmable per channel: 50, 75, 110, 134.5, 150,
200, 300, 600, 1200, 1800, 3400, 3600, 4800, 7200,
9600 and 19.2K

Line Parameters: Switch selectable. Shared by all channels
Data Bit: 7 or 8
Parity: Odd, even or none
Stop Bit: 1 or 2

Operation: Full duplex

Interface Type: RS-232C

Bus Load: One DC load

Optional Cables: Requires two 12-ft, 4-channel cables, each terminated
with four DB25P connectors. Terminals require null modem cable with DB25S to SCD-DLV11J/8P's terminated connectors.

Optional Panel: Mounts the eight DB25P connectors for convenient
rear rackmount cabling to RS-232C devices.

Installation: Plugs directly into any standard Q bus slot that provides continuous BIAK1 and BIAKO lines.

Dimensions: Single dual-wide module: 5.2"W x 8.9"H (13.2cmW x 22.8cmH)

Temperature
Operating: 0°C to 50°C
Storage: -40°C to 85°C

Humidity: 10% to 90% noncondensing
Section 2 - Installation

2.1 UNPACKING AND INSPECTION

The SCD-DLV11J/8P is shipped in a special packing carton designed to keep the module from vibrating and to give it maximum protection during shipment. The packing carton should be retained in case the unit requires reshipment.

Unpack the SCD-DLV11J/8P and visually inspect it for any damage that may have occurred during shipment. If any damage has occurred notify Sigma Information Systems immediately.

2.2 FACTORY-SET PARAMETERS

The SCD-DLV11J/8P is shipped configured with DEC standard operating parameters as defined in Table 2-1. The location of the switches that determine these parameters is shown in Figure 2-1.

Before installing modules, verify that these configurations are properly selected. The following sections describe the procedures to verify and/or reconfigure these operating parameters.
TABLE 2-1: FACTORY-SET PARAMETERS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Address</td>
<td>176500</td>
</tr>
<tr>
<td>Vector Interrupt</td>
<td>300</td>
</tr>
<tr>
<td>Baud Rate</td>
<td>9600</td>
</tr>
<tr>
<td>Console</td>
<td></td>
</tr>
<tr>
<td>Channel 7</td>
<td>Enabled</td>
</tr>
<tr>
<td>Address</td>
<td>177560</td>
</tr>
<tr>
<td>Word Format</td>
<td></td>
</tr>
<tr>
<td>Character Length</td>
<td>8 bits</td>
</tr>
<tr>
<td>Parity</td>
<td>Disabled</td>
</tr>
<tr>
<td>Stop Bits</td>
<td>1</td>
</tr>
<tr>
<td>CTS Bias</td>
<td>+12V</td>
</tr>
</tbody>
</table>

FIGURE 2-1: FACTORY CONFIGURATIONS
2.3 ADDRESS SELECTION

The SCD-DLV11J/8P has switch selectable device addressing in the range of 160000 to 177776 (octal). Once an initial address is assigned, the remaining seven channels are contiguous except the console which, if selected, resides at 177560 as channel 7. Refer to Section 3.1 for a description of the device address and vector interrupt assignments. The initial address format is shown below.

```
17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

Use the following examples to set SW3. Notice that OFF = 1 and ON = 0.

<table>
<thead>
<tr>
<th>Set default standard address 176500.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDRESS BITS:</td>
</tr>
<tr>
<td>SW3 POSITIONS:</td>
</tr>
<tr>
<td>SW3 SETTINGS:</td>
</tr>
<tr>
<td>SW3 VALUE:</td>
</tr>
<tr>
<td>ADDRESS:</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Set address 176400.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDRESS BITS:</td>
</tr>
<tr>
<td>SW3 POSITIONS:</td>
</tr>
<tr>
<td>SW3 SETTINGS:</td>
</tr>
<tr>
<td>SW3 VALUES:</td>
</tr>
<tr>
<td>ADDRESS:</td>
</tr>
</tbody>
</table>

EXAMPLE 2-1: ADDRESS SELECTION

A complete list of address switch settings is shown in Appendix B.
2.4 VECTOR SWITCH SELECTION

The SCD-DLV11d/8P has switch selectable vector assignments in the range of 000-776 (octal). Once the initial vector is assigned the remaining seven vectors are contiguous except the console which, if assigned, resides at 60 as channel 7. The initial vector format is shown below.

Use the following examples to set SW1. Notice that OFF = 1 and ON = 0.

<table>
<thead>
<tr>
<th>Set standard default vector 300.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VECTOR BITS:</td>
</tr>
<tr>
<td>V8  V7  V6</td>
</tr>
<tr>
<td>SW1 POSITIONS:</td>
</tr>
<tr>
<td>4  3  2</td>
</tr>
<tr>
<td>SW1 SETTINGS:</td>
</tr>
<tr>
<td>ON  OFF  OFF</td>
</tr>
<tr>
<td>SW1 VALUES:</td>
</tr>
<tr>
<td>0  1  1</td>
</tr>
<tr>
<td>VECTOR INTERRUPT:</td>
</tr>
<tr>
<td>3  0  0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Set vector 200.</th>
</tr>
</thead>
<tbody>
<tr>
<td>VECTOR BITS:</td>
</tr>
<tr>
<td>V8  V7  V6</td>
</tr>
<tr>
<td>SW1 POSITIONS:</td>
</tr>
<tr>
<td>4  3  2</td>
</tr>
<tr>
<td>SW1 SETTINGS:</td>
</tr>
<tr>
<td>ON  OFF  ON</td>
</tr>
<tr>
<td>SW1 VALUES:</td>
</tr>
<tr>
<td>0  1  0</td>
</tr>
<tr>
<td>VECTOR INTERRUPT:</td>
</tr>
<tr>
<td>2  0  0</td>
</tr>
</tbody>
</table>

EXAMPLE 2-2: VECTOR INTERRUPT SELECTION

A complete list of vector interrupt switch settings is shown in Appendix B.
2.5 **BAUD RATE SELECTION**

All channels share the same programmable baud rate. The baud rate format is shown below.

```
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
BR3 BR2 BR1 BRO
```

where BRO-BR3 define programmable baud rates and SW2 defines switch selectable baud rates as shown in Table 2-2.

<table>
<thead>
<tr>
<th>BAUD RATE</th>
<th>XCSR BITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>15</td>
</tr>
<tr>
<td>50</td>
<td>ON</td>
</tr>
<tr>
<td>75</td>
<td>ON</td>
</tr>
<tr>
<td>110</td>
<td>ON</td>
</tr>
<tr>
<td>134.5</td>
<td>ON</td>
</tr>
<tr>
<td>150</td>
<td>ON</td>
</tr>
<tr>
<td>200</td>
<td>ON</td>
</tr>
<tr>
<td>300</td>
<td>ON</td>
</tr>
<tr>
<td>600</td>
<td>ON</td>
</tr>
<tr>
<td>1200</td>
<td>OFF</td>
</tr>
<tr>
<td>1800</td>
<td>OFF</td>
</tr>
<tr>
<td>2400</td>
<td>OFF</td>
</tr>
<tr>
<td>3600</td>
<td>OFF</td>
</tr>
<tr>
<td>4800</td>
<td>OFF</td>
</tr>
<tr>
<td>7200</td>
<td>OFF</td>
</tr>
<tr>
<td>9600*</td>
<td>OFF</td>
</tr>
<tr>
<td>19.2K</td>
<td>OFF</td>
</tr>
</tbody>
</table>

*Factory preset

**Table 2-2: Baud Rate Selection**

If programmable baud rate is enabled (XCSR bit 11 is set), the XCSR bits 15-12 override SW2 baud rate selection. See Section 3.4.3 for programmable baud rate selection.
2.6 **LINE PARAMETERS SWITCH SELECTION**

All eight channels share the same line parameters. The start bit is 1, but data bit, parity and stop bits can be assigned via switch SW2 as shown in Table 2-3.

<table>
<thead>
<tr>
<th>LINE PARAMETER</th>
<th>SW2 POSITION</th>
<th>DEFINITION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Character Length</td>
<td>4</td>
<td>ON = 7 bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>*OFF = 8 bits</td>
</tr>
<tr>
<td>Parity Enable</td>
<td>3</td>
<td>*ON = disable parity</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF = enable parity</td>
</tr>
<tr>
<td>Parity Type</td>
<td>2</td>
<td>ON = odd parity</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF = even parity</td>
</tr>
<tr>
<td>Stop bits</td>
<td>1</td>
<td>*ON = 1 stop bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OFF = 2 stop bits</td>
</tr>
</tbody>
</table>

*Factory preset

**TABLE 2-3: LINE PARAMETERS SWITCH SELECTION**

2.7 **CONSOLE SELECTION**

The console, if selected, is assigned channel 7. The SCD-DLV11J/8P is shipped with the console enabled. To disable the console set switch SW3-5 as shown in Table 2-4.

<table>
<thead>
<tr>
<th>CONSOLE STATUS</th>
<th>SW3-5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled</td>
<td>ON</td>
</tr>
<tr>
<td>Enabled</td>
<td>*OFF</td>
</tr>
</tbody>
</table>

*Factory preset

**TABLE 2-4: CONSOLE ENABLE**
2.8 **BREAK RESPONSE**

Channel 7 can be configured to either bootstrap, halt (console emulation mode), or have no response to a receive break condition. A bootstrap operation upon a receive break condition causes the CPU to execute the bootstrap program starting at the memory location defined by the power-up mode jumpers of the CPU. A halt operation upon a receive break condition causes the processor to halt and the console octal debugging technique (ODT) microcode to be invoked. Configurations are shown in Table 2-5.

<table>
<thead>
<tr>
<th>BREAK RESPONSE</th>
<th>E1-E2</th>
<th>E1-E3</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>None</em></td>
<td>OUT</td>
<td>OUT</td>
</tr>
<tr>
<td>Boot</td>
<td>IN</td>
<td>OUT</td>
</tr>
<tr>
<td>Halt</td>
<td>OUT</td>
<td>IN</td>
</tr>
</tbody>
</table>

*Factory Preset

**TABLE 2-5: BREAK CONFIGURATIONS**

2.9 **CTS BIAS**

The Clear To Send (CTS) signal bias is factory configured for +12V. The CTS bias can be reconfigured for -12V; however, it is recommended that the factory configuration remain unchanged. CTS configurations are shown in Table 2-6.

<table>
<thead>
<tr>
<th>CTS BIAS</th>
<th>E4-E5</th>
<th>E5-E6</th>
</tr>
</thead>
<tbody>
<tr>
<td><em>+12V</em></td>
<td>OUT</td>
<td>IN</td>
</tr>
<tr>
<td>-12V</td>
<td>IN</td>
<td>OUT</td>
</tr>
</tbody>
</table>

*Factory Preset

**TABLE 2-6: CTS BIAS CONFIGURATION**

2.10 **CABLING**

The SCD-DLV11J/8P has two optional 40-pin connectors, each terminating in four DB25P connectors. The 40-pin connectors and associated 25-pin terminating connector pin assignments are defined in Table 2-7.
<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>DESCRIPTION</th>
<th>25-PIN DB25P</th>
<th>40-PIN CONNECTOR ---LINE NUMBER---</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit Data</td>
<td>Data transmitted from SCD-DLV11J/8P to terminal</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>33</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>23</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>13</td>
<td>3</td>
</tr>
<tr>
<td>Receive Data</td>
<td>Data received by SCD-DLV11J/8P from terminal</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>38</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>28</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8</td>
<td>J1</td>
</tr>
<tr>
<td>Clear to Send</td>
<td>Signal sent by device to SCD-DLV11J/8P to indicate readiness for transmitted</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>data</td>
<td>34</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>24</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>J2</td>
</tr>
<tr>
<td>Ground</td>
<td>Signal Ground*</td>
<td>7</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>39</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12</td>
<td>7</td>
</tr>
<tr>
<td>Ground</td>
<td>Protective Ground*</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>22</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>J1</td>
</tr>
</tbody>
</table>

*Signal and Protective Grounds are connected.

**TABLE 2-7: CABLE PIN ASSIGNMENTS**

The SCD-DLV11J/8P provides a Clear to Send input which can be driven by the attached serial line device to cause the SCD-DLV11J/8P channel to stop transmitting. The common use for this feature is with a printer that does not support XON-XOFF, but does provide a buffer full signal. This buffer status signal can be used to assert the CTS signal and effectively control transmission of data to the printer from the SCD-DLV11J/8P.

Cabling to terminals requires null modem cables with DB25S sockets between the SCD-DLV11J/8P connectors and associated terminal connectors.

2.11 MODULE INSTALLATION

The SCD-DLV11J/8P plugs directly into any Q bus slot, providing BIAK1 and BIAK0 lines from the interface to the CPU are continuous. Bus signals and associated pin assignments are listed in Appendix A.
2.12 RACKMOUNT PANEL (OPTION)

An optional rackmount panel provides convenient mounting for the eight DB25P connectors. The panel accepts connectors from two 8-channel devices. The panel is illustrated in Figure 2-2.

FIGURE 2-2: RACKMOUNT CONNECTOR PANEL
Section 3 - Programming

3.1 INTRODUCTION

The SCD-DLVIIJ/8P is controlled by four device registers per channel for a total of 32 device registers. The four device registers provided for each of the eight channels are:

- RCSR  Receive Control/Status Registers
- RBUF  Receive Buffer
- XCSR  Transmit Control/Status Register
- XBUF  Transmit Buffer

With the exception of the console channel, the device registers are assigned in a contiguous block by setting the address of channel 0. If the SCD-DLVIIJ/8P is used as the console device, channel 7 is assigned the console address and vector. If the SCD-DLVIIJ/8P is not used as the console, channel 7 is assigned as the last contiguous address set. Table 3-1 illustrates an initial address and vector assignment with contiguous locations.
<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>REGISTER</th>
<th>VECTOR</th>
<th>CHANNEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>176500</td>
<td>RCSR</td>
<td>300</td>
<td>0</td>
</tr>
<tr>
<td>176502</td>
<td>RBUF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>176504</td>
<td>XCSR</td>
<td>304</td>
<td>0</td>
</tr>
<tr>
<td>176506</td>
<td>XBUF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>176510</td>
<td>RCSR</td>
<td>310</td>
<td>1</td>
</tr>
<tr>
<td>176512</td>
<td>RBUF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>176514</td>
<td>XCSR</td>
<td>314</td>
<td>1</td>
</tr>
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<tr>
<td>176560</td>
<td>RCSR</td>
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<td>6</td>
</tr>
<tr>
<td>176562</td>
<td>RBUF</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>XCSR</td>
<td>364</td>
<td>6</td>
</tr>
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<td></td>
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<td>RCSR</td>
<td>370</td>
<td>7</td>
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<td>RBUF</td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

*If the console is selected it resides at channel 7, and the last four addresses in this table are:

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>REGISTER</th>
<th>VECTOR</th>
<th>CHANNEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>177560</td>
<td>RCSR</td>
<td>60</td>
<td>7</td>
</tr>
<tr>
<td>177562</td>
<td>RBUF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>177564</td>
<td>XCSR</td>
<td>64</td>
<td>7</td>
</tr>
<tr>
<td>177566</td>
<td>XBUF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 3-1: STANDARD ADDRESS AND VECTOR ASSIGNMENTS**
3.2 DEVICE ADDRESS FORMAT

The address format is shown below.

```
  17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
  1  1  1  1  1 A12 A11 A10 A9  A8  A7  A6
```

Bank 7

Selected (1)

Initial Address

(See Section 2.3)

Channel (Device) Select

<table>
<thead>
<tr>
<th>Bit</th>
<th>Channel Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>5  4 3</td>
<td>CH 0</td>
</tr>
<tr>
<td>0  0  0</td>
<td>CH 1</td>
</tr>
<tr>
<td>0  0  1</td>
<td>CH 2</td>
</tr>
<tr>
<td>0  1  0</td>
<td>CH 3</td>
</tr>
<tr>
<td>0  1  1</td>
<td>CH 4</td>
</tr>
<tr>
<td>1  0  0</td>
<td>CH 5</td>
</tr>
<tr>
<td>1  0  1</td>
<td>CH 6</td>
</tr>
<tr>
<td>1  1  0</td>
<td>CH 7</td>
</tr>
</tbody>
</table>

Register Select

<table>
<thead>
<tr>
<th>Bit</th>
<th>Interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>2  1</td>
<td></td>
</tr>
<tr>
<td>0  0</td>
<td>RCSR</td>
</tr>
<tr>
<td>0  1</td>
<td>RBUF</td>
</tr>
<tr>
<td>1  0</td>
<td>XCSR</td>
</tr>
<tr>
<td>1  1</td>
<td>XBUF</td>
</tr>
</tbody>
</table>

Byte Pointer
3.3 VECTOR INTERRUPT FORMAT

The interrupt vector format is shown below.

```
   17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
```

Initial Vector

(See Section 2.4)

Channel Requesting Interrupt

<table>
<thead>
<tr>
<th>Bit</th>
<th>Channel</th>
<th>Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>CH 0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>CH 1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>CH 2</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>CH 3</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>CH 4</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>CH 5</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>CH 6</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>CH 7</td>
</tr>
</tbody>
</table>

Interrupt

<table>
<thead>
<tr>
<th>Bit 2</th>
<th>Interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Receiver Interrupt</td>
</tr>
<tr>
<td>1</td>
<td>Transmitter Interrupt</td>
</tr>
</tbody>
</table>

All bits not used are read as 0.
3.4 WORD FORMATS

The four word formats, one for each device register within a channel, are described in the following sections.

3.4.1 Receive Control/Status Register (RCSR)

RX DN  RECEIVER DONE. Set when an entire character has been received and is ready for input to the CPU. Cleared when RBUF is read or BINIT L signal goes true. If RX INT (bit 6) is set, setting RX DN starts an interrupt sequence. Read only.

RX INT  RECEIVER INTERRUPT ENABLE. Set under program control to generate a receiver interrupt request (when a character is ready for input to the processor signified by bit 7 being set). Cleared under program control or by BINIT signal. Read/write.

All bits not used are read as 0.
3.4.2 Receiver Buffer (RBUF)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

<table>
<thead>
<tr>
<th></th>
<th>CH ERR</th>
<th>OVR ERR</th>
<th>FRM ERR</th>
<th>PAR ERR</th>
<th>DATA BITS</th>
</tr>
</thead>
</table>

CH ERR  CHANNEL ERROR STATUS. Logical OR of bits 14, 13, and 12. Read only.

OVR RUN  OVERRUN ERROR. When set, indicates that the reading of the previously received character was not completed (receiver done not cleared) prior to receiving a new character. Cleared by BINIT signal. Read only.

**NOTE**

When "back-to-back" characters are received, one full character time is allowed from the time instant receiver done (bit 7) is set to the occurrence of an overrun error.

FRM ERR  FRAMING ERROR. When set, indicates that the character read had no valid stop bit. Cleared by BINIT signal. Read only.

PAR ERR  PARITY ERROR. When set, indicates that the parity received does not agree with the expected parity. This bit is always 0 if no-parity operation is configured for the channel. Read only.

**NOTE**

Error bits remain valid until the next character is received, at which time the error bits are updated.

DATA BITS  DATA BITS. Contains seven or eight data bits in a right-justified format. Bit 7 = 0 when 7 data bits are enabled. Read only.

All bits not used are read as 0.
3.4.3 Transmit Control/Status Register (XCSR)

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BR3</td>
<td>BR2</td>
<td>BR1</td>
<td>BRO</td>
<td>BR</td>
<td>ENB</td>
<td>XMT</td>
<td>XMT</td>
<td>XMT</td>
<td>XMT</td>
<td>XMT</td>
<td>XMT</td>
<td>XMT</td>
<td>XMT</td>
<td>XMT</td>
<td></td>
</tr>
</tbody>
</table>

**BR3-BRO**  PROGRAMMABLE BAUD RATE SELECT. When set, these bits choose a baud rate from 50-19.2K baud. BR END must be set for the baud rate to be affective. See section 2.5 to configure baud rate. Write only.

**BR ENB**  PROGRAMMABLE BAUD RATE ENABLE. Must be set in order to select a new baud rate indicated by bits 12-15. Write only.

**XMT RDY**  TRANSMIT READY. Set when XBUF is empty and can accept another character for transmission. It is also set by INIT, during power-up or during a reset instruction. Read only.

**XMT INT**  TRANSMIT INTERRUPT ENABLE. Set under program control when it is desired to generate a transmitter interrupt request when transmitter is ready to accept a character for transmission. Cleared under program control, during power-up or reset instruction. Read/write.

**XMT BRK**  TRANSMIT BREAK. Set or reset under program control. When set, a continuous space level is transmitted. However, transmit done and transmit interrupt can still operate, allowing software timing of break. When not set, normal character transmission can occur. Cleared by BINIT. Read/write.

All bits not used are read as 0.

3.4.4 Transmit Buffer (XBUF)

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DATA BITS</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits 0-7 contain the seven or eight right-justified data bits, which are loaded under program control for serial transmission. Bits not used are read as 0.
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
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<tbody>
<tr>
<td>AA1</td>
<td>BIRDQ5L</td>
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<td></td>
<td>AA2</td>
<td>+5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AB1</td>
<td>BIRDQ6L</td>
<td></td>
<td></td>
<td>AB2</td>
<td>-12V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AC1</td>
<td>BDAL16L</td>
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<td>AD2</td>
<td>+12V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>AE1</td>
<td>*SSI</td>
<td>STOP L</td>
<td>SINGLE STEP</td>
<td>AE2</td>
<td>BDOUTL</td>
<td></td>
<td></td>
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<tr>
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<td>*SRUNL</td>
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<td>AF2</td>
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<td>AP2</td>
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<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
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</tr>
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<td>BPOKH</td>
<td></td>
<td></td>
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<td></td>
</tr>
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<td>BE2</td>
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<td></td>
</tr>
<tr>
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<td>MMUDAL21H</td>
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</tr>
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</tr>
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<td></td>
<td>BJ2</td>
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<td></td>
</tr>
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<td>NOT USED</td>
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<td>BDAL6L</td>
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<tr>
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<td>BL2</td>
<td>BDAL7L</td>
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<td></td>
<td></td>
<td>BN2</td>
<td>BDAL9L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BP1</td>
<td>BIRDQ7L</td>
<td></td>
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<td>BP2</td>
<td>BDAL10L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BR1</td>
<td>BEVNTL</td>
<td></td>
<td>+12VB</td>
<td>BR2</td>
<td>BDAL11L</td>
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<td></td>
</tr>
<tr>
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<td>PSPARE4</td>
<td></td>
<td></td>
<td>BS2</td>
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<td></td>
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</tr>
<tr>
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<td></td>
<td></td>
<td>BU2</td>
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</tr>
<tr>
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<td></td>
<td>BV2</td>
<td>BDAL15L</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*NOT BUSSED

Q BUS PIN ASSIGNMENTS

A-1
SCD-DLV11J/8P ADDRESS ASSIGNMENTS VIA SW3 SWITCH SETTINGS

NOTES: SW3 POSITIONS ARE NOT LISTED IN NUMERICAL ORDER.
SW3-5 IS CONSOLE ENABLE/DISABLE.

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>---SW3 SWITCH POSITIONS---</th>
<th>---ADDRESS BITS---</th>
<th>ADDRESS</th>
<th>---SW3 SWITCH POSITIONS---</th>
<th>---ADDRESS BITS---</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1  2  3  4  8  7  6</td>
<td>A12  A11  A10  A09  A08  A07  A06</td>
<td></td>
<td>1  2  3  4  8  7  6</td>
<td>A12  A11  A10  A09  A08  A07  A06</td>
</tr>
<tr>
<td>160000</td>
<td>ON  ON  ON  ON  ON  ON  ON</td>
<td></td>
<td>160000</td>
<td>ON  ON  ON  ON  ON  ON  ON</td>
<td></td>
</tr>
<tr>
<td>160100</td>
<td>ON  ON  ON  ON  ON  ON  OFF</td>
<td></td>
<td>165000</td>
<td>ON  OFF  ON  OFF  ON  ON  ON</td>
<td></td>
</tr>
<tr>
<td>160200</td>
<td>ON  ON  ON  ON  ON  OFF  ON</td>
<td></td>
<td>165100</td>
<td>ON  OFF  ON  OFF  ON  ON  ON</td>
<td></td>
</tr>
<tr>
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<td>ON  ON  ON  ON  OFF  ON  ON</td>
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Refer to DEC's "Microcomputer Interface Handbook, 1980" for recommended address assignments.