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1.0 INTRODUCTION

The SA4600 Disk Controller is a complete preprogrammed microprocessor based controller for the Shugart SA4000 series disk drives and SA800/850 Floppy Disk Drive.

The SA4600 Disk Controller is designed to perform asynchronous data transfers between the SA4000 and a host CPU.

The SA4600 features a general purpose DMA type interface designed to easily adapt to commercially available DMA controller chips.

Several optional configurations also make this interface adaptable to virtually any type of mini or micro computer. Some main features of this controller are as follows:

A) Control of one to four SA4000 drives and one to four SA800/850 Floppy Disk Drives.
B) Asynchronous DMA transfer with full sector buffering.
C) Four user selectable formats — 32 sectors of 512 bytes, 60 sectors of 256 bytes, 104 sectors of 128 bytes, or 26 sectors of 256 bytes (Floppy option only).
D) Overlap seek operation (up to four drives).
E) Single five volt supply.

2.0 SPECIFICATION SUMMARY

Environmental Limits
Ambient temperature = 0°C to 50°C
Relative humidity = 20% to 80%

DC Voltage Requirements
+5 VDC ± 5% 7.0A typical, 7.5 maximum (with floppy option)

Heat Dissipation = 120 BTU/hr. typical

Mechanical Dimensions (reference Figure 8)
Length = 18” (45.72cm)
Width = 12.5” (31.75cm)
Height = 1” (2.54cm)

3.0 SA4000 DRIVE INTERFACE DESCRIPTION (Reference Figure 1)

The SA4000 drives are interfaced through connectors J1, J2, J3, J4 and J5.

J1 is a 50 pin ribbon cable type edge connector which connects the SA4000 drives in a daisy chain configuration. Up to four drives may be bussed together on this cable. This cable should not exceed 20 feet (6 meters). Refer to section 9.1.5 — Cable Termination Description.

J2 through J5 are 20 pin ribbon cable type edge connectors which are the radial connectors for up to four drives. J2 is the radial connector for Drive 1. J3 is the radial connector for Drive 2, etc. These cables should not exceed 20 feet (6 meters). Refer to Figure 2 for a diagram of the pinouts for J1 and J2 through J5.

Refer to section 12.2 for Connector Physical Description.
4.0 HOST CPU INTERFACE DESCRIPTION

The SA4600 host CPU interface is a general purpose DMA type interface which is accomplished through connector J6. J6 is a 50 pin ribbon type cable edge connector. Refer to Figure 3 for pin assignments. All signals to the CPU interface are TTL negative true, 48MA. This cable should not exceed 10 feet (3 meters).

A description of the CPU interface lines follows:

4.1 Reset

This line will cause the controller to cease all operation, clear local ram memory, reset the command, status, and result registers, and go into a normal wait loop. A reset during a write operation may cause improper data to be written. The RESET pulse width must be at least 200 nanoseconds. The SA4600 will not accept a command for 3 milliseconds after a reset. The host CPU must time out for 3 ms.

4.2 Controller Select

This signal functions as a device select and should only be active when one of the four registers in the controller are to be operated on.

4.3 Address

The address line selects which register will be read/written. See Table 1.
4.4 Read

When this line is active along with controller select, one of two read only registers will be read onto the data bus. See Table 1 and host interface timing, Figure 4.

4.5 Write

When this line is active along with controller select, one of two write only registers will be written to from the data bus. See Table 1 and Figure 4.

4.6 Data Bus 0-7

The data bus consists of 8 bit bi-directional tri-state lines with data bus bit 0 being the least significant bit. See Section 8.0 for an optional configuration.

Table 1. Interface Register Map

<table>
<thead>
<tr>
<th>READ ONLY REGISTERS</th>
<th>WRITE ONLY REGISTERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDRESS = 1</td>
<td>STATUS</td>
</tr>
<tr>
<td>ADDRESS = 0</td>
<td>RESULT</td>
</tr>
</tbody>
</table>
4.7 DMA Request
After a data transfer command has been received and data is ready to be transferred, the controller will make this line active to request a memory cycle. Refer to Figure 5 (DMA timing). See Section 8.0 for optional configuration.

4.8 DMA Acknowledge
This signal is made active by the host CPU to indicate that a memory cycle has been granted, and that data is either present on the data bus or data has been written into memory from the data bus. The data bus is active during acknowledge for either a read or write operation. Refer to Figure 5 (DMA timing). See Section 8.0 for optional configuration.

4.9 Interrupt
This signal is made active by the controller to indicate that an operation has terminated and it is in need of service for presenting the ending result byte. The interrupt is reset when the result register is read. All commands end with an interrupt.
5.0 HOST CPU INTERFACE REGISTER DESCRIPTION

There are four registers in the controller (shown in Table 1) that provide the control functions. They are the command, parameter, status, and result registers. These registers are available on the data bus when the associated read, write, and address lines are activated (see Figure 4).

5.1 Command Register

This is a 8 bit write only register that when loaded signifies the beginning of a command sequence. This register may not be reloaded until a result has been presented to the host CPU. Table 2 lists the commands executed by the controller and their binary bit patterns. Section 6.0 describes each command in detail.

5.2 Parameter Register

All commands issued to the controller require additional data to be executable. The parameter register is a 8 bit write only register that serves to transfer the parameter data to the controller. Table 2 lists the number of parameter bytes required for each command and Table 3 describes the usage for each of the four possible parameters.

Commands will not be executed until the last parameter byte has been transferred.
The status register provides the means for control information to be passed between the host CPU and the controller. Contents of the status register is not valid during DMA transfer. The status register bit assignment is as follows:

5.3.1 Command Busy and Command Reg Full
When the Host CPU sets a command into the command register, both the command full and command busy bits will be set. When the controller reads the command and begins execution, it will reset the command register full bit. During execution, the command busy bit remains set. The controller will then set interrupt at the completion of the command sequence and reset command busy after the result register has been read. The exception to this rule is the seek command where command busy is reset when the seek is implemented so that overlapped seeks may be performed.

5.3.2 Parameter Reg Full
When the Host CPU loads a byte into the parameter register this bit will be set. The controller will reset this bit after the parameter register has been read, at which time the Host CPU may send the next parameter byte.
### Table 2. Command Code Chart

<table>
<thead>
<tr>
<th>Command</th>
<th>MSB</th>
<th>BIT</th>
<th>LSB</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Read ID</td>
<td>X</td>
<td>0</td>
<td>1</td>
<td>0 0 0 0 0</td>
</tr>
<tr>
<td>2. Read Diagnostic</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 0</td>
</tr>
<tr>
<td>3. Verify Data</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 0 0 1</td>
</tr>
<tr>
<td>4. Verify Data and Special</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 0 0 1</td>
</tr>
<tr>
<td>5. Seek</td>
<td>X</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 1</td>
</tr>
<tr>
<td>6. Recalibrate</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 1</td>
</tr>
<tr>
<td>7. Terminating Sector Request</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 0 0 0 1</td>
</tr>
<tr>
<td>8. Read Data</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 0 0 1</td>
</tr>
<tr>
<td>9. Read Data and Special</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 1 0 0</td>
</tr>
<tr>
<td>10. Search Data Equal</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 1 0 0</td>
</tr>
<tr>
<td>11. Search Data Equal and Special</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 1 0 0</td>
</tr>
<tr>
<td>12. Search High or Equal</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 1 1 0</td>
</tr>
<tr>
<td>13. Search High or Equal and Special</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 1 1 0</td>
</tr>
<tr>
<td>14. Search Low or Equal</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 1 1 1</td>
</tr>
<tr>
<td>15. Search Low or Equal and Special</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>0 0 1 1 1</td>
</tr>
<tr>
<td>16. Write ID</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 0 1 0 0</td>
</tr>
<tr>
<td>17. Format Cylinder</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1 0 0 0 0</td>
</tr>
<tr>
<td>18. Initialize</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1 0 0 0 1</td>
</tr>
<tr>
<td>19. Write Data</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1 1 0 0 0</td>
</tr>
<tr>
<td>20. Write Special Data</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>1 1 0 0 0</td>
</tr>
<tr>
<td>21. Write Buffer</td>
<td>0</td>
<td>X</td>
<td>0</td>
<td>1 1 1 0 0</td>
</tr>
</tbody>
</table>

---

**5.3.3 Result Reg Full**

This bit is set at the completion of a command sequence to indicate that the Host CPU must read the result register. This bit is reset when the result register is read by the Host CPU. The result register is only valid when this bit is set.

**5.3.4 Interrupt**

The controller will set this bit when it requires service. This bit will also activate the interrupt line (Figure 3). The interrupt bit and line will be reset when the result register is read by the Host CPU.

**5.4 Result Register**

The result is loaded after the completion of a command sequence. Its content indicates any abnormal occurrence during the execution of the command. Certain commands may be retried if an error occurs (see Section 11.0). If a retry was successful, only the good completion result will be sent. However, if after 2 retries (3 attempts including the initial execution) the error still exists, the error result is sent. See Table 5 for the result byte configuration.
Table 3. Parameter Description

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Drive Address: Drive 0-3 are fixed disks, 4-7 are floppy disks.</td>
</tr>
<tr>
<td>2</td>
<td>Not Used</td>
</tr>
<tr>
<td>1</td>
<td>Head Address: Bit 4 is the second side for 2 sided floppy’s.</td>
</tr>
<tr>
<td>0</td>
<td>Fixed Head: The head address is interpreted as the fixed head address.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Cylinder Address</td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Starting Sector Address</td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Multiple Sector Count</td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Table 4. Status Register Map

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Command Busy</td>
</tr>
<tr>
<td>6</td>
<td>Command Reg Full</td>
</tr>
<tr>
<td>5</td>
<td>Parameter Reg Full</td>
</tr>
<tr>
<td>4</td>
<td>Result Reg Full</td>
</tr>
<tr>
<td>3</td>
<td>Interrupt</td>
</tr>
<tr>
<td>2</td>
<td>Not Used</td>
</tr>
<tr>
<td>1</td>
<td>Not Used</td>
</tr>
<tr>
<td>0</td>
<td>Not Used</td>
</tr>
</tbody>
</table>

LSB | MSB
--- | ---
0   | 7
1   | 6
2   | 5
3   | 4
4   | 3
5   | 2
6   | 1
7   | 0
5.4.1 Result Byte Description

There are four types of result bytes that are further broken down to give more specific information. These are shown by the completion codes (bits 6, 5, and 4 respectively). Refer to Table 5.

5.4.1.1 Good Completion (Completion Type 00)

000 – Command completed without error.
001 – Srch Not Met – The specified argument and the specified sector(s) did not satisfy the search command.
010 – Srch Met Equal – The argument and the sector contents are identical where specified.
011 – Srch Met High or Low – The unequal search was satisfied.
100 thru 111 – Seek complete – Result byte issued after a seek command is complete and drive is ready to read or write.

5.4.1.2 Sub-System Error (Completion Type 01)

This type of error indicates an error occurred in the drive or control unit.

000 – Seek Error – Posted only for imbedded seeks when the control unit cylinder or head register does not match the cylinder or head address read off the disk in the ID field of a sector. The control unit will re-calibrate and re-seek the head arm if retry is not inhibited before posting this result.

001 – CRC Error ID Field – The control unit detected a CRC error in an ID field.

Table 5. Result Register Map

<table>
<thead>
<tr>
<th>Completion Type</th>
<th>Good Completion</th>
<th>Sub-System Error</th>
<th>Operator Intervention</th>
<th>Command Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Good Completion</td>
<td>Seek Error*</td>
<td>Drive Not Ready</td>
<td>Illegal Length</td>
</tr>
<tr>
<td>001</td>
<td>Srch Not Met</td>
<td>CRC Error ID* Field</td>
<td>Write Protection Check (floppy only)</td>
<td>Record Not Found*</td>
</tr>
<tr>
<td>010</td>
<td>Srch Met Equal</td>
<td>CRC Error* Data Field</td>
<td>Restore Error</td>
<td>Invalid Command</td>
</tr>
<tr>
<td>011</td>
<td>Srch Met High or Low</td>
<td>Sector Error</td>
<td>Write Fault</td>
<td>Late DMA</td>
</tr>
<tr>
<td>100</td>
<td>Seek Complete Drive 1</td>
<td>ID Sync Err*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>101</td>
<td>Seek Complete Drive 2</td>
<td>Data Sync Err*</td>
<td></td>
<td></td>
</tr>
<tr>
<td>110</td>
<td>Seek Complete Drive 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>111</td>
<td>Seek Complete Drive 4</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*With inhibit retry bit in command not set these error conditions are retried 2 times before result is sent. With seek inhibit set in the command these errors will not be retried.
010 – CRC Error Data Field – The controller was unable to read the data field. If retry is inhibited this result will be sent after the DMA transfer of the data in error has been sent. When retry is enabled the controller will attempt to read the data twice and if this is not successful the result will be posted before any DMA transfer of data takes place.

011 – Sector Error – The controller has determined that the time between sectors does not agree with the maximum sector code sent in the initialize command.

100 – ID Sync Error – The controller was unable to find the sync byte for an ID field within a 4 byte tolerance.

101 – Data Sync Error – The controller was unable to find the sync byte for a data field within a 4 byte tolerance.

5.4.1.3 Operator Intervention (Completion Type 10)
This type of error cannot be resolved without outside help.

100 – Drive Not Ready – The ready line from the disk is not active after the drive is selected.

101 – Write Protection Check – This error can only occur on a floppy disk write operation when the diskette is write protected.

110 – Restore Error – While stepping the maximum number of cylinders during a recal command the controller was unable to detect track 00 line active.

111 – Write Fault – The write fault line was active at the end of a write operation. The controller will reset the write fault at the beginning of a new command.

5.4.1.4 Command Error (Completion Type 11)
This type of result is sent when the control unit cannot execute the command as specified.

000 – Illegal Length – The parameters for the command exceed the maximum cylinder, head or sector capacity of the drive as specified by the initialize command for that drive.

001 – Record Not Found – The specified sector did not occur in any of the ID fields read from the track. Cylinder and head numbers did match.

010 – Invalid Command – The command code is undefined.

011 – Late DMA – Can only occur on a write operation where the host DMA has not supplied a byte of data before it was required. The data field does not contain the desired data and should be re-written.

6.0 COMMAND DESCRIPTION
The commands are organized into three groups: (1) control, (2) read/write and (3) control read/write. There are three optional bits set with the certain command codes: Inhibit retry, multiple sector and inhibit imbedded seek. Refer to table 2. If retry is inhibited, controller will only try operation for one revolution, instead of three. If imbedded seek is inhibited, the controller will not accept a new head address, but will use the head address from the previous command.

6.1 Control Commands

6.1.1 Initialize
The initialize command is used by the system to specify to the controller what the physical characteristics of the drives are at each address. This command has different parameters than those used for all other commands. They are listed in table 6.
The initialize command must be issued to each drive attached to the controller after a power on or a reset. The sector interleave code is specified by this command and is discussed in Section 6.1.1.1. The sector interleave codes allow for slow DMA transfer of data to take place without waiting for a complete revolution of the disk on a multiple sector operation. Care should be taken to insure that the code issued for the initialize command matches that on the disk when a reformat of disk is not going to be done.

6.1.1.1 Sector Interleave Code

A sector interleave code must be specified during an initialize command allowing for multiple sector reads or writes to occur without having to wait one revolution of the disk for each sector transfer. Sequential sector transfers are not possible due to timing limitations of the controller firmware:

The sector interleave code specifies the spacing between logical sectors. The following example shows an interleave code of 7 with a 32 sector format:

**Physical Sector:**

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

**Logical Sector:**

0 7 14 21 28 1 8 15 22 29 2 9 16 23 30 3 10 17 24 31 24 31 4 11 18 25 5 12 19 26 6 13 20 27

Note that this interleave code has 4 sectors between consecutive sectors at the beginning of the track but only 3 toward the end. This example is given to show that the interleave code must be chosen carefully.

Several codes for each sector size option that give a constant number of interleaved sectors are shown in the following table:
Table 7. Interleave Code

<table>
<thead>
<tr>
<th>Sectors/Track</th>
<th>Interleave Code</th>
<th>Interleave</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>16</td>
<td>1</td>
</tr>
<tr>
<td>32</td>
<td>11</td>
<td>2</td>
</tr>
<tr>
<td>32</td>
<td>8</td>
<td>3</td>
</tr>
<tr>
<td>60</td>
<td>30</td>
<td>1</td>
</tr>
<tr>
<td>60</td>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td>60</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>60</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td>104</td>
<td>52</td>
<td>1</td>
</tr>
<tr>
<td>104</td>
<td>35</td>
<td>2</td>
</tr>
<tr>
<td>104</td>
<td>26</td>
<td>3</td>
</tr>
<tr>
<td>104</td>
<td>21</td>
<td>4</td>
</tr>
</tbody>
</table>

6.1.2 Recalibrate

A recalibrate will step the head arm towards track 00 until the drive sends the track 00 indication. After each step the controller waits for seek complete. This is different than a seek to zero in that the controller does not calculate and then issue the required number of step pulses. The controller will reset its cylinder register with this command. An interrupt is set upon completion of a recalibrate.

6.1.3 Seek

A seek command will move the head arm assembly the required number of cylinders to position over the addressed track and select the desired head. A seek command will not read an ID field to verify operation, however, track 00 switch is monitored for errors. After issuing a seek on a fixed disk drive the controller will drop command busy and is free to accept a command to another drive. An interrupt is set upon completion of the seek with a seek complete result byte. Note that command busy bit is not set with this interrupt.

6.1.4 Terminating Sector Request

This command is valid after a read, write, search or verify data command. There are seven bytes DMA transferred to the CPU memory. The first three bytes are the cylinder, head and sector for the last sector the controller operated on. If an error occurred that was associated with the ID field for that sector, the last four bytes transferred are the flag, cylinder, head and sector bytes read from the disk. Note that the last four bytes are only valid after a defective ID found, an ID CRC error, or a seek error.

The first three bytes are used to determine:

A) At what sector a search was met.

B) At what sector an error occurred on a multiple sector command.

After DMA is complete an interrupt is sent and a good completion result is set.

6.2 Read/Write Commands

Read and write commands transfer data to or from CPU memory via DMA transfer. A full sector buffer (512 bytes) is used in the controller to avoid data overruns. Two CRC bytes with a generator polynomial of $X^{16} + X^{12} + X^5 + 1$ are appended to all records on the track for error detection.
All read/write commands, unless otherwise specified, will perform a seek to the specified cylinder and head and search for the desired sector before attempting to read or write the data field. Any errors encountered during this procedure cause a retry (maximum of two) before the error is posted. Retry may be inhibited with a bit in the command code. Read/write operations may be single or multiple sector transfers. An interrupt is set after DMA transfer is complete.

6.2.1 Format Cylinder
A seek to the specified cylinder will be performed by the controller and the ID fields written according to the interleave code specified in the initialize command. All heads in that cylinder are formatted. Data fields are not written. With the fixed head bit set all fixed heads are formatted.

6.2.2 Write ID
A write ID command will orient to the field specified in the parameters according to the interleave code and write the ID field with the DMA data. The data field will not be changed.

For the fixed disk drives, a flag, cylinder, head and sector byte must be transferred. See Section 10.0 for flag byte definition. For a floppy disk four bytes are required; cylinder, head, sector, and a record size byte. Refer to Section 10.0 track formats. An interrupt is set when command is complete.

6.2.3 Write Data
This command will write the data field of the length specified in the initialize command. Data transfer from memory will begin filling the sector buffer before the sector is under the read/write head and DMA overrun will be checked during the write operation.

6.2.4 Write Data Special
This command operates the same as a write data except a unique address mark is written at the beginning of the data field.

6.2.5 Read ID
A Read ID will transfer the first ID field encountered back to the CPU. This command will not perform an imbedded seek. This command is intended as a diagnostic and for alternate sector assignment.

6.2.6 Read Data
The specified data is DMA transferred to memory. If a special sync byte is encountered, no data for that sector is transferred and the special data found bit is set in the result. After DMA transfer is complete for all sectors an interrupt is sent and result reg full is set. See Section 11.0 for retry conditions.

6.2.7 Read Data and Special
This command operates the same as a write data except a special sync byte is written at the beginning of the data field.

6.2.8 Search Data Equal
This command will read the specified sector(s) and compare this data with the data in memory. Once the data in memory is DMA transferred to the sector buffer no further transfer is required. Any hex 'FF' byte will not be compared; all others will be compared for equivalence. Special data fields will be ignored.
6.2.9 Search Data Equal and Special
Special data will also be compared.

6.2.10 Search Data High or Equal
A comparison where data on the disk is of greater binary value or equal to that in memory will satisfy this search.

6.2.11 Search Data High or Equal and Special
Special data will also be compared.

6.2.12 Search Data Low or Equal
This search is satisfied if data on the disk is of lower binary value or equal to data in memory.

6.2.13 Search Data Low or Equal and Special
Special data is included in the search.

6.2.14 Verify Data
No DMA transfer of data will occur, however, data will be read into the sector buffer and the CRC checked for errors.

6.3 Control Read/Write

6.3.1 Read Diagnostic
This command is used when an ID field is unreadable. When issued the controller will orient to the specified track and sector then skip over the ID field, and transfer the data field to memory.

6.3.2 Write Buffer
This command provides the system with the capability to copy a sector on one drive to an equal length sector on the same or different drive without transferring data through memory. The sector address specified in this command will be a physical sector address.

The write buffer command writes the present contents of the sector buffer to the specified sector. The sector buffer may be filled with a read data, write data or verify data command.

7.0 COMMAND PROCEDURE

The controller operates on one command at a time except in the case of a seek where all 4 drives may be seeking. In general the following description gives the sequence of events for a command. The controller is designed to be used with DMA logic located at the CPU.

A) The CPU sets up its DMA logic for the transfer of data if the command calls for it.

B) The CPU then checks the status reg for a zero condition and initiates the command, the controller in turn sets the command full and busy bits in the status register.

C) The controller will read the command and reset the command full bit.

D) The CPU will then send the required number of parameters for the particular command. Each time a parameter is sent, the parameter full bit in the status is set. After the controller reads the parameter it will reset this bit.
E) When the last parameter is read the controller operates on the command and DMA transfers data if required, or if an error condition occurs before DMA an interrupt is set with the result. Minimum time from last parameter to DMA transfer is 100 microseconds.

F) After DMA transfer is complete the controller sets an interrupt after loading the result reg and setting the result full bit.

G) The interrupt is acknowledged by the CPU by reading the result register which in turn resets the interrupt.

H) When the CPU reads the result, the command busy and result full bits in the status will be reset and the command is complete.

8.0 OPTIONAL HOST CPU INTERFACE CONFIGURATIONS

The 4600 has cut trace options that provide a separate 8 bit input bus and an 8 bit output bus. In addition there are 4 jumper options that provide different DMA data transfer techniques.

The data bus option is accomplished by cutting 8 traces that remove the bi-directional tri-state data bus signals from even pins 20 through 34 and adding 8 jumper plugs that connect the data bus outputs to even pins 36 through 50. Input data is now received on even pin 20 through 34. See Figure 6. (Also see Appendix B/Schematics).

8.1 R and W Jumper Description

The DMA request and DMA acknowledge along with read and write accomplish data transfer directly to host CPU memory as described in Section 4.0 and timing diagram, Figure 5. There are two jumpers (R and W) on the SA4600, that when removed, the request and acknowledge are the only signals required to transfer data. In this case, data going to the host CPU is enabled during acknowledge and data from the host CPU is latched in the controller on the trailing edge of acknowledge.

---

Figure 6. Optional Host CPU Interface Connection
8.2 RQ and A Jumper Description
There are two additional jumpers that provide further interface modification (RQ and A). In the normal configuration data transferred to/from the controller is latched on the trailing edge of acknowledge. (Refer to Figure 5.)

The data being transferred may be accomplished on the leading edge of acknowledge by cutting the trace underneath the RQ and A jumpers and installing the jumper plug in the alternate position. (See Figure 7 and Figure 7.1)

8.3 Jumper Description
Jumper F must be installed for proper operation.

9.0 SA4000 DRIVE OPTION DESCRIPTION
To achieve proper operation from the SA4000 interfaced to the SA4600, certain jumper options on the SA4000 drive must be set. They are as follows:

9.1 Control PCB

9.1.1 Drive Select
The Jumper X must be opened and one of the four drive select lines (DS 1, 2, 3, 4) must be jumpered. DS 1 corresponds to the controller drive 0.

Figure 7. RQ Jumper Option Timing (Read Mode)

Figure 7.1 A Jumper Option Timing (Write Mode)
9.1.2 Byte Clock/Sector Mark
Jumper ST must be jumpered. SC must be jumpered. BC must be open.

9.1.3 Miscellaneous
Jumper RY (ready) must be jumpered. Jumper IX (index) must be jumpered. Jumper T (bypass warmup) should be installed. Jumper D must be jumpered. Jumper E must be open. Jumper C (seek complete) must be open. Jumper S2 (index delete) must be jumpered. Jumper S1 (index add) must be open.

9.1.4 Sector Counter Options
The SA4600 has three possible formats which are described in Section 10.0 (format). Depending on the format selected by the user, the sector counter option must be set accordingly. Use the following table 8 to select sector size.

<table>
<thead>
<tr>
<th>Sector Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 SECTORS</td>
</tr>
<tr>
<td>60 SECTORS</td>
</tr>
<tr>
<td>104 SECTORS</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MSB</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
</tr>
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<tbody>
<tr>
<td>2048</td>
<td>1024</td>
<td>512</td>
<td>256</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MSB</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
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</thead>
<tbody>
<tr>
<td>128</td>
<td>64</td>
<td>32</td>
<td>16</td>
<td>8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MSB</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>2</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MSB</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>30</td>
<td>15</td>
<td>8</td>
<td>4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MSB</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
<th>IX</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MSB</th>
<th>IX</th>
</tr>
</thead>
<tbody>
<tr>
<td>512</td>
<td>256</td>
</tr>
</tbody>
</table>

X = JUMPERED

9.1.5 Cable Termination Description
In a multiple drive system, only the last drive on the J1 daisy chain cable should be terminated. A 220/330 OHM terminator pack is located at location 3H. Removal of 3H unterminates the drive. In a single drive system, 3H must be in place.

9.2 Data Separator Board
Jumper C (sync up on 0’s) must be jumpered. Jumper D (sync on 1’s) must be open.

All other jumpers must be configured for the host system’s individual requirements. Refer to the SA4000 OEM manual part number 39005.

10.0 FORMAT DESCRIPTION
As mentioned in the introduction, the SA4600 is capable of formatting four different formats. Only the three formats for the SA4000 will be discussed. Each track is divided up into data block or sectors. Each sector may contain 128, 256 or 512 Bytes. A full sector buffer is provided so that the host interface may transfer data at a rate compatible with its own timing requirements.

Each sector (Data Field) is preceded by an identification field (ID Field). The ID Field contains four Bytes of information. The first byte is a flag byte which contains a defective sector bit (LSB) which is set by the host system when using the write ID command. If a sector is read with this bit set, bit 0 of the result byte will be set. (Refer to Table 5.) The remaining 7 bits may be used by the host CPU for special purpose flags.
The 2nd, 3rd, and 4th bytes are cylinder, head and sector bytes. These bytes are used by
the controller to verify correct location of the data field and are also available to the host
CPU by using the read ID command.

At the end of the ID Field and Data Field, there are two bytes known as CRC (cyclic
redundancy check). This 16 bit binary number is a polynomial generated from the contents
of the ID field or Data Field and is used to verify the data during a read.

At the beginning of the ID field is a unique character known as a sync byte. The sync byte
is used to flag the beginning of the ID field and data fields. It is also used by the controller
to align Byte Boundries.

A gap of 15 bytes of zero’s is placed between the end of the ID field and the beginning of
the data field to provide a VFO lock on area since when a write data operation is performed,
only the data field is changed—not the ID field.

Two types of sync marks are used to flag the beginning of the data field. A Hex ‘0D’ is the
normal sync byte data pattern. A Hex ‘0B’ is used to flag special data fields (user defined).

Refer to Figure 8 for a layout of the SA4600 format.

Figure 8. SA4600 Format

11.0 ERROR RETRY
The controller will retry certain error conditions two times before posting an error in the
result register. The types of errors are:

A) Any CRC error on an ID or data field.
B) Unable to find a sync byte for an ID or data field.
C) The imbedded seek on read or write operations where the ID field must be read. The
retry may be inhibited with a bit in the command.

12.0 PHYSICAL DESCRIPTION

12.1 P.C. Board
The SA4600 will control four SA4000 fixed disk drives and four SA800/850 floppy disk
drives, and consists of a single 12.5" x 18" PCB.

Connection to the disk drives and the CPU is made via card edge connectors.
12.2 Connectors

Three types of connectors are required: A 50 pin edge connector, a 20 pin edge connector and a 4 pin plug for power.

12.2.1 50 Pin Connectors

50 contact edge connectors are provided for the SA4000 multiplex cable, the SA800/850 interface and the CPU interface. The dimensions for these connectors are shown in Figure 10. The pins are numbered 1 through 50 with the even pins on the component side of the board. The recommended mating connector is Scotchflex ribbon connector P/N 3415-0001 or Amp twin-leaf printed circuit connector P/N 583717-1 utilizing Amp contacts P/N 1-583616-1.

12.2.2 20 Pin Connectors

These edge connectors match those read/write connectors on the SA4000 series drive. The dimensions are shown in Figure 11. The recommended mating plug is Scotchflex ribbon connector P/N 3461-0001 or Amp P/N 581717-1 with Amp contacts P/N 1-683616-1.

12.2.3 Power Connectors

The control unit uses +5VDC power with a socket mounted on the board. The mating plug for this socket is AMP P/N 1-480424-0 with pins P/N 61473-1. Figure 12 shows the pin configuration with pins 1 and 4 being ground and pin 2 and 3 the +5VDC.
Figure 10. 50 Pin Connector Drawing

Figure 11. 20 Pin Connector Drawing

Figure 12. DC Connector Drawing
Appendix A

Basic Command Process Flowchart (Sheet 1)
Basic Command Process Flowchart (Sheet 2)
Appendix B/Schematics