

THE Q1/LMC MAINTENANCE MANUAL

004-91001

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1. Introduction

The Q1/LMC system is a general purpose computer, utilizing TTL and MOS logic technologies. The processor is implemented with a single chip CPU and has a bus structure for data to and from the I/O and memory devices.

The standard I/O peripherals are a keyboard, a printer, a display, and an IBM compatible floppy disk. Each peripheral has a controller which interfaces the peripheral to the I/O bus.

1.1 Scope

This manual is intended for use by a service technician in servicing and debugging the Q1/LMC system. The manual contains schematics and circuit descriptions.

Field service should be limited to replacement and not the repair of faulty components.

There is little or no preventive maintenance required on the system.

1.2 Reference Documents

The following documents will be useful, but not necessary for the service man to have:

- Q1/LMC Reference Manual (004-73001)

- Shugart SA900/902 Maintenance Manual

- Diablo Model 1200 Printer Maintenance Manual

- Intel 8080 Reference Manual

- Burroughs Reference Manual

1.3 Required Test Equipment

A standard tool kit is required plus the following equipment and supplies:

- Disk with test programs

- Spare PC boards for all electronics

- Volt meter with 1.0% accuracy or better

- Logic probe

- Oscilloscope with bandwidth of 50 MHz or better
(for lab use, not field service)

- Alignment disk and Q1 Disk Test Panel

2. System Definition

2.1 System Components

The use and programming of each peripheral is described in the Q1/LMC Reference Manual (004-73001).

The operation and debugging of the electronics is described in later sections.

2.2 Use of the Q1/LMC System

To use the system, turn on the power switch located on the desk unit, depress the restart switch, and insert a diskette in disk drive No. 1. Then follow the directions for the program which was loaded.

3. I/O Bus

3.1 Signal Definitions

ADR0- thru ADR15- : ADDRESS bus

Both the memory and the I/O peripheral controllers use these lines to define an address. The I/O, however, only uses ADR0- thru ADR4-. Logic "0" is a high level. Logic "1" is a low level. These lines are driven by the test panel in a MEMORY READ or MEMORY WRITE operation. During a memory cycle these lines contain the memory address. During an I/O operation, these lines contain the address of the I/O device.

DATA0- thru DATA7- : DATA bus

Logic "0" is a high level. Logic "1" is a low level. These are bi-directional lines used for transferring data to and from the processor.

START MEMORY CYCLE- : Memory Control line

This line pulses low when the processor wants to read or write a byte of memory data. If the memory is refreshing, it responds by lowering the MEMORY READY line. If not, a memory cycle starts. If this signal is not followed by a START WRITE CYCLE, the memory cycle will be a read cycle. The data presented as a result of a read cycle remains stable until the next memory operation.

START WRITE CYCLE- : Memory Control line

This line pulses low to initiate a memory write operation.

MEMORY READY : Processor Control line

This line indicates to the processor that the memory is ready for a data transfer. If not, the memory responds to a START MEMORY CYCLE by lowering this line until the memory becomes ready.

OUTPUT- : I/O Control line

This line going low indicates that an I/O operation is an output function. If the line does not go low during an I/O operation, the I/O is an input cycle.

STROBE- : I/O Control line

This line is used as a data strobe for I/O cycles.

MSTROBE- : Memory Control line

This line is used during a memory read cycle to enable memory data on the DATA bus.

PRST- : System Control line

This line is used as a system reset. It goes low for several milliseconds after power turn on.

INTR- : Processor Control line

This line pulses low when an I/O device wants to interrupt the processor.

3.2 Electrical Definitions

All data bus lines are standard TTL levels. The ADR, DATA, and MEMORY READY lines are driven with open collector gates.

4. Q1/LMC Processor Board

4.1 Schematic Diagrams (004-51008)

4.2 Functional Description

The processor board can be divided into functional blocks. The basic clocks are controlled by a crystal oscillator in the Timing Generator section. The CPU controls all I/O and memory operations, as well as arithmetic, logical and other operations associated with any CPU cycle.

Address and data lines are buffered in order to drive cables. A multiplexer is used for panel and interrupt data operations. The processor board also contains 8K bytes of PROM and a programmable timer.

4.3 Circuit Description and Theory of Operation

4.3.1 CPU Status

During the T2 state of each processor cycle the D₀ through D₇ data lines contain CPU status information. This information indicates the type of cycle in process, e.g., memory read, memory write, input, output, etc. As shown on schematic sheet 1, the status is latched with the leading edge of STBT2.

If an interrupt is acknowledged, INTA status bit is set, the multiplexer enables a RESTART instruction to the D bus which forces the processor to location 00 and stores the program counter in the stack.

4.3.2 Memory Control

During normal processor operation START MEMORY CYCLE— is enabled to all memory during each STBT2 as seen on schematic sheet 2. If the current operation is a memory write, START WRITE CYCLE— will be enabled to the 16K memory boards by the AND function of WR and OUT—.

When the Panel is not Ready, or during the Wait period following a HALT instruction, START MEMORY CYCLE— line will be pulsed every 50μ seconds. This pulse permits the Panel to read memory when addressed as described later, and also will initiate a Memory Refresh operation at the appropriate time as described in the 16K Memory section 5.3.3.

SMR is enabled when the Panel is not Ready (PRDY low), or the CPU has acknowledged a Halt instruction (HLTA— low). SMR fires a 50μ second mono which subsequently clocks a delay flip-flop to the set state. With the Delay flop set, the next 01B pulse sets the WTEN flip-flop, which in turn gates 01 to the START MEMORY CYCLE— line. In addition, WTEN resets the Delay flip-flop. The AND function of WTEN and 01B enables SWS. This process is repeated approximately every 50μ seconds until an Interrupt instruction or suitable instructions from the Panel are jammed into the CPU.

While SMR is high Panel data may be written into memory. To achieve this the Panel enables PWRITE— low. The next WTEN sets the PWR flip-flop. PWR gates SWS to the START WRITE CYCLE— line.

READY and Memory Address Enable logic is shown on sheet 3. The system may go Not Ready and Ready asynchronously with the CPU. Not Ready condition results from the Panel not in the ready state, RAM memory accessed while in a refresh cycle.

When the Ready line goes low the CPU enters the TW (wait) state after the next T2 state. The CPU remains in the TW state until the Ready line has remained high for the duration of one 01B pulse.

As seen on schematic sheet 3, CPU Address lines A0 through A15 are enabled to the I/O Bus lines ADR0- through ADR15- by MADEN. However, during Panel Read or Write operation, MADEN is gated low enabling Panel Address lines to the ADR0- through ADR15- bus. This condition exists while the PWR flip-flop is set for writing from the Panel or after a Panel Read request. A Panel Read causes PREAD- to go low, setting the PRR flip-flop at the beginning of the next WTEN pulse. PRR gates ADR0- through ADR15- lines into the open state and provides a low on the MADEN line to the Panel.

4.3.3 HOLD- Signal

HOLD- line is provided for future DMA capability. A low on this line will force the CPU into the HOLD state, driving the CPU data and address lines into a high impedance state.

4.3.4 I/O Control Signals

As previously described, a low on the OUTPUT- line indicates that a I/O operation is an output function. If the line does not go low during an I/O operation, the I/O is an input cycle. The STROBE- line is used as a data strobe for I/O cycles. The MSTROBE- line is used during a memory read cycle to enable memory data to the DATA0- through DATA7- bus. The DATA0- through DATA7- bus is controlled by the Processor's DATA IN signal as seen on schematic sheet 4.

CPU status line OUT drives the OUTPUT- line and also gates the AND function of WR, WAIT-, and 02 to the STROBE- line. The STROBE- line is also enabled low by the AND function of CPU status INP and the CPU DATA IN control signal. With the absence of a Panel Write Request PWR- is high enabling CPU status line MEMR to gate DATA IN to the MSTROBE- line.

DATA IN true steers the DATA0- through DATA7- lines to the input direction. With DATA IN true and a low on the DDN line (Panel not enabled, or the absence of an interrupt) the DATA0- through DATA7- lines will be enabled to the D bus via tri state gates. DATA IN false places the DATA0- through DATA7- lines in the output direction and the signals on these lines follow the data present on the DO and D busses.

4.3.5 Power-On Reset

When the system power is turned on, and each time either the Console or Panel Reset pushbuttons are depressed, the system is initialized by the PRST- signal. As seen on schematic sheet 5, C47 is discharged when power is first turned on, or if either the Console or Panel Reset pushbuttons are depressed pulling the PNLRST- line low. As the +5V power rises or after the Reset pushbutton is released, the signal on C47 slowly rises to +5V. This signal is coupled to the input of a Shmitt-Trigger inverter by emitter follower Q2. The output of the Shmitt snaps low when the slow rising input exceeds its threshold. The Shmitt output is complimented and drives the PRST- line low. During the interval over which +5V is at its nominal level and the PRST- line is low, certain logic elements throughout the system are held in the reset or cleared state.

The positive transition of PRST- fires the 2 usecond RESET Mono.

The leading edge of RESET sets RSI flip-flop which remains set until after the program issues an I/O instruction to Device Address 00x. At this time STBA0 resets the RSI.

The RESET signal is also applied to CPU. During the 2 useconds Reset period, the contents of the program counter and instruction register are set to zero. At the end of the Reset period, the program will start at address 00_x .

4.3.6 System Interrupts

Any interrupting I/O device tied to the INTR- line will set the INT flip-flop by pulsing this line low. The INT signal is sent to the Panel and the CPU. The CPU recognizes an interrupt request on this line at the end of the current instruction or while in the TW (Halt) state provided the internal Interrupt Enable flip-flop had been set by a Previous EI instruction. The CPU acknowledges the interrupt request by setting the INTA line high during SYNC1, INTA in turn resets INT. During the next instruction fetch cycle the Program Counter is not advanced and a one byte RST instruction, C7 (Restart address 00_x) is jammed into the CPU via the tri state^x input multiplexer on schematic sheet 1.

4.3.7 Timing Generator

The processor Timing Generator on schematic sheet 5 consists of a 20 MHz₂ oscillator, Schottky decade counter, appropriate decoding logic and a pair of MOS clock drivers.

4.3.8 ROM Memory

Sheets 6 and 7 of the Processor schematic contain 16K bytes of Read Only Memory and related logic. This local ROM area is accessed by addressing memory below 2000_x or 8000_x to $9FFF_x$.

During a MEMR cycle MEMSEL is enabled by decoding ADR13- and ADR14- and the appropriate PROM device is selected by ADR10- through ADR12-. MISTROBE gates the eight RM data lines to the DATA-bus.

4.3.9 Programmable Timer

A system timer with device address 00_x may be used to issue an interrupt request after a prescribed delay. As seen on schematic sheet 8 the 2 MHz 02 clock from the Processing Timing Generator is divided down to a 2.048 millisecond period CLOCK by two 6 bit binary rate multipliers. To load and enable the programmable timer, an OUT 00 is issued with the A register containing the binary equivalent of the desired delay in milliseconds divided by 2.048 milliseconds and rounded. STBA 0 is the decode of address 00 . OUT and STBA 0 sets Count Enable flip-flop enabling the 2.048 millisecond clock to an 8 bit binary counter chain. The AND function of OUT and STBA 0 also loads the data on the DATA bus into the 8 bit counter chain by direct preset inputs. This counter may be programmed for delays in steps of 2.048 milliseconds from 2.048 milliseconds to 525.288 milliseconds. Since the load and count enable operation is asynchronous with the 2.048 millisecond clock there

is an inherent + zero — 2.048 millisecond delay ambiguity. When the terminal count has arrived, the second Q_D output of the counter chain makes a high to low transition firing a 1 usecond mono. The Q output of this mono enables an open collector line driver, which in turn lowers the INTR— line and the CPU is interrupted as previously described. Firing of the 1 usecond mono also resets Count Enable.

An INPUT 00 will also place the status of the Count Enable flop and RSI flop on DATA0 and DATA1— lines respectively.

5. Q1/LMC Memory Board

5.1 Schematic Diagrams (004—51009)

5.2 Block Diagram and Functional Description

The major logic area of the 16K memory board is the Refresh, Chip Enable and Write Enable logic. Address lines are conditioned and decoded to provide Memory access. Four main input control lines initiate the Read, Write and Refresh cycles. Two output signal lines provide Memory Status and synchronize Refresh cycles. Output data lines are buffered. The board may be provided with 4K to 16K memory capability in 4K increments.

5.3 Timing Diagrams, Circuit Description and Theory of Operation

5.3.1 Memory Control

Sheet 1 of the 16K Memory schematic contains the memory Read and Write logic, Refresh logic, Chip Enable and memory Write drivers. A read or write memory cycle is initiated by START MEMORY CYCLE— going low. For a normal write memory cycle, the START WRITE CYCLE— is pulsed low approximately 500u Sec. after the start memory request. The REY signal synchronizes all RAM refresh cycles with the 16K Memory board adjacent to the Processor in the card cage.

This is implemented on the back plane by connecting all memory board P23's together. REX is connected to REY on the back plane for the first memory board location. With REX high a refresh cycle will be initiated immediately after the completion of a memory access. Refresh is performed every two milliseconds by cycling through 64 states of Addresses A0 through A5. A refresh cycle is completed in approximately 35.2u seconds.

5.3.2 Memory Ready Cycle

A negative pulse on START MEMORY CYCLE— line set the RRL FF. In the absence of a Refresh cycle, Q1 exhibits a high impedance (open circuit) when looking into its emitter. RRL— fires the CER mono and CDY goes high for approximately 700n seconds. This signal is enabled to the appropriate CE driver by a high on one of the RS1 through RS4 lines. The enable CE driver provides a +12V pulse to its associated 8 memory devices. The trailing edge of CERW fires a 330 nsecond mono enabling DOUTCLK low for this period. DOUTCLK resets the RRL FF. The trailing edge of DCY also clocks the REFACT FF. The positive edge of DOUTCLK strobes the memory read data into an 8 bit latch.

5.3.3 Refresh Cycle

If at this time the controlling 2m Sec. REFRESH MONO had timed out, setting the REFRESH FF, REX is now high and CERW sets the REFACT FF. Q1 is turned on, placing R16 in parallel with R12. REFACT— also fires the CER Mono. CDY now goes high for only 400n Sec. REFACT enables CDY to RAD CLK. The trailing edge of RAD CLK clocks Row Address Counter IC50 and IC59. CERW causes C34 to discharge and puts a high on pin 1 of CER MONO IC35. Approximately 150n Sec. after CERW goes low, IC35—1 goes low and the CER MONO is refired. This sequence continues until RAD CLK has clocked the Row Address Counter to overflow. On overflow IC59—2 fires mono IC46 for approximately 330 nSec. IC46—12 resets REFACT FF and fires the 2 mSec. REFRESH MONO. The MEMORY READY line goes low for the duration of the Refresh period.

5.3.4 Memory Write Cycle

If during the above refresh period the processor issued a Start Memory Cycle request the RRL FF stores this request. After REFACT has been reset RRL— fires CER MONO once more and CERW goes high for 700n Sec.

If a Write Memory cycle is to be executed, the Processor will issue a negative pulse on the START WRITE CYCLE— line approximately 50C n-Sec. after a Start Memory Cycle request. A Write Memory request will only be issued by the processor if memory is not being refreshed. START WRITE CYCLE— pulse fires the CEW MONO. CEW is OR'd with the current CDY pulse and this function (CERW) is steered to the appropriate CE driver. BD SEL gates CEW to the WE— line. CEW MONO time out is approximately 350n Sec.; therefore a write memory cycle takes approximately 850 nSec. while read cycle takes approximately 700 nSec.

5.3.5 Minus 3V Power Source

Resistor network R21, 22 and 23 and Q2 form a -3V power source for the memory devices.

5.3.6 Power Turn-On

System reset pulse PRST— is conditioned and fires PRSTM Mono. PRSTM goes high for approximately 300 nSec. fires the 2 mSec. MONO, and initializes the memory control logic.

5.3.7 Memory Device Selection

Sheet 2 of the 16K Memory schematic contains the following logic: A 12 bit Address Multiplexer for routing either Memory Address or Refresh Row Address to the memory device address lines. Input data buffers and output data latch and drivers. A CS and RS decoder.

A common 16K Memory board is used in the system. Memory board select is a function of data on memory address lines MA14 and 15 and the status of RANK switch S1. Table 1 on sheet 2 tabulates Memory Addresses which will enable BD SEL as a function RANK SWITCH status. With BD SEL enabled address signal MA12 and 13 select one of four rows of memory devices by a two-to-four line decoder, IC52. This decoder drives four chip select lines CS1— to CS4— which in turn enable one of four row Select Lines, RS1 to RS4. As described previously, Row Select enables the CE drivers. During a refresh cycle REFACT— enables all four Row Select lines so that all memory devices are provided with CE pulses. Chip Select lines need not be active during refresh. During a Refresh cycle RAD0 to RAD5 from the Row Address Counter are enabled to memory device address lines A0 to A5 and A6 to A11. DOUTCLK is pulsed low for each Memory Read or Write Cycle, latching memory output data.

5.3.8 Output Data Latch

Memory device output data is strobed into an 8 bit high speed output data latch at the trailing edge of DOUT CLK. MSTROBE— from the processor raises the DOUT ENA line gating the contents of the output data latch to the DATA Bus via high speed open collector line drivers.

5.3.9 Memory Device Bussing

Sheet 3 of the 16K Memory schematic shows data, address, and clock line bussing to up to 32 memory devices.

5.3.10 ADR— Bus Conditioning

Sheet 4 of the 16K Memory schematic shows the filters and threshold receivers that condition the 16 line ADR— bus.

6. Q1/LMC PROM Board

6.1 Schematic Diagrams (004-51014)

6.2 Block Diagram and Functional Description

The PROM Board provides the system with up to 16K bytes of Read Only Memory capability for stored programs. The PROM board may be loaded with memory devices in 256 byte increments. The PROM board is accessed by Read Memory request in the same manner as the 16K Memory board. Address lines ADR14— and 15— select the PROM board. The current memory devices of the PROM board have an access time which is too slow for the Processor therefore each time PROM is accessed the MEMORY READY line will go low for a period greater than 1 uSec. PROM data is gated to I/O Bus DATA— lines by MSTROBE—.

6.3 Timing Diagrams, Circuit Description and Theory of Operation

6.3.1 ADR— Lines

Sheet 1 of the PROM schematic shows the line filter and threshold receivers on the 16 ADR— lines. The filters and threshold receivers reject ADR— noise spikes 80 nSec. or less in duration. When the Processor addresses the PROM board BSEL goes as a result of ADR14F, 15F and the state of S1. ADR11F to 13F and BSEL are decoded by IC13 and the appropriate RSEL(N)— line goes low selecting one PROM device. ADR0F to ADR7F address the byte of data in the selected PROM device.

6.3.2 PROM Read Cycle

The Processor issues a Read Memory request by pulsing the START MEMORY CYCLE— line low. BSEL gates this signal to a 1.7 uSec. PROM Busy mono IC4. The Q output of IC4 drives the MEMORY READY line low for the duration of the mono time out. Prior to the time out of IC4, the selected PROM devices respond to the address data and select command applied to it and the addressed byte of data is placed on the 8 DO lines. Shortly after MEMORY READY goes high, the processor outputs a negative pulse on the MSTROBE— line. This pulse is buffered and enables the DO lines to the I/O Bus DATA— lines.

Sheets 2 and 3 show the chip select decoders CS(N)—, as well as address, data, and chip select bussing to all 64 PROM devices.

Sheet 4 shows DO bus gated to the I/O Bus DATA— lines by MSTROBE— and BSEL.

7. Q1/LMC Disk Controller Board

7.1 Schematic Diagrams (004—51012)

7.2 Timing Diagrams, Circuit Description and Theory of Operation

7.2.1 Address Decoding

The Disk Controller uses four I/O addresses for data transfer and disk control. These addresses are selected and decoded (sheet 1 of schematic) by 7486 exclusive OR gates, 7408 AND gates, and 7420 NAND gates. The decoded addresses, ADR0S through ADR3S, are ANDed with the filtered STROBE— line to generate STB0 through STB3. These signals initiate I/O transfer, control, and status transfer.

7.2.2 Input Selection

IC77 and IC80 (sheet 2) multiplex data and status for an IN instruction. Data is selected for a STB0 and status is selected for a STB1. The data lines FDB0 through FDB7 are output from the FIFO buffer. This will be discussed later.

7.2.3 Data Lines

When the data bus is transferring data to the controller, the data is buffered by 7404 gates and appears DOA0 through DOA7. This data represents the contents of the A-register for an OUT instruction.

7.2.4 Track Stepping

If the disk track is to be stepped down a STB must be generated by an OUT instruction with DOA1 set (sheet 3). IC59—8 will cause the STEP BUSY one-shot to fire, indicating a busy status bit. The STP one-shot will also be fired causing a pulse on the STEP— line to the disk drive.

If the disk track is to be stepped up STB1 with DOA0 must be generated. STEP BUSY one-shot operates as before, but now the DIR— line to the disk drive must be set up before the STEP— pulse is generated. F1 is a free running clock.

7.2.5 Drive Select

To select one out of four disk drives, a STB1 is needed with either a DOA2, DOA3, DOA4, or DOA5. This will set the appropriate latch on IC94 (sheet 3), and set line SEL1—, SEL2—, SEL3—, or SEL4— to the disk drives. If DOA6 is set, all select lines will be reset.

The PRST— reset line is filtered and ORed with the programmed reset of DOA7 and STB1T to generate a master reset for the disk system, MRST—.

7.2.6 Disk Ready

The S.D. Ready line, generated at IC47—2, is a status line indicating that a disk is loaded in the selected drive. The status is reset under any of the following conditions:

- ** A master reset, MRST—
- ** A new drive is selected by SELSTB—
- ** The retriggeable one-shot, IC23—13, is not retrigged by index pulses. That is, the diskette was removed.

7.2.7 Controller Clocks

The disk controller clocks are generated by a 5MHz crystal oscillator (sheet 4), and a divide-by-10 counter with the outputs decoded.

Also shown on sheet 4 of the schematic is the generation of the HL signal. HL becomes true 20 mSec. after a selected disk becomes Ready. This allows for head loading time, and no read or write operations can be initiated if HL is not true.

7.2.8 FIFO

A First-In-First-Out (FIFO) storage buffer is used to buffer data to and from the disk drive. This is necessary as the programmed data transfer is halted for approximately 35 uSec. during the time when the dynamic memory is refreshing. The schematic of this FIFO is shown on sheet 5.

The storage elements are four 74170 registers arranged to store four 16 bit bytes. Sixteen bits are needed as both data and clock patterns are significant. There is a clock bit associated with each data bit. IC42 and IC43 store clock patterns.

IC31 is a two flip-flop counter which points to the next input location of the storage elements.

IC21 is a two flip-flop counter which points to the next output location of the storage elements. The output counter "chases" the input counter.

Both counters start at zero. If the two counters are equal, there is no data in the FIFO. FDORDY indicates the non-equal state of the counters. The exclusive-or at IC22-6 and IC22-3 test this condition. If FDORDY is high, there is a byte available in the storage elements.

The FIFO is full if the input counter has caught up to the output counter. That is, the input counter is 1 count less than the output counter. This condition is detected by IC22-11, IC22-8, and IC10-3. FDIRDY being true means that there is room in the storage elements for an additional byte.

The WR signal indicates that the controller is writing data on the disk. The BYTE RDY status therefore means that the Processor can load another byte into the FIFO.

If the controller is in the Read mode (WR—), and an Address Mark has been detected (AM DET), the BYTE RDY indicates that the Processor can read a byte from the FIFO.

In the write mode the FDI0 through FDI7 lines contain the data that will be written on the disk. The FCI0 through FCI7 lines contain the clock pattern, if the clock pattern is not all ones.

An output STB0 generates a pulse at IC7-8. This pulse loads the storage elements with FDS and increments the input counter. Because the IC20-5 flip-flop is reset, FDS can come through and generate FCS—. This line loads a clock pattern. Since CEN is low, the clock pattern will be all ones. (IC41 and IC44 inhibit the FCI0 through FCI7 lines.)

If the clock pattern is to be other than all ones, an output STB3 generates a pulse at IC7-6. FCLK is generated, CEN is set (enabling FCI0 through FCI7), and FCS— loads the storage elements. IC20-6 is now low so that when the data is loaded FCS— will not be generated again.

In the read mode the FIFO works in a similar manner. BR7 is a bit counter which is used to strobe clocks and data. FCLK and FCS— are generated, loading the clock pattern. The 1 uSec.one-shot, IC24—5, is used to generate FDS and load the data.

7.2.9 Address Mark Detection

A detailed description of the circuit on sheets 6 and 7 of the schematic is contained in "Shugart Associates IBM Compatibility Manual," Pub. No. 5A0006. The following are some signal definitions.

EXCLK — Extra clock is generated when a clock bit is missing.

AMSTART — This is set when the beginning of an address mark is detected.

AMDET — This is set when an address mark has been detected. It is used to enable the bit ring counter.

BR7 — This pulse occurs on the last bit of a data byte after an address mark has been detected. It is used to generate a byte strobe to the FIFO.

SHIFT DATA REG — This is used as a clock input to the data shift register.

SHIFT CLOCK REG — This is used as a clock input to the clock pattern shift register.

DATA BIT — This is the data input for the data shift register in a read mode. It is gated with WRCLK in the write mode to generate WRITE DATA— for the disk drive.

CLOCK BIT — This is the data input for the clock pattern shift register in a read mode. It is gated with WRCLK in the write mode to generate WRITE DATA—.

WRITE DATA— — This line to the disk drive contains clock and data information and is generated by the circuitry on sheet 6. It is always running, although the data is ignored by the drive if Write Gate is not set.

BC8 — This is a pulse which is used to strobe data into the shift registers during a write mode.

7.2.10 FIFO Input

On sheet 8 of the schematic, four 74157's are used to select the FIFO data input. The input is from the I/O bus for a write mode, and from shift registers for a read mode.

7.2.11 Start Read

To start a read operation a STB2 is needed with DOA0 set. The generated SR— signal initializes the read circuitry.

7.2.12 Write Start

To start a write operation a STB2 is needed. If DOA6 is set a whole track can be written. If DOA7 is set a single sector can be written

IC4-5 and IC1-5 are used to synchronize the write gate with the index pulse when a track is to be written.

IC30 and I29 are used to determine the time when the write gate will be turned on, based on the location of the address mark of the sector header.

WRST- terminates a write operation when the FIFO is empty.

The controller is put in write track mode when STB2 is anded with DOA6 high, setting WTR. STB2 resets FIFO address counters and BC8 counter with BC8 going high. IC1 pin 6 goes low on second index pulse after WTR. WG goes high and WRCLK sets WRITE GATE FF IC96. With BC8 and WG high, next SWRCK gives a WRLD-Pulse at IC5 pin 8. WRLD has 4 functions.

1. Sets BC8 low
2. Generates FOSTB which enables FIFO outputs and increments FIFO output address counter IC21.
3. Enables parallel loading of FIFO data into data and clock registers IC53 to IC56.
4. Resets IC4 pin 2 HI. CLKBEN gated with WG and SWRCK thru IC27 pin 8 generates the SHIFT DATA REG and SHIFT CLOCK REG pulses necessary for parallel load and shifting of these registers.

WRCLK and SWRCK have a 2 USEC period as shown on sheet 4 of schematics. CLKBEN therefore has a 4 USEC period generating SHIFT DATA REG and SHIFT CLOCK REG pushing data out on WRITE. DATA- line via DATA BIT and CLOCK BIT from IC16 pins 8 and 12. Coincident with loading and shifting of data, WRITE GATE enables WRCLK to IC34 input, a divide by 16 counter. IC34 pin 11 will go low after 32 USEC setting BC8 high. The following SWRCK will again generate WRLD-repeating the same cycle. When the processor has finished inputting to FIFO and last byte is taken from FIFO, FDORDY- goes high indicating FIFO is empty. If FDORDY- is still high when next WRLD occurs they are anded through IC5 generating WRST- and resetting all write mode CKTS. Minimum time for write track mode is 167 MSEC, index period of the disk drive.

8. Q1/LMC Keyboard Interface

8.1 Schematic Diagrams (004—51001)

Pages 22 to 25 missing in the original

10. Q1/LMC Printer Interface

10.1 Schematic Diagrams (004—51004)

Pages 27 to 28 missing in the original

11. Q1 POWER SYSTEMS

11.1 Wiring Diagrams and Schematics

LMC Power Wiring Diagram 006-53015

Console Power Wiring Diagram 006-53016 - missing

Plus and Minus 12 V Power Source 004-51013-1

30 V Power Supply 006-51007

250 VDC Power Supply 004-51017

H.V. Power Supply.

11.2 Functional Description

The Power System provides the computer with eight D.C. voltages necessary for system operation. The main power supply is a switching regulated power supply, requiring 115/230 VAC 50/60 Hz input for LMC systems and 28 VDC for Field Unit systems. The input and output voltage for these supplies are tabulated in Figure 11.2-1.

<u>Description</u>		<u>LMC Systems</u> <u>(Supply P/N 4135Q1)</u>	<u>Field Unit Systems</u> <u>(Supply P/N 40152Q1)</u>
<u>Input</u>		115/230 VAC 6/3A 50/60 Hz	28 VDC 20A
Output	1	+5 VDC	+5 V
	2	+15 VDC	+15 VDC
	3	-15 VDC	-15 VDC
	4	+24 V	250 VAC

Figure 11.2-1 SWITCHING POWER SUPPLY VOLTAGES

The fourth output differs from LMC to Field Unit systems. In LMC systems this output furnishes 24 VDC at 2 A to the Disk Drives. In Field Unit systems, this output provides 250 VAC at 200 mA to a 250 MDC power supply.

In either system, the plus and minus 15 VDC outputs are applied to two series regulators providing plus and minus 12 VDC. The minus 15 VDC is also applied to a minus 9 VDC power source.

Two 90,000 uF capacitors on the plus and minus 15 volt DC outputs provide additional current to the printer during peak periods.

Primary power is switched by an On-Off circuit breaker and is distributed to the system cooling fans, the main power supply, and, in LMC systems, to the Disk Drives.

11.3 Circuit Description

11.3.1 Plus and Minus 12 V Power Source

Sheet 004-51013-1 contains the plus and minus 12 V series regulators. CR2 and Q1 form the plus 12 V power source. CR5 and Q2 form the minus 12 V power source. Both regulators are capable of delivering 3 A, each, continuously, within the regulation limits of the ± 15 V sources.

11.3.2 Minus 9 V Power Source

Sheet 004-51013-2 contains the minus 9 V series regulator. CR5 and Q2 form the minus 9 V power source. The regulator is capable of delivering 3 A continuously, within the regulation limits of the -15 V source.

11.3.3 Plus 250 V Power Source

Sheet 004-51017 contains the plus 250 V series regulator and the rectifying bridge. CR3, CR6, and Q1 form the plus 250 V power source. The regulator is capable of delivering over 100 mA DC.

LMC Power System Resistance Test with 8 Line Display Console
Use Simpson 260.

<u>Output</u>	<u>Typical Vom Condition</u>	
	<u>- Lead on Ground</u>	<u>+ Lead on Ground</u>
+5V	7 ohms	2 ohms
-15V Allow ample charge time	12	400
+15V Allow ample charge time	400	12
+24V	50	8
-12V Allow ample charge time	25	1.2K
+12V Allow ample charge time	1.2K	25
+30V	15K	4.7K
-250V	6.2K	3 meg.