DESCRIPTION:
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Revision History:

jrp 6-1-83 Added 6 more procciks for better buffering. One will be used for I/O boards exclusively.
THIS PROGRAM REPLACES AN EARLIER VERSION "MEMC1".
CORRECTS ERRORS IN THE DEFINITION OF A, B, DO, D1
THEY SHOULD BE SET TO THE VALUE REQUIRED BY THE
NEXT STATE, NOT THE CURRENT STATE.

THIS PROGRAM DEFINES THE STATE TRANSITIONS FOR
THE DISPLAY MODULE MEMORY CONTROLLER. THE MEMORY
CONTROLLER DETERMINES A SEQUENCE OF MEMORY HALF-
CYCLES TO ALLOW IMAGE MEMORY TO BE ACCESSED FOR
SCREEN REFRESHES, DYNAMIC RAM REFRESHERS AND BIT
SLICE DRAWING PROCESSOR READS AND WRITES. THERE
ARE FIVE INPUT SIGNALS: 1. HSYNCH IS THE HORIZ-
\ONTAL SYNCH SIGNAL. IT IS USED TO INITIATE REFRESH CYCLES.
NOTE THAT BLOL CANNOT BE USED FOR THIS PURPOSE BECAUSE
STAYS LOW DURING VERTICAL BLANKING AND WOULD PREVENT PROPER
REFRESH. 2. BLOL IS THE COMPOSITE BLANKING SIGNAL
WHICH INDICATES WHEN THE CONTROLLER SHOULD ALLOW REFRESH
AND PROCESSOR ACCESS CYCLES. 3. RCYLH INDICATES WHEN
A FULL RAS-CAS CYCLE IS REQUIRED DURING PROCESSOR ACCESS.
IT IS USED BY THE CONTROLLER TO SELECT RAS-CAS OR PAGE MODE
CYCLES. 4. NOZOOMH INDICATES THAT A 1X HORIZONTAL ZOOM
FACTOR IS IN USE. THIS ALLOWS THE CONTROLLER TO ELIMINATE
DYNAMIC RAM REFRESH CYCLES AND THUS IMPROVES DRAWING SPEED.
5. PWRUPL INDICATES THAT A POWERUP INIT HAS OCCURRED.
UNTIL THIS SIGNAL IS CLEARED BY THE DRAWING PROCESSOR, THE
MEMORY CONTROLLER ALLOWS ONLY PROCESSOR RAS-CAS CYCLES TO
AVOID HANGING OR ERRATIC OPERATION AT POWERUP BEFORE THE
CRT CONTROLLER HAS BEEN INITIALIZED AND HSYNCH AND BLOL
MAY BE INVALID.

INPUT SIGNAL DEFINITIONS
HSYNCH, BLOL, RCYLH, NOZMH, PWRUPL

OUTPUT SIGNAL DEFINITIONS
A, B, DO, D1

STATE DEFINITIONS
SCRAS, SCCAS, PRASO, PCASO, RRASO, RCKO, RRAS1, &
RCK1, RRAS2, RCK2, PRAS1, PCAS1, PCAS2, WAIT, &
Puras, PUCAS

BEGIN WITH STATE 0 TRANSITIONS
SCRAS ALWAYS FOLLOWED BY SCCAS
SCRAS, PWRUPL=X> SCCAS, A=1, B=0, D1=0, DO=0

SCCAS STATE HAS THREE POSSIBLE TRANSITIONS:
TO SCRAS, TO PRASO AND TO PURAS
SCCAS, BLOL=1, PWRUPL=1> SCRAS, A=1, B=0, D1=1, DO=1
SCCAS, BLOL=0, PWRUPL=1> PRASO, A=0, B=0, D1=1, DO=1
SCCAS, PWRUPL=0> PURAS, A=0, B=0, D1=1, DO=1

PRASO HAS TWO POSSIBLE TRANSITIONS: ONE TO PCAS0 AND
ONE TO PCAS2
PRASO, BLOL=0> PCASO, A=0, B=0, D1=0, DO=0
PRASO, BLOL=1> PCAS2, A=0, B=0, D1=0, DO=0
\texttt{PCASO} has six transitions: to \texttt{PCAS2}, to \texttt{WAIT}, to \texttt{RRASO}, to \texttt{PURAS}, to \texttt{PRASO} and to itself. Note that there are actually two separate conditions for the transitions to itself and to \texttt{PRASO}: one for \texttt{HSYNCH=0} and one for \texttt{NOZM=1}. With \texttt{HSYNCH=0}:

- \texttt{PCASO, BLOL=1, RCYLH=0, PWRUPL=1} > \texttt{PCAS2, A=0, B=0, D1=0, DO=1}
- \texttt{PCASO, BLOL=1, RCYLH=1, PWRUPL=1} > \texttt{WAIT, A=0, B=0, D1=1, DO=0}
- \texttt{PCASO, BLOL=0, HSYNCH=1, NOZM=0, PWRUPL=1} > \texttt{RRASO, A=1, B=1, D1=1, DO=1}
- \texttt{PCASO, PWRUPL=0} > \texttt{PURAS, A=0, B=0, D1=1, DO=1}
- \texttt{PCASO, BLOL=0, HSYNCH=1, RCYLH=1, PWRUPL=1} > \texttt{PRASO, A=0, B=0, D1=1, DO=1}
- \texttt{PCASO, BLOL=0, HSYNCH=0, RCYLH=1, PWRUPL=1} > \texttt{PCASO, A=0, B=0, D1=0, DO=1}

\texttt{PCASO} has five transitions: one to \texttt{PRAS1}, one to itself, one to \texttt{PRASO}, one to \texttt{PCASO} and one to \texttt{PURAS}.

\texttt{PCAS1} has five transitions: one to \texttt{PRAS1}, one to itself, one to \texttt{PRASO}, one to \texttt{PCASO} and one to \texttt{PURAS}.

\texttt{RRASO} has an unconditional transition to \texttt{RCKO}.

\texttt{RCKO} has two transitions: one to \texttt{RRAS1} and one to \texttt{PURAS}.

\texttt{RCK1} has two transitions: one to \texttt{RRAS2} and one to \texttt{PURAS}.

\texttt{RRAS2} has an unconditional transition to \texttt{RCK2}.

\texttt{RCK2} has two transitions: one to \texttt{PRAS1} and one to \texttt{PURAS}.

\texttt{PRAS1} has an unconditional transition to \texttt{PCAS1}.
PCAS1, PWRUPL=1, HSYNCH=1, RCYLH=0 > PCAS1, A=0, B=0, & D1=0, D0=1

PCAS1, PWRUPL=1, HSYNCH=0, RCYLH=1 > PRASO, A=0, B=0, & D1=1, D0=1

PCAS1, PWRUPL=1, HSYNCH=0, RCYLH=0 > PCASO, A=0, B=0, & D1=0, D0=1

PCAS1, PWRUPL=0 > PURAS, A=0, B=0, D1=1, D0=1

; PCAS2 HAS TWO TRANSITIONS: ONE TO SCRAS AND ONE TO PURAS
PCAS2, PWRUPL=1 > SCRAS, A=1, B=0, D1=1, D0=1

PCAS2, PWRUPL=0 > PURAS, A=0, B=0, D1=1, D0=1

; WAIT HAS TWO TRANSITIONS: ONE TO SCRAS AND ONE TO PURAS
WAIT, PWRUPL=1 > SCRAS, A=1, B=0, D1=1, D0=1

WAIT, PWRUPL=0 > PURAS, A=0, B=0, D1=1, D0=1

; PURAS HAS ONE TRANSITION: TO PUCAS
PURAS, PWRUPL=X > PUCAS, A=0, B=0, D1=0, D0=0

; PUCAS HAS TWO TRANSITIONS: ONE TO PURAS AND ONE TO PRASO
PUCAS, PWRUPL=0 > PURAS, A=0, B=0, D1=1, D0=1

PUCAS, PWRUPL=1 > PRASO, A=0, B=0, D1=1, D0=1

; END OF PROGRAM
DESCRIPTION:
This PAL decodes branch instructions from the microcode into the appropriate control signals for the 2909-11 microsequencer. The three BS inputs provide eight instructions:

0        fourway branch using R
1        fourway branch using C
2        conditional branch using R
3        conditional branch using C
4        conditional branch to subroutine using R
5        conditional branch to subroutine using C
6        return from subroutine

IF(VCC) /SO = BS1 * /BS2 * CC1 * /CC1S4 + BS1 * /BS2 * /CC1 * CC1S4 + /BS1 * BS2 * CC1 * /CC1S4 + BS1 * BS2

IF(VCC) /S1 = /BS0 + BS1 * CC1 * /CC1S4 + BS1 * /CC1 * CC1S4 + BS2 * CC1 * /CC1S4 + BS2 * /CC1 * CC1S4

IF(VCC) /FE = /BS1 * BS2 * CC1 * CC1S4 + /BS1 * BS2 * /CC1 * CC1S4 + BS0 * BS1 * BS2 * CC1 * CC1S4 + BS0 * BS1 * BS2 * /CC1 * CC1S4

IF(VCC) /ORO = BS1 + BS2 + CC1 * /CC1S4 + /CC1 * CC1S4

IF(VCC) /OR1 = BS1 + BS2 + CC2 * /CC2S2 + /CC2 * CC2S2

IF(VCC) /CN = /BS0 * BS0

IF(VCC) /ST = CC1S3