iSBX™ 270
VIDEO DISPLAY TERMINAL CONTROLLER BOARD HARDWARE REFERENCE MANUAL

Order Number: 143444-001

intel®

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PREFACE

This manual provides general information, installation instructions, programming information, principles of operation, and service information for the iSBX 270 Multimodule Video Display Terminal Controller board. Additional information is available in the following documents.

- *Intel iSBX Bus Specification*, Order Number: 142686.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBX 270 Multimodule Video Display Terminal Controller (VDTC) is a member of Intel's growing line of expansion boards designed to augment the iSBC microcomputers. The iSBX 270 VDTC board provides a video interface for iSBC boards that support the iSBX Multimodule concept.

A keyboard interface is also provided that accepts up to eight parallel data lines and one strobe. In addition a light pen may be connected to the module, allowing the user to read the coordinates of the light pen target.

1-2. DESCRIPTION

The Multimodule board, shown in Figure 1-1, is designed to plug into any iSBC microcomputer that contains an iSBX connector.

The iSBX 270 Multimodule Video Display Terminal Controller (VDTC) is a double wide Multimodule expansion board that will interface to most black and white and RGB color display monitors. The interface provides a display of 25 lines of 80 characters each. Each character is formed on a 7 X 9 matrix (default). When driving a black and white display monitor, two intensity levels may be displayed. When driving a color display monitor, up to eight colors (seven colors and black) may be displayed.

The board is controlled by an 8041A/8741A Universal Peripheral interface 8-bit microcomputer (UPI). The UPI contains the firmware that controls all onboard functions. In addition the UPI is the interface to the iSBX bus. The iSBX 270 VDTC board contains 4K bytes of memory which is used for storing all characters that are to be displayed.

1-3. EQUIPMENT SUPPLIED

The following is supplied with the iSBX 270 VDTC board.

Schematic Diagram

Three nylon spacers
Six nylon screws

1-4. COMPATIBLE EQUIPMENT

The iSBX 270 VDTC Multimodule board must be used with a microcomputer that includes an iSBX bus connecter.

Signals from the Multimodule board are accesible to the video terminal and keyboard by means of the keyboard interface connector (J1) and the CRT interface connector (J2).

1-5. SPECIFICATIONS

Specifications for the iSBX 270 VDTC board are listed in Table 1-1.

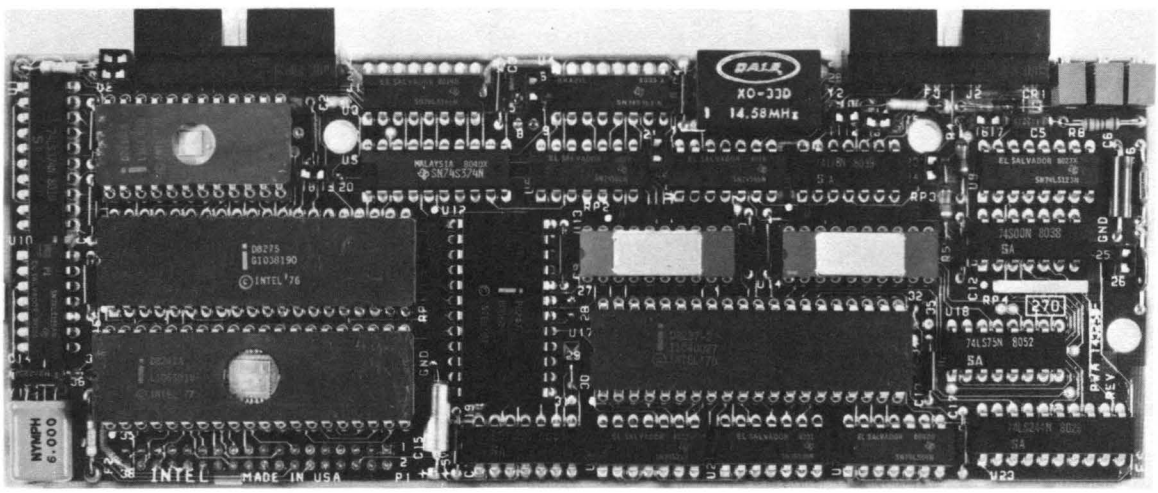


Figure 1-1. iSBX 270™ VDTC Board

Table 1-1. Specifications

PHYSICAL CHARACTERISTCS:	
Width:	7.82 cm (3.08 inches)
Length:	19.05 cm (7.50 inches)
Height:	2.05 cm (0.80 inches) iSBX 270 VDTC board only. 2.90 cm (1.14 inches) iSBX 270 VDTC board and iSBC base board.
Weight:	175.54 gm (6.19 oz.)
ENVIRONMENTAL CHARACTERISTICS:	
Operating Temperature:	0° to 55° C (32° to 131° F).
Relative Humidity:	To 95% without condensation.
POWER REQUIREMENTS:	
V_{CC} = +5 ± 5%	
V_{CC} = 1.3 A	

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBX 270 VDTC board. These instructions include unpacking and inspection; installation considerations such as physical dimensions, power requirements, cooling, and mounting requirements; jumper configurations; ac and dc characteristics; connector assignments; and installation procedures.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment contact the Intel Product Service HOTLINE to obtain a return authorization number and further instructions (see section 5-2). A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

2-3. INSTALLATION CONSIDERATIONS

The iSBX 270 VDTC board is designed to mount on an iSBC board that contains a Multimodule connector. Installation considerations such as power, cooling, mounting and physical size requirements, are outlined in the following paragraphs.

CAUTION

Remove power from the system before inserting or removing iSBC or iSBX microcomputer boards into/from a cardcage. Failure to do so could result in damage to the boards.

Do not remove or install board cables with power applied. Removing or installing cables with power applied may cause the iSBX 270 fuses to blow. Fuses are not covered under factory warranty.

2-4. POWER REQUIREMENTS

The board requires +5V (±0.25V) at 1.3 A maximum for operation. There is also +5V, +12V, and -12V routed to the keyboard and CRT interface connectors. ny requirements for these supplies must be added to those of the iSBX VDTC board. The current limit for the +5V, +12V, and -12V is 500 mA per supply per connector. The total of all supply currents from the base board must not exceed 3 amps. All the voltages for the iSBX VDTC board are supplied by the base board.

2-5. COOLING REQUIREMENTS

The iSBX 270 VDTC board dissipates 96 gram-calories/minute (0.39 BTU/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F).

2-6. MOUNTING REQUIREMENTS

Figure 2-1 shows the iSBX bus connector and stand-off locations. The Multimodule boards will mount onto any iSBC microcomputer containing an iSBX bus connector and the required stand-off holes. The mounting hardware supplied as part of the Multimodule board includes:

a. 6 nylon screws, 1/4 inch x 6/32, separate from board.

b. 3 nylon stand-offs, 1/2 inch x 6/32, separate from the board.

c. 36-pin connector P1, factory-installed onto the board.

NOTE

The Multimodule board, when installed onto a host microcomputer, occupies an additional card slot adjacent to the component side of the host microcomputer in an iSBC 604/614 cardcage.

2-7. PHYSICAL DIMENSIONS

Physical dimensions of the iSBX 270 VDTC board are as follows:

Figure 2-1 shows the physical dimensions and Figure 2-2 shows clearances for an iSBX 270 VDTC board mounted on a host iSBC microcomputer. The dimensions shown in Figure 2-2 are maximum heights.

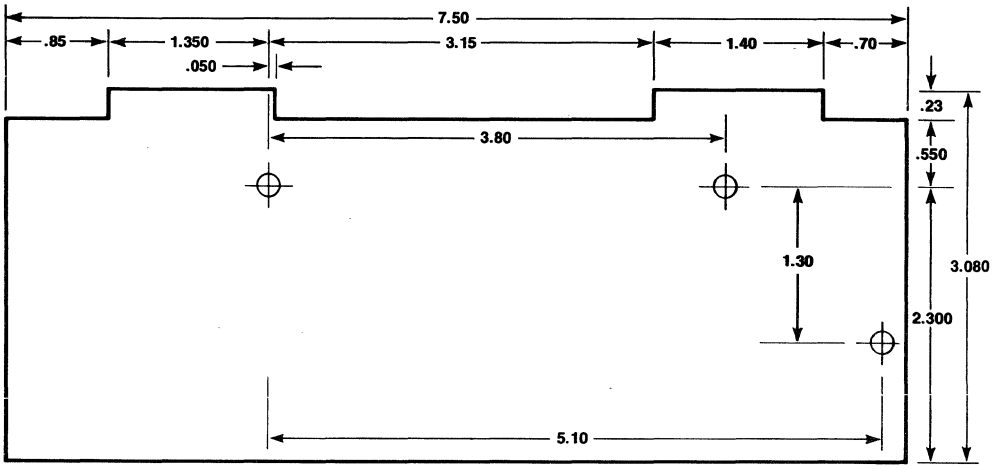


Figure 2-1. Board Dimensions (Inches)

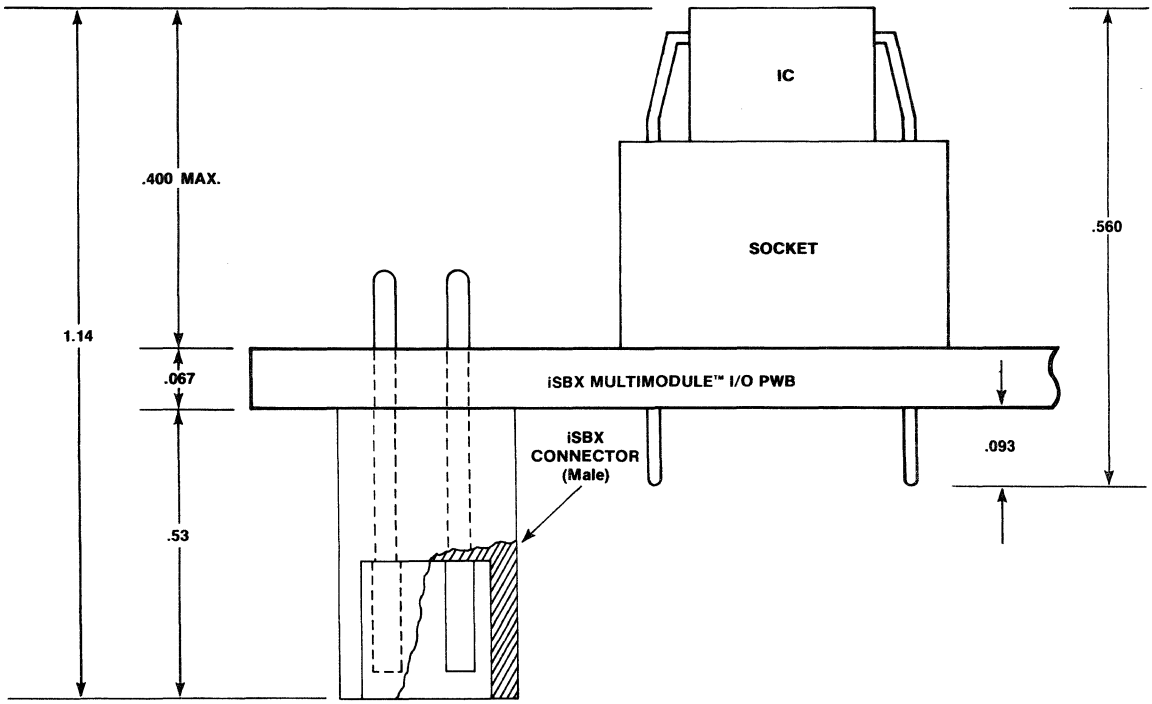


Figure 2-2. Mounting Clearances (Inches)

2-8. iSBX BUS INTERFACE

Connector P1 interfaces all data and control signals between the host iSBC microcomputer and the iSBX 270 VDTC board. The signals found on each pin of the P1 connector are listed in Table 2-1 and descriptions of the signal functions are listed in Table 2-2.

Table 2-1. Connector P1 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+12	+12 Volts	2	-12V	-12 Volts
3	GND	Signal Ground	4	+5V	+5 Volts
5	RESET	Reset	6	MCLK	M Clock
7	—	Reserved	8	MPST/	iSBX Multimodule Board Present
9	—	Reserved	10	—	Reserved
11	MA0	M Address 0	12	MINTR1	M Interrupt 1
13	IOWRT/	I/O Write Command	14	MINTR0	M Interrupt 0
15	IORD/	I/O Read Command	16	—	Reserved
17	GND	Signal Ground	18	+5V	+5 Volts
19	MD7	MDATA BIT 7	20	—	Reserved
21	MD6	MDATA BIT 6	22	MCS0/	M Chip Select 0
23	MD5	MDATA BIT 5	24	—	Reserved
25	MD4	MDATA BIT 4	26	—	Reserved
27	MD3	MDATA BIT 3	28	OPT1	Option 1
29	MD2	MDATA BIT 2	30	OPT0	Option 0
31	MD1	MDATA BIT 1	32	MDACK/	M DMA Acknowledge
33	MD0	MDATA BIT 0	34	MDRQT	M DMA Request
35	GND	Signal Ground	36	+5V	+5 Volts

All undefined pins are reserved.

Table 2-2. Connector P1 Signal Functions

SIGNAL	DESCRIPTION
IORD/	*I/O Read.* Indicates that the address lines are valid and that the selected Multimodule should perform a read operation.
IOWRT/	*I/O Write.* Indicates that the address lines and data are valid and that the selected Multimodule board should perform a write operation.
MA0	*Address.* This address line, in conjunction with the chip select line, establishes the I/O port address being accessed.
MCLK	*Clock.* Timing signal from the base board (10MHz+0, -10%).
MCS0/	*Chip Select.* This chip select line, in conjunction with the address line line, establishes the I/O port address being accessed.
MD0-MD7	*Data.* These 8 bidirectional data lines transmit and receive data to or from the Multimodule port. BD7 is the most-significant bit.
MDACK/	*DMA Acknowledge.* Signal from the base board DMA device acknowledging that the requested DMA cycle has been granted.
MDRQT	*DMA Request.* These two lines transmit interrupt requests to the base board.
MINTR0-MINTR1	*Interrupt Request.* These two lines transmit interrupt requests to the base board.
MPST/	*iSBX Multimodule Board Present.* Indicates to the base board that the iSBX Multimodule board is attached.
OPT0-OPT1	*Option Lines.* These two lines are for any unique requirements that the user may have for communication between the base board and the Multimodule board. On the iSBX 270 board, these lines are routed to the J1 connector.
RESET	*Reset.* Resets the Multimodule board to a known internal state.

The dc characteristics of the iSBX Bus interface signals are provided in Table 2-3. The ac characteristics of the iSBX Bus interface signals are provided in Table 2-4. The timing diagrams for the ac characteristics are shown in figures 2-3 through Figure 2-6.

Table 2-3. iSBX Bus Interface DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
IORD/,	V_{IL}	Input Low Voltage			0.8	C
IOWRT/	V_{IH}	Input High Voltage		2.0		V
	V_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-1.0	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.4V		100	uA
	*C_L	Capacitive Load			40	pF
MA0	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-0.5	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.4V		70	uA
	*C_L	Capacitive Load			40	pF
MCLK	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-2.4	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.4 V		100	uA
	*C_L	Capacitive Load			40	pF
MCS0/	V_{IL}	Input Low Voltage		0.8	V	
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-4.0	mA
	I_{IL}	Input Current at HIGH V	V_{IN} = 2.4V		100	uA
	*C_L	Capacitive Load			40	pF
MD0-MD7	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -200 uA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-0.5	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.4V		70	uA
	*C_L	Capacitive Load Input			40	pF
	*C_L	Capacitive Load Output			130	pF
MDACK/	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-1.0	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.4V		100	uA
	*C_L	Capacitive Load			40	pF
MDRQT	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -50 uA	2.4		V
	*C_L	Capacitive Load			40	pF

Table 2-3. iSBX Bus Interface DC Characteristics (Continued)

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
MINTR0- MINTR1	V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -100 uA	2.4		V
	*C_L	Capacitive Load			40	pF
OPT0- OPT1**	V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.5	V
	V_{OH}	Output High Voltage	I_{OH} = -50 uA	2.4		V
	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	V_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-2.0	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.4V		100	uA
	*C_L	Capacitive Load			40	pF
RESET	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at LOW V	V_{IN} = 0.4V		-2.1	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.4V		40	pF

*Capacitive load values are approximations.
**These are recommended specifications. These lines are user defined, so it is the responsibility of the user to ensure adequate drive.

Table 2-4. iSBX Bus Interface AC Characteristics

Parameter	Min (ns)	Max (ns)	Description
t_1	50		Address stable before read
t_2	30		Address stable after read
t_3	300		Read pulse width
t_4	0	250	Data valid from read
t_5	0	150	Data float after read
t_6		*	Time between reads or writes
t_7	25		CS stable before command
t_8	30		CS stable after command
t_9	50 Msec		Power up reset pulse width
t_{10}	50		Address stable before write
t_{11}	30		Address stable after write
t_{12}	300		Write pulse width
t_{13}	250		Data valid to write
t_{14}	30		Data valid after write
t_{15}	100	110	MCLK cycle
t_{16}	35	65	MCLK width
t_{18}	10 Msec		Reset pulse width
t_{20}	100		DACK set up to I/O command
t_{21}	30		DACK hold
t_{22}		200	Command to RQT removed

* The status register must be checked for IBF low before writing a new command or data byte. The OBF bit of the status register will go active when new data is available to be read.

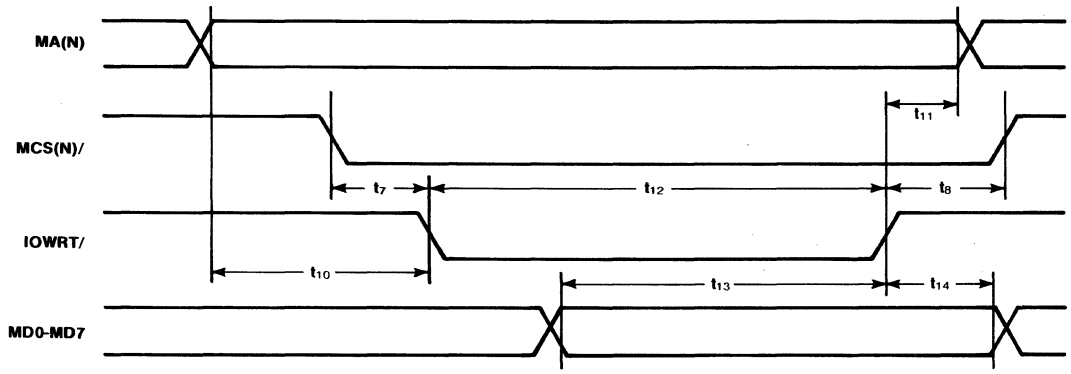


Figure 2-3. iSBX Multimodule Board I/O Write Timing

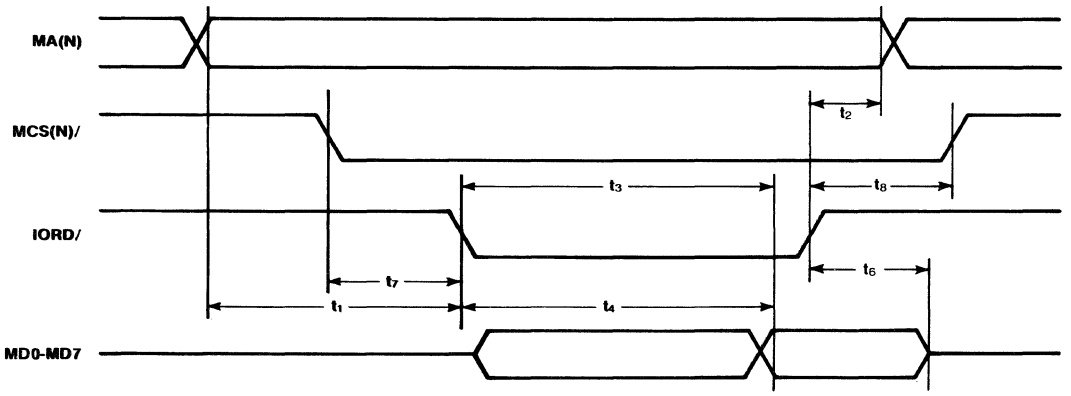


Figure 2-4. iSBX Multimodule Board I/O Read Timing

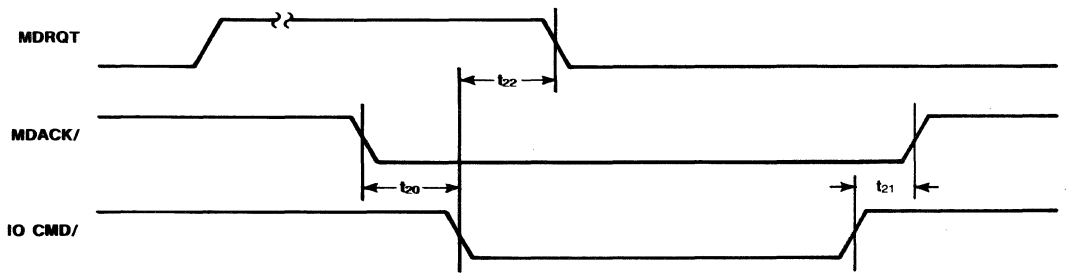


Figure 2-5. iSBX Multimodule Board I/O DMA Timing

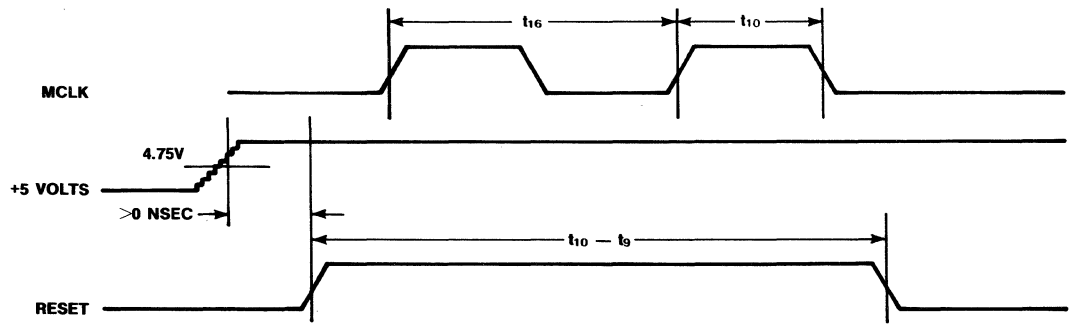


Figure 2-6. iSBX Multimodule Board I/O Reset Timing

2-9. KEYBOARD/LIGHT PEN INTERFACE

Connector J1 on the iSBX 270 VDTC board interfaces all data and control signals between the Multimodule board and the keyboard/light pen. The signals found on each pin of the J1 connector are listed in Table 2-5 and descriptions of the signal functions are listed in Table 2-6.

The dc characteristics of the keyboard/light pen interface signals are provided in Table 2-7. The ac characteristics of the keyboard/light pen interface signals are provided in Table 2-8. The timing diagram for the ac characteristics is shown in Figure 2-7.

2-10. CRT INTERFACE

Connector J2 on the iSBX 270 VDTC board interfaces all data and control signals between the Multimodule board and the CRT. The signals found on each pin of the J2 connector are listed in Table 2-9 and descriptions of the signal functions are listed in Table 2-10.

The dc characteristics of the CRT interface signals are provided in Table 2-11. The ac characteristics of the CRT interface signals are provided in Table 2-12. The timing diagram for the ac characteristics is shown in Figure 2-8.

2-11. JUMPER CONFIGURATION

The iSBX 270 VDTC board contains thirty-seven jumper pads labeled E1 through E37. The functions of each are outlined in the following paragraphs. Table 2-13 lists the jumpers in numerical sequence and identifies the factory default configuration.

2-12. 50/60 HERTZ OPTION. When jumper E27-E28 is not installed, 60 hertz operation is selected. This is the factory default condition utilizing a 14.58 MHz crystal and resulting in 25 character rows, each with 10 raster lines, and a vertical retrace period of 2 character rows.

Table 2-5. Connector J1 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	GND	+Signal Ground	2	+5V	+5 Volts
3	GND	Signal Ground	4	+5V	+5 Volts
5	GND	Signal Ground	6	LPEN	Light Pen Detected
7	GND	Signal Ground	8	BSTB/	Bell Strobe
9	GND	Signal Ground	10	KEYACK/	Keyboard Acknowledge
11	GND	Signal Ground	12	STROBE/	Keyboard Data Strobe
13	GND	Signal Ground	14	CNTL0	Control 0
15	KBRST/	Keyboard Reset	16	CNTL1	Control 1
17	B6	Keyboard Bit 6	18	B4	Keyboard Bit 4
19	B2	Keyboard Bit 2	20	B0	Keyboard Bit 0
21	B7	Keyboard Bit 7	22	B5	Keyboard Bit 5
23	B3	Keyboard Bit 3	24	+12V	+12 Volts
25	-12V	-12 Volts	26	B1	Keyboard Bit 1

Table 2-6. Connector J1 Signal Functions

SIGNAL	DESCRIPTION
B0-B7	*Data.* Keyboard data from the keyboard to the iSBX Multimodule VDTC board. B7 is the most significant bit.
BSTB/	*Bell Strobe.* Signal to activate the external bell circuit.
CNTL0-CNTL1	*Optional Control Lines.* These two optional control lines are available for use by the user. These lines correspond to OPT0 and OPT1, respectively, on the iSBX Bus interface.
KBRST/	*Reset.* Resets the keyboard to a known internal state.
KEYACK	*Keyboard Acknowledge.* Indicates that the iSBX Multimodule VDTC board has accepted the previous keyboard data character from the keyboard latch.
LPEN	*Light Pen.* Indicates to the iSBX Multimodule VDTC board that a light pen pulse has been detected. Triggered on rising edge.
STROBE/	*Data Strobe.* Indicates that the data from the keyboard is valid.

Table 2-7. Keyboard/Light Pen Interface DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
B0-B7	V_{IL}	Input Low Voltage			0.8	V
	V_{IH}	Input High Voltage		2.0		V
	V_{IL}	Input Current at LOW V	V_{IN} = 0.8V		-0.4	mA
	I_{IH}	Input Current at HIGH V	V_{IN} = 2.7V		20	uA
	*C_L	Capacitive Load			40	pF
BSTB/, KEYACK/	V_{OL}	Output Low Voltage	I_{OL} = 4.5 mA			0.45 V
	V_{OH}	Output High Voltage	I_{OH} = 200 uA	2.4		V
	*C_L	Capacitive Load			40	pF
KBRST	V_{OL}	Output Low Voltage	I_{OL} = 2.5 mA		0.4	V
	V_{OH}	Output High Voltage	I_{OH} = -500 uA	4.0		V
	*C_L	Capacitive Load			40	pF
KPEN, STROBE	V_{IL}	Input Low Voltage		0.8	V	
	V_{IH}	Input High Voltage		2.0		V
	I_{IL}	Input Current at LOW V	V_{IN} = 0.8V		-1.5	mA
	I_{IL}	Input Current at HIGH V	V_{IN} = 2.7V		30	uA
	*C_L	Capacitive Load			40	pF

*Capacitive load values are approximations.

Table 2-8. Keyboard/Light Pen Interface AC Characteristics

Parameter	Min (ns)	Max (ns)	Description
t_1	20		Data setup to strobe
t_2	15		Data hold from strobe
t_3	500		Strobe pulse width
t_4	20 Msec		Strobe pulse separation
t_5	5 usec		Bell pulse width
t_6	5 usec		KEYACK pulse width
t_7	0		KEYACK to strobe setup
t_8		50	Light pen rise time
t_9	100		Light pen hold time
t_{10}	10 Msec		Keyboard reset pulse width

Table 2-9. Connector J2 Pin Assignments

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	TP1	Test Point	2	-12V	-12 Volts
3	TP2	Test Point	4	+5V	+5 Volts
5	TP3	Test Point	6	+5V	+5 Volts
7	GND	Signal Ground	8	+12V	+12 Volts
9	GND	Signal Ground	10	A VIDEO	
11	GND	Signal Ground	12	G VIDEO	
13	GND	Signal Ground	14	B VIDEO	
15	GND	Signal Ground	16	R VIDEO	
17	GND	Signal Ground	18	HSYNC	
19	GND	Signal Ground	20	GPA1	
21	GND	Signal Ground	22	HLGT	
23	GND	Signal Ground	24	VSYNC/	
25	GND	Signal Ground	26	GPA0	

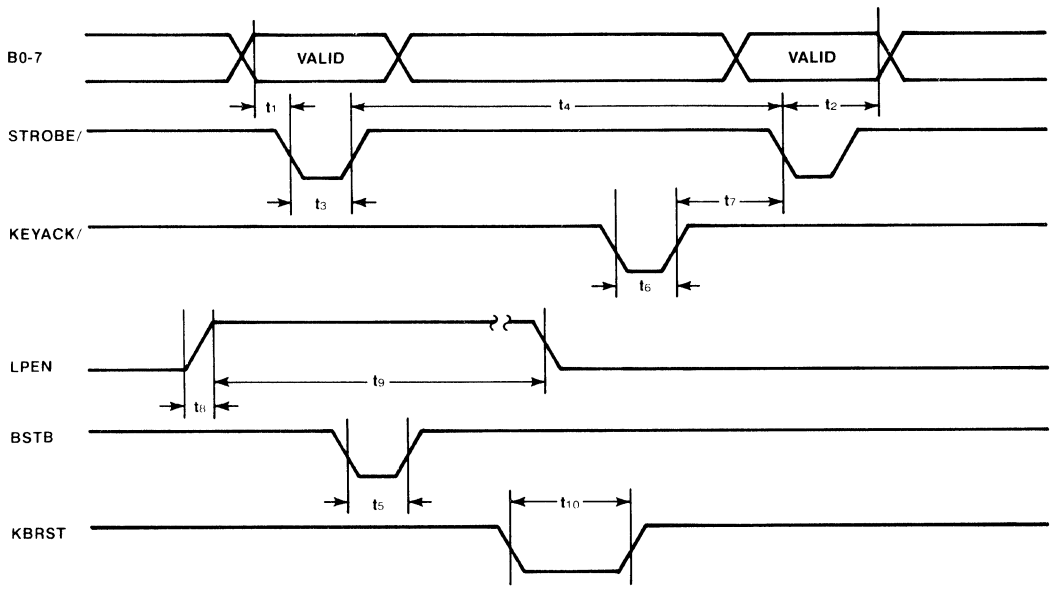


Figure 2-7. Keyboard/Light Pen Interface Timing

Table 2-10. Connector J2 Signal Functions

SIGNAL	DESCRIPTION
B VIDEO	*Blue Video.* This signal is the blue video gun driver signal.
G VIDEO	*Green Video.* This signal is the green video gun driver signal.
GPA0-GPA1	*General Purpose Attribute.* These signals indicate to the CRT that the general purpose attribute is active.
HLGT	*Highlight.* This signal indicates to the CRT that the highlight attribute is active.
HSYNC	*Horizontal Sync.* This signal synchronizes the horizontal retrace on the CRT.
R VIDEO	*Red Video.* This signal is the red video gun driver signal.
A VIDEO	*Adjustable Video.* The adjustable-contrast video signal that is fed to most black and white monitors.
VSYNC/	*Vertical Sync.* This signal synchronizes the vertical retrace on the CRT.

Table 2-11. CRT Interface DC Characteristics

Signals	Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
B VIDEO, G VIDEO, R VIDEO, HSYNC	V_{OL} V_{OH} *C_L	Output Low Voltage Output High Voltage Capacitive Load	I_{OL} = 48 mA I_{OH} = -13 mA	 2.4	0.4 40	V V pF
GPA0-, GPA1, HLGT, VSYNC/	V_{OL} V_{OH} *C_L	Output Low Voltage Output High Voltage Capacitive Load	I_{OL} = 17 mA I_{OH} = 6 mA	 2.4	0.5 40	V V pF
A VIDEO**	V_{OH} *C_L	Output High Voltage Capacitive Load	R_L = 120 ohms	0	3.0 40	V pF

*Capacitive load values are approximations.
**The high-level output voltage is adjustable over the range shown with the contrast trim pot.

Table 2-12. CRT Interface AC Characteristics

Parameter	Min (ns)	Max (ns)	Typ	Unit	Description	Notes
t_1			88	nS	Dot pulse width	1
			77	nS		2
			66	nS		3
			64	nS		4,5
t_2	4.5	23		uS	Horiz sync width	6
t_3	135	186	160	uS	Vert sync width	
t_4	11.33	11.35	11.34	MHz	Video dot rate	1
	12.95	12.97	12.96	MHz		2
	14.57	14.59	14.58	MHz		3
	15.65	15.69	15.67	MHz		4,5
		13.72		MHz		7
t_5	16.18	16.22	16.20	KHz	Horiz scan rate	1,2,3
	19.18	19.22	19.20	KHz		4,5

Notes:
1. Y2 = 11.34 MHz (5x7 dot matrix)
2. Y2 = 12.96 MHz (6x8 dot matrix)
3. Y2 = 14.58 MHz (7x9 dot matrix)
4. Y2 = 15.67 MHz (6x8 dot matrix)
5. For use with high resolution monitors
6. The horizontal sync pulse width is adjustable, over the range show, with the horizontal sync pulse width trim pot.
7. This is the highest allowable video rate.

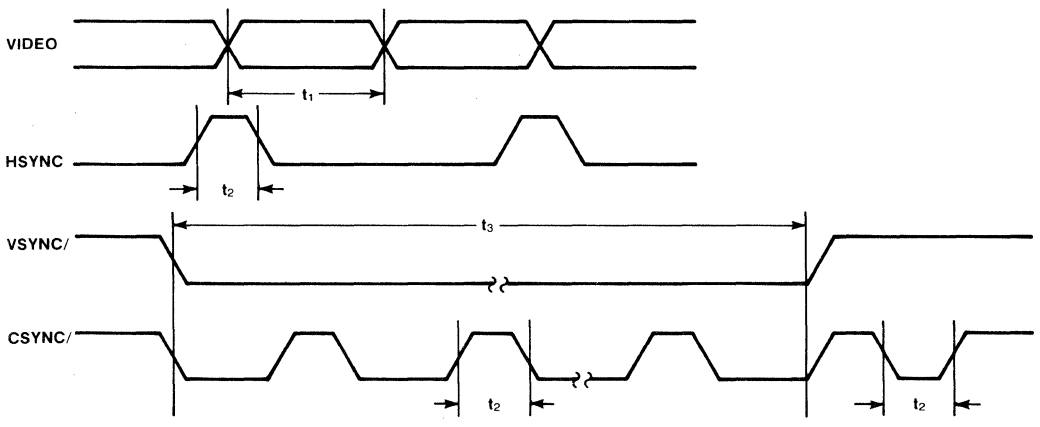


Figure 2-8. CRT Interface Timing

Table 2-13. Jumper Options

Jumper Installed	Function	Logic Ref.
E1-E2*, E3-E4*	Active low keyboard strobe	3ZC7
E1-E3, E2-E4	Active high keyboard strobe	3ZC7
E5-E7, E8-E9	Creates a 6 x 8 character matrix	3ZA7
E6-E7*	Creates a 7 x 9 character matrix	3ZA7
E8-E9	Creates a 5 x 7 character matrix	3ZA7
E10-E11	Creates an active low combined sync	3ZA2
E11-E12*	Causes HSYNC to be active high	3ZA2
E11-E12 (Jumper out)	Causes HSYNC to be active low	3ZA2
E13-E14*	Causes VSYNC to be active low	3ZA4
E14-E15	Causes VSYNC to be active high	3ZA4
E16-E17*, E23-E24*	Enables black and white with dual density	3ZB2
E18-E19*	For 2716 type character generator	3ZC5
E19-E20	For 2732A type charcter generator	3ZC5
E21-E22*	Enable black and white	3ZB4
E21-E22 (Jumper out)	Enable color	3ZB4
E25-E26*	Normal VSYNC	3ZA4
E25-E26 (Jumper out)	Extended VSYNC	3ZA4
E27-E28	50 hertz operation	2ZC6
E27-E28 (Jumper out)*	60 hertz operation	2ZC6

*Factory configuration.

When jumper E27-E28 is installed, 50 hertz operation is selected. This option will produce 25 character rows, each with 11 raster lines and a vertical retrace period of 4 character rows. The mode of operation (50 or 60 hertz) is sampled whenever the board is reset.

The polarity of the strobe signal from the keyboard may be selected by the user. The factory default includes jumpers at E1-E2 and E3-E4. This configuration will support active-low strobe signals (negative logic).

If an active-high strobe is to be used (positive logic), the jumpers must be changed to E1-E3 and E2-E4.

2-13. KEYBOARD STROBE SIGNAL POLARITY. The polarity of the strobe signal from the keyboard may be selected by the user. The factory default includes jumpers at E1-E2 and E3-E4. This configuration will support active-low strobe signals (negative logic).

If an active-high strobe is to be used (positive logic), the jumpers must be changed to E1-E3 and E2-E4.

2-14. KEYBOARD CONTROL LINES. Two control lines are connected to the OPT 0 and OPT 1 signals from the iSBX bus interface for visual or audio indicators on the keyboard. These lines are unbuffered and must be driven from a source on the host iSBC board.

Two jumper pins (E37 for Opt 0, E36 for Opt 1) are connected to the option lines to allow the user to pass signals on the iSBX 270 board down to the host processor board. For example, a 60 Hz interrupt signal which is synchronous with vertical retrace may be sent to the base board by connecting pin E14 to one of the option pins. The user would then wire the option pin on the base board into the interrupt controller.

2-15. OPTIONAL CHARACTER GENERATOR. When the factory supplied 2716-1 character generator is replaced by a user-supplied and programmed 2732A, jumper E18-E19 must be removed and jumper E19-E20 must be installed. The 2732A font is selected by placing the appropriate attribute code in the display memory preceeding the data to be displayed. When the 2732A character generator is used, GPA0 can no longer independently control the green video. This limits the output to four colors.

2-16. CLOCK GENERATOR. The iSBX 270 VDTC board will support three sizes of character blocks: 7 x 10 (for 5 x 7 characters); 8 x 10 (for 6 x 8 characters); or 9 x 10 (for 7 x 9 characters). In addition, the iSBX 270 VDTC board will support monitors with a standard 15.75 KHz horizontal rate or high resolution monitors with a 19.2 KHz horizontal rate. The required crystal frequencies and jumper configurations are shown in Table 2-14.

Table 2-14. Clock Generator Options

Char Block Size	Char Format	Jumper Connections	Horiz Rate	Y2 Crystal Frequency	Notes
7 X 10	5x7	E8-E9	16.2KHz	11.34MHz	2, 3
8 X 10	6x8	E5-E7, E8-E9	16.2KHz	12.96MHz	2, 3
8 X 10	6x8	E5-E7, E8-E9	19.2KHz	15.67MHz	2, 3, 4
9 X 10	7x9	E6-E7	16.2KHz	14.58MHz	1

NOTES:
1. Factory Default.
2. Replacement crystal user-supplied.
3. Also requires replacement of character generator PROM with a user-supplied and programmed PROM.
4. For use with high resolution monitors.

2-17. VIDEO OUTPUT SIGNAL. A variable contrast video signal (A video) is obtained with jumper E21-E22 (factory default), with the contrast adjustment provided onboard (R2). Two levels of intensity (highlight), are supplied by jumpers E16-E17 and E23-E24. This is the factory default and will interface directly with most OEM black-and-white display monitors. The difference between highlighted and normal characters may be adjusted with onboard potentiometer R1.

If RGB (red, green, blue) color operation is desired, jumpers E16-E17, E21-E22, and E23-E24 must be removed. This allows the video signal to be combined with attribute signals to create red, green, and blue video signals. No contrast adjustment is provided with this configuration.

2-18. HORIZONTAL SYNC. Horizontal sync (HYSNC) is normally active high with jumper E13-E14 installed. It may be inverted to active low by removing jumper E11-E12. An active low combined sync (VSYNC XORed with HSYNC) may be obtained by adding jumper E10-E11 (jumper E13-E14 must be installed). Combined sync must be used with RGB color display monitors.

The pulse width of the horizontal sync signal is variable from 4.5 μs to 23 μs with trim potentiometer R3.

2-19. VERTICAL SYNC. Vertical sync (VYSNC) is normally active low with jumper E13-E14 installed. It may be inverted to active high by removing jumper E13-E14 and adding jumper E14-E15. The vertical sync pulse width may be changed with jumper E25-E26. When this jumper is installed (factory default), the vertical sync pulse width will nominally be 160 μs (for use with standard monitors). When this jumper is removed, the vertical sync pulse width will be extended to approximatly 570 μs (for use with high resolution monitors).

2-20. MULTIMODULE INSTALLATION PROCEDURE

The iSBX 270 VDTC board mounts onto the host iSBC board (that has a Multimodule connector) as follows:

a. With the nylon 1/4 inch x 6/32 screws, secure the 1/2 inch plastic spacers (3) to the host iSBC board as shown in Figure 2-14.

CAUTION

Do not overtighten screws as damage to the board could result.

b. Locate pin 1 of the iSBX bus connector (P1) and align it with pin 1 of the Multimodule connector on the host iSBC board.

c. Align the Multimodule mounting holes with the spacers on the host iSBC board; reference Figure 2-1 for hole locations.

d. Gently press the two boards together until the connector seats.

e. Secure the Multimodule board to the top of the spacers with the remaining 1/2 inch x 6/32 screws.

NOTE

The placement of an installed Multimodule board and the host board connector number may vary according to the type of host iSBC board that is used.

2-21. CRT AND KEYBOARD INSTALLATION

The CRT is connected to the iSBX Multimodule board via a user supplied cable that connects to J2. The keyboard is connected to the iSBX Multimodule board via a user supplied cable that connects to J1. The make up of these cables depends on the manufacturer and type of CRT and keyboard attached. Appendix B lists the pinout and other cable information for some of the common CRTs and keyboards. Table 2-15 lists the part number and the manufacturer for some connectors that will attach to J1 and J2.

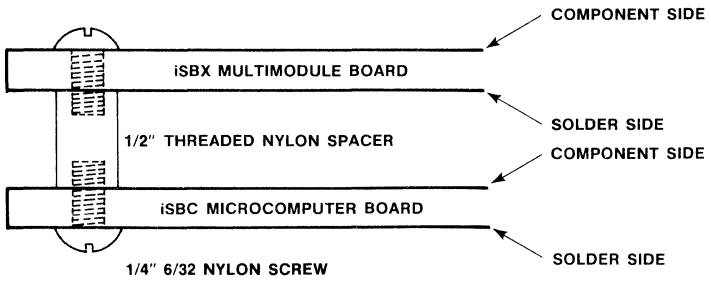


Figure 2-9. Mounting Technique

Table 2-15. CRT and Keyboard Connectors

Connector	No. of Pairs/ Pins	Connector Type	Vendor	Vendor Part No.
J1,J2	13/26	Wire Type	BERG	65043
J1,J2	13/26	Wire Type (Keyed)	BERG	65846-819
J1,J2	13/26	Flat-cable	BERG	65485-011
J1,J2	13/26	Flat-cable (Keyed)	BERG	65847-027
J1,J2	13/26	Flat Cable	3M	3399

NOTE:
It is recommended that the keyed connectors be used to prevent the connectors from being inserted upside down.

2-22. CABLING

The signals provided by the iSBX 270 VDTC board while in B & W mode are standard TTL signals. For optimum display quality, the cables for the video, VSYNC, and HSYNC signals should be twisted pairs (with ground) with an impedance of approximately 120 ohms. The video line should be terminated at the display monitor with a load of 120 ohms. The cable length should be limited to about 5 feet.

When operating in color mode, the cables should be 75 ohm coax and must be terminated with a 75 ohm load. Cable lengths of more than 15 feet have been used with no problems.

The Keyboard cable is non-critical, with either twisted pair or flat cable being satisfactory. However, due to the susceptibility of keyboards to electro static discharge (ESD), the user must ensure that the frame of the keyboard is properly grounded with a braided heavy-gauge cable back to the main system chassis. A shield on the keyboard signal cable is also advisable.

The Light Pen is also particularly susceptible to ESD, both from the user, and from the surface of the CRT screen. Again, the user should provide a heavy gauge ground to the case of the Light Pen, and the cables should be shielded.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter provides the programming information for the iSBX 270 VDTC board. All on-board functions are controlled by firmware contained in a factory-supplied UPI (8041A/8741A). Consequently, the programming description will be limited to the user interface via the iSBX bus. There are four types of operations that can be performed with the iSBX 270 VDTC board: Write Data, Write Command, Read Data and Read Status.

3-2. INITIALIZATION

On power-up or following a hardware or software Reset, the iSBX 270 VDTC board is configured for 25 rows of 80 characters each. The keyboard and light pen interfaces are disabled. The iSBX Bus DMA transfer and interrupt signals are also disabled. The entire screen is cleared to spaces, a blinking-underline cursor is placed in the upper left-hand corner (Home), and the iSBX 270 VDTC board will be placed in scroll mode (non-transparent attributes). Following this automatic initialization, data, commad, or status transfers may take place.

3-3. READ STATUS

The status of the iSBX 270 VDTC board may be read at any time to determine its state. This is done by performing an I/O Read to the status port (Base + 1) here. The following diagram defines the status byte.

MSB LSB

B	E	K	L	R	R	I	O

O = Output Buffer Full — When set to 1, indicates that data is available in the data port. This bit is cleared when the host processor reads the data port.

I = Input Buffer Full — When set to 1, indicates that the input buffer to the iSBX 270 VDTC board is full - that is, it has not yet been accepted by the board. The host processor should wait for a zero in this bit before writing another command or data byte to the board.

R = Reserved. When set to 1, Should be masked off by the user's program.

L = Light Pen Data Ready — When set to 1, indicates that a light pen hit has been detected and that the coordinates will be available on the Data port. This bit is reset at the completion of reading the light pen coordinates.

K = Keyboard Data Ready — When set to 1, indicates that a keyboard hit has been detected and that the data will be available on the Data port. This bit is reset at the completion of reading the keyboard data byte.

E = VDTC Error — When set to 1, indicates an error has occurred on the iSBX 270 VDTC board. The command Read Error Status should be given to obtain more detail. This bit is reset upon completion of the Read Error Status command.

B = VDTC Busy — When set to 1, indicates that the iSBX 270 VDTC board is in the process of executing a command and any data read or written will be interpreted as parameters. This bit is reset when the command is completed.

A special condition may occur with the O bit of the status word. Normally, the Output Buffer Full (OBF) bit will set in response to a command in which parameters must be read by the host processor. In this case, the B bit (VDTC Busy-command in progress) will also be set.

If either the Keyboard or Light Pen interfaces (or both) are enabled, a data byte will be written to the output buffer when a hit has been detected on either interface. This allows the generation of an interrupt on a Keyboard or Light Pen hit if interrupts are enabled. This sequence will be indicated with a O bit = 1 and a B bit = 0. When this condition is detected, the user should note which interface is ready (Keyboard or Light Pen) through the status bits, read the data port to clear the O bit and the interrupt, and obtain the interface data. Two interrupts will occur in the case of the Light Pen interface: one for the X coordinate and one for the Y coordinate. See paragraph 3-18 for details on interrupts.

3-4. WRITE DATA

All data is written to I/O address Base + 0 where Base is the base address for the module, as determine by the host board. After initialization, data may be displayed by simply writing to the data port. The display will begin in the home position and proceed left-to-right until the end of the line or a control code

is encountered. At the end of a line, an automatic carriage return/line feed will occur and the next character will be placed at the beginning of the following line. The internal memory and cursor position pointers are automatically incremented.

In addition to the normal upper and lower case alphanumeric characters, several graphic characters may be displayed by writing control codes which are otherwise unused by the iSBX 270 VDTC board. An even greater number of graphic characters may be obtained by proceeding certain control codes with a lead-in character. A lead-in character is also used to create Escape Sequences for special control applications. Table 3-1 summarizes the ASCII codes and displayed characters. Table 3-2 lists the graphic characters codes and shows the resulting graphic character. Table 3-3 lists the escape sequences for special control codes. Table 3-11 gives a routine to display all valid characters.

As shown in Table 3-1, there are a group of codes reserved for attributes which determine the characteristics of the display following the code, up to another attribute code or the end of the screen. The bit assignment of these attribute codes are as follows:

Table 3-1. ASCII Code Assignment

ASCII Data (HEX)	Displayed* Character	ASCII Data (HEX)	Displayed* Character	ASCII Data (HEX)	Displayed* Character
00	None	2C	,	58	X
01	GC1	2D	-	59	Y
02	GC2	2E	.	5A	Z
03	GC3	2F	/	5B	[
04	GC4	30	0	5C	\
05	GC5	31	1	5D	]
06	GC6	32	2	5E	^
07	Bell	33	3	5F	—
08	Back Space	34	4	60	`
09	GC9	35	5	61	a
0A	Line Feed	36	6	62	b
0B	GC11	37	7	63	c
0C	GC12	38	8	64	d
0D	Carriage Ret	39	9	65	e
0E	GC14	3A	:	66	f
0F	GC15	3B	;	67	g
10	Right Cursor	3C	<	68	h
11	GC lead-in	3D	=	69	i
12	GC18	3E	>	6A	j
13	GC19	3F	?	6B	k
14	GC20	40	@	6C	l
15	GC21	41	A	6D	m
16	GC22	42	B	6E	n
17	GC23	43	C	6F	o
18	GC24	44	D	70	p
19	GC25	45	E	71	q
1A	GC26	46	F	72	r
1B	Escape	47	G	73	s
1C	GC28	48	H	74	t
1D	GC29	49	I	75	u
1E	GC30	4A	J	76	v
1F	GC31	4B	K	77	w
20	Space (blank)	4C	L	78	x
21	!	4D	M	79	y
22	"	4E	N	7A	z
23	#	4F	O	7B	{
24	$	50	P	7C	!
25	%	51	Q	7D	}
26	&	52	R	7E	~
27	'	53	S	7F	GC32
28	(	54	T	80-BF	Attributes
29	)	55	U	C0-FF	Illegal**
2A	*	56	V		
2B	+	57	W		

NOTES:
*GC=Graphic Character (see Table 3-2)
**Any character in the range of C0-FF is illegal and MUST NOT be given to the iSBX 270 VDTC board or an undefined operation may occur.

Table 3-2. Graphic Characters

Graphics Character	Code	Display	Graphics Character	Code	Display
0*	00		17*	11	
1	01		18	12	
2	02		19	13	
3	03		20	14	
4	04		21	15	
5	05		22	16	
6	06		23	17	
7*	07		24	18	
8*	08		25	19	
9*	09		26	1A	
10*	0A		27*	1B	
11	0B		28	1C	
12	0C		29	1D	
13*	0D		30	1E	
14	0E		31	1F	
15	0F		32	7F	
16*	10				

NOTE:
All graphic character codes may be preceeded with a lead-in code of 11H. Those graphic characters marked with an asterisk require a lead-in of 11H.

Table 3-3. Escape Sequences

ASCII Code	Action
08H	Left Cursor
0BH	Down Cursor
0CH	Up Cursor
0FH	Clear to End of Line from current cursor position
10H	Right Cursor
12H	Home Cursor
18H	Clear to End of Screen from current cursor position

NOTE:
All codes require a lead-in of 1BH. For any other code following a lead-in of 1BH, the escape sequence is ignored.

MSB LSB

1	0	B5	B4	B3	B2	B1	B0

where:

B0: Highlight or Red Video off
B1: Blink
B2: GPA0, Green Video off, or select alternate character font (with user-supplied character generator PROM)
B3: GPA1 or Blue Video off
B4: Reverse Video
B5: Underline

NOTE

A one in any of the bit positions activates the indicated characteristic.

Note that while operating with a color monitor, the initial color displayed is white. As attribute bits are set, the colors are removed or turned off. If all color attribute bits are set, black (no display) will be selected. Table 3-4 lists the attribute codes for the various colors.

Some commands require parameters to be written to the iSBX 270 VDTC board through the data port (Base + 0). After all required parameters have been written, the iSBX 270 VDTC board will revert to accepting data for display via the data port.

Data written to the iSBX 270 VDTC board will be displayed in one of two modes: Scroll or Page.

Table 3-4. Attribute Codes for Color Selection

Color	Attribute
White	None or 80H
Red	8CH
Green	89H
Blue	85H
Magenta	84H
Cyan	81H
Yellow	88H
Black	8DH

NOTE:
Other attribute codes may be combined with the above codes by O Ring the appropriate bit pattern.

3-5. SCROLL MODE DISPLAY

This mode is normally used for simple alphanumeric character display. Characters will be displayed starting on the top line, proceeding left to right until a carriage return and/or line feed is received (or the end of the line is reached). The next line down will not be cleared, but data will be written over any existing characters (normally there will be none since the screen is cleared on power up). When the last character position in the bottom right-hand corner of the screen is filled or a line feed on the last line takes place, the entire display is moved up one line. The bottom line is cleared and the data on the top line is moved off the screen. All data entry after this will take place on the bottom line, with the display moving up one line for every line feed. Data previously scrolled off the screen is lost.

While in scroll mode, any attributes written to the display will take up one character position on the screen and be displayed as a blank. Thus if an alternate character font or different colors are to be displayed, each change will be separated by a space on the screen. Care must be exercised in specifing attributes that effect more than one line. As the display is scrolled, the attribute may be moved off the screen and its effect lost for subsequent lines.

3-6. PAGE MODE DISPLAY

If Page Mode is selected by means of the Set VDTC Mode command, data display will begin as in scroll mode; however when the last line is reached, the display will not move up. Characters written after the last character position on the screen will be lost. While in this mode, the iSBX 270 VDTC board will not clear any lines, therefore the user must pad any short lines with spaces to ensure that the previous data is cleared.

Attributes are invisible in this mode, allowing the user to change colors or character fonts without spaces being displayed on the screen. This mode is especially useful for displaying graphics. The maximum number of attributes per line is 16 and two attributes may not be adjacent. Because it is not practical for the iSBX 270 VDTC board to keep track of all the attributes on the screen, the iSBX 270 VDTC board may not properly move the cursor to the display position that the memory pointer is addressing. It is the responsibility of the user program on the host board to either disable the cursor or keep track of the memory pointer address to cursor position mapping. If this mapping is done, the Set Cursor Position command should be executed first to properly position the cursor, then the Set Memory Pointer command should be executed to point to the corresponding display memory address. Most of the cursor move commands (Left, Right, Up, Down, Carriage Return, Line Feed and Clear to End of Line) will not operate properly because of the invisible attributes and should not be used while in Page Mode. In order to ensure proper data entry, the user should send a Home Cursor escape sequence before writing a new page of data. Clear to End of Screen may be used to clear old data before displaying new data.

3-7. COMMANDS

Eight commands are implemented by the iSBX 270 VDTC board, which allow the user to modify the characteristics of the board and/or read special data. A command is initiated by writing the specified code to the Command port (Base + 1) followed by any required parameters transfered via the Data port (Base + 0). A command may be written at any time, even while the iSBX 270 VDTC board is expecting additional parameters from a previous command. The previous command will be terminated, the iSBX 270 VDTC board will return to command level, and the new command will be executed. Note that prematurely terminating a command may leave some internal registers in an undefined state.

In addition, two psuedo-commands (Read Keyboard Data and Read Light Pen Coordinates) will automatically be executed whenever the iSBX 270 VDTC board is at command level and a Keyboard or Light Pen hit is detected.

Table 3-5 summarizes the commands implemented by the iSBX 270 VDTC board while the following paragraphs describe the individual commands. All commands and parameters are in hexidecimal.

Table 3-5. iSBX 270 VDTC Board Commands

Code	Description	Parameters
00	NOP	0
01	Set CRT Screen Format	4
02	Set VDTC Mode	1
03	Set Cursor Position	2
04	Set Memory Pointer	2
05	Read Cursor Position	2
06	Read Error Status	1
07	Reset VDTC	0

NOTE:
Any code other than that listed above is reserved.

3-8. NOP

This command will terminate any command in progress and return the iSBX 270 VDTC board to command level, awaiting the next command. No parameters are required.

3-9. SET CRT SCREEN FORMAT

This command is used to change the screen composition from the normal 25 rows of 80 characters. The firmware will properly position the cursor for the new line and/or screen length if this command is given before any data is written to the screen. This command does not clear any data previously written to the screen. If the user programs transparent field attributes, the firmware will not be able to keep the cursor properly aligned with the memory pointer (see section 3-6.)

Four parameters must be written following this command; Table 3-6 describes these parameters. The default parameter values are:

Screen Composition Byte for default operation:
1: 01001111B (4FH)
2: 60Hz = 01011000B (58H), 50Hz = 11011000B (0D8H)
3: 60Hz = 01111001B (79H), 50Hz = 01111010B (7AH)
4: 01011001B (59H)

Table 3-6. CRT Screen Format Parameters

Parameter 1 = S H H H H H H H

where:
S = Functions
- 0 normal rows
- 1 spaced rows

H = Horizontal Characters Per Row
- 0 0 0 0 0 0 0 0 1
- 0 0 0 0 0 0 0 1 2
- 0 0 0 0 0 0 1 0 3
- .
- .
- .
- 1 0 0 1 1 1 1 1 80
- 1 0 1 0 0 0 0 0 undefined
- .
- .
- .
- 1 1 1 1 1 1 1 1 undefined

Parameter 2 = V V R R R R R R

where:
V = Vertical Retrace Row Count
- 0 0 1
- 0 1 2
- 1 0 3
- 1 1 4

R = Vertical Rows Per Frame
- 0 0 0 0 0 0 1
- 0 0 0 0 0 1 2
- 0 0 0 0 1 0 3
- .
- .
- .
- 1 1 1 1 1 1 64

Parameter 3 = U U U U L L L L

where:
U = Underline Placement
- 0 0 0 0 1
- 0 0 0 1 2
- 0 0 1 0 3
- .
- .
- .
- 1 1 1 1 16

L = Number of Lines Per Character Row
- 0 0 0 0 1
- 0 0 0 1 2
- 0 0 1 0 3
- .
- .
- .
- 1 1 1 1 16

Parameter 4 = M F C C Z Z Z Z

where:
M = Line Counter Mode
- 0 Mode 0 (non-offset)
- 1 Mode 1 (offset by 1 count)

F = Field Attribute Mode
- 0 transparent
- 1 non-transparent

C = Cursor Format
- 0 0 blinking reverse video block
- 0 1 blinking underline
- 1 0 non-blinking reverse video block
- 1 1 non-blinking underline

Z = Horizontal Retrace Count
- 0 0 0 0 2
- 0 0 0 1 4
- 0 0 1 0 6
- .
- .
- .
- 1 1 1 1 32

NOTE:
If the most significant bit of parameter 3 is a 1, the top and bottom lines will be blanked.

If the screen Parameters are changed, the user must insure that the master crystal Y2's frequency is correct to produce the desired horizontal scan rate and vertical frame rate.

When using a high resolution monitor the following parameter values should be specified immediately following power up. These values will yield 30 rows of 80 characters, 10 lines per row (11 for 50 Hz), and 2 Horizontal rows for Vertical Retrace (4 for 50 Hz). The user must also change Y2 to a 15.67 MHz crystal, set the dot matrix size to 8 x 10 and provide a character generator PROM with a 6 x 8 matrix size. The resulting horizontal scan rate is 19.2 KHz.

Screen Composition Byte for high resolution monitor:

1: 01001111B (4FH)
2: 60Hz = 01011101B (5DH), 50Hz = 11011101B (0DDH)
3: 60Hz = 01111001B (79H), 50Hz = 01111010B (7AH)
4: 01011010B (5AH)

3-10. SET VDTC MODE

This command specifies the operating mode of the iSBX 270 VDTC. One parameter must be written to the data port following this command.

MSB LSB

C	P	I	O	R	D	L	K

where:

K = Keyboard Enable
  0 = Keyboard Disabled
  1 = Keyboard Enabled

L = Light Pen Enable
  0 = Light Pen Disabled
  1 = Light Pen Enabled

D = DMA Enable (across iSBX Bus Interface)
  0 = Normal transfer mode
  1 = DMA Mode

R = Reserved

O = Output Buffer Full Interrupt Enable
  0 = Interrupt Disabled
  1 = Interrupt Enabled

I = Input Buffer Empty Interrupt Enable
  0 = Interrupt Disabled
  1 = Interrupt Enabled

P = Page Mode
  0 = Scroll Mode
  1 = Page Mode

C = Cursor Disable
  0 = Cursor Visible
  1 = No Cursor

3-11. SET CURSOR POSITION

This command is used to set the cursor position on the screen. In addition, the memory pointer is moved to the corresponding address, as specified in the formula in the following paragraph. Two parameters must be written to the data port.

1 - Cursor X position
2 - Cursor Y position

The Home position is 0, 0; the 2nd character on the first line is 1, 0, etc. Specifing a cursor position beyond the limits of the screen will yield undefined results. The memory pointer is updated by the formula: MP=Y * CL+X, where MP is the memory pointer; CL is the number of characters per line; and X and Y are as specified previously. If Page mode is selected, this formula may yield an incorrect memory address.

3-12. SET MEMORY POINTER

This command is used to set the internal Screen Refresh Memory pointer to a specified value. Since the RAM size is 4K, the memory pointer may take on values from 000H to 0FFFH. Two parameters must be written to the data port; the first is the Low Byte of the pointer, the second is the High Byte.

This command does not change the value of the cursor position pointer and thus is useful for operation in Page mode. The user program can position the cursor at the correct point with the Set Cursor Position command and then move the memory pointer to the correct address.

3-13. READ CURSOR POSITION

This command is used to read the X, Y coordinates of the cursor (Home being 0, 0). The two parameters that must be read from the data port following this command indicate the X and then the Y coordinates.

3-14. READ ERROR STATUS

Once it has been determined by a status read that an iSBX 270 VDTC board error has occurred, this command may be used to obtain additional information about the error. The one parameter read from the data port is defined as follows

MSB LSB

I	R	U	O	L	K	C	R

R = Reserved

C = Checksum Incorrect — during initialization, the iSBX 270 VDTC board performs a checksum on all internal code to verify program integrity. If an improper checksum is detected, this bit is set. The 8041A/8741A should be replaced.

K = Keyboard Buffer Overflow — indicates that a second keyboard data byte was received from the keyboard interface before the first byte was read by the host processor. The second byte is lost.

L = Light Pen Buffer Overflow — indicates that a second light pen hit was received before the coordinates of the first hit were read by the host processor. The coordinates of the second hit are lost.

O = CRT FIFO Overrun — indicates that the attribute buffer in the CRT controller has overflowed. Caused by more than 16 attributes in a character line while in page mode.

U = CRT DMA Underrun — indicates that the CRT controller chip did not receive DMA service when required. The display is blanked for the remainder of the frame.

I = CRT Improper Command — indicates that the CRT controller chip received an improper command byte sequence from the 8041A/8741A.

All error bits including the VDTC Error bit in the status word are reset when this command is completed.

3-15. RESET VDTC

This command causes the iSBX 270 VDTC firmware to re-initialize the iSBX 270 VDTC board just as though a power-up or hardware reset had occurred.

3-16. READ KEYBOARD DATA

This psuedo-command is automatically executed when a keyboard hit is detected. Several conditions must exist for this command to be invoked: the iSBX 270 VDTC board must be at command level (no command in progress); the Keyboard interface must be enabled; and a Keyboard hit must have occured. When this command is invoked, the Keyboard Data Ready flag in the Status word will be set first, then the Keyboard data will be placed in the output buffer. The placement of data in the output buffer will cause the OBF (Output Buffer Full) flag to be set, indicating that data is ready. If interrupts are enabled, an OBF interrupt will also be generated.

3-17. READ LIGHT PEN COORDINATES

This psuedo-command functions like the read keyboard data command. The following conditions must exist for this command to be invoked: the iSBX 270 VDTC board must be at command level; the light pen interface must be enabled; and a light pen hit must have occured. This command will set the light pen data ready flag in the status word, then place the X coordinate of the light pen hit in the output buffer. This will set the OBF flag and generate an OBF interrupt, if enabled. Once the host processor has read the X coordinate, the Y coordinate will be placed in the output buffer and the OBF flag will again be set.

The host processor must read both bytes before executing another command. When the second byte has been read, the light pen data ready and the OBF flags will be reset. The coordinates read will be in error by several character positions due to internal and external delays. The user software must correct the X co-ordinate by an empirically-determined constant.

Note that both the light pen and keyboard interfaces may be enabled. If both interfaces receive a hit, the firmware will pass the light pen hit to the user first, followed by the keyboard hit.

3-18. INTERRUPTS

Two interrupts may be generated by the iSBX 270 VDTC board to the host processor via the iSBX bus interface. An IBE (Input Buffer Empty, MINTR1) interrupt is generated whenever the board is ready to accept a new data or command byte. This interrupt signal is reset whenever a byte is written to the board. An OBF (Output Buffer Full, MINTR0) interrupt is generated whenever the board has a data byte ready for the host processor to read. This normally occurs when a read-type command is being executed by the iSBX 270 VDTC board and parameters are available. The OBF interrupt is cleared by a read of the data port. The OBF interrupt may also be generated by a keyboard or light pen hit.

Both the IBE and OBF interrupts have enable bits associated with them. These are initialized to 0 (interrupts disabled) but may be modified with the Set VDTC Mode command. When the interrupts are enabled, the OBF interrupt will reflect the state of the OBF bit in the VDTC status word; the IBE interrupt will be the complement of the IBF bit in the iSBX 270 VDTC board status word.

3-19. DMA OPERATION

Data may be transferred to the iSBX 270 VDTC board over the iSBX bus interface by a DMA controller on the host processor if DMA mode has been enabled by the Set VDTC Mode command. DMA transfers will take place one byte at a time and only data may be transferred (no commands). Note that the transfer direction must be from the host processor to the VDTC. If a DMA Transfer has been selected, the MDRQT (DMA Request) line will go active (High) whenever the iSBX 270 VDTC board is ready to accept a new data byte. When MDACK/ /(DMA Acknowledge) is asserted from the host board (active low) the iSBX 270 VDTC iSBX bus interface will be enabled and the data port selected. An I/O write signal from the host will write the data and clear the MDRQT signal.

3-20. RECOMMENDED PROGRAMMING PROCEDURES

For ease of illustration in the following paragraphs, the iSBX 270 VDTC board commands may be broken down into two types: Read-type and Write-type.

The Read-type commands are those commands which result in the host board reading information. These commands are: Read Cursor Position, Read Error Status, Read Keyboard Data, and Read Light Pen Co-ordinates.

The Write-type commands are those commands which require the host board to write parameters to the iSBX 270 VDTC board. For simplicity, the commands which require no parameters are also included in this group. The Write-type commands are: NOP, Set CRT Screen Format, Set VDTC Mode, Set Cursor Position, Set Memory Pointer, and Reset VDTC.

A command may be written to the iSBX 270 VDTC board anytime the input buffer is empty (indicated by the IBF flag = 0); however, the command will not be acted upon immediately if a read-type command is in progress. Since the read keyboard and read light pen commands are automatically invoked and since the keyboard and light pen hits are asynchronous to the iSBX 270 VDTC board and host board, it is possible to write a command to the iSBX 270 VDTC board while one of these two commands is executing, without the knowledge of the host board program. Therefore, the host board routine which issues the new command must be prepared to handle the results of a previous command. Figures 3-1 through 3-3 show flowcharts for the recommended handling of writing commands.

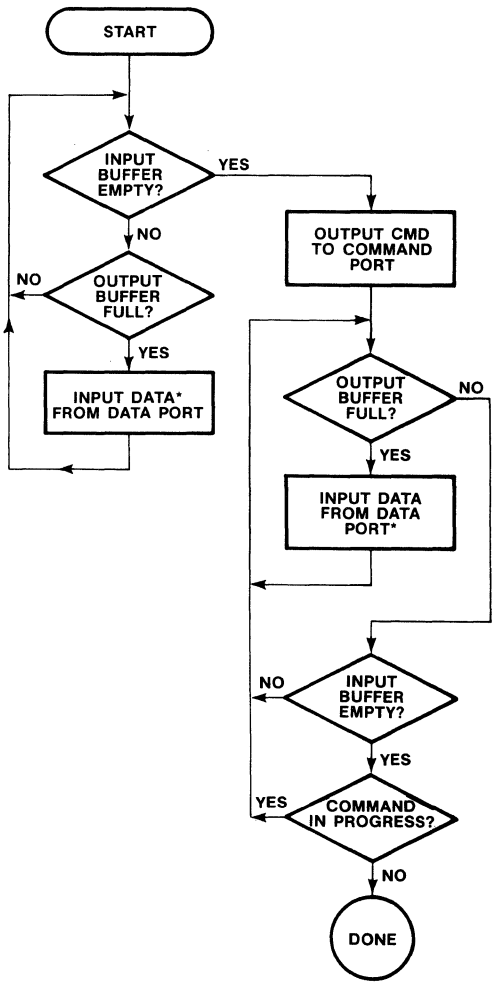
If a command is issued while a Write-type command is in progress, the current command will be aborted immediately. This may result in some memory locations containing a mixture of old and new parameters. Therefore it is not recommended to intentionally abort a Write-type command, except to issue a software Reset.

3-21. PROGRAMMING EXAMPLES

Figure 3-4 is a flow chart of a program to read and display the keyboard and light pen inputs. The main loop program shown in Figure 3-4 calls four subroutines. The first subroutine called is the keyboard hit (figure 3-5). This subroutine checks for an input from the keyboard. If there is no input from the keyboard, control is returned to the main loop program. If an input from the keyboard is detected, the subroutine loads the data into the FIFO and updates the FIFO pointer then returns to main loop. The second subroutine called is the light pen hit (figure 3-6). This subroutine checks for an input from the light pen. If there is no input from the light pen, control is returned to the main loop program. If an input from the light pen is detected, the subroutine loads the X coordinate (adjusted for propogation delays) into the FIFO and updates the FIFO pointer then the Y coordinate is loaded into the next location of the FIFO and the FIFO pointer is again updated and control is returned to main loop.

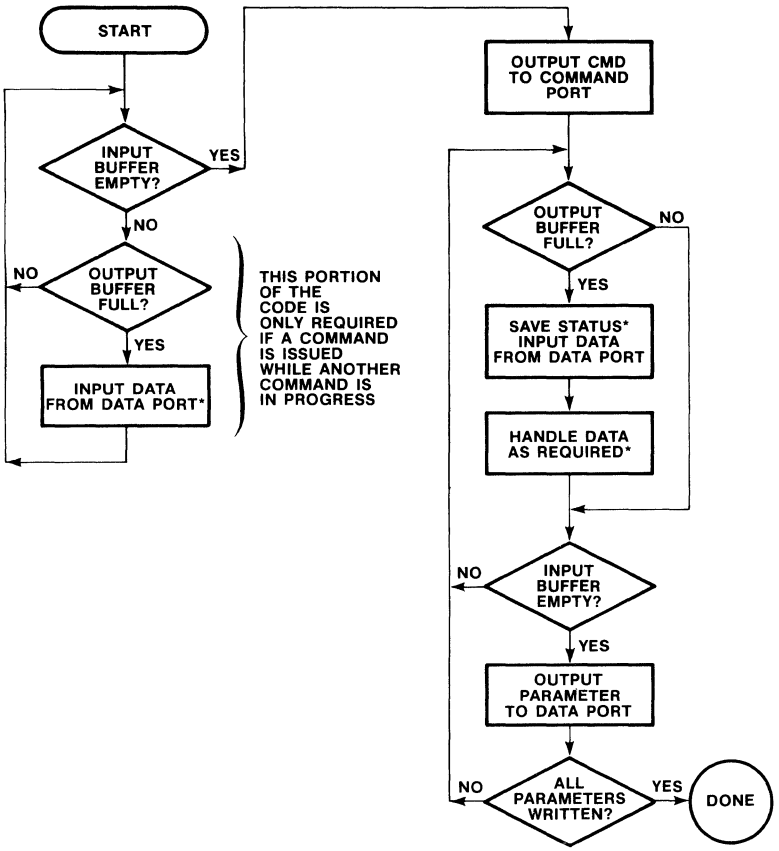
The next two subroutines take the data from a display data FIFO and display it. The flow chart for displaying data information is shown in Figure 3-7.

The program listings for each of the flow charts are shown following it's flow chart (table 3-7 through 3-10).



NOTES:
*The user may discard this data, or the status register may be checked to indicate if the data is from the keyboard or light pen.

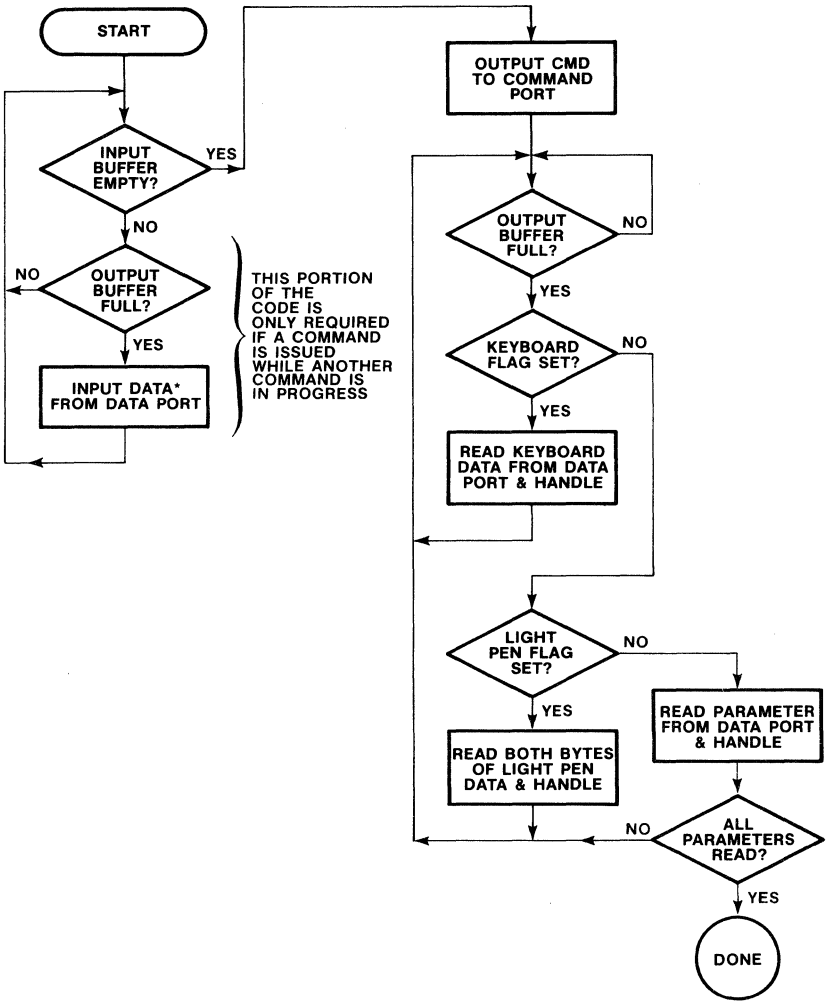
Figure 3-1. Recommended Procedure For Issuing a VDTC Reset or NOP Command



NOTES:

*The user may discard this data, or the status register may be checked to indicate if the data is from the keyboard, light pen, or a result of a previous command (if the data was not from the keyboard or light pen).

Figure 3-2. Recommended Procedure For Issuing a Set Format, Set Mode, Set Cursor, or Set Address Command



NOTES:

*The user may discard this data, or the status register may be checked to indicate if the data is from the keyboard or light pen.

Figure 3-3. Recommended Procedure For Issuing a Read Cursor or Read Error Status Command

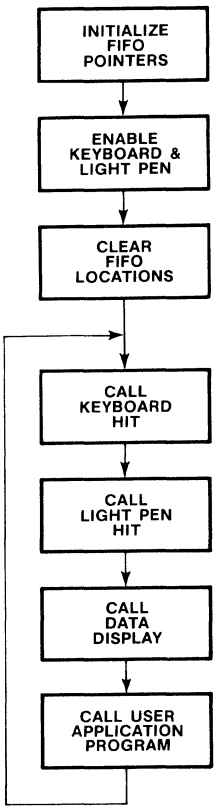


Figure 3-4. Flow Chart Of Main Loop Program

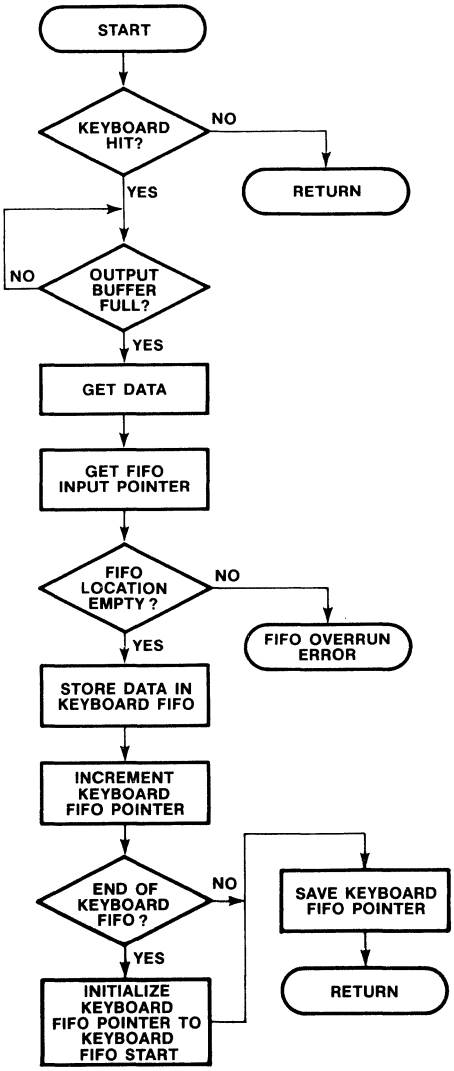


Figure 3-5. Flow Chart of Keyboard Hit Subroutine

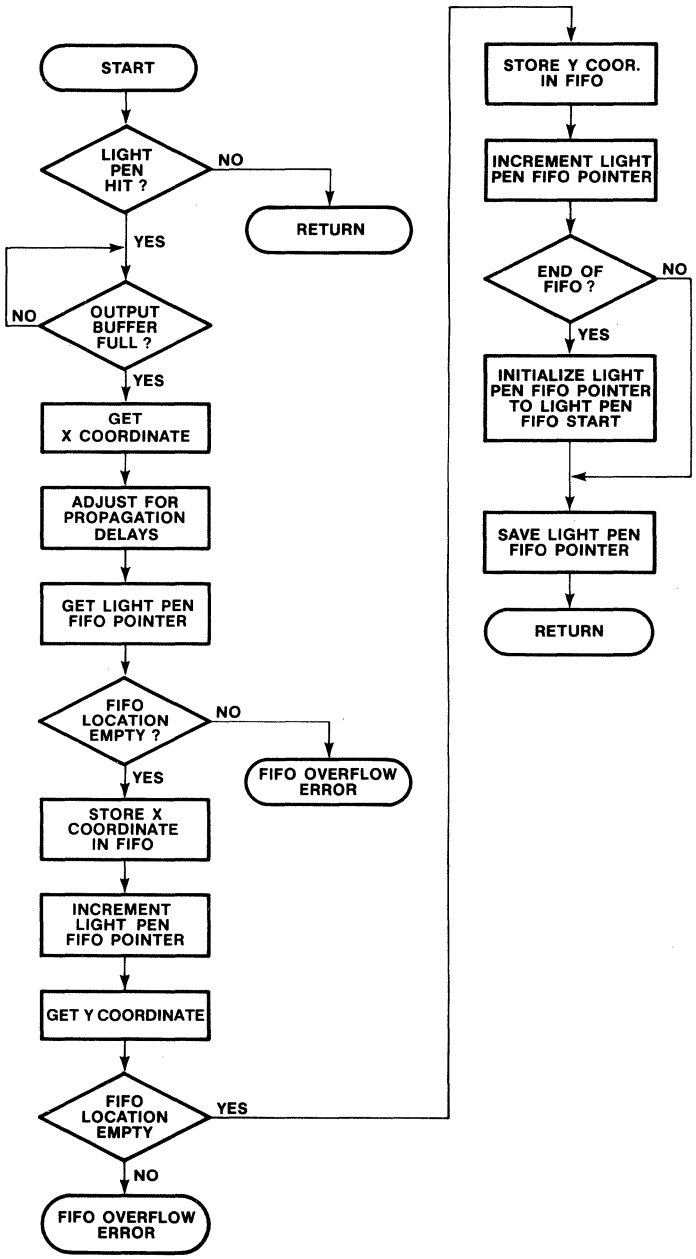


Figure 3-6. Flow Chart of Light Pen Hit Subroutine

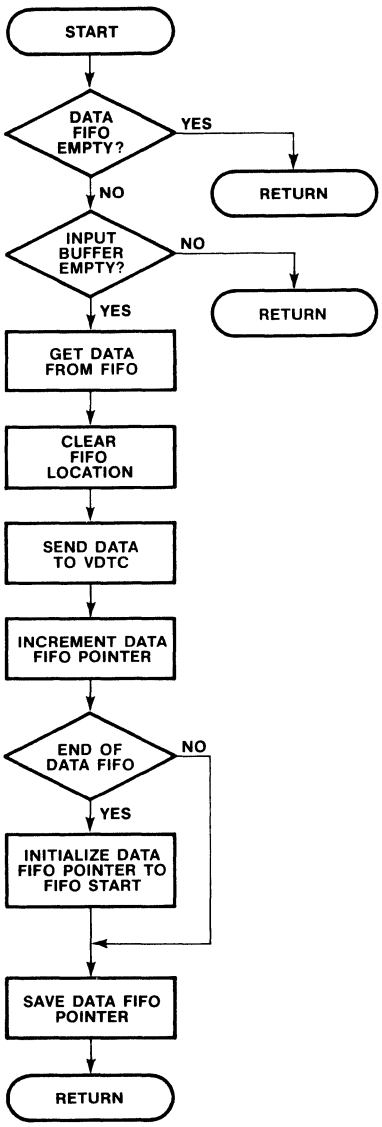


Figure 3-7. Flow Chart Of Data Display Subroutine

Table 3-7. Main Loop Program Listing

```
 1  KBSTRT     EQU     3300H           ;KEYBOARD FIFO START ADDRESS
 2  LPSTRT     EQU     3320H           ;LIGHT PEN FIFO START ADDRESS
 3  DISTRT     EQU     3340H           ;DATA DISPLAY FIFO START ADDRESS
 4  KBFIN      EQU     3360H           ;KEYBOARD FIFO INPUT POINTER
 5  KBFOUT     EQU     3362H           ;KEYBOARD FIFO OUTPUT POINTER
 6  LPFIN      EQU     3364H           ;LIGHT PEN FIFO INPUT POINTER
 7  LPFOUT     EQU     3366H           ;LIGHT PEN FIFO OUTPUT POINTER
 8  DISIN      EQU     3368H           ;DATA DISPLAY FIFO INPUT POINTER
 9  DISOUT     EQU     336AH           ;DATA DISPLAY FIFO OUTPUT POINTER
10  KBFEND     EQU       10H           ;KEYBOARD FIFO END DETECT
11  LPFEND     EQU       30H           ;LIGHT PEN FIFO END DETECT
12  DISEND     EQU       50H           ;DATA DISPLAY FIFO END DETECT
13  BASE       EQU      0F0H           ;VDTC I/O BASE ADDRESS
14  KBHIT      EQU       20H           ;KEYBOARD HIT STATUS BIT
15  LPHIT      EQU       10H           ;LIGHT PEN HIT STATUS BIT
16  OBFULL     EQU       01H           ;OUTPUT BUFFER FULL STATUS BIT
17  IBFULL     EQU       02H           ;INPUT BUFFER FULL STATUS BIT
18  XDELAY     EQU       05H           ;COMPENSATION FOR PROPAGATION DELAYS
19  WRAPA      EQU       80H           ;WRAPAROUND COMPENSATION
20  KBEN       EQU       01H           ;ENABLE KEYBOARD PARAMETER
21  LBEN       EQU       01H           ;ENABLE LIGHT PEN PARAMETER
22  SETMOD     EQU       02H           ;SET VDTC MODE COMMAND
23
24                 ORG     3000H
25
26  MAINLP:        LXI     H,KBSTRT        ;INITIALIZE KEYBOARD FIFO
27                 SHLD    KBFIN           ;INPUT AND OUTPUT POINTERS
28                 SHLD    KBFOUT
29                 MVI     C,16            ;CLEAR KEYBOARD FIFO
30                 CALL    LOOP
31                 LXI     H,LPSTRT        ;INITIALIZE LIGHT PEN FIFO
32                 SHLD    LPFIN           ;INPUT AND OUTPUT POINTERS
33                 SHLD    LPFOUT
34                 MVI     C,16
35                 CALL    LOOP            ;CLEAR LIGHT PEN FIFO
36                 MVI     C,SETMOD
37                 CALL    SNDCMD          ;SEND SET MODE COMMAND
38                 MVI     C,LPEN OR KBEN  ;AND PARAMETERS TO ENABLE
39                 CALL    SNDDAT          ;THE KEYBOARD AND LIGHT PEN
40                 LXI     H,DISTRT        ;INITIALIZE DATA DISPLAY
41                 SHLD    DISIN           ;FIFO INPUT AND OUTPUT POINTERS
42                 SHLD    DISOUT
43                 MVI     C,16
44                 CALL    LOOP            ;CLEAR DATA DISPLAY FIFO
45  AGAIN:         CALL    KBDET           ;SEE IF DATA FROM KEYBOARD
46                 CALL    LPDET           ;SEE IF DATA FROM LIGHT PEN
47                 CALL    DATADS          ;DISPLAY DATA IN DISPLAY FIFO
48                 CALL    USER            ;USER ROUTINE TO HANDLE DATA
49                 CALL    USER            ;USER ROUTINE TO HANDLE DATA
51  LOOP:          MVI     M,OFFH          ;THIS ROUTINE FILLS FIFO'S
52                 INX     H               ;WITH FF'S TO CLEAR FIFO'S
53                 DCR     C
54                 JNZ     LOOP
55                 RET
56
57  SNDCMD:        IN      0F1H            ;SEE IF INPUT BUFFER EMPTY
58                 ANI     02              ;TO RECEIVE COMMAND
59                 JNZ     SNDCMD
60                 MOV     A,C             ;GET COMMAND
61                 OUT     0F1H            ;AND SEND TO VDTC
62                 RET
63
64  SNDDAT:        IN      0F1H            ;SEE IF INPUT BUFFER EMPTY
65                 ANI     02              ;TO RECEIVE PARAMETER
66                 JNZ     SNDDAT
67                 MOV     A,C             ;GET PARAMETER
68                 OUT     0F0H            ;AND SEND TO VDTC
69                 RET
70
71                 END
```

Table 3-8. Program Listing of Keyboard Hit Subroutine

```
51
52  KBDET:      IN      LOW BASE+1      ;SEE IF THERE WAS A KEYBOARD HIT
53              ANI     LOW KBHIT       ;DETECTED
54              RZ                      ;RETURN OR MAINLP IF NOT
55  WAITOB:     IN      LOW BASE+1      ;SEE IF OUTPUT BUFFER IS FULL
56              ANI     LOW OBFULL
57              JZ      WAITOB
58              IN      LOW BASE+0      ;GET DATA
59              MOV     C,A
60              LHLD    KBFIN           ;LOAD KEYBOARD INPUT POINTER
61              MOV     A,M             ;MAKE SURE FIFO LOCATION EMPTY
62              CMA
63              ANA     A
64              JNZ     KBERR           ;FIFO OVERFLOW ERROR
65              MOV     M,C             ;STORE DATA IN KEYBOARD FIFO
66              INX     H               ;INCREMENT POINTER
67              MOV     A,L
68              CPI     LOW BKFEND      ;SEE IF AT END OF KB FIFO
69              JNZ     SVKBIN
70              LXI     H,KBSTRT
71  SVKBIN:     SHLD    KBFIN           ;SAVE KB FIFO IN POINTER
72              RET
73
74  KBERR:                              ;HANDLE AS REQUIRED
75              RET
76
```

Table 3-9. Program Listing of Light Pen Hit Subroutine

```
78
79  LPDET:      IN      LOW BASE+1      ;SEE IF LIGHT PEN HIT DETECTED
80              ANI     LPHIT
81              RZ                      ;RETURN TO MAINLP IF NOT
82              CALL    WAIT2           ;SEE IF OUTPUT BUFFER FULL
83              IN      LOW BASE+0      ;GET X COORDINATE
84              SBI     LOW XDELAY      ;DELAY MAY VARY FOR DIFFERENT LIGHT PENS
85              JP      CONTIN          ;IF NEGATIVE, WRAP AROUND OCCURED
86              ADI     LOW WRAPA
87  CONTIN:     MOV     C,A
88              LHLD    LPFIN           ;LOAD LP FIFO IN POINTER
89              MOV     A,M             ;SEE IF FIFO LOCATION EMPTY
90              CMA
91              ANA     A
92              JNZ     LPERR           ;FIFO OVERFLOW ERROR
93              MOV     M,C             ;STORE X COORDINATE IN L FIFO
94              INX     H               ;INCREMENT INPUT POINTER
95              CALL    WAIT2           ;SEE IF OUTPUT BUFFER FULL
96              IN      LOW BASE+0      ;GET Y COORDINATE
97              MOV     C,A
98              MOV     A,M             ;SEE IF FIFO LOCATION EMPTY
99              CMA
100             ANA     A
101             JNZ     LPERR           ;FIFO OVERFLOW ERROR
102             MOV     M,C             ;STORE Y COORDINATE IN FIFO
103             INX     H
104             MOV     A,L             ;SEE IF AT END OF LP FIFO
105             CPI     LOW LPFEND
106             JNZ     SVLPIN
107             LXI     H,LPSTRT
108 SVLPIN:     SHLD    LPFIN           ;SAVE LP FIFO IN POINTER
109             RET
110
111 WAIT2:      IN      LOW BASE+1      ;SEE IF OUTPUT BUFFER FULL
112             ANI     LOW OBFULL
113             JZ      WAIT2
114             RET
115
116 LPERR:                              ;HANDLE AS REQUIRED
117             RET
118
```

Table 3-10. Program Listing of Keyboard Display Subroutine

```
120
121  DATADS:    IN      LOW BASE+1    ;SEE IF INPUT BUFFER EMPTY
122             ANI     LOW IBFULL
123             RNZ                   ;RETURN TO MAINLP IF INPUT BUFFER FULL
124             LHLD    DISOUT        ;LOAD DISPLAY FIFO OUT POINTER
124             MOV     A,M           ;SEE IF DATA IN DISPLAY FIFO
125             CMA
127             ANA     A
128             RZ                    ;RETURN TO MAINLP IF FIFO EMPTY
129             MOV     A,M
130             OUT     LOW BASE+0    ;SEND DATA TO VDTC FOR DISPLAY
131             MVI     M,0FFH        ;CLEAR DISPLAY FIFO LOCATION
132             INX     H             ;INCREMENT DISPLAY OUT POINTER
133             MOV     A,L           ;SEE IF AT END OF DISPLAY FIFO
134             CPI     LOW DISEND
135             JNZ     SVDOUT
136             LXI     H,DISTRT
137  SVDOUT:    SHLD    DISOUT        ;SAVE DISPLAY FIFO OUT POINTER
138             RET
139
140
141
142
143  USER:                            ;USER ROUTINE TO HANDLE DATA LOCATED IN THE KEY-
144                                   ;BOARD AND LIGHT PEN FIFO'S. THIS PROGRAM PRESUMES
145                                   ;THE DATA WAS HANDLED BY THIS ROUTINE AND THEN PUT
146                                   ;INTO THE DISPLAY FIFO.
147
148             RET
149
150             END
```

Table 3-11. Display Valid Characters Routine

```
1   ;ROUTINE TO DISPLAY ALL VALID CHARACTERS
2
3   START:     NVI     C,O
4   AGAIN:     CALL    DATOUT        ;ROUTINE TO SEND DATA TO VDTC
5              INR     C
6              MOV     A,C
7              CPI     128           ;SEE IF AT END OF CHARACTERS
8              JNZ     AGAIN         ;CONTINUE IF NOT
9              JMP     START         ;CONTINUE TO LOOP ON DISPLAY
10
11  DATOUT:    MVI     B,11H         ;LEADIN GRAPHIC CHARACTER
12             CALL    CHECK         ;SEE IF INPUT BUFFER EMPTY
13             MOV     B,C
14             CALL    CHECK         ;GO DISPLAY CHARACTER
15             RET
16
17  CHECK:     IN      0F1H
18             ANI     02            ;SEE IF INPUT BUFFER EMPTY
19             JNZ     CHECK
20             MOV     A,B           ;GET CHARACTER
21             OUT     0F0H          ;AND SEND FOR DISPLAY
22             RET
23
24             END
```

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description of the iSBX 270 VDTC board. Figure 4-1 is a simplified block diagram of the iSBX 270 VDTC Board.

4-2. FUNCTIONAL DESCRIPTION

A brief description of the functional blocks of logic comprising the iSBX 270 VDTC board is given in the following paragraphs.

4-3. INTERFACE CONTROLLER

The major portions of the interface controller are UPI U16 (2ZD7) and port expander U12 (2ZD5). The major functions of the interface controller are under control of the firmware contained in the UPI. The firmware will not be described in this section, but the basic functions it performs will be.

The UPI interfaces to the host processor via the data, chip select, and control lines of the iSBX bus interface. The UPI drives three lines to the host processor: two interrupt and one DMA request line. The interrupt lines are buffered to provide increased drive.

The UPI communicates with other chips on the VDTC via an on board data bus connected to I/O port P1 (U16-27 through U16-34). The UPI inputs or outputs data as required via this port, which is placed in the input state when not in use to prevent bus contention. Port P2 (U16-21 through U16-24 and U16-35,36,37) is used to generate DMA and interrupt signals to the iSBX bus interface and to control the port expander.

The port expander drives the address bus via P4 (U12-2 through U12-5) to allow the UPI to select various chip registers. When not in use, this port is placed in the input mode, to avoid bus contention. Port P5 (U12-1,21,22,23) drives the chip select lines to the Memory Controller, the CRT Controller, and the Keyboard Interface. In addition, a strobe line for an external bell is provided. These lines are all driven High when not in use.

Port P6 (U12-17,U12-20) controls the I/O read line, the I/O write line, the Memory Controller Ready

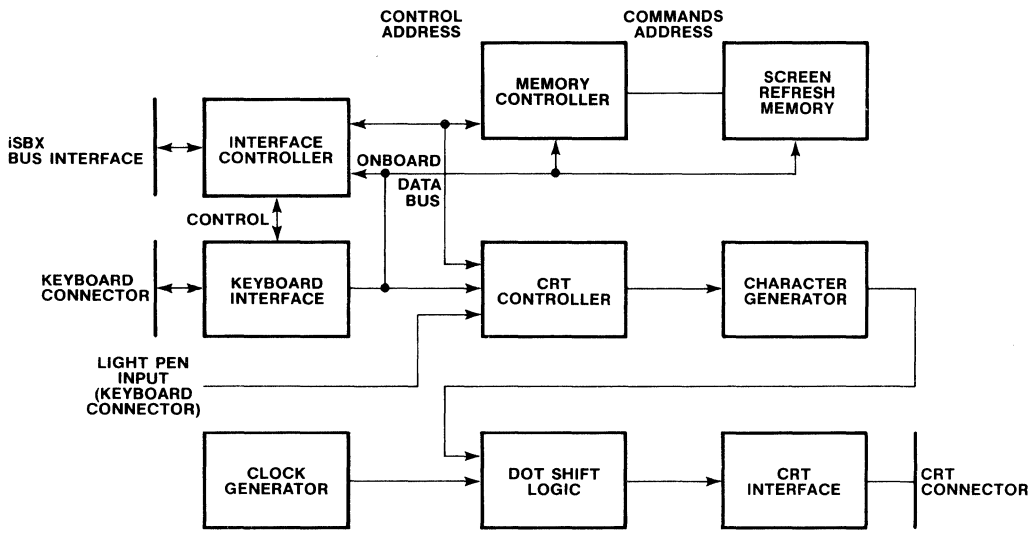


Figure 4-1. VDTC Block Diagram

line, and the Enable line to the Memory Controller. The I/O read line is driven by U10-8 (2ZC4), which is controlled by port P6 bit P60. When inactive, this line is tri-stated and pulled up. Port P6 bit P61 enables tri-state buffer U10-11 (2ZC5) which gates the PROG (U12-7) pulse, to the port expander, out to the chips. This arrangement allows the UPI to strobe data into an on board chip and change to the next address in only one cycle. The ready line (Port P6 bit P62) allows the UPI to control the speed of a memory transfer, so that the UPI has time to send or accept the data. Figure 4-2 shows the ready handshake. In addition, the ready line is used to clear end-of-process (EOP) latch U15 (2ZA3). Port P6 bit P63 allows the UPI to disable the Memory Controller, so that the UPI may obtain the on-board bus.

Port P7 and UPI inputs T0 and T1 monitor the rest of the VDTC circuitry. Port P7 bit P70 passes the state of the EOP latch to the firmware. When the EOP latch is set, it indicates that the memory controller has completed an operation (clear line or clear screen). Port P7 bit P71 tells the firmware whether the VDTC is to operate in 50Hz or 60Hz mode. Port P7 bit P72 informs the UPI that the CRT controller is requesting DMA service and that the UPI should not request the on board bus. Port P7 bit P73 informs the firmware that the CRT controller has entered vertical retrace and requires service. Input T0 (on the UPI), when Low, indicates that the Memory Controller has relinquished the on board bus and that the UPI may use it. Input T1 is used as an input to the UPI's internal counter. A transition from High to Low on this input (caused by a keyboard strobe) will cause the counter to increment setting an internal flag.

4-4. MEMORY CONTROLLER

The memory controller is the workhorse of the VDTC. It can control the on board buses when allowed to by the interface controller. The major portions of the memory controller are the DMA controller U17 (2ZB4), clock divider U19 (2ZA7), ready synchronizer/inverter and hold acknowledge generator U20 (2ZB5), and a quad transparent latch U18 (2ZB3). All memory transfers are done by the DMA controller chip, including screen refresh, writing data to the screen, and clearing display lines (or the whole screen).

The DMA controller requires a 5 MHz clock for proper operation. Flip-flop U19-9 (2ZA7) divides the 10 MHz MCLK by two, producing the required signal. This clock not only drives the DMA controller, but also the ready synchronizer/inverter U20-5 and the hold Acknowledge generator U20-8. The DMA controller has a requirement that Hold Acknowledge (HLDA) be separated from Hold Request (HRQ) by

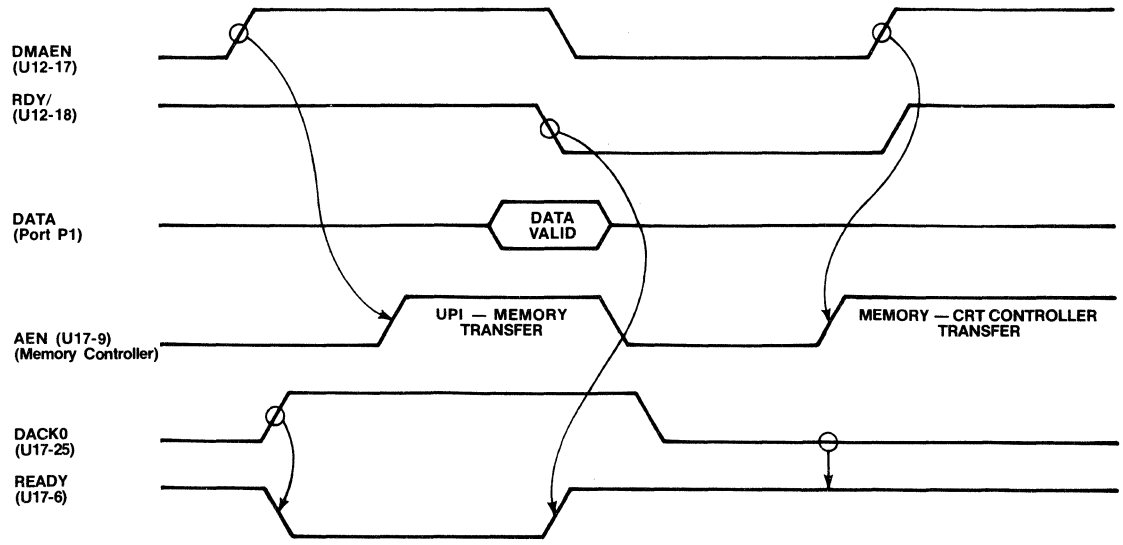


Figure 4-2. Ready Handshake Timing

one clock cycle, and that HLDA must not go inactive while HRQ is active. Figure 4-3 shows the waveforms for the circuit which handles this.

Quad transparent latch U18 (2ZB3) is used to latch the four most significant memory address bits. This is done on the falling edge of ADSTB from the DMA controller. Note that the highest four bits of the 16 bit address are not used or latched; this means that if an address above 0FFFH is accessed, it will be evaluated modulo 4096 and mapped into the memory.

The four channels of the DMA controller (U17) are each dedicated to a specific function. Channel 0 is used by the UPI to write (or read) data to the screen refresh memory. Note that the DMA controller is provided with a ready signal (via U21) except when DMA channel 0 is active, in which case the UPI controls ready via port P6 bit P62 . The UPI requests a transfer on channel 0 by a software DMA request, after loading the address register and a word count of 1. Block mode is used.

Channel 1 is reserved.

Channel 2 is used to refresh the CRT controller. The CRT controller requests service via DRQ2 and an acknowledge is given by DAK/. The DMA controller will perform a memory read to get the data, and an I/O write to give it to the CRT controller. Single byte transfer mode is used.

Channel 3 is used to clear the screen refresh memory to spaces. The UPI will load the address register of the DMA controller with the starting address, and load the word count register with the number of bytes to be cleared. The UPI then requests DMA by unmasking the DRQ input (which is tied high) and releases the bus. The DMA will transfer the specified number of bytes from space code generator U23 (2ZC3) into memory. The space code generator is an octal tri-state buffer whose inputs have been tied such that the output, when enabled, will place the ASCII code for a space (20H) on the internal data bus. The space code generator is enabled when DACK3 and IOR/ are both active. The DMA controller is programmed for single byte transfer to allow channel 2 to interleave. The DMA controller signals the completion of a line clear by pulsing the EOP line, which sets the EOP latch.

4-5. SCREEN REFRESH MEMORY

This 4K block of RAM consists of two 2168 chips U13 and U14 (3ZD5). Memory read and memory write are OR'ed together to create a chip select, and memory write connects to the write enable input of the RAM's. The RAM's connect directly to the on board data bus and receive address information from the memory controller.

4-6. KEYBOARD INTERFACE

The Keyboard Interface consists of octal latch U1 (3ZB7) with tri-state outputs. This latch will save the data present on its inputs when its clock line rises.

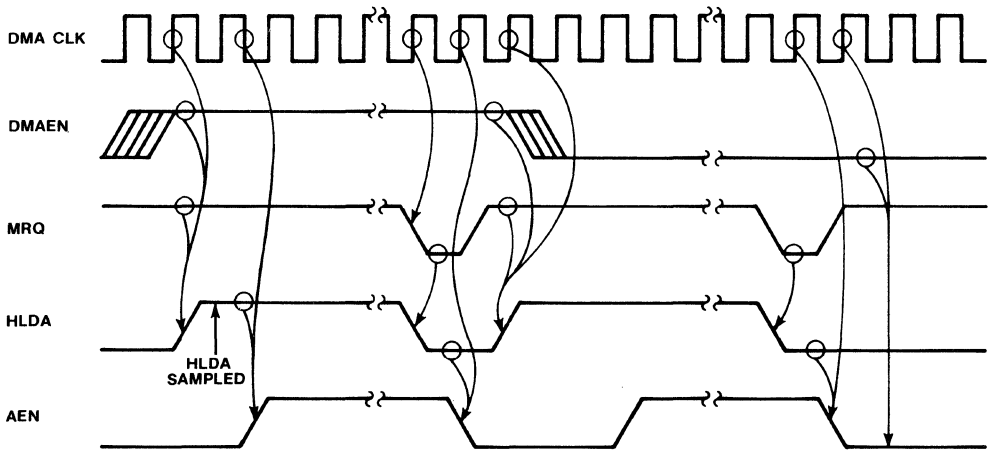


Figure 4-3. Hold Request and Hold Acknowledge Timing

The clock line comes from the Keyboard Strobe line via jumper stake group E1-E4. The UPI is informed of a keyboard hit by input T1, which is a falling-edge triggered signal also from jumper stake group E1-E4. Once the data has been latched into U1, the UPI can read the data by enabling the output of U1 (via port P5 bit P52). This line also is routed to the J1 connector as KEYACK/ to inform the keyboard that the data has been read from the keyboard latch. In addition, port P5 bit P53 is routed to the J1 connector as a Bell strobe (active low). When the VDTC receives a BEL (code 07H) from the host processor, this output will pulse low for a minimum of 5 μsec.

4-7. CRT CONTROLLER

The CRT controller U11 (3ZB6) performs all timing and data buffering functions for the CRT. Refer to the 8275 data sheet for additional details. The CRT controller also receives a light pen input from the keyboard connector.

The light pen interface consists of the light pen input (LPEN), which is rising edge triggered. This signal should be externally latched to prevent multiple light pen hits.

Light pen hits are detected during a status read of the 8275 every vertical retrace.

4-8. CHARACTER GENERATOR

The character generator U2 (3ZB6) consists of a 2716-1 PROM which is programmed with the proper pattern. The pattern in the PROM is active-low, that is an illuminated dot is programmed as a zero. The four least significant bits are used to specify the line number that is currently being displayed. The next 7 bits specify the character. Thus the character "A" (ASCII Code 41H) occupies addresses 410H to 41FH. The dot pattern is shifted out least-significant bit first. Figure 4-4 shows the coding sample for one character in a 5 x 7 matrix. For more information on the character generator coding see Appendix A.

4-9. CLOCK GENERATOR

The clock generator consists of hybrid crystal oscillator Y2 (3ZB7), which is mounted in a socket, and synchronous counter U4 (3ZA7). The crystal oscillator frequency is determined by the Horiz rate and the dot matrix size. A chart is shown on the schematic which defines the required clock rates.

The synchronous counter is loaded with a value that depends on the dot matrix size. When a matrix of 5 x 7 is used, the counter is a divide-by-seven (figure 4-5). When a matrix of 6 x 8 is used, the counter is a divide-by-eight (figure 4-6). When a matrix of 7 x 9 is used, the counter is a divide-by-nine (figure 4-7). Under default conditions, a character clock is produced which is 1.62 MHz. This clock drives the CRT controller.

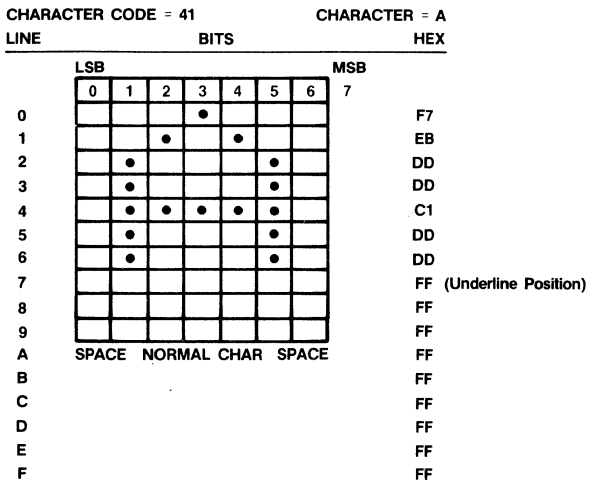


Figure 4-4. Sample Character Generator Dot Pattern

4-10. DOT SHIFT REGISTER

The purpose of dot shift register U3 (3ZB5) is to take the parallel data from the character generator and serialize it to a video signal. This is accomplished by U3, a synchronous parallel-load, serial-out shift register. This shift register is clocked by the output from the clock generator.

It is important to note that the character being displayed is always one character behind the CRT controller. Therefore, the attribute information for a character must be saved. This is done by octal latch U5 (3ZA5).

4-11. CRT INTERFACE

The serial video output of the dot shift register is combined with video suppress (VSP), light enable (LTEN), and reverse video (RVV) by gates U6 (3ZB4) and U7 (3ZB4) to obtain a complete video signal. This video signal is ANDed with the attribute signals by driver U8 (3ZB3), which also provides 75 ohm line drive capability. The outputs of U8 are the Red, Green, and Blue Video signals.

For color operation, jumper E21-E22 (3ZB4) must be removed. This will cause the input to the Green

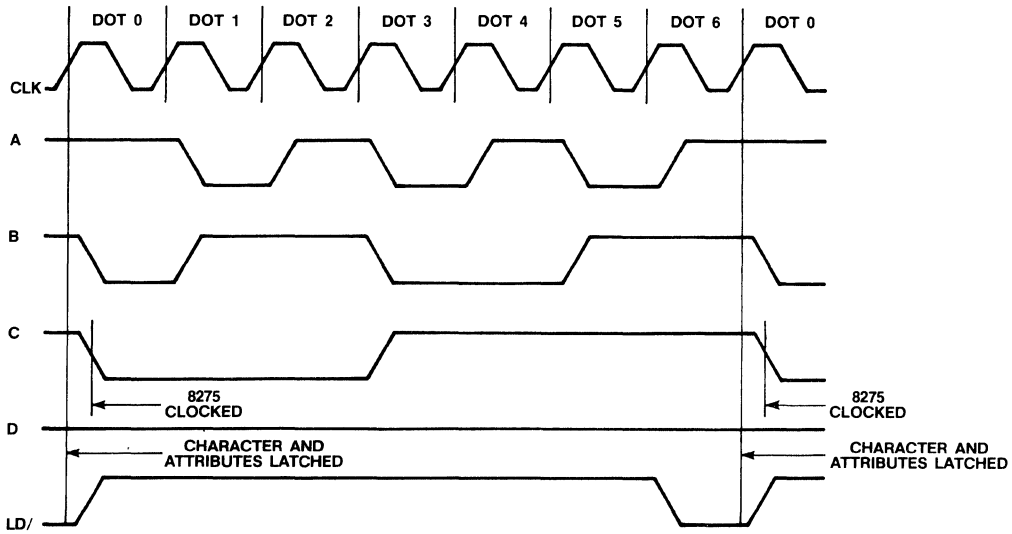


Figure 4-5. Clock Generator Timing For 5 X 7 Matrix

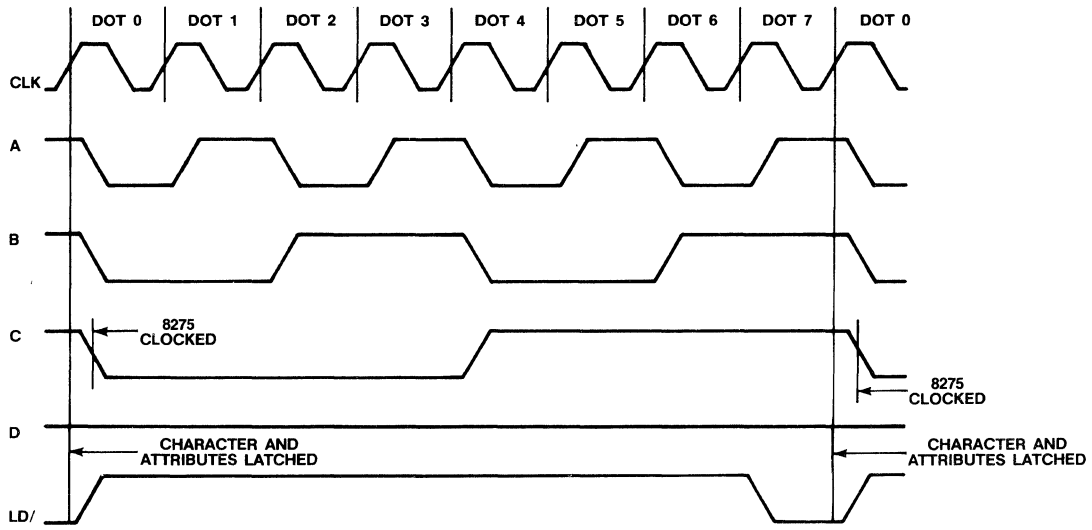


Figure 4-6. Clock Generator Timing For 6 X 8 Matrix

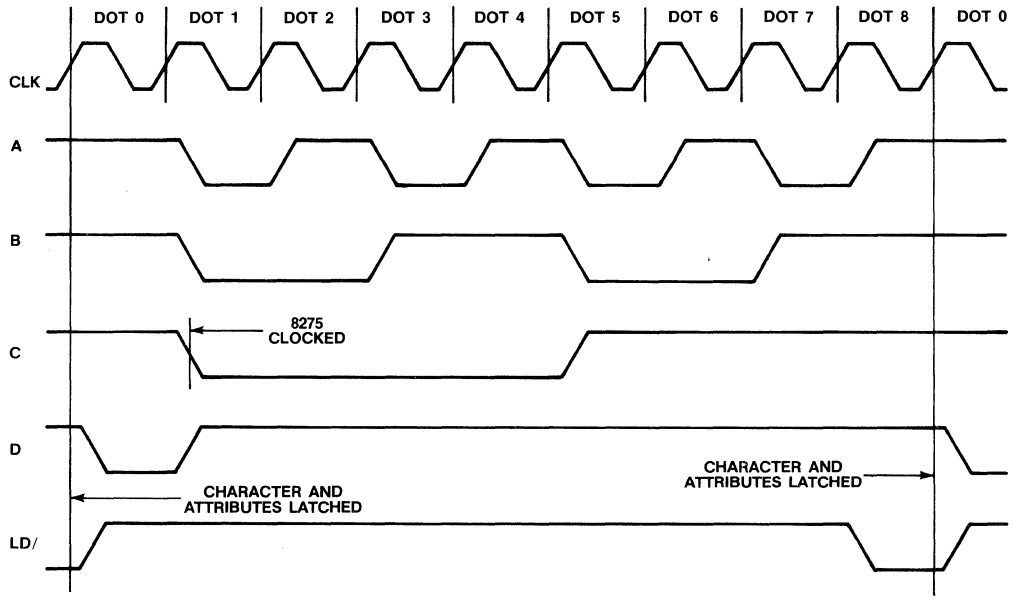


Figure 4-7. Clock Generator Timing For 7 X 9 Matrix

Video line driver (U8) to be gated by the inactive status of GPAO. Thus if GPA0 is not active, the Green Video signal will be enabled. The removal of jumper E21-E22 also causes the output of U6-10 (3ZB4) to go low, converting U7-6 (an exclusive-or gate) to a non-inverting buffer. Red Video then becomes gated with the inactive state of Highlight (HLGT) at line driver U8. The Blue Video signal is gated with the inactive state of GPA1 at line driver U8. The inverted operation of the attribute lines allows all color guns to be on (white will be displayed) immediately after power-up, without the need to write any attributes. As attributes are written, the various colors are disabled, allowing a total of seven colors plus black to be displayed.

If Black and White operation is required, jumper E21-E22 must be installed, enabling the Green Video driver regardless of the state of GPA0. At the same time, exclusive-OR U7-6 (3ZB3) becomes an inverting buffer, so that Red Video is only enabled when the highlight attribute is active. A resistor and diode connected to jumpers E16-E17 (3ZB3) and E23-E24 (3ZB2) combine the highlighted video and the normal video to form a dual-intensity level combined video signal, with adjustable contrast. A single intensity level may be obtained by installing jumper E23-E24 only.

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, and service assistance instructions for the iSBX 270 VDTC board.

5-2. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance by contacting the Intel Product Service Hotline in Phoenix, Arizona. Customers outside the United States should contact their sales source (Intel Sales Office or Authorized Distributor) for service information and repair assistance.

Before calling the Product Service Hotline, you should have the following information available:

a. Date you received the product.

b. Complete part number of the product (including dash number). On boards, this number is usually silk-screened onto the board. On other MCSD products, it is usually stamped on a label.

c. Serial number of product. On boards, this number is usually stamped on the board. On other MCSD products, the serial number is usually stamped on a label.

d. Shipping and billing addresses.

e. If your Intel product warranty has expired, you must provide a purchase order number for billing purposes.

f. If you have an extended warranty agreement, be sure to advise the Hotline personnel of this agreement.

Use the following numbers for contacting the Intel Product Service Hotline:

TELEPHONE

All U.S. locations, except Alaska, Arizona, & Hawaii:

(800) 528 - 0595

All other locations: (602) 869 - 4600

TWX NUMBER:

910 - 951 - 1330

Always contact the Product Service Hotline before returning a product to Intel for repair. You will be given a repair authorization number, shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If you are returning the product because of damage sustained during shipment or if the product is out of warranty, a purchase order is required before Intel can initiate the repair.

In preparing the product for shipment to the Repair Center, use the original factory packing material, if possible. If this material is not available, wrap the product in a cushioning material such as Air Cap TH - 240, manufactured by the Sealed Air Corporation, Hawthorne, N.J. Then enclose in a heavy duty corrugated shipping carton, and label "FRAGILE" to ensure careful handling. Ship only to the address specified by Product Service Hotline personnel.

5-3. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the iSBX 270 VDTC board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in Table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as COML; every effort should be made to procure these parts from a local (commercial) distributor.

5-4. SERVICE DIAGRAMS

The parts diagram and schematic diagrams of the iSBX 270 VDTC board are provided in figures 5-1 and 5-2, respectively. On the schematic diagrams, a signal mnemonic that ends with a slash (e.g., BSTB/) is active low. Conversly, a signal mnemonic without a slash (e.g., MEMRD) is active high.

The schematic diagrams in Figure 5-2 are current when the manual is printed. However, minor revisions to the diagrams may occur between manual printings. Therefore, Intel provides copies of the current schematic diagrams with the board, when it is shipped from the factory. These diagrams should be inserted into this manual for future reference. In most instances the diagrams shipped with the board will be identical to those included in the manual.

Table 5-1. Replaceable Parts

Reference Designator	Description	Mfr. Part No.	Mfr. Code	Qty.
C1-4,7-13,16,17	Cap., Cer., .1 uf, +80%	MA205E104ZAA	AVX	13
C5	Cap., Cer., 1200 pf, 5%, 50V	MD015A122JAA	AVX	1
C6	Cap., Cer., .01 uf, 5%, 50V	MA405A103JAA	AVX	1
C14	Cap., Cer., 22 pf, 5%, 50V	MD015A220JAA	AVX	1
C15	Cap., Tant., 22 uf, 10%, 15V	T110B226K015AS	KEM	1
C18	Cap., Cer., 180 pf, 5%, 50V	MD015A181JAA	AVX	1
CR1	Diode, 1N270	OBD	COML	1
F1-3	Fuse, Pico, 1 Amp, 125V	276-001	LTF	3
J1,J2	Conn., 26 Pin, Rt. Angle	65461-005	BERG	2
P1	Conn., 18/36-pin, iSBX Male	000292-0001	VIK	2
R1	Res., 12 Turn Pot, 200 ohms, .5w	3262X-201	BOI	1
R2	Res., 12 Turn Pot, 500 ohms, .5w	3262X-501	BOI	1
R3	Res., 12 Turn Pot, 50K ohms, .5w	3262X-503	BOI	1
R4,R5	Res., 120 ohms, 1/4w, 5%	CB-1215	AB	1
R6	Res., 43.2K, 1/4w, 1%	CC-432-F	AB	1
R7	Res., 110K, 1/4w, 1%	CC-1103-F	AB	1
R8	Res., 6.81K, 1/4w, 1%	CC-6811-F	AB	1
RP1-3	Res. Pack, 10K, 8 Pin	A4308R-101-103	BOI	3
RP4	Res. Pack, 1K, 6 Pin	4306-101-102	BOI	1
U1	IC, 74LS374, Octal D-type Latch	74LS374	TI	1
U2	IC, Intel 2716-1, EPROM	2716-1	INTEL	1
U3	IC, 74LS166, 8-Bit Shift Register	74LS166	TI	1
U4	IC, 74S163, Sync 4-Bit Counter	74S163	TI	1
U5	IC, 74S374, Octal D-Type Latch	74S374	TI	1
U6	IC, 74S02, Quad 2-Input-Positive-NOR Gate	74S02	TI	1
U7	IC, 74S86, Quad 2-Input Exclusive-OR Gate	74S86	TI	1
U8	IC, 74128, 50-Ohm line Driver	74128	TI	1
U9	IC, 74LS123, Dual Multivibrator	74LS123	TI	1
U10	IC, 74LS125, Quad Bus Buffer	74LS125	TI	1
U11	IC, INTEL 8275, Prog. CRT Cont.	8275	INTEL	1
U12	IC, Intel 8243, I/O Expander	8243	INTEL	1
U13,14	IC, Intel 2168, Static RAM	2168	INTEL	2
U15	IC, 74S00, Quad 2-Input NAND	74S00	TI	1
U16	IC, Intel 8741A, UPI	8741A	INTEL	1
U17	IC, Intel 8237A-2, DMA Controller	8237A-2	INTEL	1
U18	IC, 74LS75, 4-Bit bistable Latch	74LS75	TI	1
U19	IC, 74LS74A, Dual D-type Flip-Flop	74LS74A	TI	1
U20	IC, 74S74, Dual D-type Flip-Flop	74LS74	TI	1
U21	IC, 74S08, Quad 2-Input Positive AND Gate	74S08	TI	1
U22	IC, 74LS04, Hex Inverter	74LS04	TI	1
XU2	Socket, 24 Pin, DIP	524-AG37D	AUG	1
XU16,17	Socket, 40 Pin, DIP	540-AG37D	AUG	2
XY2	Socket, 14 Pin, DIP	514-AG37D	AUG	1
Y1	Crystal, 6.00 MHz	CY6B	CRY	1
Y2	Crystal, 14.58 MHz	K1115A-14.58MHZ	MOT	1

Table 5-2. List of Manufacturer's Codes

Mfr. Code	Manufacturer	Address	Mfr. Code	Manufacturer	Address
AB	Allen-Bradley Co	Highland Hts, OH	INTEL	Intel Corp	Santa Clara, CA
AUG	Augut Inc	Attleboro, MA	KEM	Kemet	Greenville, SC
AVX	AVX Ceramics	Myrtle Beach, SC	LTF	Littlefuse Co	Des Plaines, IL
BERG	Berg Electronics	New Cumburland, PA	MOT	Motorola Inc	Phoenix, AZ
BOI	Bourns Inc	Riverside, CA	TI	Texas Instruments	Dallas, TX
CRY	Crystek Crystals Corp	Ft. Meyers, FL	VIK	Viking Connectors Inc	Chatsworth, CA
COML	Available from any commercial source. Order by description (OBD).				

5-5. INTERNAL SIGNALS

Internal board signals which traverse from one sheet to another in Figure 5-2 are identified by a single alpha character within a box (e.g., C). The signal mnemonic is shown adjacent to the boxed character, along with the source or destination sheet number (e.g., SH 2, DAK/ F). Signals coming into the sheet are shown on the left side of the diagram. Conversely, signals leaving the sheet are shown on the right side.

To follow a signal from one sheet to another, read the sheet number and boxed character, then look for the same boxed character on the indicated sheet. For example, if you are going to trace the path of IOR/ when it exits sheet 2, the first step would be to turn to the indicated sheet. Since IOR/ will be entering sheet 3, as shown on sheet 2, look for the E symbol on the left side of the sheet. Notice that the inputs also list the source sheet number (sheet 2 in this example).

Each signal will keep the same boxed character throughout Figure 5-2. This will enable you to trace the signal to any sheet with minimal effort.

The internal board signal mnemonics are listed and defined in Table 5-3. The signals are listed according to boxed code alphabetical order.

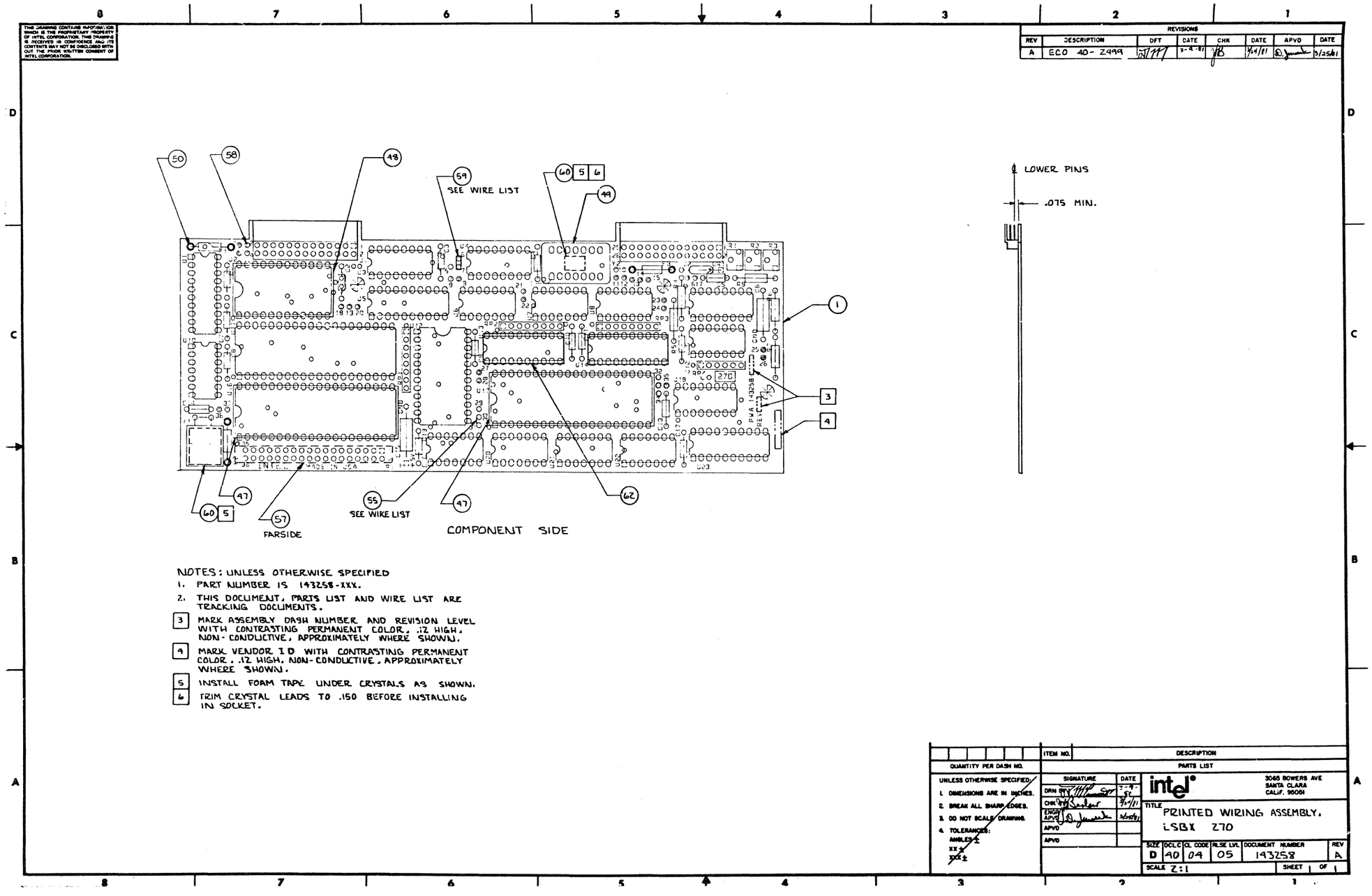


Figure 5-1. Parts Location Diagram

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

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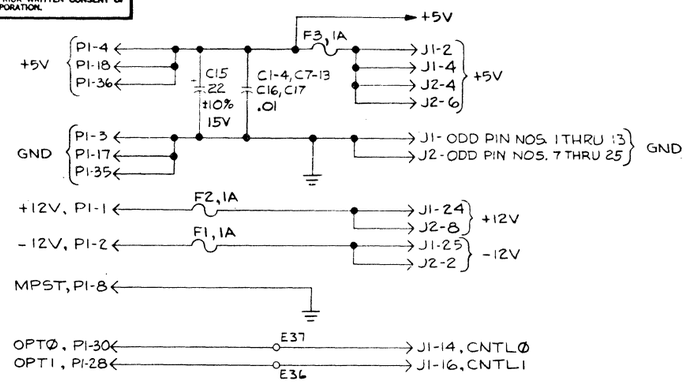
DWG NO. 143985 SH 1 REV A

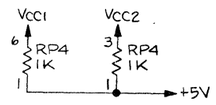
REVISIONS

ZONE	REV	DESCRIPTION	DFT	CHK	DATE	APPROVED
	A	ECO 40-2956				



POWER, GND AND SPARE GATE LOCATOR

REF DES	DEVICE TYPE	POWER GND	POWER +5V	SPARE GATES OUTPUT PINS
Y2	SEE NOTE 3	7	14	
U13,14	2168	10	20	
U2	2716-1	12	24	
U17	8237A-5	20	31	
U12	8243	12	24	
U11	8275	20	40	
U16	8741A	20	40	
U15	74S00	7	14	
U6	74S02	7	14	13
U22	74LS04	7	14	10
U21	74S08	7	14	
U20	74S74	7	14	
U19	74LS74	7	14	
U7	74S86	7	14	
U9	74LS123	8	16	
U10	74LS125	7	14	
U8	74128	7	14	
U4	74S163	8	16	
U3	74LS166	8	16	
U18	74LS75	12	5	
U23	74LS244	10	20	
U5	74S374	10	20	
U1	74LS374	10	20	



REFERENCE DESIG. LAST USED	NOT USED
U23	RP1-3
C18	
R8	
RP4	
J2	
E37	
Y2	
F3	
P1	

[3]

DOT MATRIX SIZE	Y2 FREQUENCY	JUMPERS	HORIZONTAL RATE
7 x 10	11.34 MHz	E8-E9	16.2KHz
9 x 10	14.58 MHz	E7-E6	16.2KHz
8 x 10	12.96 MHz	E8-E9	16.2KHz
	15.67 MHz	E5-E7	19.2KHz

NOTES: UNLESS OTHERWISE SPECIFIED
1. CAPACITANCE VALUES ARE IN MICROFARADS, +80%-20%, 50V.
2. RESISTANCE VALUES ARE IN OHMS 1/4W, 5%.
[3] Y2 IS A HYBRID CLOCK OSCILLATOR. STANDARD FACTORY DEFAULT IS AS SHOWN FOR 9X10 DOT MATRIX. CUSTOMER ADJUSTMENT OF DOT MATRIX SIZE IS POSSIBLE BY CHANGING Y2 AND JUMPERS AS SHOWN IN THE TABLE.

ITEM NO.	PART NUMBER	DESCRIPTION
QUANTITY PER DASH NO.		PARTS LIST

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ± 2° XX ± .030 XXX ± .010
SURFACE FINISH √

SIGNATURE	DATE
DRN BY	
CHK BY	
ENGR APVD	
APVD	
APVD	

NEXT ASSY | USED ON

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

TITLE SCHEMATIC, SBX270 VIDEO DISPLAY TERMINAL CONTROLLER MULTIMODULE

SIZE	CODE	CLASS	DWG NO.	REV
D	40	01	143985	A

SCALE NONE SHEET 1 OF 3

9300021

Figure 5-2. Schematic Diagram (page 1 of 3)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

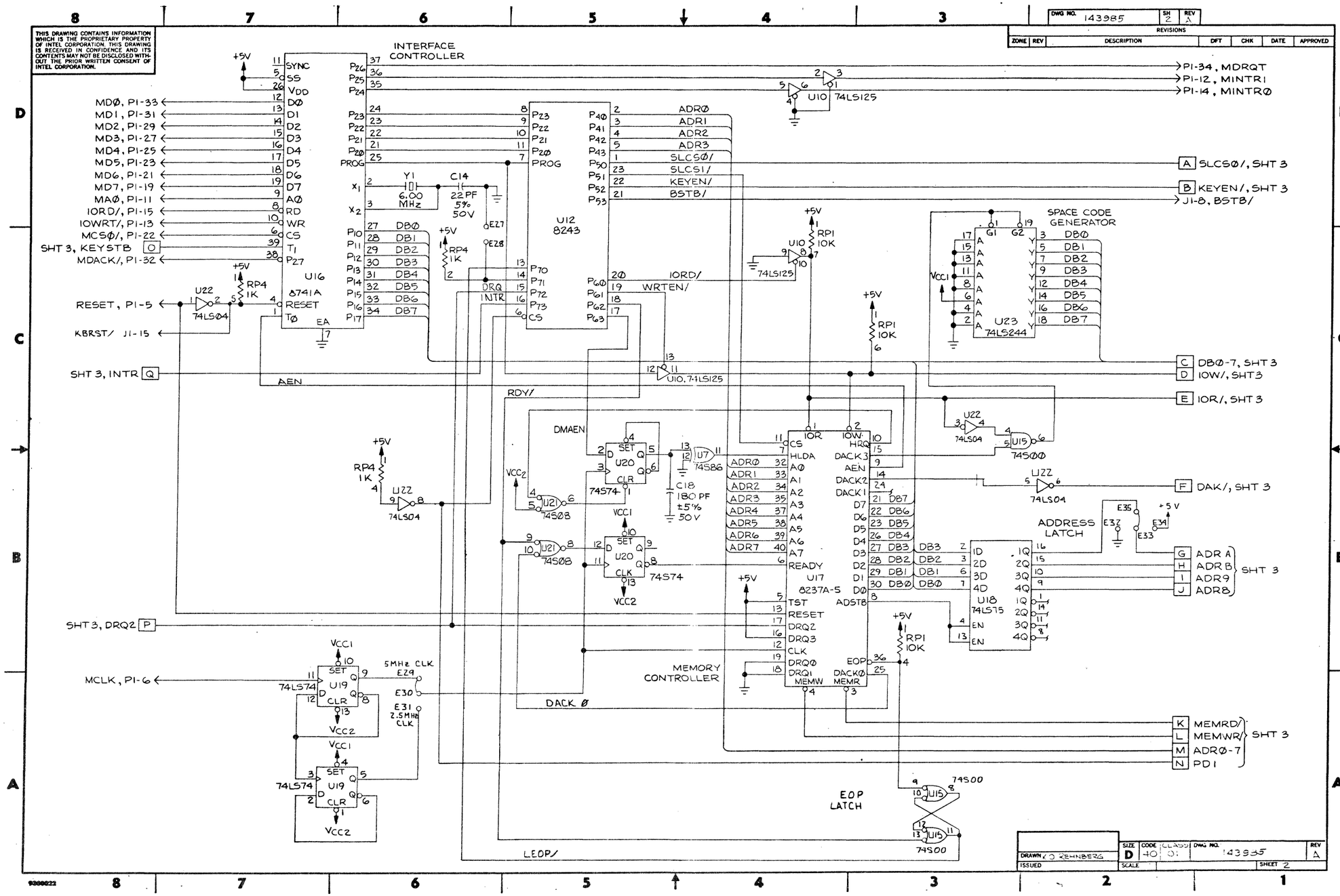


Figure 5-2. Schematic Diagram (page 2 of 3)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

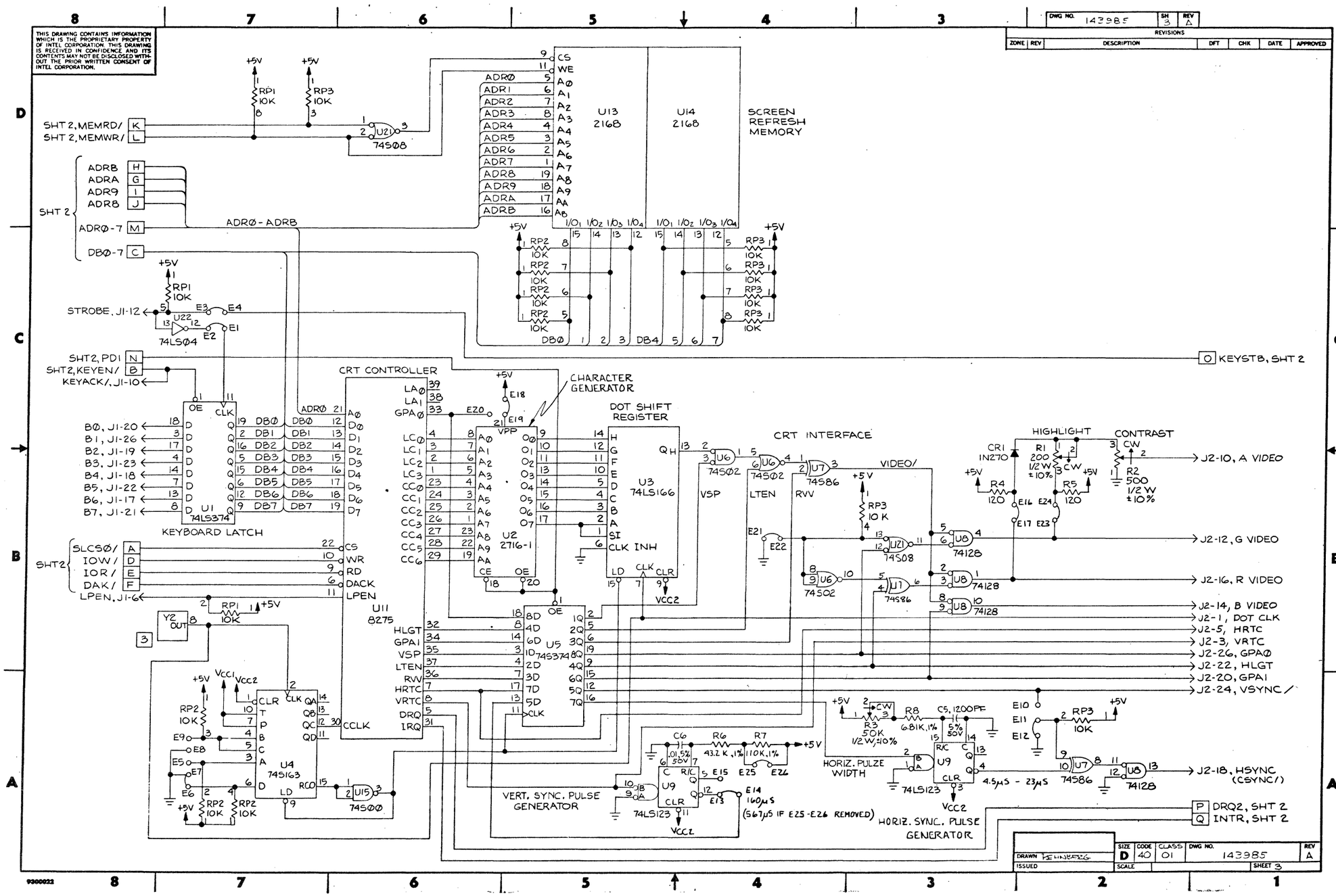


Figure 5-2. Schematic Diagram (page 3 of 3)

CAUTION: These schematic diagrams may have been revised. See "Service Information" chapter for details.

Table 5-3. Glossary of Internal Signal Mnemonics

Code	Signal Mnemonic	Description
A	SLCS0/	Slave Chip Select 0
B	KEYEN/	Keyboard Enable
C	DB0-DB7	Data Bus Bits 0-7
D	IOW/	I/O Write
E	IOR/	I/O Read
F	DAK/	DMA Acknowledge
G	ADR A	Address bit A
H	ADR B	Address bit B
I	ADR 9	Address bit 9
J	ADR 8	Address bit 8
K	MEMRD/	Memory Read
L	MEMWR/	Memory Write
M	ADR0-ADR7	Address Bits 0-7
N	PD1	Pull Down 1
O	KEYSTB	Keyboard Strobe
P	DRQ2	DMA Request
Q	INTR	Interrupt Request

APPENDIX A
CHARACTER GENERATOR PROM PROGRAMMING

A-1. INTRODUCTION

The character font and special characters that are displayed on the CRT are stored in PROM U2. If the user desires to modify the character font or any of the special characters, PROM U2 must be modified. A machine readable source file of the character generator PROM contents is available in the Insite library. Three versions are available: 7 x 9 (factory default), 6 x 8, or 5 x 7 character size.

Table A-1 is a hexadecimal listing of the contents of U2 as it is shipped from the factory.

Table A-1. Character Generator Contents

Address ASCII CODE	Character Line Number 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHAR
000X	7F	7F	BF	9F	CF	E7	F3	F9	FC	FC	FC	FF	FF	FF	FF	FF	GC0
001X	FC	FC	F9	F3	E7	CF	9F	BF	7F	7F	7F	FF	FF	FF	FF	FF	GC1
002X	7C	7C	B9	93	C7	C7	93	B9	7C	7C	7C	FF	FF	FF	FF	FF	GC2
003X	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	GC3
004X	E7	E7	E7	E7	07	07	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC4
005X	FF	FF	FF	FF	07	07	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	GC5
006X	FF	FF	FF	FF	E0	E0	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	GC6
007X	E7	E7	E7	E7	E0	E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC7
008X	FF	FF	FF	FF	00	00	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC8
009X	E7	E7	E7	E7	00	00	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC9
00AX	E7	E7	E7	E7	07	07	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	GC10
00BX	E7	E7	E7	E7	E0	E0	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	GC11
00CX	FF	FF	FF	FF	00	00	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	GC12
00DX	E7	E7	E7	E7	00	00	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	GC13
00EX	E0	E0	E0	E0	E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC14
00FX	0F	0F	0F	0F	0F	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC15
010X	FF	FF	FF	FF	FF	E0	E0	E0	E0	E0	E0	FF	FF	FF	FF	FF	GC16
011X	FF	FF	FF	FF	FF	0F	0F	0F	0F	0F	0F	FF	FF	FF	FF	FF	GC17
012X	E0	E0	E0	E0	E0	0F	0F	0F	0F	0F	0F	FF	FF	FF	FF	FF	GC18
013X	0F	0F	0F	0F	0F	E0	E0	E0	E0	E0	E0	FF	FF	FF	FF	FF	GC19
014X	00	00	00	00	00	E0	E0	E0	E0	E0	E0	FF	FF	FF	FF	FF	GC20
015X	00	00	00	00	00	0F	0F	0F	0F	0F	0F	FF	FF	FF	FF	FF	GC21
016X	00	00	00	00	00	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC22
017X	FF	FF	FF	FF	FF	00	00	00	00	00	00	FF	FF	FF	FF	FF	GC23
018X	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	E0	FF	FF	FF	FF	FF	GC24
019X	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	FF	FF	FF	FF	FF	GC25
01AX	E0	E0	E0	E0	E0	00	00	00	00	00	00	FF	FF	FF	FF	FF	GC26
01BX	0F	0F	0F	0F	0F	00	00	00	00	00	00	FF	FF	FF	FF	FF	GC27
01CX	FF	FF	FF	83	83	83	83	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC28
01DX	7F	BF	DF	EF	E0	E0	EF	DF	BF	7F	7F	FF	FF	FF	FF	FF	GC29
01EX	FC	FB	F7	EF	0F	0F	EF	F7	FB	FC	FC	FF	FF	FF	FF	FF	GC30
01FX	E7	E7	E7	E7	E7	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	GC31
020X	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	SPACE
021X	F7	F7	F7	F7	F7	FF	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	!
022X	EB	EB	EB	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	"
023X	EB	EB	80	EB	80	EB	EB	FF	FF	FF	FF	FF	FF	FF	FF	FF	#
024X	EB	81	EA	C1	AB	C0	EB	FF	FF	FF	FF	FF	FF	FF	FF	FF	$
025X	BD	DA	ED	F7	DB	AD	DE	FF	FF	FF	FF	FF	FF	FF	FF	FF	%

Table A-1. Character Generator Contents (Continued)

Address ASCII CODE	Character Line Number 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHAR
026X	F3	ED	ED	F1	CE	DE	A1	FF	FF	FF	FF	FF	FF	FF	FF	FF	&
027X	F7	FB	FD	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	'
028X	F7	FB	FD	FD	FD	FB	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	⊂
029X	F7	EF	DF	DF	DF	EF	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	⊃
02AX	F7	B6	D5	E3	D5	B6	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	*
02BX	FF	F7	F7	C1	F7	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	+
02CX	FF	FF	FF	FF	FF	F9	F9	FB	FD	FF	FF	FF	FF	FF	FF	FF	,
02DX	FF	FF	FF	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	-
02EX	FF	FF	FF	FF	FF	F9	F9	FF	FF	FF	FF	FF	FF	FF	FF	FF	.
02FX	BF	DF	EF	F7	FB	FD	FE	FE	FF	FF	FF	FF	FF	FF	FF	FF	/
030X	C1	9E	AE	B6	BA	BC	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	0
031X	F7	F3	F5	F7	F7	F7	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	1
032X	C1	BE	DF	E3	FD	FE	80	FF	FF	FF	FF	FF	FF	FF	FF	FF	2
033X	C1	BE	BF	C7	BF	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	3
034X	EF	E7	EB	ED	80	EF	EF	FF	FF	FF	FF	FF	FF	FF	FF	FF	4
035X	80	FE	FE	C0	BF	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	5
036X	83	FD	FE	C0	BE	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	6
037X	80	DF	EF	F7	FB	FD	FD	FF	FF	FF	FF	FF	FF	FF	FF	FF	7
038X	C1	BE	BE	C1	BE	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	8
039X	C1	BE	BE	81	BF	DF	E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	9
03AX	FF	FF	F3	F3	FF	F3	F3	FF	FF	FF	FF	FF	FF	FF	FF	FF	:
03BX	FF	FF	F3	F3	FF	F3	F3	F7	FB	FF	FF	FF	FF	FF	FF	FF	;
03CX	EF	F7	FB	FD	FB	F7	EF	FF	FF	FF	FF	FF	FF	FF	FF	FF	<
03DX	FF	FF	C1	FF	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	=
03EX	FB	F7	EF	DF	EF	F7	FB	FF	FF	FF	FF	FF	FF	FF	FF	FF	>
03FX	C1	BE	BF	CF	F7	FF	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	?
040X	C1	BE	B6	86	E6	FE	81	FF	FF	FF	FF	FF	FF	FF	FF	FF	@
041X	F7	EB	DD	BE	80	BE	BE	FF	FF	FF	FF	FF	FF	FF	FF	FF	A
042X	C0	BE	BE	C0	BE	BE	C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	B
043X	C1	BE	FE	FE	FE	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	C
044X	C0	BD	BD	BD	BD	BD	C0	FF	FF	FF	FF	FF	FF	FF	FF	FF	D
045X	80	FE	FE	F0	FE	FE	80	FF	FF	FF	FF	FF	FF	FF	FF	FF	E
046X	80	FE	FE	F0	FE	FE	FE	FF	FF	FF	FF	FF	FF	FF	FF	FF	F
047X	C1	BE	FE	FE	86	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	G
048X	BE	BE	BE	80	BE	BE	BE	FF	FF	FF	FF	FF	FF	FF	FF	FF	H
049X	E3	F7	F7	F7	F7	F7	E3	FF	FF	FF	FF	FF	FF	FF	FF	FF	I
04AX	8F	DF	DF	DF	DE	DE	E1	FF	FF	FF	FF	FF	FF	FF	FF	FF	J
04BX	DE	EE	F6	Fa	F4	EE	DE	FF	FF	FF	FF	FF	FF	FF	FF	FF	K
04CX	FE	FE	FE	FE	FE	FE	80	FF	FF	FF	FF	FF	FF	FF	FF	FF	L
04DX	BE	9C	AA	B6	B6	BE	BE	FF	FF	FF	FF	FF	FF	FF	FF	FF	M
04EX	BE	BC	BA	B6	Ae	9E	BE	FF	FF	FF	FF	FF	FF	FF	FF	FF	N
04FX	C1	BE	BE	BE	BE	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	O
050X	C0	BE	BE	C0	FE	FE	FE	FF	FF	FF	FF	FF	FF	FF	FF	FF	P
051X	E3	DD	BE	BE	AE	DD	A3	FF	FF	FF	FF	FF	FF	FF	FF	FF	Q
052X	C0	BE	BE	C0	EE	DE	BE	FF	FF	FF	FF	FF	FF	FF	FF	FF	R
053X	C1	BE	FE	C1	BF	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	S
054X	80	F7	F7	F7	F7	F7	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	T
055X	BE	BE	BE	BE	BE	BE	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	U
056X	BE	BE	BE	BE	DD	EB	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	V
057X	BE	BE	BE	B6	B6	AA	DD	FF	FF	FF	FF	FF	FF	FF	FF	FF	W
058X	BE	DD	EB	F7	EB	DD	BE	FF	FF	FF	FF	FF	FF	FF	FF	FF	X

Table A-1. Character Generator Contents (Continued)

Address ASCII CODE	Character Line Number 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	CHAR
059X	BE	BE	DD	EB	F7	F7	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	Y
05AX	80	DF	EF	F7	FB	FD	80	FF	FF	FF	FF	FF	FF	FF	FF	FF	Z
05BX	E0	FC	FC	FC	FC	FC	E0	FF	FF	FF	FF	FF	FF	FF	FF	FF	[
05CX	FE	FD	FB	F7	EF	DF	BF	FF	FF	FF	FF	FF	FF	FF	FF	FF	\
05DX	83	9F	9F	9F	9F	9F	83	FF	FF	FF	FF	FF	FF	FF	FF	FF	]
05EX	FF	F7	EB	DD	BE	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	^
05FX	FF	FF	FF	80	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	—
060X	FD	FB	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	`
061X	FF	FF	C3	BF	83	BD	83	FF	FF	FF	FF	FF	FF	FF	FF	FF	a
062X	FD	FD	FD	C1	BD	BD	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	b
063X	FF	FF	C3	BD	FD	BD	C3	FF	FF	FF	FF	FF	FF	FF	FF	FF	c
064X	BF	BF	BF	83	BD	BD	83	FF	FF	FF	FF	FF	FF	FF	FF	FF	d
065X	FF	FF	C3	BD	C1	FD	83	FF	FF	FF	FF	FF	FF	FF	FF	FF	e
066X	CF	B7	F7	E3	F7	F7	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	f
067X	FF	FF	83	BD	BD	83	BF	BF	C1	FF	FF	FF	FF	FF	FF	FF	g
068X	FD	FD	C5	B9	BD	BD	BD	FF	FF	FF	FF	FF	FF	FF	FF	FF	h
069X	FF	F7	FF	F7	F7	F7	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	i
06AX	FF	BF	FF	BF	BF	BF	BF	BD	C3	FF	FF	FF	FF	FF	FF	FF	j
06BX	FD	DD	ED	F5	E9	DD	BD	FF	FF	FF	FF	FF	FF	FF	FF	FF	k
06CX	F7	F7	F7	F7	F7	F7	EF	FF	FF	FF	FF	FF	FF	FF	FF	FF	l
06DX	FF	FF	C9	B6	B6	B6	B6	FF	FF	FF	FF	FF	FF	FF	FF	FF	m
06EX	FF	FF	C5	B9	BD	BD	BD	FF	FF	FF	FF	FF	FF	FF	FF	FF	n
06FX	FF	FF	C3	BD	BD	BD	C3	FF	FF	FF	FF	FF	FF	FF	FF	FF	o
070X	FF	FF	C1	BD	BD	C1	FD	FD	FD	FF	FF	FF	FF	FF	FF	FF	p
071X	FF	FF	83	BD	BD	83	BF	BF	BF	FF	FF	FF	FF	FF	FF	FF	q
072X	FF	FF	C5	B9	FD	FD	FD	FF	FF	FF	FF	FF	FF	FF	FF	FF	r
073X	FF	FF	83	FD	C3	BF	C1	FF	FF	FF	FF	FF	FF	FF	FF	FF	s
074X	FF	FB	FB	E0	FB	FB	C7	FF	FF	FF	FF	FF	FF	FF	FF	FF	t
075X	FF	FF	BD	BD	BD	BD	A3	FF	FF	FF	FF	FF	FF	FF	FF	FF	u
076X	FF	FF	DD	DD	EB	F7	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	v
077X	FF	FF	BE	B6	B6	AA	DD	FF	FF	FF	FF	FF	FF	FF	FF	FF	w
078X	FF	FF	DD	EB	F7	EB	DD	FF	FF	FF	FF	FF	FF	FF	FF	FF	x
079X	FF	FF	BD	BD	BD	83	BF	BF	C1	FF	FF	FF	FF	FF	FF	FF	y
07AX	FF	FF	81	DF	EF	F7	83	FF	FF	FF	FF	FF	FF	FF	FF	FF	z
07BX	C7	FB	FB	FD	FB	FB	C7	FF	FF	FF	FF	FF	FF	FF	FF	FF	{
07CX	F7	F7	F7	FF	F7	F7	F7	FF	FF	FF	FF	FF	FF	FF	FF	FF	|
07DX	F1	EF	EF	DF	EF	EF	F1	FF	FF	FF	FF	FF	FF	FF	FF	FF	}
07EX	FF	FF	F9	B6	CF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	~
07FX	00	00	00	00	00	00	00	00	00	00	00	FF	FF	FF	FF	FF	GC32

APPENDIX B
CRT AND KEYBOARD CONNECTOR CONFIGURATIONS

B-1. INTRODUCTION

This appendix describes several different configurations for keyboards and CRTs that have been checked by Intel for compatibility with the iSBX 270 VDTC board. This information is for reference only. Refer to manufactures documentation for details. Table B-1 lists the manufacturer's addresses.

B-2. KEYBOARD CONNECTOR CONFIGURATIONS

The following tables describe some of the possible keyboard configurations. Any connector positions that are not listed should be left open. Figure B-1 shows the orientation for all the keyboard reference numbering drawings.

NOTE

Connector numbering may not agree with keyboard numbering.

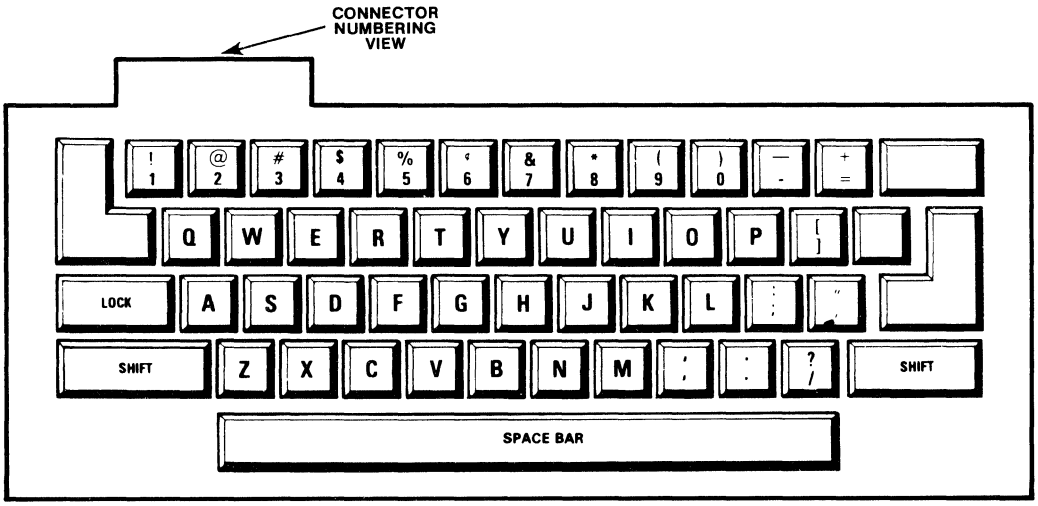


Figure B-1. Keyboard Connector Numbering Orientation

KEYBOARD TYPE: ADVANCED INPUT DEVICES SK-067
KEYBOARD CONNECTOR TYPE: 25 position single readout

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	14	Ground	2	15	+5V
3		Ground	4		+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10		KEYACK/
11		Ground	12	11	STROBE
13		Ground	14	10	CNTL 0
15		KBRST/	16		CNTL1
17	7	B6	18	5	B4
19	3	B2	20	1	B0
21	8	B7	22	6	B5
23	4	B3	24		+12V
25	13	-12V	26	2	B1

Keyboard Numbering:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

KEYBOARD TYPE: CHERRY B70-05AB
KEYBOARD CONNECTOR TYPE: 22 position, double readout edge connector

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	P	Ground	2	M	+5V
3	13	Ground	4	11	+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10		KEYACK/
11		Ground	12	16	STROBE
13		Ground	14	22	CNTL 0
15		KBRST/	16	18	CNTL1
17	7	B6	18	5	B4
19	3	B2	20	1	B0
21	8	B7	22	6	B5
23	4	B3	24		+12V
25		-12V	26	2	B1

Keyboard	Z	Y	X	W	V	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A
Numbering:	22	21	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

KEYBOARD TYPE: CHERRY CB80-07AA
KEYBOARD CONNECTOR TYPE: 22 position, double readout edge connector

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	21	Ground	2	Z	+5V
3	Y	Ground	4	22	+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10		KEYACK/
11		Ground	12	U	STROBE
13		Ground	14	W	CNTL 0
15		KBRST/	16		CNTL1
17	3	B6	18	5	B4
19	7	B2	20	9	B0
21	2	B7	22	4	B5
23	6	B3	24		+12V
25		-12V	26	8	B1

Keyboard	Z	Y	X	W	V	T	S	R	P	N	M	L	K	J	H	F	E	D	C	B	A
Numbering:	22	21	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

KEYBOARD TYPE: CHOMERICS AN26109 keyboard with AE26203 encoding module
KEYBOARD CONNECTOR TYPE: 16 pin IC socket

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Function Connector	
1	2	Ground	2	R	+5V
3		Ground	4		+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10		KEYACK/
11		Ground	12	3	STROBE
13		Ground	14	7	CNTL 0
15		KBRST/	16	8	CNTL1
17	15	B6	18	13	B4
19	11	B2	20	9	B0
21	16	B7	22	14	B5
23	12	B3	24		+12V
25	4	-12V	26	10	B1

NOTE:
To obtain true ASCII characters the B7 bit must be masked. The strobe from this keyboard is positive.

KEYBOARD TYPE: CORTRON 35-500014
KEYBOARD CONNECTOR TYPE: Berg 20 pin header

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	19	Ground	2	18	+5V
3	17	Ground	4	20	+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10	9	KEYACK/
11		Ground	12	3	STROBE
13		Ground	14		CNTL 0
15		KBRST/	16		CNTL1
17	10	B6	18	8	B4
19	7	B2	20	2	B0
21	11	B7	22	6	B5
23	4	B3	24		+12V
25		-12V	26	1	B1

NOTE:
Cut trace on keyboard at U8-15 to inhibit second strobe generated from key release. Data from keyboard is non ASCII encoded and is inverted.

Keyboard										
Numbering:	19	17	15	13	11	9	7	5	3	1
	20	18	16	14	12	10	8	6	4	2

KEYBOARD TYPE: KEYTRONIC L1648
KEYBOARD CONNECTOR TYPE: 12 position edge connector, double readout

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	1	Ground	2	2	+5V
3		Ground	4		+5V
5		Ground	6		LPEN
7		Ground	8	BSTB/	
9		Ground	10		KEYACK/
11		Ground	12	D	STROBE
13		Ground	14	J	CNTL 0
15		KBRST/	16	K	CNTL1
17	9	B6	18	11	B4
19	5	B2	20	7	B0
21	3	B7	22	10	B5
23	4	B3	24		+12V
25		-12V	26	6	B1

NOTE:
Keyboard does not have lower case alpha.

Keyboard												
Numbering:	N	M	L	K	H	G	F	E	D	C	B	A
	12	11	10	9	8	7	6	5	4	3	2	1

KEYBOARD TYPE: KEYTRONIC L1660
KEYBOARD CONNECTOR TYPE: 10 position edge connector, double readout

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	C	Ground	2	B	+5V
3	D	Ground	4	9	+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10		KEYACK/
11		Ground	12	F	STROBE
13		Ground	14		CNTL 0
15		KBRST/	16		CNTL1
17	6	B6	18	8	B4
19	2	B2	20	4	B0
21	5	B7	22	7	B5
23	1	B3	24		+12V
25	A	-12V	26	3	B1

Keyboard	L	K	J	H	F	E	D	C	B	A
Numbering:	10	9	8	7	6	5	4	3	2	1

KEYBOARD TYPE: KEYTRONIC L1674-03
KEYBOARD CONNECTOR TYPE: 10 position edge connector, double readout

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	4	Ground	2	6	+5V
3		Ground	4		+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10		KEYACK/
11		Ground	12	A	STROBE
13		Ground	14	B	CNTL 0
15		KBRST/	16	C	CNTL1
17	E	B6	18	F	B4
19	L	B2	20	9	B0
21	10	B7	22	H	B5
23	K	B3	24		+12V
25		-12V	26	J	B1

NOTE:
Data from keyboard is non ASCII encoded and is inverted.

Keyboard	L	K	J	H	F	E	D	C	B	A
Numbering:	10	9	8	7	6	5	4	3	2	1

KEYBOARD TYPE: KEYTRONIC L1752
KEYBOARD CONNECTOR TYPE: 10 position edge connector, double readout

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	2	Ground	2	1	+5V
3	B	Ground	4	A	+5V
5		Ground	6		LPEN
7		Ground	8	BSTB/	
9		Ground	10		KEYACK/
11		Ground	12	7	STROBE
13		Ground	14	11	CNTL 0
15		KBRST/	16	8	CNTL1
17	6	B6	18	5	B4
19	4	B2	20	3	B0
21	F	B7	22	E	B5
23	D	B3	24		+12V
25		-12V	26	C	B1

Keyboard Numbering:	1	2	3	4	5	6	7	8	9	10	11	12
	A	B	C	D	E	F	H	J	K	L	M	N

KEYBOARD TYPE: MICROSWITCH 66SD6-7
KEYBOARD CONNECTOR TYPE: 10 position edge connector, double readout

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	3	Ground	2	1	+5V
3	4	Ground	4	2	+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10		KEYACK/
11		Ground	12	12	STROBE
13		Ground	14	5	CNTL 0
15		KBRST/	16		CNTL1
17	L	B6	18	J	B4
19	F	B2	20	D	B0
21	M	B7	22	K	B5
23	H	B3	24		+12V
25	6	-12V	26	E	B1

Keyboard Numbering:	N	M	L	K	J	H	F	E	D	C	B	A
	12	11	10	9	8	7	6	5	4	3	2	1

KEYBOARD TYPE: MICROSWITCH 87SD30-8
KEYBOARD CONNECTOR TYPE: 26 pin header

iSBX 270 VDTC Connector J1	Keyboard Connector	Function	iSBX 270 VDTC Connector J1	Keyboard Connector	Function
1	14	Ground	2	16	+5V
3	15	Ground	4	17	+5V
5		Ground	6		LPEN
7		Ground	8		BSTB/
9		Ground	10	24	KEYACK/
11		Ground	12	25	STROBE
13		Ground	14		CNTL 0
15	16	KBRST/	16		CNTL1
17	7	B6	18	5	B4
19	3	B2	20	1	B0
21	8	B7	22	6	B5
23	4	B3	24		+12V
25		-12V	26	2	B1

Keyboard Numbering:

13	12	11	10	9	8	7	6	5	4	3	2	1
o	o	o	o	o	o	o	o	o	o	o	o	o
o	o	o	o	o	o	o	o	o	o	o	o	o
26	25	24	23	22	21	20	19	18	17	16	15	14

B-3. BLACK AND WHITE CRT CONNECTOR CONFIGURATIONS

The following table describes some of the possible black and white CRT connector configurations. Any connector positions that are not listed should be left open.

CRT TYPE: BALL BROTHERS TTL 120, TV 120, TV 50 Black and white
MOTOROLA M3570 Black and white
TSD MDC-15 black and white
ELSTON DM30-12B0-51-A04 high resolution black and white
CRT CONNECTOR TYPE: 10 pin edge connector — Cinch 251-10-90-160 or equivalent

iSBX 270 VDTC Connector J2	CRT Connector	Function	iSBX 270 VDTC Connector J2	CRT Connector	Function
1		Ground	2	-12V	
3		Ground	4		+5V
5		Ground	6		+5V
7		Ground	8		+12V
9	1	Ground	10	8	VIDEO
11		Ground	12		G VIDEO
13		Ground	14		B VIDEO
15		Ground	16		R VIDEO
17	5	Ground	18	6	HSYNC
19		Ground	20		GPA1
21		Ground	22		HLGT
23	10	Ground	24	9	VSYNC/
25		Ground	26		GPA0

NOTES:
Use twisted pair between CRT pins 8 and 10, 6 and 10, and 9 and 10. Place a 150 ohm resistor between CRT pins 8 and 10 on all except Motorola. for CRT TV 120, 12 or 15 volt dc power must be supplied to pins 1 and 7. External brightness control is option (user supplied and installed.)

Keyboard Numbering:

10	9	8	7	6	5	4	3	2	1

B-4. COLOR CRT CONNECTOR CONFIGURATIONS

The following table describes some of the possible COLOR CRT connector configurations. Any connector positions that are not listed should be left open.

CRT TYPE: BALL BROTHERS 7-015-0131 color
INDUSTRIAL DATA TERMINALS 19AC color
CONRAC 5711C13 color
CRT CONNECTOR TYPE: Coax/BNC

iSBX 270 VDTC Connector J2	Function	iSBX 270 VDTC Connector J2	Function
12	G VIDEO	14	B VIDEO
16	R VIDEO	18	CSYNC/

NOTES:
Use 75 ohm coax for all connections.

CRT TYPE: NEC 1202DH Color
CRT CONNECTOR: Coax/Special (supplied with monitor)

iSBX 270 VDTC Connector J2	CRT Connector	Function
11	1	Ground
12	3*	G Video
13	5	Ground
14	4*	B Video
15	6	Ground
16	2*	R Video
18	7 & 8*	CSYNC/

*Connect a 75 ohm, ¼ watt resistor from the indicated pin to ground for termination.

Manufacturer's References

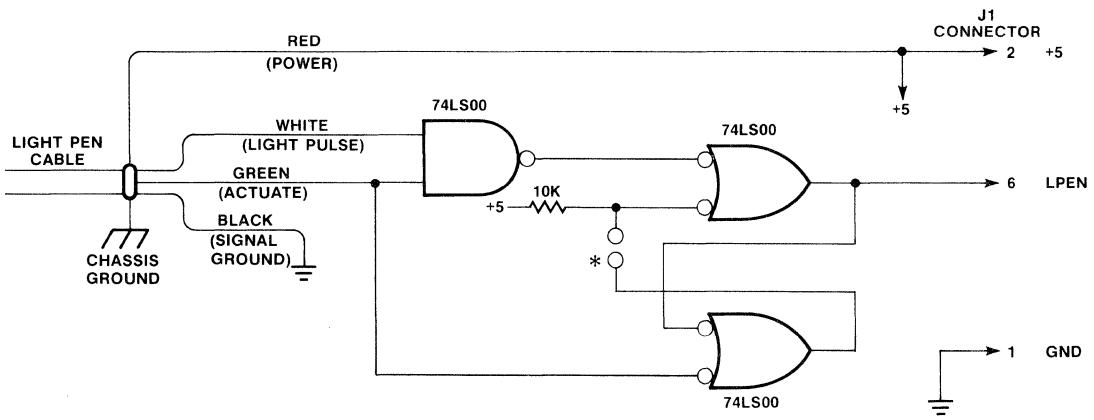
Advanced Input Devices	Advanced Input Devices Box 1818 Coeur d'Alene, Idaho 83814
Cherry	Cherry Electrical Products Corp. 3600 Sunset Ave. Waukegan, Illinois 60085
Chomerics	Chomerics 77 Dragon Court Woburn, Massachusetts 01888
Cortron	Cortron 400 W. Grand Ave. Elmhurst, Illinois 60126
Keytronic	Keytronic International Keyboards P.O. Box 14687 Spokane, Washington 99214
Microswitch	Microswitch Freeport, Illinois 60132
Ball Brothers	Ball Electronic Display Division P.O. Box 43376 St. Paul, Minnesota 55164

Motorola	Motorola Display Systems 1155 Harvester Road West Chicago, Illinois 60185
TSD	TSD Display Products, Inc. 35 Orville Drive Bohemia, New York 11716
Elston	Elston Electronics, Inc. 27 E. Main Street Phelps, New York 14532
Industrial Data Terminals	Industrial Data Terminals Corp. 1550 W. Henderson Road Columbus, Ohio 43220
Conrac	Conrac Division Conrac Corp. 600 N. Rimsdale Avenue Covina, California 91722
NEC	NEC America Inc. 130 Martin Lane Elk Grove Village, Illinois 60007
Information Control Corp.	Information Control Corp. 9610 Bellanca Avenue Los Angeles, California 90045
Electrahome	Electrahome Electronics 809 Wellington Street, N. Kitchener, Ontario, Canada N2G4J6

B-5. LIGHT PEN CONNECTIONS

TYPE: INFORMATION CONTROL
LP-770-P-LH-AH-R

Light Pen Cable is supplied without a connector. The following gating circuit is required:



***NOTES:**

The light pen tip is touch-activated. If the indicated jumper is installed, one light pen "hit" will be registered when the light pen is touched to the screen. In order to register another hit, the pen tip must be raised from the screen and reactuated. If the indicated jumper is removed, multiple light pen hits will be registered (one per frame) allowing the selected symbol to be "dragged".

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