401 FLOPPY DISK CONTROLLER 8"
JA - ETCHED \ADDRESS 80\}
JB - 5 ONLY \VECTOR INTERRUPT VI5\}
JC - 1 AND 6 \WRITE PRECOMPENSATION 125ns\}
JD - ON FOR NO MOTOR CONTROL
OFF FOR MOTOR CONTROL

431 FLOPPY DISK CONTROLLER 5"
JA - TO RIGHT \ADDRESS C0\}
JB - 5 ONLY \VECTOR INTERRUPT VI5\}
JC - OFF FOR SINGLE SIDED
ON FOR DOUBLE SIDED

444 I/O BOARD (STANDARD SHUNTING)
JA - TOP \PARALLEL PORT A SELECT -OUTPUT MODE-\}
JB - OFF \PARALLEL PORT B SELECT -INPUT MODE-\}
JC - PC0 1-2 & 31-32 ON VERTICALLY \PARALLEL PORT &
PC4 NO SHUNTS !!!!
PC6 13-20 & 14-19 ON HORIZONTALLY HORZ.=INPUT\}
JD - \2708 EPROM\} LEFT TO CENTER
JD - \2716 EPROM\} TOP TO CENTER
JD - \2732 EPROM\} BOTTOM TO CENTER
JE - \2708 EPROM\} TO LEFT
JE - \2716 OR 2732 EPROM\} TO RIGHT
JF - \2708 EPROM\} BOTH PAIRS VERTICALLY CONNECTED
JF - \2716 EPROM\} RIGHT PAIR VERTICALLY CONNECTED
JF - \2732 EPROM\} NONE CONNECTED
JG - \2708 EPROM\}
ALL ON HORIZONTALLY
JG - \2716 EPROM\}
TOP 5 ON HORIZONTALLY
A10 OFF
RE ON \ROM ENABLED\}
JG - \2732 EPROM\}
TOP 4 ON HORIZONTALLY
A9 OFF
A10 OFF
RE ON \ROM ENABLED\}
JH - BOTTOM \ON BOARD TIMER CLOCK\}
JJ - 1 \RELATIVE TIME CLOCK INTERRUPT VI7\}
JK - 3 \UART 0 TRANSMIT/RECEIVE INTERRUPT VI3\}
JL - 3 \UART 1 TRANSMIT/RECEIVE INTERRUPT VI3\}
JI - NONE \PARALLEL PORT B INTERRUPT\}
JB - NONE \PARALLEL PORT A INTERRUPT\}
JP - A5,A6,A7 \I/O DEVICE SELECT ADDRESS 10\}

444 I/O (SHUNTED FOR NEC PRINTER)
SAME AS STANDARD EXCEPT:
JB = ON \{PARALLEL PORT B OUTPUT MODE\}
JC = ALL ON HORIZONTALLY \{PARALLEL PORT C INPUT MODE\}
ALSO: INSTALL A 330 OHM RESISTOR PACK AT LOCATION 12A

444 I/O (2ND BOARD)
SAME AS FIRST BOARD EXCEPT:
JG = TOP 5 ON HORIZONTALLY
RE OFF \{DISABLE ROM\}
JP = A4, A5, A7 \{I/O DEVICE SELECT ADDRESS 40\}
NO ROM INSTALLED

451 80 PROCESSOR
JA = NONE \{START UP ADDRESS 00\}

465 64K D RAM 1ST BOARD
JA = ON CENTER & BOTTOM \{MEMORY SPEED 125ns RAM\}
JB = ON \{ENABLE I/O\}
JC = ALL ON \{I/O ADDRESS 00\}
JD = ON \{PHANTOM LINE\}
JE = OFF \{NORMAL MODE\}
JF = OFF \{8080 SHUNT -OFF FOR 8080 PROCESSOR-\}
JG = VI 2 ONLY \{PARITY VECTOR INTERRUPT VI2\}
JH = ON CENTER & LEFT \{INSAI FRONT PANEL SHUNT\}

465 64K D RAM 2ND BOARD
SAME AS FIRST BOARD EXCEPT:
JC = 0 OFF ALL OTHERS ON \{I/O ADDRESS 01\}
JE = OFF \{BANK MODE ENABLED FOR OLD MPU SYSTEMS ONLY\}
JG = ALL OFF \{NO PARITY VECTOR INTERRUPT\}

465 64K D RAM 3RD BOARD
SAME AS 2ND BOARD EXCEPT:
JC = 1 OFF ALL OTHERS ON \{I/O ADDRESS 02\}

465 64K D RAM 4TH BOARD
SAME AS SECOND BOARD EXCEPT:
JC = 0 & 1 OFF ALL OTHERS ON \{I/O ADDRESS 03\}
ETC.

480 4SI/O (1ST BOARD) ------ A OR C OPTION SYSTEMS
JA = 6 & 7 ONLY \{I/O ADDRESS 20\}
JB = BOTTOM HORIZONTALLY \{ON BOARD OSCILLATOR\}
JC = 3 ONLY \{UART 0 VECTOR INTERRUPT VI3\}
JD = 3 ONLY \{UART 1 VECTOR INTERRUPT VI3\}
JE = 3 ONLY \{UART 2 VECTOR INTERRUPT VI3\}
JF = 3 ONLY \{UART 3 VECTOR INTERRUPT VI3\}

480 4SI/O (2ND BOARD) ------ A OR C OPTION
SAME AS FIRST BOARD EXCEPT:
JA = NO SHUNTS \{I/O ADDRESS E0\}

480 4SI/O ------ B OPTION OR WITH 971

BD8HUNT,LST   PG. 2   12/10/85
JA = NO SHUNTS \[I/O ADDRESS EO\]
ALL OTHER SHUNTS SAME AS C OPTION SYSTEM

480 4SI/O 1270 280B SYSTEM
JA = NO SHUNTS \[I/O ADDRESS EO\]
JB = BOTTOM HORIZONTALLY \[ON BOARD OSCILLATOR\]
JC = 2 ONLY \[UART 0 VECTOR INTERRUPT 2\]
JD = 2 ONLY \[UART 1 VECTOR INTERRUPT 2\]
JE = 2 ONLY \[UART 2 VECTOR INTERRUPT 2\]
JF = 2 ONLY \[UART 3 VECTOR INTERRUPT 2\]

491 CMD HARD DISK CONTROLLER
JD = 4 ONLY \[VECTOR INTERRUPT VI4\]
NOTE: INSTALL ILP-H EPROM ON (645,971, OR 444)

631 SPIO-B-BD (STANDARD SHUNTING) ----- B OPTION SYSTEM
JA = A7,A6 ON \[I/O ADDRESS 20\]
JB = PC6 3-30 & 4-29 ON HORIZONTALLY \[PARALLEL PORT C \PC4 NO SHUNTS ! ! ! !
PC0 15-16 & 17-18 ON VERTICALLY HORZ.=INPUT\}
JC = NONE \[PARALLEL PORT A DRIVER/RECEIVER -OUTPUT MODE-\}
JD = ON \[PARALLEL PORT B DRIVER/RECEIVER -INPUT MODE-\}
JE = VI2 \[UART 0 VECTOR INTERRUPT VI3\]
JG = VI2 \[UART 1 VECTOR INTERRUPT VI3\]
JH = NONE \[PARALLEL PORT B VECTOR INTERRUPT\}
JJ = NONE \[PARALLEL PORT A VECTOR INTERRUPT\}

631 SPIO-B-BD ----- B OPTION SYSTEM (SHUNTED FOR NEC PRINTER)
SAME AS STANDARD SHUNTING EXCEPT:
JB = ALL ON HORIZONTALLY \[PARALLEL PORT C INPUT MODE-\}
JD = OFF \[PARALLEL PORT B DRIVER/RECEIVER -OUTPUT MODE-\}

631 SPIO-B-BD ----- C OPTION OR WITH 971
SAME AS B OPTION AND NEC SHUNTING EXCEPT:
JA = NONE \[I/O ADDRESS EO\}

631 SPIO-B-BD ----- 1270 280B SYSTEM
JA = A7,A6 OFF \[I/O ADDRESS EO\}
JB = PC6 3-30 & 4-29 ON HORIZONTALLY \[PARALLEL PORT C \PC4 NO SHUNTS ! ! ! !
PC0 15-16 & 17-18 ON VERTICALLY HORZ.=INPUT\}
JC = NONE \[PARALLEL PORT A DRIVER/RECEIVER -OUTPUT MODE-\}
JD = ON \[PARALLEL PORT B DRIVER/RECEIVER -INPUT MODE-\}
JE = VI2 \[UART 0 VECTOR INTERRUPT VI2\]
JG = VI2 \[UART 1 VECTOR INTERRUPT VI2\]
JH = NONE \[PARALLEL PORT B VECTOR INTERRUPT\}
JJ = NONE \[PARALLEL PORT A VECTOR INTERRUPT\}

645 ZPU-B-BD
2716 – SHUNT NEAT TO R0H IS IN "16" POSITION
2732 – SHUNT NEAT TO R0H IS IN "32" POSITION
662 VIDEO DISPLAY BOARD
JA = ETCHED \( RS232 \) INPUT
JB = 2-3 \( \text{HORIZONTAL SYNC POLARITY} - + \) PLUS - \( \text{MINUS} - \)\)
JC = 1-2 \( \text{VERTICALLY SYNC POLARITY} - + \) PLUS - \( \text{MINUS} - \)\)
JD = ETCHED \( \text{CHARACTER GENERATOR FOR 2715 EPROM} \)
DIP SWITCH SW1
1 - OFF \( 9600 \) BAUD RATE
2 - ON \( \) BAUD RATE
3 - ON \( \) BAUD RATE
4 - ON \( \) BAUD RATE
5 - ON \( \) BAUD RATE
6 - OFF \( \) BAUD RATE
7 - ON \( \) BAUD RATE
8 - ON/OFF \( \) BAUD RATE
DIP SWITCH SW2
1 - OFF \( 7 \) BITS
2 - ON \( \) BITS
3 - ON \( \) BITS
4 - ON \( \) BITS
5 - ON \( \) BITS
6 - ON \( \) BITS
7 - OFF \( \) BITS
8 - ON \( \) BITS

801 8" WINCHESTER INTERFACE CARD
JA = WINCH UNIT SELECT
1 = WINCH UNIT 0
2 = WINCH UNIT 1
3 = WINCH UNIT 2
4 = WINCH UNIT 3
NOTE: ON MULTIPLEXED WINCH SYSTEMS REMOVE THE 220/330 OHM RESISTOR PACK AT LOCATION 3A ON THE INTERFACE CARDS NOT LOCATED AT THE END OF THE DATA CABLE

820-5 5" WINCHESTER DISK CONTROLLER
ADRS = ETCHED \( I/O \) ADDRESS A0
ECC = TOP \( \text{ECC RUN} \)
INT = ETCHED \( \text{VECTOR INTERRUPT VI4} \)

821-5 5" WINCHESTER DISK CONTROLLER
ADRS = TOP \( I/O \) ADDRESS A0
ECC = TOP \( \text{ECC RUN} \)
INT = ETCHED \( \text{VECTOR INTERRUPT VI4} \)

820-8 8"WINCHESTER DISK CONTROLLER
ADRS = TOP \( I/O \) ADDRESS A8
ECC = TOP \( \text{RUN ECC} \)
INT = ETCHED \( \text{VECTOR INTERRUPT VI4} \)

821-8 8" WINCHESTER DISK CONTROLLER
ADRS = BOTTOM \( I/O \) ADDRESS A8
ECC = TOP \( \text{RUN ECC} \)
INT = ETCHED \( \text{VECTOR INTERRUPT VI4} \)
900 5" WINCHESTER INTERFACE BOARD
JA - WINCH UNIT SELECT
  1 = WINCH UNIT 0
  2 = WINCH UNIT 1
  3 = WINCH UNIT 2
  4 = WINCH UNIT 3

NOTE: ON MULTI-WINCH SYSTEMS REMOVE THE 220/330 OHM RESISTOR PACK AT LOCATION 3A ON THE INTERFACE CARDS NOT LOCATED AT THE END OF THE DATA CABLE
862 I/O PROCESSOR
JA - ON 1-16 \SIO PORT A RECEIVE/TRANSMIT BAUD CLOCK RS232\)
JB - ON 1-4 \SIO PORT B RECEIVE/TRANSMIT BAUD CLOCK RS232\)
JD - OFF \RESET DISABLE\)
JE - \I/O ADDRESS SELECTION\)
---STARTING FROM THE TOP SHUNT---

<table>
<thead>
<tr>
<th>BOARD #</th>
<th>I/O ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>1</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>2</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>3</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>4</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>5</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>6</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>7</td>
<td>ON-OFF-ON-ON-ON-ON-ON</td>
</tr>
<tr>
<td>8</td>
<td>OFF-OFF-OFF-ON-ON-ON</td>
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<tr>
<td>9</td>
<td>OFF-OFF-OFF-ON-ON-ON</td>
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<tr>
<td>10</td>
<td>OFF-OFF-OFF-ON-ON-ON</td>
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<tr>
<td>11</td>
<td>OFF-OFF-OFF-ON-ON-ON</td>
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<tr>
<td>12</td>
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<tr>
<td>13</td>
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</tr>
<tr>
<td>14</td>
<td>OFF-OFF-OFF-ON-ON-ON</td>
</tr>
<tr>
<td>15</td>
<td>OFF-OFF-OFF-ON-ON-ON</td>
</tr>
</tbody>
</table>

\CAUTION: THE 9th 862 ADDRESS E0 WILL CONFLICT WITH:
B OPTION SYSTEMS WITH A 480
C OPTION SYSTEMS WITH A 631
971 SYSTEM WITH A 480 OR 631

862 8 BIT CPU SET UP FOR RS422
JA - ON 2-15 ONLY (JA 1-2 ETCH IS CUT ON BACK OF BOARD)
JB - ON 2-3 ONLY

881 8088 16 BIT PROCESSOR
JA - BOTTOM \SELECT 2732/64 EPROM\)

930-5 5"FLOPPY DISK CONTROLLER
JA - TOP/BOTTOM \TOP IF USING A 645 OR 971 CPU\)
\BOTTOM IF USING A 451 CPU\)
JB - ETCHED \VECTOR INTERRUPT VI5\)
SW1 - \SEE 930 WRITE UP FOR SWITCH FUNCTIONS\)
DRIVE SW1-1 SW1-2 SW1-3 SW1-4 SW1-5 SW1-6 SW1-7 SW1-8
5"DS 36TPI ON OFF ON OFF ON OFF OFF ON
5"DS 48TPI ON OFF OFF ON ON OFF OFF ON
5"DS 48/96 ON OFF ON ON OFF OFF ON
SW2 - \WRITE PRECOMPENSATION 0\)
SW2-1 SW2-2 SW2-3 SW2-4 SW2-5 SW2-6 SW2-7 SW2-8
OFF OFF OFF ON ON OFF OFF OFF
930-8  8" FLOPPY DISK CONTROLLER
  JA - TOP/BOTTOM {TOP IF USING A 645 OR 971 CPU}
  {BOTTOM IF USING A 451}
  JB - ETCHED \VECTOR INTERRUPT VI5}
  SW1 - \SEE 930 WRITE UP FOR SWITCH FUNCTIONS}
  DRIVE  SW1-1 SW1-2 SW1-3 SW1-4 SW1-5 SW1-6 SW1-7 SW1-8
  8"DS ON OFF OFF ON OFF ON OFF ON
  8"SS ON ON ON OFF OFF ON OFF ON
  SW2 - \WRITE PRECOMPENSATION 125ns}
  SW2-1 SW2-2 SW2-3 SW2-4 SW2-5 SW2-6 SW2-7 SW2-8
  OFF ON OFF OFF ON OFF ON

961  256K DYNAMIC RAM ----- (1st BOARD)
  JA - 1 \BOARD ADDRESS 00000-3FFF]
  JB - ON \PARITY VECTOR INTERRUPT VI2]
  JC - OFF \PHANTOM LINE}
  JD - ALL ON \I/O PORT ADDRESS 00}

961  256K DYNAMIC RAM ----- (2nd BOARD)
  JA - 2 \BOARD ADDRESS 40000-7FFF]
  JB - ON \PARITY VECTOR INTERRUPT VI2]
  JC - OFF \PHANTOM LINE}
  JD - 1-OFF \I/O PORT ADDRESS 01}

961  256K DYNAMIC RAM ----- (3rd BOARD)
  JA - 3 \BOARD ADDRESS 80000-BFFF]
  JB - 2 \PARITY VECTOR INTERRUPT VI2]
  JC - OFF \PHANTOM LINE}
  JD - 2-OFF \I/O PORT ADDRESS 02}

961  256K DYNAMIC RAM ----- (4th BOARD)
  JA - 4 \BOARD ADDRESS C0000-FFFF]
  JB - 2 \PARITY VECTOR INTERRUPT VI2]
  JC - OFF \PHANTOM LINE}
  JD - (1 AND 2)-OFF \I/O PORT ADDRESS 03}

971  CPU-I/O BOARD
  JC - 2 & 3 \2716 EPRO4]
  JC - 1 & 2 \2732 EPRO1}

1010  ANALOG TO DIGITAL BOARD
  JA THRU JJ - 1 {REFERENCE DESIGNATION DIFFERENTIAL INPUT}
  JJ = LEFT \NORMAL INPUT}
  JK = \I/O ADDRESS]
  1st BOARD \ADDRESS 96]  2nd BOARD \ADDRESS 98]
  1 - OFF  1 - ON
  2 - OFF  2 - ON
  3 - ON   3 - OFF
  4 - OFF  4 - OFF
  5 - ON   5 - ON
  6 - ON   6 - ON
  7 - OFF  7 - OFF
1001 GRAPHICS BOARD

662 VIDEO BOARD SYSTEMS:

INSTALL ROHS ON 662 VIDEO BOARD;

SACR3B, GRAPH, 3E00D AT LOCATION 9D
SACR3B, GRAPH, 20F3 AT LOCATION 8D

SHUNT AS FOLLOWS;

<table>
<thead>
<tr>
<th>662 BOARD</th>
<th>1001 BOARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>JB 2-3</td>
<td>JA 1-2</td>
</tr>
<tr>
<td>JC 2-3</td>
<td>JA 2-3</td>
</tr>
<tr>
<td></td>
<td>(VSYNC -)</td>
</tr>
<tr>
<td></td>
<td>(VSYNC +)</td>
</tr>
</tbody>
</table>

1061 VIDEO BOARD SYSTEMS:

ROHS ON 1061 BOARD SHOULD BE;

ULTII, 431E, U40, REV 1.3 AT LOCATION U40
ULTII, 2152, U41, REV 1.3 AT LOCATION U41
CEGEN-1, REV 1.1, 7E25 AT LOCATION U8
CEGEN-2, AB53 AT LOCATION U6

SHUNT AS FOLLOWS;

<table>
<thead>
<tr>
<th>1061 BOARD</th>
<th>1001 BOARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>JE 1-2</td>
<td>JA DON'T CARE</td>
</tr>
<tr>
<td>JF 1-2</td>
<td>JB DON'T CARE</td>
</tr>
<tr>
<td>JF 2-3</td>
<td>JC 1-2</td>
</tr>
<tr>
<td></td>
<td>JD 1-2</td>
</tr>
<tr>
<td></td>
<td>Z80 SHUNT;</td>
</tr>
</tbody>
</table>

CABLING FOR 1061 OR 662 BOARD SYSTEMS:

INSTALL 16 PIN RIBBON CABLE FROM 1061/662 J6 TO 1001 J1.
REMOVE 10 PIN CABLE FROM 1061/662 J3, INSTALL IT ON 1001 J2.
1021 64K DYNAMIC RAM (1ST BOARD)
JA - ALL ON \[I/O ADDRESS 00\]
JB - BOTTOM HORIZONTALLY \[MAIN MEMORY\]
JC - ON \[1ST MEMORY\]
JD - ON VERTICALLY SECOND FROM LEFT \[VECTOR INTERRUPT VI2\]
JE - OFF \[PHANTOM LINE NOT SELECTED\]

1021 64K DYNAMIC RAM (2ND BOARD)
JA - TOP SHUNT OFF \[I/O ADDRESS 01\]
JB - TOP HORIZONTALLY \[BANK MODE\]
JC - OFF \[BANK MODE\]
JD - OFF \[VECTOR INTERRUPT VI2\]
JE - OFF \[PHANTOM LINE NOT SELECTED\]

1021 64K DYNAMIC RAM (3RD BOARD)
JA - MIDDLE SHUNT OFF \[I/O ADDRESS 02\]
THE REST SHUNTED THE SAME AS THE 2ND 1021 BOARD

1021 64K DYNAMIC RAM (4TH BOARD)
JA - TOP 2 SHUNTS OFF \[I/O ADDRESS 03\]
THE REST SHUNTED THE SAME AS THE 2ND 1021 BOARD

1030 ISOLATED I/O BOARD
SW1 - \[I/O ADDRESS\]
1st BOARD \[\ADDRESS 9B\] 2nd BOARD \[\ADDRESS 9C\]
0 - OFF 0 - ON
1 - OFF 1 - ON
2 - ON 2 - OFF
3 - OFF 3 - OFF
4 - OFF 4 - OFF
5 - ON
6 - ON
7 - OFF

1061 ULTIMA II VIDEO BOARD
JB - ON 1-2 \[-CTS\]
JC - ON 1-3 \[RS232\]
JE - ON 1-2 \[HORIZONTAL SYNC\]
JF - ON 1-2 \[VERTICAL SYNC +\]
JF - ON 2-3 \[VERTICAL SYNC -\]
ALL OTHERS OFF

1061 ULTIMA II VIDEO BOARD (RS422)
SAME AS ABOVE EXCEPT:
JC - ON 2-3 \[RS422\]

BDSHUNT.LST  PG. 9  12/10/85
1081 16 BIT MPU BOARD WITH RS232

<table>
<thead>
<tr>
<th>JA</th>
<th>1 - 10</th>
<th>ON</th>
<th>JB</th>
<th>1 - 10</th>
<th>ON</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2 - 9</td>
<td>OFF</td>
<td></td>
<td>2 - 9</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>3 - 8</td>
<td>ON</td>
<td></td>
<td>3 - 8</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>4 - 7</td>
<td>OFF</td>
<td></td>
<td>4 - 7</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>5 - 6</td>
<td>ON</td>
<td></td>
<td>5 - 6</td>
<td>ON</td>
</tr>
</tbody>
</table>

(REFER TO 862 BOARD SHUNTING FOR ALL OTHER SHUNTS)

1081 16 BIT MPU WITH RS422

<table>
<thead>
<tr>
<th>JA</th>
<th>1 - 10</th>
<th>OFF</th>
<th>JB</th>
<th>1 - 10</th>
<th>OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2 - 9</td>
<td>ON</td>
<td></td>
<td>2 - 9</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>3 - 8</td>
<td>OFF</td>
<td></td>
<td>3 - 8</td>
<td>OFF</td>
</tr>
<tr>
<td></td>
<td>4 - 7</td>
<td>ON</td>
<td></td>
<td>4 - 7</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>5 - 6</td>
<td>ON</td>
<td></td>
<td>5 - 6</td>
<td>ON</td>
</tr>
</tbody>
</table>

DS-100 TAPE BACK UP CONTROLLER BOARD

SW1 - \{I/O ADDRESS DO\}  
1 - ON  
2 - ON  
3 - OFF  
4 - ON  

IDXCS-100 16 BIT TAPE BACKUP CONTROLLER

SW1 - 1-off  
2-off  
3-off  
4-off  
5-off  
6-off Tape 4 Disk  
7-off  
8-off  

1100 D+4A WINCHESTER CONTROLLER

JA - ON 2-3 MAXTOR EXTRA HEAD SELECT  
JA - ON 1-2 NON MAXTOR DRIVES (LOW CURRENT)  
JB - ON 2-3 FOR 5" DRIVES  
JB - ON 1-2 FOR 8" DRIVES  
JC - ON 1-2 FOR USE WITH A 451 PROCESSOR  
JC - ON 2-3 FOR ALL OTHER PROCESSORS  
JD - ETCHED (VECTOR INTERRUPT 4)  
JE - ON 2-3 (I/O ADDRESS A0-A1)

1120 QIC 02 TAPE INTERFACE CONTROLLER (WANGTEK)

JA - TOP/BOTTOM \{TOP IF USING A 645 OR 971 CPU\}  
\{BOTTOM IF USING A 451 CPU\}  
JB - NO SHUNTS (NO INTERRUPTS)  
JC - NO SHUNTS (RESERVED FOR FUTURE USE)

1180 ULT V VIDEO REV. F (1184 PWB ASSY)

JA - ON 1-2 (H SYNC +)  
JB - ON 1-2 (V SYNC +)  
JC - ETCHED ON = 1 EXTRA WAIT STATE DURING I/O CYCLE  
JD - ETCHED ON 1-2  
JE - ETCHED ON 1-2 ALLOWS IHS 672 KYBD INPUT AND MAKES PRINTER PORT 1 DIRECTION ONLY  
JF - ON 2-3 INVERT RS232 SIGNAL / SPACE = CTS
1230 80186 S100+ MASTER PROCESSOR (1232 PCB)
JA - 1-2-3 NOT SHUNTED, USED IN NECESSARY REWORK
ON 4-5 IF NO OTHER S100+ BOARDS IN SYSTEM
ON 5-6 IF OTHER S100+ BOARDS IN SYSTEM
JB - ON 1-2 IPL
JC - ON 1-2 SLOWER I/O FOR USE WITH MOST CONTROLLERS

1230 80186 S100+ MASTER PROCESSOR (1233 PCB)
JA - ON 2-3 IF OTHER S100+ BOARDS IN SYSTEM (TOP)
ON 1-2 IF NO OTHER S100+ BOARDS IN SYSTEM (BOTTOM)
JB - ON 1-2 IPL
JC - ON 1-2 SLOWER I/O FOR USE WITH MOST CONTROLLERS

1240 80186 S100+ SLAVE
JA - S100+ ADDRESS 01H TO 1EH WITH JA PINS 1,2,3 THE MOST
SIGNIFICANT BIT AND JA PINS 13,14,15 THE LEAST
SIGNIFICANT BIT. FOR EXAMPLE, ADDRESS 12H=:
3  15
  . . .
  ! . .
  . ! !
1  13
JB - ON 1-2 FOR INTERMEDIATE SLAVE
ON 2-3 FOR LAST SLAVE ON S100+ BUS
JC - ON 1-2 IPL
JD - 1-2, 4-5 FOR 64K DRAM CHIPS
2-3, 5-6 FOR 256K DRAM CHIPS

1250 6810 BOARD
JA - ETCHED FOR CENTRONICS
JA - FOR NEC:
CUT TRACES BETWEEN JA 7&13,8&14,9&15,10&16,11&17,12&18
INSTALL 3X6 SHUNT JACK ON JA
SHUNTS ON JA 1&7,2&8,3&9,4&10,5&11,6&12
JB - FOR TURBODO3 FIRST BOARD AT E0, SECOND BOARD AT F0
JB - FOR CDOS ANY ADDRESS FROM 00 TO 50
(WITH 1ST BRD AT 00, 2ND AT 10, ETC)
EXAMPLE:
ADDRESS 50
  JB A4 SHUNT ON 1  A4 ...  1 0
  JB A5 SHUNT ON 0  A5 ...  0 1
  JB A6 SHUNT ON 1  A6 ...  1 0
  JB A7 SHUNT ON 0  A7 ...  0 1

1260 1 MEG MEMORY BOARD
JA - ON 1-2 FOR 64K DRAM CHIPS
ON 2-3 FOR 256K DRAM CHIPS
JB - OFF (PHANTOM NOT USED)
1270 Z80 B MASTER
JA - ON 1-2 FOR SINGLE USER SYSTEM
    ON 2-3 FOR MULTI USER SYSTEM
JB S100+ ADDRESS BUS ADDRESSABLE FROM 00H TO 1EH, HOWEVER
    THE MASTER IS USUALLY ADDRESSED AT 00H, EXAMPLE:
    3    15
    . . . .
    . . . .
    ! ! ! ! !
    1    13
JC - OFF (TEST SHUNT)
JD - ON 1-2 RDY OK SHUNT
    ON 4-5 KRDY OK SHUNT
    ON 7-8 MASTER SHUNT
JE - ON 2-3 VI 0
    ON 5-6 VI 2
    ON 8-9 VI 4
    ON 11-12 VI 5
    ON 14-15 VI 7
JF - ALWAYS OFF, NEVER USED
1270 Z80 B SLAVE
JA - ON 1-2 IF LAST BOARD ON S100+ BUS
     ON 2-3 IF INTERMEDIATE BOARD ON S100+ BUS
JB - S100+ ADDRESS FROM 01H TO 1EH WITH JB PINS 1, 2, 3 BEING
     THE MOST SIGNIFICANT BIT, AND JB PINS 13, 14, 15 BEING
     THE LEAST SIGNIFICANT BIT. FOR EXAMPLE ADDRESS 03H =
     \[
     \begin{array}{ccc}
     3 & 15 \\
     . & . & . \\
     ! & ! & ! \\
     1 & 13
     \end{array}
     \]
JC - OFF (TEST SHUNT)
JD - ON 2-3 SHUNT "PARKED"
     ON 5-6 SHUNT "PARKED"
     ON 8-9 SLAVE SHUNT
JE - ALL OFF (NO EXTERNAL INTERRUPTS FROM S100 BUS)
JF - OFF NEVER USED

1280 RS422 PADDLEBOARD
JA - ON 2-3 (TRX CLOCK IS OUTPUT)

1300 KALEIDO CARD (IBM COLOR GRAPHICS BOARD)
JA - ON 1-2 ETCHED
JB - ON 1-2 H SYNC +
     ON 2-3 H SYNC -
JC - ON 1-2 V SYNC +
     ON 2-3 V SYNC -

1320 Z80H SLAVE PROCESSOR
SW1:
1  ON FOR LAST S100+ BUS BOARD
1  OFF FOR INTERMEDIATE S100+ BUS BOARD
2 - 6  S100+ BUS ADDRESS WITH 6 BEING THE
     MOST SIGNIFICANT BIT AND 2 LEAST SIGNIFICANT
     FOR EXAMPLE ADDRESS 13:
\[
\begin{array}{ccccccc}
6 & 5 & 4 & 3 & 2 & 1 \\
\end{array}
\]
\[
\begin{array}{ccccc}
0 & 0 & 0 & 0 & 0 \\
N & F & F & N & N \\
\end{array}
\]
JC - ON 1-2 IPL POSITION
JF - OFF SPECIAL INTERRUPT MODE NOT USED

1360 Z80H S100+ SLAVE w/8087 MATH COPROCESSOR
SW1:
1  ON FOR LAST S100+ BUS BOARD
1  OFF FOR INTERMEDIATE S100+ BUS BOARD
2 - 6  S100+ BUS ADDRESS WITH 6 BEING THE
     MOST SIGNIFICANT BIT AND 2 LEAST SIGNIFICANT
     FOR EXAMPLE ADDRESS 13:

BDSHUNT.LST  PG. 13  12/10/85
1390 P/S-MAIN 40V CONVERTER

1400 P/S 5,8,12,16 V

1410 P/S 5,24,-12

1420 P/S CRT/TSA

1430 L/F NET PADDLEBOARD

<table>
<thead>
<tr>
<th>Switch</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1</td>
<td>NODE ADDRESS</td>
</tr>
<tr>
<td>SW2</td>
<td>NODE ADDRESS</td>
</tr>
<tr>
<td>SW3</td>
<td>NODE ADDRESS</td>
</tr>
<tr>
<td>SW4</td>
<td>NODE ADDRESS</td>
</tr>
<tr>
<td>SW5</td>
<td>DOWN=CONTROLLER UP (NORMAL)=NON CONTROLLER</td>
</tr>
<tr>
<td>SW6</td>
<td>NO FUNCTION</td>
</tr>
</tbody>
</table>

---

SW1:

6 5 4 3 2 1

X X 0 0 0 0

SW2:

F N N N

NODE ADDRESS 7

---

INSERT TERMINATOR PLUG IN LAST NODE

BDSSHUNT.LST  PG. 14  12/10/85
1440 L/F NET IBMPC PADDLE BOARD
   SW1: NODE ADDRESS LSB 0 DOWN
   SW2: NODE ADDRESS STRAIGHT BINARY ADDRESSING 00 THRU 15
   SW3: NODE ADDRESS
   SW4: NODE ADDRESS MSB 1 UP
   SW5: NO FUNCTION
   SW6: NO FUNCTION
   /
   /
   X X O O O O
   /
   /
   /
   /
   /
   /
   /
   /

1460 BATTERY CHARGER

1480 P/S DUAL 8,16V

1500 CRT UPS P/S

1510 80186 S100+ SLAVE
   SW1:
   1 ON FOR LAST S100+ BUS BOARD
   1 OFF FOR INTERMEDIATE S100+ BUS BOARD
   2 - 6 S100+ BUS ADDRESS WITH 6 BEING THE
   MOST SIGNIFICANT BIT AND 2 LEAST SIGNIFICANT
   FOR EXAMPLE ADDRESS 13:
   /
   /
   /
   /
   /
   /
   /
   /
   /
   /
   /
   /
   /
   /
   /
   /

   JC - ON 1-2 IPL POSITION
   JP - OFF SPECIAL INTERRUPT NODE NOT USED
   JD -