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Example:
To select an address of 16010, switches 1 through 9 would be in the ON position, switch #9 would be OFF. Note that the number of switch does not correspond to the bit position on the Unibus, i.e., SW doesn't sample BUS A8.

1.2.0 Interrupt Vector Address
The Dlll Vectors also fall into the floating interrupt vector space. The first vector of the floating scheme is address 378. This would be the vector of the first Dlll in a system that consisted of devices which did not precede the Dlll in the floating address scheme. In this floating address scheme the Dlll uses four address spaces starting on a zero boundary and is preceded by the Dlll (i.e., 16040-50). Once the position of the Dlll has been determined in the floating address scheme, the Unibus address is selected by the rocker switches on the Dlll block.

1.2.1 Setting the Interrupt Vector
The vector is determined by the position of jumpers W9 through W14. During an interrupt sequence a BUS D line will be asserted as a logical '1' if a jumper is in place. As cited earlier the Dlll occupies two vectors. Only the first vector need be considered and it must start on a zero boundary. The second vector is simply controlled by W9-W14 and BUS D #2 which is controlled by the hardware.

Example:

1.3.8 Miscellaneous Jumper—Modify only at customer's request with the exception of W15, W16, W14-W9.

Drawing # Jumper # Function
5 W2 This jumper is normally IN. If this jumper is in, the receiver logic will synchronize on one sync character instead of the recommended two.
6 W4 This jumper is normally IN. If this jumper is left out, Bits 1-3 of the RXER will not be cleared by Master Reset or BUSINIT. In some cases the connection with the data set may be required to be excluded from the effects of Master Reset or Bus Init.
4 W14 Set vector 8 bit 0 when installed
W13 Set vector 8 bit 1 when installed
W12 Set vector 8 bit 2 when installed
W11 Set vector 8 bit 3 when installed
W10 Set vector 8 bit 4 when installed
W9 Set vector 8 bit 5 when installed

Note: If any of the miscellaneous jumpers have been changed with the exception of W15 and W16, new parameters must be entered into the diagnostic program through its keyboard monitor.

1.4.0 Mounting Information
1.4.1 Dulll-DA
The Dulll-DA is compatible with all small peripheral controller slots (SBC) to date, with the exception of those internal to the KAI.
1.7.3 Verification of the Unibus, Bus D line drivers
A. Press start to issue CLR in the DUll.
B. Press start to issue CLR in the DUll.
C. Examine the last DlUl register, TXOBUF, (Sel. 6). The contents should read back as all ones. This proves that all DUll unibus D line drivers turn on.

1.7.4 Verification of the Unibus, Bus D line drivers
A. Press start to issue CLR in the DUll.
B. Press start to issue CLR in the DUll.
C. Examine the last DUll register, TXOBUF, (Sel. 6). The contents should read back as all ones. This proves that all DUll unibus D line drivers turn on.

1.7.5 Verification of slave sync inhibit delay
With same loop used in 1.7.2 load the PARCSR address (Sel. 2) into the console SMR.
A. Start the program. With the first scope probe verify the LD PARCSR one shot at B612. This output should be low for at least 65ns. (Refer Fig. A).
B. Use probe on channel one of the scope with the second probe verify that BUS SSYH is inhibited for at least 35ns after the rising edge of the LD PARCSR pulse. (Refer Fig. A)

Figure A

<table>
<thead>
<tr>
<th>Channel 1</th>
<th>LD PARCSR (E6812)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>+3</td>
</tr>
<tr>
<td></td>
<td>65ns</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Channel 2</th>
<th>SSYH EN (E5905)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>+3</td>
</tr>
<tr>
<td></td>
<td>MV</td>
</tr>
</tbody>
</table>

A greater than 35ns but less than 1.2 us

1.7.6 Environmental Specifications

Temperature:
- Operating range: +10°C to +50°C
- Storage range: -25°C to +70°C

Humidity:
- Operating range: 5% to 95%
- Non-condensing

Input/Output:
- Power requirements: +5V at 200mA, +15V at 150mA
- Environmental Specifications

1.7.7 Preliminary Testing
1.7.8 Voltage Checks
With the DUll plugged into the back panel check the voltages at the following points. A 453 scope should suffice if it's calibrated.

1.8 Testing with diagnostics
1.8.1 DUll-DA
With the BC53-C cable connected to the M7822 module and the opposite end of the cable terminated by the H115 test connector, start testing with DDU-DA. All diagnostics from DDU-DA to DDU-FA should run in the external mode. At least 3 passes of each diagnostic should be made. This concludes DUll-DA testing, remove the H115 connector and plug the BC53-C into the module.

1.8.2 DUll-FA
Starting with DDU-FA through DDU-FA, run all diagnostics with the diagnostic running in the internal maintenance mode. At least 3 passes of each diagnostic should be made. Connect the 8ry connector of the BC53-W into the M7822 module. If the module is not a ball 381 or 3s1, special cables might be required to connect to the modem. This must be done through the local office and not part of the DUll-EA installation.

If the module in question is something other than those cited, installation testing is concluded here.

With the cited modules, plug the Burndry connector of the BC53-W into the SRC connector of the data set. This concludes DUll-DA testing.

1.9 Verification of address recognition logic
With the test loop the correct operation of the address decoding logic can be verified.

1.9.1 Verification of address recognition logic
With the test loop the correct operation of the address decoding logic can be verified.

Note: If W16 is in place, the voltage on E12 14 will be +8V, +12V or 0V.
1.9.0 Systems Test

1.9.1 Using the DECX11 DULL module DUA_, run all DULL's on the system. Up to 8 DULL's may be exercised on a system. At least 3 passes of each DULL should be made.

2.0 Customer Acceptance

2.1.0 DULL-DA

Customer acceptance is based on the satisfactory conclusion of Steps 1.8.1 and 1.9.1.

2.1.1 DULL-EA

Customer acceptance is based on the satisfactory conclusion of Steps 1.8.2 and 1.9.1.
<table>
<thead>
<tr>
<th>ITEM NO.</th>
<th>DWG NO. / PART NO.</th>
<th>DESCRIPTION</th>
<th>QTY.</th>
</tr>
</thead>
<tbody>
<tr>
<td>H315</td>
<td></td>
<td>TEST CONNECTOR</td>
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</tr>
<tr>
<td>BC05C - 25</td>
<td></td>
<td>MODEM CABLE</td>
<td>1</td>
</tr>
<tr>
<td>DF11-G</td>
<td></td>
<td>CURRENT MODE OPTION</td>
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<tr>
<td>DEC11-HDUMA-AD</td>
<td></td>
<td>MAINTENANCE MANUAL</td>
<td>1</td>
</tr>
<tr>
<td>LIBKIT-II-DUA-A-K</td>
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<td>DIAGNOSTIC PACKAGE</td>
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<tr>
<td>DEC-X-II-DUA-</td>
<td></td>
<td>DEC-X-EXERCISER</td>
<td>1</td>
</tr>
</tbody>
</table>

**Title:** SINGLE LINE PGM SYNCH. INT

**Assy. No.:** AAL

**Size Code:** Dull-0-3

**Rev:** A

**Eco No.:** 00001

**Sheet:** 1 of 1
NOTES:
1. MANUFACTURING SHOULD USE MACHINE CRIMPER TOOL FOR CRIMPING PINS (ITEM #7) MUST BE 
   DIE FROM BERG ELECT.
2. ONLY DEP P/N 100000-00 MAY BE 
   USED AS SH.
3. PLACE ITEM "B" (THIS SIDE UP STICKER) ON LETTERED SIDE OF ITEM #6 (BERRY HOUSING) AS SHOWN.
4. USE ITEM #7 (907352-11) IN TWO PLACES ON PNP-7 TO PREVENT SHORTING.
5. USE ITEM #8 (907352-911) ON ALL STRAIN RELIEF SOLDER PINS PER PERIOD 200300.
6. DUE TO TOLERANCES WITH DIFFERENT 
   MANUFACTURING THE HOUSING (ITEM #1) MAY 
   VARY 31/4 IN OUTSIDE DIAMETER CAUSING POTENTIAL 
   STRAIN RELIEF GRIP PROBLEM SHOWN ON DRAWING.
7. ITEM #1 (910726-11) MAY BE 
   USED AS ITEM #6 (OVER SHORT WIRE 1-3, 2-4, 8-7)
NOTES:

- Ar. --------+---+------|
- GNAND SV ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE.
- DEC FOR NO_DRO.3>
I. FUNCTIONS OF MODEM JUMPERS (WHEN INSTALLED)

A. EIA - SECONDARY TRANSMIT & RECEIVE DATA LINES TO EIA Pins 1 & 5
B. S02 - SECONDARY TRANSMIT & RECEIVE DATA LINES TO EIA PIN 1 & 2
C. S01 - ALLOW OPERATION OF RING AND DATA TERMINAL READY FUNCTIONS WITH BELL 202 SERIES
D. B01 - ALLOW TRANSPORT FUNCTION IS MONITORED BY SECONDARY RECEIVE LINES.
E. BUSY - FORCE BUSY FUNCTION ADOPTED WITH REQUEST TO SEND
F. 301 - REMOVE FOR BELL 301 USE ONLY

II. TABLE OF PARTS, REFERENCE, AND QUANTITY

<table>
<thead>
<tr>
<th>PART</th>
<th>REFERENCE</th>
<th>QUANTITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>