IDENTIFICATION

PRODUCT CODE: AC-9031H-MC

PRODUCT NAME: CZOKHQ T17-4K SYSTEM EXERCISER

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MAINTAINER: DIAGNOSTIC GROUP

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1. ABSTRACT

This program is a Memory Expandable Interactive Bus Ejer-
ciser for a Paper Tape Oriented PDP-11. It performs a
test of instructions and concurrent operations of I/O
equipment simultaneously. It may also perform the
same operation independently. This program is not
to be considered a total check of the system. If an error
is detected in an I/O device, it will probably be necessary
to correct the malfunction with the respective diagnostic
for that device.

In this version the interrupt service routine for the
disks, K11, plus the stack and the I/O data buffers are
relocated to the current bank.

2. REQUIREMENTS

2.1 EQUIPMENT

2.1.1 Optional hardware that the program will exercise

MM11  up to 28K of memory
RC11  disk
RK11  disk
RP11  disk
RF11  disk (256K)
TC11  decktape-transport one
KE11A Extended arithmetic unit
KW11  line clock
PC11  high speed reader/punch
BL11  ASR33 or ASR35 teleprinter-LC11, VT05
LP11  line printer
LS11  line printer...see 5.2.11

2.2 STORAGE

2.2.1 Program storage - the routine uses
4K of memory

3. LOADING PROCEDURE

3.1 METHOD

Procedure for normal absolute tapes should be followed.
STARTING PROCEDURE

THIS PROGRAM HAS BEEN MODIFIED TO RUN WITH OR WITHOUT A
CONSOLE PROCESSOR.
IF A CONSOLE MACHINE IS USED, THEN THE PROGRAM
LOOKS AT THE HARDWARE SWITCH REGISTER.
IF A CONSOLE-LESS MACHINE IS USED, THEN THE PROGRAM
AUTOMATICALLY LOOKS AT THE CONTENTS OF LOCATION
SR (176) AS A SWITCH REGISTER.

IT'S THE RESPONSIBILITY OF THE OPERATOR TO SET UP
THIS LOCATION PRIOR TO STARTING THE PROGRAM.

THE PROGRAM REQUIRES TWO BELLS ON THE TTY
TO MAKE ONE TRUE PASS OF THE PROGRAM. THE FIRST BELL
OCURRS AFTER ONE PASS OF THE INSTRUCTION TEST WITH
THE 'TRACE' BIT CLEARED. THE SECOND BELL MARKS THE
END OF AN INSTRUCTION TEST PASS WITH THE 'TRACE' BI
SET.

CONTROL SWITCH SETTING

STARTING AT SA 200 ALL SWITCHES SHOULD BE SET AS INDICATED.

4.1 STARTING ADDRESS OR ADDRESSES

(A) 200 = SR = 000000 TEST PROCESSOR ONLY—WITHOUT CORE EXPANSION
(B) 200 = SR = 001000 TEST PROCESSOR ONLY—4K INHIBIT
(C) 200 = SR = 000000 TEST I/O ONLY
(D) 200 = SR = 000000 - CORE EXPAND AND TEST ALL AVAILABLE
I/O DEVICES

SWD = 1 INHIBIT TTY OUTPUT
SWI = 1 INHIBIT TTY INPUT
SHD = 1 INHIBIT MSR
SHI = 1 INHIBIT SHR
SHLD = 1 INHIBIT LINE CLOCK
SHLP = 1 INHIBIT RPII, RRPII, RC11 AND RP11 DISK(S)
SCH = 1 INHIBIT TC11 DECTAPE
SWP = 1 INHIBIT LINE PRINTER --- IF LINE PRINTER IS USED.
AND MUST RESTART AT SDP
IF EAE EXIST IT WILL BE AUTOMATICALLY SELECTED
4.3 PROGRAM AND OPERATOR ACTION

LOAD PROGRAM INTO MEMORY.
SET SWITCH REGISTER TO STARTING ADDRESS.
LOAD ADDRESS.
SET SWITCHES TO INHIBIT NON EXISTANT DEVICES
PRESS START.
THE PROGRAM WILL LOOP AND
BELL WILL RING ONCE PER PASS OF THE PROGRAM.
A MINIMUM OF TWO PASSES SHOULD
ALWAYS BE RUN.

5. OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

5.1.1 AT SA 200... THE INSTRUCTION AND LOGIC TEST WITH ALL SWITHCES
DOWN THE PROGRAM WILL TEST ALL DEVICES AND PRINT OUT ON ERRORS
AND CONTINUE IN TEST. (BELL WILL RING AT COMPLETION OF A PASS)

5.1.2 SWITCH SETTINGS ARE

SW15 = 1 OR UP ... HALT ON ERROR
SW9 = 1 OR UP ... LOOP
SW13 = 1 OR UP ... INHIBIT DEBUG
SW12 = 1 OR UP ... INHIBIT TRapping
SW11 = 1 OR UP ... INHIBIT ITERATION LOOP
SW10 = 1 OR UP ... INHIBIT PROCESSOR TEST
SW9 = 1 OR UP ... INHIBIT VARIABLE CORE EXPANSION
SW8 = 1 OR UP ... RESTART ON ERROR

5.1.3

5.2 SUBROUTINE ABSTRACTS

5.2.1 BEGIN SA 200

5.2.2 SCOPE

----- THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST IN THE
INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH
SUB-TEST AS IT IS BEING ENTERED.
IF A SCOPE LOOP IS REQUESTED WITH SW14=1, THEN
IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP
IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL
BE EITHER A FIXED OR RANDOM NUMBER OF ITERATIONS ON THAT SUB-
TEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A :
INHIBITS ITERATION OF SUBTESTS.
5.2.3 **HLT**

---

**IS A ROUTINE THAT PRINTS-OUT AN ADDRESS "HALT" ACS THE FAILURE, TEST **

**THE STATUS REGISTER AT THE TIME OF THE FAILURE, AND THE PROCESSOR TEST BEING EXECUTED AT THE TIME OF **

**FAILURE**

5.2.4 **TRAP**

**TRAP**

**THIS ROUTINE WILL ALLOW THE TRAP BIT TRAP TO BE SET AFTER **

**FIRST LOOP OF THE PROGRAM. UNDER NORMAL TESTING THE TRAP **

**BIT WILL BE SET ON ALTERNATE LOOPS OF THE PROGRAM. WHEN **

**SET IT CAUSES A TRAP AFTER EACH INSTRUCTION. THE FIRST **

**INSTRUCTION EXECUTED UPON TRAPPING IS AN "RTI" WHICH RE-EXECUT TO **

**THE INTERRUPTED SEQUENCE OF INSTRUCTION.**

5.2.5 **TRAPCATCHER**

**TRAPCATCHER**

**THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION **

**D. DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND **

**INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF **

**MEMORY.**

**THE PRINCIPLE OF THIS ROUTINE IS: THE VECTOR ENTRANCE **

**ADDRESS POINTS TO THE NEXT SEQUENTIAL WORD WHICH CONTAINS A HALT (0000). THIS LOCATION IS ALSO THE STA-**

**TUS FOR THAT VECTOR ENTRANCE, BUT THIS HAS NO EFFECT IT ALSO BEING THE NEXT INSTRUCTION).**

**IF A HALT OCCURS IN THE TRAP OR INTERRUPT VECTOR AREA, **

**REGISTER SIX SHOULD BE EXAMINED TO DETERMINE ITS CON-**

**TENT. THEN USE REGISTER SIX CONTENTS AS AN ADDRESS TO **

**DETERMINE THE LOCATION WHERE THE PROGRAM WAS AT WHEN **

**THE INTERRUPT OR TRAP OCCURRED.** (MEMORY AS SPECIFIED **

**BY RS CONTAINS THE PC OF THE INSTRUCTION FOLLOWING THE **

**INSTRUCTION WHERE THE TRAP OCCURRED).**

5.2.6 **TTYIN1 (TTY INPUT)**

**TTYIN1 (TTY INPUT)**

**THIS ROUTINE OPERATES IN THE INTERRUPT MODE **

**AND CHECKS FOR A COUNT PATTERN IN THE READER OF THE TTY. THE ROUTINE WILL ACCEPT AN INFINITE **

**NUMBER OF ZERO BYTES (BLANK TAPE). BUT THE FIRST BYTE THAT IS NOT A ZERO MUST BE A ONE **

**AND ALL SEQUENTIAL BYTES MUST BE ONE GREATER. **

**IF THE ROUTINE DETECTS AN ERROR IN THE COUNT **

**PATTERN, IT CHECKS TO SEE IF IT IS A **

**ZIP (bell). IF SO IT IS IGNORED, IF NOT A **

**COMPARTMENT ERROR IS FLAGGED.**

**WHEN TESTING THE TTY **

**READER THE TAPE MUST HAVE A COUNT PATTERN AND BE **

**LOCATED ON THE LEADER PORTION WHEN STARTING TTY**

5.2.7 **TTYOUT (TTY OUTPUT)**
5.2 G

THIS IS A ROUTINE THAT OUTPUTS A COUNT PATTERN IN
THE INTERRUPT MODE TO THE TELEPRINTER. IF A PAPER
TAPE IS PUNCHED IT MAY HAVE 20'S (BELLS) IN IT
PUNCHED WHEN THE BELL FOR PASS COMPLETE RINGS.

5.2.0

AFSTART (AF-11 DISK)

THIS ROUTINE PERFORMS A WRITE AND A WRITE CHECK OF THE DISK.
THE DATA THAT IS WRITTEN ON THE DISK IS PART OF TEST PROGRAM
CODE THAT IS NEVER MODIFIED. THIS SEGMENT OF CORE IS WRITTEN
IN CONTIGUOUS BLOCK THRU THE DISK MEMORY. AFTER THE TOTAL
DISK(S) HAS BEEN WRITTEN A WRITE CHECK IS USED TO VERIFY THAT
THE DATA HAS BEEN WRITTEN CORRECTLY ON THE DISK. NOTE THAT "DATA"
ARE USED IN EXERCISING THE DISK (DATA IS NOT TRANSFERRED
INTO CORE).

THE INTERRUPT SERVICE ROUTINE AND
DATA BUFFER IS TRANSFERRED TO THE CURRENT
BANK THAT INSTRUCTIONS ARE BEING EXECUTED IN.

5.2.9

FENDZ (TC11 FORWARD END ZONE)

FENDZ IS THE FIRST ADDRESS IN THE DECTAPE INTERRUPT
VECTOR (214). THIS ROUTINE WILL READ, IN REVERSE, BLOCK
NUMBERS UNTIL THE REVERSE END ZONE IS FOUND. AT THIS
POINT THE INTERRUPT VECTOR AND COMMAND REGISTER ARE MODIFIED
TO READ ALL BLOCK NUMBERS IN THE FORWARD DIRECTION. EACH
BLOCK NUMBER READ IS COMPARED WITH THE EXPECTED BLOCK NUM-
BER COUNT AND DISCOMPARISONS REPORTED. WHEN EACH BLOCK IS
FOUND (WITH THE EXCEPTION OF BLOCK 0) A BLOCK (400 WORDS)
OF TEST DATA IS WRITTEN TO TAPE. AFTER ALL BLOCK NUMBERS
HAVE BEEN READ THE TAPE IS DRIVEN INTO THE FORWARD END ZONE
WHERE THE DIRECTION IS REVERSED AND ALL BLOCK NUMBERS ARE REAC-
IN REVERSE STARTING WITH BLOCK 1100(8) THROUGH BLOCK 0.
THE DATA IS READ FROM TAPE. THE SAME BUFFER IS USED FOR BOTH READ
AND WRITE OPERATIONS.

IF THE DATA BUFFER IS
DESTROYED DURING A READ OPERATION IT MAY BE NECESSARY TO
RELOAD THE PROGRAM.

5.2.10

LCLO (LINE CLOCK)

THIS TEST OF THE LINE CLOCK IS IN THE INTERRUPT
MODE. IF OPERATING CORRECTLY THE SYSTEM 1.0
WILL RUN A FULL SPEED FOR 55 SECONDS THEN ALL
THE GATE IS SIX OR LESS WILL STALL FOR 5 SECONDS.
THIS IS BASED ON 50 CYCLES AS THE LINE FREQUENCY.

5.2.11

LPI (LINE PRINTER)

THIS ROUTINE OUTPUTS TO THE LINE PRINTER IN
THE FLAG MODE WHILE FILLING THE BUFFER IN
THE INTERRUPT MODE WHILE THE BUFFER IS BEING
PRINTED.
FOR 132 COLUMN PRINTER CHANGE LOCATION LPB FROM 11
TO 12.
5.2.12 **WRITE PCI1 INPUT**

This routine operates in the interrupt mode and checks for a count pattern in the PCI1 reader. The routine will accept an input (e.g., a number of zero bytes (blank tape), but the input byte that is not a zero must be a ones and all sequential bytes must be one greater. If the routine detects an error in the count pattern, a data error is flagged. When testing the reader, the tape must have a count pattern and be located on the leader portion when starting test.

5.2.13 **HPOUT (PCI1 OUTPUT)**

This is a routine that outputs a count pattern in the interrupt mode to the high speed punch.

5.2.14 **RKSTART (RK-11 DISK)**

This routine performs a write and a write check of the disk. The data that is written on the disk is part of test program code that is never modified. This segment of code is written in contiguous block thru the disk memory. After the total disk has been written, a write check is used to verify that the data has been written correctly on the disk. Note that no "DATI" are used in exercising the disk (data is not transferred into core). The interrupt service routine and data buffer are transferred to the current bank that instructions are being executed in.

5.2.15 **RCSTART (RC-11 DISK)**

This routine performs a write and a write check of the disk. The data that is written on the disk is part of test program code that is never modified. This segment of code is written in contiguous block thru the disk memory. After the total disk has been written, a write check is used to verify that the data has been written correctly on the disk. Note that no "DATI" are used in exercising the disk (data is not transferred into core). The interrupt service routine and data buffer are transferred to the current bank that instructions are being executed in.

5.2.16 **RPSTART (RP-11 DISK)**

This routine performs a write and a write check of the disk. The data that is written on the disk is part of test program code that is never modified. This segment of code is written in contiguous block thru the disk memory. After the total disk has been written, a write check is used to verify that the data has been written correctly on the disk. Note that no "DATI" are used in exercising the disk (data is not transferred into core). The interrupt service routine and data buffer are transferred to the current bank that instructions are being executed in. (For the RPD3 the ISR must be modified to test the full surface...
CORE EXPANSION DET:

THIS ROUTINE IS CONTROLLED BY SWITCH 3. THE PROCESSOR MAINLINE CODE WILL BE EITHER 4KW OR EXPANDS TO THE MAXIMUM CORE THAT IS AVAILABLE. THE ROUTINE DETERMINES THE MAXIMUM CORE SIZE BY DOING A "DATA" TO A LOCATION IN EACH BANK. IF THE BANK DOES NOT EXIST A TIME OUT WILL OCCUR WHEN CORE SIZE IS DETERMINED AN IMAGE OF BANK 0 IS TRANSFERRED TO EACH EXISTING BANK. THEN THE CODE IN EACH BANK IS MODIFIED SO THAT WHEN THE LAST SUB TEST IN A MEMORY BANK IS EXECUTED THERE IS A JUMP INSERTED TO THE FIRST SUB TEST OF THE NEXT BANK. WHEN IN THE LAST BANK THE MODIFIED INSTRUCTION WILL TRANSFER YOU TO BANK 0.

THE LISTING SHOWS ONLY THE CODE OF BANK ZERO. WHEN AN ERROR OCCURS OR NOT IN BANK ZERO, IGNORE THE BANK BITS OF THE PRINT OUT AND USE THE LISTING FOR BANK ZERO.

5.3 PROGRAM AND/OR OPERATOR ACTION

5.3.1 LOADING AND STARTING AT 200 WITH ALL SWITCHES DOWN IS WORSE CASE TESTING. IF AN ERROR IS DETECTED HERE THERE WILL BE A PRINTOUT. WHEN AN ERROR IS DETECTED AND IT IS NECESSARY TO SCOPE ON IT SET SW15 TO HALT ON ERROR, THEN SW14 TO LOOP ON ERROR, THEN SW13 TO DELETE PRINTOUTS, THEN THE MACHINE MUST BE CONTINUED.

6. ERRORS

6.1 ERROR PRINTOUT


6.2 ERROR RECOVERY

FOR TTY READER AND HSR, TAPE MUST BE REPOSITIONED TO LEADER BEFORE RESUMING TEST. IF YOU DESIRE TO HAVE THE PROGRAM RESTART ON AN ERROR MAKE SWITCH REGISTER BIT # AN ONE.

7. RESTRICTIONS

7.1 STARTING RESTRICTION

IF LINE PRINTER IS USED RESTART ADDRESS MUST BE 400 FOR HSR AND TTY READER, TAPE MUST BE ON LEADER.

7.2 OPERATIONAL RESTRICTION
IF OPERATION UNDER MONITORS, THE CONSOLE IS EMPTY AND THE SYSTEM DEVICE IS NOT TESTED.

6. MISCELLANEOUS

TRACKING DOWN UNUSUAL FAILURES

FAILURES THAT MAY OCCUR BECAUSE OF A FALSE ENTRY INTO A SUBTEST, OR A FAILURE IN A CONTROL ROUTINE RATHER THAN A SUBTEST. DETECTION OF THESE MAY BE ACCOMPLISHED BY SEVERAL PROCEDURES. THERE IS A LOCATION CALLED "RETURN" THAT RECORDS THE LAST SUCCESSFUL SUBTEST COMPLETED. THERE IS ANOTHER LOCATION CALLED "SCOPED" THAT SHOWS HOW MANY TIMES THE SUBTEST HAS BEEN EXECUTED. THERE IS ANOTHER LOCATION CALLED "COUNT" THAT CONTAINS THE ITERATION COMPARISON VALUE. THE STACK "RS" SHOULD BE EQUAL TO "BUFF" WHEN THE FIRST INSTRUCTION OF THE SUBTEST IS ENTERED. TO REDUCE INSTRUCTION EXECUTION IN A CONFUSING SITUATION, THE "SCOPE" LOCATION FOLLOWING THE SUBTEST SHOULD BE CHANGED TO A BRANCH TO THE FIRST INSTRUCTION OF THE SUBTEST (THE FIRST LOCATION FOLLOWING THE PREVIOUS SCOPE LOCATION) AND THE "HIT" LOCATION MAY BE REPLACED WITH A "NOP".

A USER MAY ADD A UNIQUE ROUTINE TO THIS TEST TO EXERCISE A NON DEC OPTION, FOR CHECKING BUS INTERACTION WITH HIS EXISTING DEC OPTIONS.

FOR TROUBLE FREE INTERACTION THERE ARE A FEW GROUND RULES THAT SHOULD BE FOLLOWED:

1. USE NO REGISTERS.
2. THE ROUTINE SHOULD BE STAND ALONE.
3. THE EXISTING "HIT" SHOULD BE USED FOR ERROR DETECTION.
4. CODE IN THE PRIMING AREA SHOULD SET INTERRUPT ENABLE, INITIALIZE DATA AND RAISE A FLAG IF NECESSARY.
5. THE INTERRUPT VECTOR STATUS WORD SHOULD CONTAIN THE PRIORITY LEVEL OF THE DEVICE.
6. THE INTERRUPT VECTOR SHOULD POINT TO YOUR STAND ALONE ROUTINE.
7. THE STAND ALONE ROUTINE WHEN COMPLETING ALL HOUSE KEEPING OPERATION AND DATA COMPARISONS SHOULD THEN EXECUTE A "RTI" TO RETURN TO MAINLINE CODE.

INSERTION OF USER I/O ROUTINES

1. MAY BE INSERTED IN BANK ZERO WHERE I/O ROUTINES EXIST.

FOR DEVICES THAT THE USEP DOES NOT HAVE, IF CORE EXPANSION...
2. If the user has more than 4KW of core, the routine may be placed in any of the extra banks and core expansion be inhibited.

3. In the priming code several instructions before the tag "mainline" there is an instruction JSR 07 USER. The selector word of that instruction is an absolute address that the user may change to point to his routine. The user should exit his priming routine with a RTS 07 instruction.

8.1 EXECUTION TIME

Execution varies with number of devices, for 4KW systems with TTY and HSR only, about 1 minute with the trace bit cleared, about 1.5 minutes with the trace bit set.

9. PROGRAM DESCRIPTION

The design of this system exerciser is predicated upon it being primarily intended for a paper tape system with four KW of core, and that it be easy to run and understand. Also, that it may be modified easily to exercise a wide multitude of peripherals, including those of the customer's own design. The concept is to have all desired I/O running concurrently with the processor test for background. The decision which I/O devices to be used is made at start-up time. The data patterns used in the exerciser are fixed. For mechanical devices, such as the TTY reader, there is no automatic resynchronization if it's tape becomes out of phase with the data. It will become necessary to stop the exerciser and manually resynchronize the tape and restart the exerciser.

There is no monitor in the conventional sense, each device that is to be exercised has its own stand-alone routine that operates in the interrupt mode. These routines need no supervision or monitoring after they are initiated. There is a primer area that checks the switch register to see what devices are to be initiated. The primer area sets the interrupt enable bit in the device status register, initializes the data pattern and initiates an operation to raise data flags on devices that can not initiate themselves. Then, the primer jumps to the processor test where the individual devices are serviced at the interrupt rate.

The instruction exerciser is a straight line test of instructions. The sequence in which they are executed is the same sequence in which they are
Showed in the listing, each area of code from "scope to scope" is an individual sub-test. With switch H up, the sub-test is executed one time and then the next sub-test is executed, and so on until all sub-tests are executed. However, if switch H is down, the sub-test will be executed some "H" number of times before entering the next sub-test. If switch H is up, you will never leave the current sub-test. This is intended for trouble-shooting a malfunction in a sub-test. The first group of sub-tests are the binary and unar's whose instructions are tested in the index mode: source only, destination only, then both source and destination. The same instructions are then tested using the immediate mode indirect. These modes are tested against other modes, which may be a register or memory location. These will be swapped between source and destination.

After the modes and instruction have been proven in the word mode, they are then tested in the byte mode. Other testing is also done where the "split" instruction is tested in nested combinations. All combinations of numbers are tested using the compare, rotate, add and complement instructions. There is also a minimum test of power fail and auto recovery, which is not enabled until after the first pass of the program.

The reason for executing all instructions with the trace bit set is to take us into service at the end of each instruction.

The core layout is broken into five distinct parts:

1. The trap catcher.
2. The set up and I/O primer area and I/O test routines.
3. The processor tests and
4. Control and utility routines.
5. Core detector and expansion routine.

10. Listing

11. Flow chart(s)

.PRE
.ENDR
.ENABLE ABS

:PDPI PRELIMINARY SYSTEM TEST --- ITY-PC11, LP11, RF11, TC11, KW11, RV11, RC11, RP11 AND KE11
:TEST SIMULTANEOUS RUNNING OF I/O, WITH PROCESSOR INSTRUCTION TEST AND WITH
:WITH TRACE BIT ENABLED TO BE CONSIDERED MAINLINE CODE

000240 NOP-240
104000 HL=EMT ;TRAP USED FOR ERROR PRINTOUT
104000 SCOPE=TRAP ;TRAP USED SCOPE LOOP AND ITERATION OF SUB PROBLEMS

177776
01:100
00:0000
00:0001
00:0002
1B:0000
1B:0001
1B:0002
00:0000
00:0000
00:0010

IDSR=ICSR

BUFF=IN
R100=x
R101=x
RSR=x

RFR=RDCT=2000
RCWORDCT=-2000+40
RFWORDCT=-2000+40
XX=0

.REPT 100
        TRAP ENTRANCE
        TRAPPED TO PREVIOUS LOCATION

        HALT
        .ENDR
        SEQ,ME

+2
        :FALSE TRACE TRAP

+2
        :FOR HALT TRAPS

00:00014
00:00016
00:00000
00:00024
00:016526
00:00026
00:00340
00:00030
00:00024
00:00034
00:00034
00:00036
00:00000
00:00046
00:015556
00:00052
00:04000

:RETURN TO MONITOR ADDRESS

:EXECUTION TIME IS MEMORY SIZE DEPENDENT

:R6 IS THE STACK POINTER
:(R6) IS THE PC+2 OF LOCATION WHERE THE TRAP ORIGINATED

:FOR NORMAL OPERATION RUN WITH ALL SWITCHES DOWN

SR 15=1 OR UP----HALT ON ERROR
SR 14=1 OR UP----SCOPE LOOP
SR 13=1 OR UP----INHIBIT PRINT OUT
SR 12=1 OR UP----INHIBIT TRAP TRAPPING
SR 11=1 OR UP----INHIBIT SUB-PROBLEM ITERATION
SR 10=1 OR UP----INHIBIT PROCESSOR TEST
SR 09=1 OR UP INHIBIT VARIABLE CORE EXPANSION
SR 08=1 OR UP RESTART ON ERROR

SPECIAL DELETE SWITCHES-SET RESPECTIVE SWITCH TO A 1 TO INHIBIT INITIATION OF DEVICE

SW 0=1 INHIBIT TTY OUTPUT
SW 1=1 INHIBIT TTY INPUT
SW 2=1 INHIBIT HSR
SW 3=1 INHIBIT MDR
SW 4=1 INHIBIT LINE CLOCK
SW 5=1 INHIBIT RC, RF, RK, AP DISKS
SW 6=1 INHIBIT TC11 DECTAPE
SW 7=1 INHIBIT LINE PRINTER --- IF LINE PRINTER IS USED, MUST RESTART AT 502

IF EAE EXIST IT WILL BE AUTOMATICALLY SELECTED.
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**Notes:**

- **PDPI:** Simultaneous I/O
- **TTY:** Input/Output
- **MSR:** Masking Switch Register
- **MSP:** Masking Switch Priority
- **INTERRUPT VECTOR LINE:** 0-7
- **LEVEL SIX PRIORITY:**
- **MEMORY PARITY:**
CO2

START UP FOR MINI MONITOR

:BRANCH AROUND EAE ROUTINE

:SET UP STACK

:SET UP TIME OUT VECTOR

:UNDER AUTO MODE

:YES-SKIP TITLE PRINT-OUT

:PRINT TITLE

:TRY TO REFERENT THE

:LOCK OUT INTERRUPTS

:PRINT ROUTINE BUSY

:SAVE SWITCHES

:INTERRUPT ENABLE

:RESTART AFT "RESET" ENABLE

:RESET DID NOT CLEAR INTERRUPT ENABLE

:SET UP STACK

:SET A BIT

:IS IT SET

:RESET IS ON BUS TOO LONG

:IF BUS HANG, CHECK NO SACK TEMPO

:TEST FOR EAE
; TTY RECEIVER VALUES 0 TO 377

TTYINR: TSTB 2TRCSR

; IS DONE SET

FALSE RETURN FROM MAINLINE
TEST DATA FOR LEADER
IF LEADER GO BACK
NOT LEADER TEST FOR DATA
DATA COMPARISON ERROR
INCREMENT DATA
BASE DATA
START READER
RETURN TO MAINLINE
GO2

; TIME: 0

; CLEAR THE FLAG
; FOUND FLAG GO INCREMENT COUNTER

; CLEAR THE FLAG
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; RETURN TO MAINLINE
; TEST FOR DONE

; CLEAR THE FLAG
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; RETURN TO MAINLINE
; TEST FOR DONE

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; CLEAR THE FLA
MOVE TAPE TO REVERSE END ZONE

WRITE FORWARD ALL BLOCKS EXCEPT 0

FIND SEQUENTIAL BLOCK IN REVERSE DIRECTION
; READ REVERSE ALL BLOCK EXCEPT BLOCK 1101
READBK: MOV @TCRB1, @TCIV ; SET UP INTERRUPT VECTOR
MOV @TCFIRST, @TCCT ; READ ONE BLOCK
MOV #100, @TCWC ; READ THE BLOCK
JSR %7, TCI ; CHECK DATA BUFFER
RTI ; EXIT - RETURN WHEN BLOCK IS READ AND ERRORS
BPL +4 ; DECOTAPE ERROR
LDT 104000 ; NEW VECTOR FOR BLOCK SEARCH
MOV @TCRB1, @TCIV ; READ BLOCK FUNCTION
BR TCR4 ; RETURN TO BLOCK SEARCH

; THIS WRITE BUFFER LOOK THE SAME FORWARD OR REVERSE
; TCRBUF:
TCRB4: ;DECOTAPE READ/WRITE BUFFER
TCTBUF:
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<td>0 0 2 7 6</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
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<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
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<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
<td>0 0 3 1 2</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
<td>0 0 3 1 4</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
<td>0 0 3 2 0</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
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<td>DEC TAPE READ WRITE BUFFER</td>
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<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
<td>0 0 3 3 0</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
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<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
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<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
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<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
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<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
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<tr>
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<td>0 0 0 0 0 3</td>
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<td>DEC TAPE READ WRITE BUFFER</td>
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<tr>
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<td>DEC TAPE READ WRITE BUFFER</td>
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<tr>
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<td>DEC TAPE READ WRITE BUFFER</td>
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<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
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<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
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<tr>
<td>0 0 3 5 6</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
<tr>
<td>0 0 3 6 0</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
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<tr>
<td>0 0 3 6 2</td>
<td>0 0 0 0 0 3</td>
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<tr>
<td>0 0 3 6 4</td>
<td>0 0 0 0 0 3</td>
<td>0 0 0 0 0 3</td>
<td>DEC TAPE READ WRITE BUFFER</td>
</tr>
</tbody>
</table>

Note: The addresses are in hexadecimal format.
BEGIN: MOV #BEGIN,RETURN FOR SCOPING

MOV #4000,#COUNT ITERATION COUNT

TEST COMPARE INSTRUCTION INDEXED

MOV $10,%X MINS 10 TO R0

CMP R0,#125252 A INDEX BY MINUS 10 TO #125252

BEQ .+4 COMPARE WITH INDEX FAILED

.SCOPE .+4 INDEXED

.METY COMPARE FAILED DESTINATION INDE

.SET "ISB FOR DISKS AND KWIll TO CURRENT BANK

MOV $720 CURRENT BANK

BIC #0077777,0 LEAVE ONLY BANK BITS

ADD #0 #210C ADD IN CLOCK ENTRANCE

MOV $72000 #LINE CLOCK, KWIll

MOV $72000 #KWIll

.BF #11 ISR

.RF... ISR
870 006006 012700 177777 MOV 8-10, %D
871 006019 005460 016742  NEG D(10)
872 006016 002737 177777 016-32  CMP 8-1, 0@TEMP
873 006024 001401 177777 016-32  BEQ .44
874 006026 104000  MEL .44
875 006030 104000  SCOPE
876 006032 012737 000001 016732 MOV 8-1, 0@TEMP
877 006040 005460 016722
878 006050 02737 177777 016732 MOV 8-1, 0@TEMP
879 006056 001401 BEQ .44
880 006060 104000 MEL .44
881 006062 104000 SCOPE
882 006064 012737 177777 016732 MOV 8-1, 0@TEMP
883 006072 012700 177770 MOV 8-10, %D
884 006076 000261 SEC
885 006100 005560 016742 ADC D(0)
886 006107 005737 016732 TST 8@TEMP
887 006110 001401 BEQ .44
888 006112 104000 MEL .44
889 006114 104000 SCOPE
890 006116 012737 177777 016732 MOV 8-1, 0@TEMP
891 006127 012700 000001 MOV 8-10, %D
892 006130 000261 SEC
893 006132 005560 016722 TST 8@TEMP
894 006136 005737 016732 BEQ .44
895 006144 104000 MEL .44
896 006146 104000 SCOPE
897 006150 012737 000001 016732 MOV 8-1, 0@TEMP
898 006156 012700 177770 MOV 8-10, %D
899 006162 000261 SEC
900 006164 005560 016742 SUB D(0)
901 006170 005737 016732 TST 8@TEMP
902 006177 001401 BEQ .44
903 006180 104000 MEL .44
904 006182 104000 SCOPE
905 006202 012737 000001 016732 MOV 8-1, 0@TEMP
906 006210 012700 000001 MOV 8-10, %D
907 006214 000261 SEC
908 006216 005560 016722 SUB D(0)
909 006226 005737 016732 TST 8@TEMP
910 006230 001401 BEQ .44
911 006232 104000 MEL .44
912 006234 104000 SCOPE
913 006236 012700 177777 MOV %7, %D
914 006238 000261 ADD 8@10, %D
915 006242 000110 JMP 2,0
916 006244 104000 MEL .44

; NEG FAILED
; NEG FAILED
; ADC FAILED
; ADC FAILED
; SBC FAILED
; SBC FAILED
; TEST JMP INDIRECT
; JMP FAILED
:TEST INDIRECT ADDRESSING WITH INDEXING

;TEST COMPARE INSTRUCTION

CMP $125252, $125252
BEQ $125252, $125252

CMP $125252, $125252
BEQ $125252, $125252

;CMP FAILED

CMP $125252, $125252
BEQ $125252, $125252

;CMP FAILED

CMP $125252, $125252
BEQ $125252, $125252

;CMP FAILED

MOV $AB+2, $AB+2

;TEST MOVE INSTRUCTIONS

MOV $AB+2, $AB+2

;CMP FAILED
| 011004 | 014000 | MOV | $-1$, TEMP1 |
| 011006 | 014000 | MOV | $-10$, $0$ |
| 011008 | 015000 | COMB | C(0) |
| 011010 | 016000 | TSTB | TEMP1 |
| 011012 | 014000 | BEQ | .+4 |
| 011014 | 014000 | SCOPE |
| 011016 | 012737 | 177777 | 016732 |
| 011018 | 015000 | MOV | $-1$, TEMP |
| 01101A | 000000 | MOV | $10$, $0$ |
| 01101C | 015000 | COMB | C(0) |
| 01101E | 014000 | TSTB | TEMP |
| 011020 | 001400 | BEQ | .+4 |
| 011022 | 014000 | SCOPE |
| 011024 | 012737 | 177777 | 016732 |
| 011026 | 015000 | MOV | $-1$, TEMP |
| 011028 | 012700 | MOV | $10$, $0$ |
| 01102A | 000000 | COMB | C(0) |
| 01102C | 014000 | TSTB | TEMP |
| 01102E | 001400 | BEQ | .+4 |
| 011030 | 014000 | SCOPE |
| 011032 | 012737 | 177777 | 016732 |
| 011034 | 015000 | MOV | $-1$, TEMP |
| 011036 | 012700 | MOV | $10$, $0$ |
| 011038 | 000000 | COMB | C(0) |
| 01103A | 014000 | TSTB | TEMP |
| 01103C | 001400 | BEQ | .+4 |
| 01103E | 014000 | SCOPE |
| 011040 | 012737 | 177777 | 016732 |
| 011042 | 001400 | CMP | TEMP, $177400$ |
| 011044 | 014000 | CMP | TEMP, $177400$ |
| 011046 | 014000 | CMP | TEMP, $177400$ |
| 011048 | 014000 | CMP | TEMP, $177400$ |
| 01104A | 014000 | CMP | TEMP, $177400$ |
| 011050 | 014000 | CMP | TEMP, $177400$ |
| 011052 | 014000 | CMP | TEMP, $177400$ |
| 011054 | 014000 | CMP | TEMP, $177400$ |
| 011056 | 014000 | CMP | TEMP, $177400$ |
| 011058 | 014000 | CMP | TEMP, $177400$ |
| 01105A | 014000 | CMP | TEMP, $177400$ |
| 01105C | 014000 | CMP | TEMP, $177400$ |
| 01105E | 014000 | CMP | TEMP, $177400$ |
| 011060 | 014000 | CMP | TEMP, $177400$ |
| 011062 | 014000 | CMP | TEMP, $177400$ |
| 011064 | 014000 | CMP | TEMP, $177400$ |
| 011066 | 014000 | CMP | TEMP, $177400$ |
| 011068 | 014000 | CMP | TEMP, $177400$ |
| 01106A | 014000 | CMP | TEMP, $177400$ |
| 01106C | 014000 | CMP | TEMP, $177400$ |
| 01106E | 014000 | CMP | TEMP, $177400$ |
| 011070 | 014000 | CMP | TEMP, $177400$ |
| 011072 | 014000 | CMP | TEMP, $177400$ |
| 011074 | 014000 | CMP | TEMP, $177400$ |
| 011076 | 014000 | CMP | TEMP, $177400$ |
| 011078 | 014000 | CMP | TEMP, $177400$ |
| 01107A | 014000 | CMP | TEMP, $177400$ |
| 01107C | 014000 | CMP | TEMP, $177400$ |
| 01107E | 014000 | CMP | TEMP, $177400$ |
| 011080 | 014000 | CMP | TEMP, $177400$ |
| 011082 | 014000 | CMP | TEMP, $177400$ |
| 011084 | 014000 | CMP | TEMP, $177400$ |
| 011086 | 014000 | CMP | TEMP, $177400$ |
| 011088 | 014000 | CMP | TEMP, $177400$ |
| 01108A | 014000 | CMP | TEMP, $177400$ |
| 01108C | 014000 | CMP | TEMP, $177400$ |
| 01108E | 014000 | CMP | TEMP, $177400$ |
| 011090 | 014000 | CMP | TEMP, $177400$ |
| 011092 | 014000 | CMP | TEMP, $177400$ |
| 011094 | 014000 | CMP | TEMP, $177400$ |
| 011096 | 014000 | CMP | TEMP, $177400$ |
| 011098 | 014000 | CMP | TEMP, $177400$ |
| 01109A | 014000 | CMP | TEMP, $177400$ |
| 01109C | 014000 | CMP | TEMP, $177400$ |
| 01109E | 014000 | CMP | TEMP, $177400$ |
| 0110A0 | 014000 | CMP | TEMP, $177400$ |
| 0110A2 | 014000 | CMP | TEMP, $177400$ |
| 0110A4 | 014000 | CMP | TEMP, $177400$ |
| 0110A6 | 014000 | CMP | TEMP, $177400$ |
| 0110A8 | 014000 | CMP | TEMP, $177400$ |
| 0110AA | 014000 | CMP | TEMP, $177400$ |
| 0110AC | 014000 | CMP | TEMP, $177400$ |
| 0110AE | 014000 | CMP | TEMP, $177400$ |
| 0110B0 | 014000 |CMP | TEMP, $177400$ |

---

; LPB FAILED
; COMB FAILED
; COMB FAILED
; COMB FAILED
; COMB FAILED
; COMB FAILED
; INCB FAILED
; INCB FAILED
; INCB FAILED
; INCB FAILED
; DECB FAILED
; DECB FAILED
CMPB .#B+1,#B52
BEQ .+4
:CMFB FAILED

CMPB #125252,#B
BEQ .+4
:CMFB FAILED

CMPB #B,#B
BEQ .+4
:CMFB FAILED

:TEST MOVE INSTRUCTIONS

MovB #B,#B
CmpB #000252,#0
Beq .+4
:MOVFB FAILED

MovB #125252,#TEMP
CmpB #B,#TEMP
Beq .+4
:MOVFB FAILED

MovB #B,#C
CmpB #B,#C
Beq .+4
:MOVFB FAILED

:TEST UNARYS INDIRECT

Mov #1,#TEMP
Clrb #TEMP
Cmp #TEMP,#17777
Beq .+4
:CLRFB FAILED

Mov #125252,#TEMP
Cmp #TEMP,#125252
Beq .+4
:COMFB FAILED

Mov #125252,#TEMP
Cmp #TEMP,#125252
Beq .+4
:COMFB FAILED

Mov #052652,#TEMP
Cmp #TEMP,#052652
Beq .+4
:COMFB FAILED
LO4

011750 011754 005037 016732
011760 106237 016:33
011768 106232 000:40C 0:632
011770 001:40C
011772 010400

CLR @TEMP
INC @TEMP+1
CMP #C0.00@TEMP
BEQ .+4
HLT
SCOPE

:INC FAILED

011774 005037 016732
012000 106377 004:230
012004 023127 016:32 0CC377
012012 001:401
012014 104000
012016 010400
012020 005037 016732
012024 112737 000001.016733
012032 106437 016733
012036 023737 177400 016732
012044 001:401
012046 104000
012050 010400

CLR @TEMP
DECB @TEMP+2
CMP @TEMP.#377
BEQ .+4
HLT
SCOPE

:DECB FAILED

012052 127727 004624 126252
012060 001:401
012062 104000
012064 104400
12066 127727 125252 004606
012074 001:401
012076 104000
012078 104400
012080 127777 004574 004572
012090 001:401
012092 104000
012094 104400
012100 127777 004574 004572
012104 001:401
012106 104000
012108 104400

CMPB #B+2,#125252
BEQ .+4
HLT
SCOPE

:_CMPB FAILED

012110 001:401
012112 104000
012114 104400
012116 117700 004560
012124 127727 125252
012128 001:401
012130 104000
012132 104400
012134 127727 125252 004572
012142 126767 004532 016732
012150 001:401
012152 104000
012154 104400

MOV #B+2,#0
CMPB #125252,#B
BEQ .+4
HLT
SCOPE

:MOV FAILED

012156 117727 004520 004540
012164 127727 004518 016722
012172 001:401
012174 104000
012176 104400

MOV #B+2,#C+2
CMPB #B,#C
BEQ .+4
HLT
SCOPE

:MOV FAILED
"TEST" BIC INSTRUCTION INDIRECT WITH INDEXING

MOV $1-2, $0
BICB $AB-2, $0
CMPB $052525, $0
HLT .4

SCOPE

BICB FAILED

MOV $1-2, $0
BICB $AB+2, $0
CMPB $052525, $0
HLT .4

SCOPE

BICB FAILED

MOV $1-2, $0
BICB $AB+2, $0
CMPB $052525, $0
HLT .4

SCOPE

BICB FAILED

:"TEST" CMPA FAWS INDIRECT WITH INDEXING

MOV $1-2, $0
CLRB $0 TEMP+2
TSB $0 TEMP
HLT .4

SCOPE

CLRB FAILED

MOV $125252, $0
COMB $0 TEMP+2
CMPB $052525, $0 TEMP
HLT .4

SCOPE

COMB FAILED

MOV $050277, $0
INC $0 TEMP+2
CMPB $0, $0 TEMP
HLT .4

SCOPE

INC FAILED

MOV $050277, $0
DEC $0 TEMP+2
CMPB $0 TEMP+2, $0
HLT .4

SCOPE

DEC FAILED

MOV $1-2, $0
NEGB $0 TEMP+2
CMPB $1-1, $0 TEMP
HLT .4

SCOPE

NEGB FAILED

MOV $1-2, $0
NEGB $0 TEMP+2
CMPB $1-1, $0 TEMP
HLT .4

SCOPE

NEGB FAILED
BOS

; ADDRESS OF ADDRESS E 2
MOV B, #C+2, ;
CMP B, #C+1, ;
BCC B, |BOS| ;CMP FAILED

; ADDRESS OF ADDRESS E 0
MOV B, #B+4, ;
CMP B, #B+5, ;
BCC B, |BOS| ;CMP FAILED

; ADDRESS OF ADDRESS E 0
MOV B, #B+4, ;
CMP B, #B+5, ;
BCC B, |BOS| ;CMPB FAILED

; ADDRESS OF ADDRESS E 0
MOV B, #C+4, ;
MOV B, #C+5, ;
CLRB B, #1, ;
CMP B, #C+4, ;
BCC B, |BOS| ;CLRB FAILED

; ADDRESS OF ADDRESS E 0
MOV B, #1, ;
MOV B, #5, ;
MOV B, #6, ;
MOV B, #A, ;
BICB B, #B, ;
CMP B, #5726, ;
BCC B, |BOS| ;BICB FAILED

; TEST THAT RD IS NOT DESTROYED BY FALSE SELECTION
MOV B, #52525, ;
JSR C, ; THIS IS CHECK LATER IN PROGRAM

; JSR INSTRUCTION
TJSR1: JSR B, TJSR2
; PLACE PC ON STACK
TJSR2: CMP B, #TJSR1
; RETURN HERE ON RTS
JMP B, TJSR1
; CHECK FOR CORRECT PC ON STACK
BEQ B, TJSR3
; INCORRECT PC ON STACK
RTS
; RETURN TO INST AFTER JSR

; TEST THE STACK
TJSR3: TJSR3
; INSTRUCTION UNDER TEST
RTS
; TEST THE STACK
BEQ B, TJSR3+6
; PC OF JSR DID NOT GO TO STACK
HLT
; REPOSITION THE STACK

; TEST NESTED SUBROUTINES
CCC
; CLEAR CONDITION CODES
ROTEL I: SCOPE
: WILL ALLOW TWO FAST PASSES
3003 C1:106 104400
3005 C1:10 000257 177776
3006 C1:14 100002
3007 C1:16 000167 00632
3008 C1:17 :46
3009 C1:18 EASRT
: ADD AND SUBTRACT ALL NUMBERS AGAINST FIXED NUMBERS
3010 C1:22 01667 000072
3011 C1:26 02767 320001 17500
3012 C1:28 MOV #1, REF
3013 C1:34 INC REF
; TEST ALL COMBINATIONS OF NUMBERS WITH COMPARISON INSTRUCTION

; COMPARE:
; CLR %2
; INIT %2
; CMP: %2, %4
; ARE THE EQUAL
; BEQ .44
; CMP %2, %1
; BEQ CMP2
; INC %2
; INE CMP1
; CMP CMP1

; TEST COMPLEMENTING ALL NUMBERS

; CLR TEMP
; BASE DATA
; CLR TEMP+4
; BASE REFERENCE
; DEC TEMP+4
; COMPLEMENT DATA
; CMP TEMP TEMP+4
; DECREMENT REFERENCE
; BEQ .44
; TEST
; CMP TEMP TEMP+4
; COMPLEMENT OR DECREMENT FAILED
; INC TEMP
; INCREMENT AND TEST FOR DONE
; BNE TEMP
; NOT FINISHED GO COOP

; TEST COMB (EVEN BYTE)

; CLR TEMP
; BASE DATA
; CLR TEMP TEMP+4
; REFERENCE DATA
; CMP TEMP TEMP+4
; COMPARE
; BEQ .44
; COMPLEMENT OR INCREMENT BYTE FAILED

; TEST COMB (ODD BYTE)

; CLR TEMP TEMP+4
; BASE DATA
; CLR TEMP TEMP+4
; REFERENCE DATA
*TEST COMPARE ALL VALUES EVEN BYTE WITH ODD

;BASE VALUE
CLR TEMP
;COMPARE
BEQ .44
;COMPARE FAILED
BLE .44
;V IS NOT = TO N

;TEST TO SEE IF I/O DEVICES WERE SELECTED

CMPB #2777, #REGI
;BRANCH IF NO DEVICES SELECTED
BEQ WAIT4
;INTERRUPTS WILL OCCUR
;IF DEVICES ARE SELECTED

;TEST SWAB

MOV #0000, #COUNT

;TEST ALL COMBINATIONS OF SWAB

;NUMBER UNDER TEST
CLR REF
;REFERENCE NUMBER
; SET LIST ADDRESS
; NEG SIGN PRINT 1
; POS SIGN PRINT 0
; PUT MASK IN R3
; GET READY TO DOODLE NUMBER IN TOODLE
; COMPENSATES FOR COMPLEMENT DURING BIC
; AND IN OCTAL CHARACTER
; ZERO, WRITE 0 IF LIST
; COUNT UP TO
; AND RECORD
; SAME BINARY WEIGHT
; KEEP COUNT
; ADD ASCII PREFIX
; WRITE ASCII CHAR IN LIST
; EXPAND BINARY WEIGHT
; 5 CHAR IN LIST
; SET X3 FOR ADD LOOP
; MAKING SEVEN BY SEVEN
; MY SEVEN SET GET MX OCTAL
; SEND 5 CHAR TO TTY
; FINISH PRINTING GET NXT NUM
; HEAD FOR HOME

; SCOPE LOOP ROUTINE ENTERED BY USER TRAP
; SCOPE OR/AND ITERATION LOOP FOR EACH TEST 4000 TIMES
C06

MOV 3AC, (0)*+  ; STORE STACK POSITION, POWER FAIL FLAG
MOV 3MM, (0)*+  ; HALT ON POWER DOWN NORMAL
MOV 3SC, (0)*+  ; STACK IS SAVED HERE
MOV 0, SAVR6  ; RESTART, 24

177764  ; RESTART REGISTER OFF STACK
MOV 1*6+, X0  ; MQ MUST BE LOADED BEFORE AC
MOV 1*0, 3AC  ; RESTORE TIME OUT
MOV 1*0, 3AC  ; WHEN POWERING UP

181150  ; POWER FAIL OCCURRED
CLR #SERS  ; RETURN TO MAIN LINE

016612  ; FIXED VALUES FOR USE IN TEST
B: 152525  ; ADDRESS OF B
052525  ; ADDRESS OF B

A: 177774  ; ADDRESS OF A+10
-1
A+4

125252  ; ADDRESS OF A+10
052525  ; ADDRESS OF A+10 OR "D"

0  ; ADDRESS OF C

0  ; ADDRESS OF TEMP

0  ; ADDRESS OF TEMP+10

0  ; BUFFER FOR SP

0  ; OVERLAY USER ROUTINE HERE IF 4kw. USE 32"x" IF 3kw

17304  ; USE WITH VARIABLE CORE QUANTITY SYSTEMS
## CROSS REFERENCE TABLE - USER SYMBOLS

<table>
<thead>
<tr>
<th>Symbol</th>
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*Note: The table continues with a list of symbols and their descriptions.*

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**Legend:**
- #: Standard symbol
- *: Special symbol
- #: Optional symbol
- #: Rare symbol
- #:occasional symbol
- #: used in specific context

---

**Additional Information:**
- The symbols are used in various applications such as electronics, programming, and industrial design.
- Each symbol has a specific function and context of use.
- The table is designed to help users quickly identify and understand the symbols in different scenarios.

---

**References:**
- User manual for symbol interpretation.
- Technical manual for specific applications.
- ISO standards for symbol classification.
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**CROSS REFERENCE TABLE -- USER SYMBOLS**

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