PDP-11/70 HARDWARE
STUDENT HANDOUTS
PDP-11/70 PROCESSOR MAINTENANCE
COURSE OUTLINE

DAY 1

I. Introduction

II. PDP-11/70 System Description
   A. System Components
   B. Physical Configuration
   C. PDP-11/70 Addressing Space

III. KB11-B Block Diagram
   A. Data Paths Block Diagram
   B. Control Block Diagram

IV. KB11-B Timing
   A. Basic Timing
   B. Pause Timing

References: KB11-B Processor Manual Sec. I Ch. 1, Sec. II pp 1-1 to 1-6, pp 2-1 to 2-3, Ch. 4.

Reading Assignment: KB11-B Processor Manual Sec. I Ch. 1, Sec. II, Ch. 4.
DAY 2

V. Control ROM
   A. RAR and RBR Timing
   B. Address Calculation
      1. Fork
      2. Branch

VI. Flow Diagram Concepts
   A. Symbology
   B. Correlation to ROM Map and Block Diagram

VII. Control Console
   A. Flows
   B. Logic

VIIII. Load Address Operation

References: KB11-B Processor Manual Sec. II Para. 1.2 to 1.2.3, Para. 1.4 to 1.4.8, Sec. III Para. 2.1 to 2.5.2.

Reading Assignment: KB11-B Processor Manual Sec. II Para. 1.2.1, 1.4 to 1.4.4.
DAY 3

IX. Register Deposit/Deposit Step Operation
   A. General Register Selection

X. Register Examine/Examine Step Operation

XI. Examine and Examine Step Operation
   A. Unibus Data Transfers

XII. Deposit and Deposit Step Operation

XIII. Start Operation

XIV. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. II Para. 2.1.4, Ch. 5, Sec. III, Para 2.5 to 2.12

Reading Assignment: KB11-B Processor Manual Sec. II Ch. 5, Sec. III Para. 2.7.3.
DAY 4.

XV. Condition Code Instructions
   A. Flows
   B. Logic

XVI. Branch Instructions
   A. Flows
   B. Logic

XVII. Single Operand Instructions
   A. No Memory Reference
   B. Destination Operand Acquisition

XVIII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. II, Para.1.4.6.1 to 1.5.8.

Reading Assignment: KB-11-B Processor Manual Sec. II Para.1.4.6.1 to 1.5.8.
DAY 5

XIX. Double Operand Instructions

XX. Register Instructions
   A. ASH
   B. ASHC

XXI. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. II Para. 1.2.5.7, 2.1.5 to 21.8.

Reading Assignment: KB11-B Processor Manual Sec. II Para. 2.1.5 to 2.1.8.
DAY 6

XXII. Register Instructions (continued)
   A. MUL
   B. DIV

XXIII. Trap and Subroutine Operations
   A. JMP and JSR
   B. RTS
   C. TRAP
   D. RTI and RTT
   E. PSW Logic

References:  KB11-B Processor Manual Sec. II Para. 1.2.5.8, 1.2.5.9, 3.9 to 3.9.10.

Reading Assignment:  KB11-B Processor Manual Sec. II Para. 1.2.5.8, 1.2.5.9, 3.9 to 3.9.10.
DAY 7

XXIV. BRQ Operations
   A. Service Flows
   B. Interrupts and Traps
   C. Power Up and Power Down

XXV. Troubleshooting Laboratory

References: KBll-B Processor Manual Sec. II Ch. 6.

Reading Assignment: KBll-B Processor Manual Sec. II Ch. 6.
DAY 8

XXVI. Cache Concepts

XXVII. Block Diagram
   A. Address Logic
   B. Data Logic

XXVIII. Program Example

XXIX. Cache Logic
   A. Timing
   B. Power Up - Initialization
   C. Request Arbitrator
   D. Cache Registers

XXX. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. VI Ch. 1, 2, Para. 4.3 to 4.8.8.

Reading Assignment: KB11-B Processor Manual Sec. VI Ch. 1, Para. 2.1 to 2.2.3.6, 4.3 to 4.5.
DAY 9

XXXI. Cache Operations

A. Read Hit
   1. Processor
   2. Unibus Map

B. Processor Bust - Bend Cycle

C. Read Miss
   1. Processor
   2. Unibus Map

D. Write
   1. Processor
   2. Unibus Map

E. Register Read and Write

XXXII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. VI Para. 3.8 to 3.8.8.

Reading Assignment: KB11-B Processor Manual Sec. VI Para. 3.8 to 3.8.8
DAY 10

XXXIII. Memory Management
   A. Relocation
   B. Protection
   C. Multiple Modes
   D. Statistical Information

XXXIV. Memory Management Timing

XXXV. ROM Control

References: KB11-B Processor Manual Sec. IV Ch. 1, Para 2.1, 2.2, 3.1, 3.2; Ch. 6.

Reading Assignment: KB11-B Processor Manual Sec. IV Ch. 1, 6.
DAY 11

XXXVI. Memory Management Relocation Logic
   A. Selection of K, S, U Space
   B. Selection of I, D Space
   C. Generation of Physical Address

XXXVII. Memory Management Protection Logic
   A. Selection of a PDR
   B. Memory Management Trap Logic
   C. Memory Management Abort Logic

XXXVIII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. IV Chs. 3,4,5,8.

Reading Assignment: KB11-B Processor Manual Sec. IV Chs. 3,4,5,8.
DAY 12

XXXIX. Memory Management Internal Register Logic
   A. PDR A and W Bit Operation

XXX. MTP, MFP Instruction Execution

XXXI. Unibus Map
   A. Block Diagram
   B. Operation

XXXII. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. IV Ch. 7, 9, Sec. V Ch. 1.

Reading Assignment: KB11-B Processor Manual Sec. IV Ch. 7, 9, Sec. V, Ch. 1.
DAY 13

XXXIII. Unibus Map Logic
   A. Cache/Unibus Transactions
   B. Register Operations

XXXIV. Troubleshooting Laboratory

References: KB11-B Processor Manual Sec. V Ch. 2,3.

Reading Assignment: KB11-B Processor Manual Sec. V Ch. 2,3.
Day 14

XXXXV. MJ11 Core Memory

A. 3 Wire Memory Operation

B. MJ11 Operations
   1. Read
   2. Write
   3. Exchange

C. MJ11 Configuration
   1. Block Diagram
   2. Memory Controller
   3. Internal Bus
   4. Stack Module Set

D. Main Memory Bus
   1. Description
   2. Bus Protocol

E. Memory Timing Control Signals

XXXXVI. Troubleshooting Laboratory

References: MJ11 Memory System Maintenance Manual: Ch. 1, 2, Para. 3.1 to 3.5.

Reading Assignment: MJ11 Memory System Maintenance Manual: Ch. 1, Para. 3.1 to 3.5.
DAY 15

XXXXVII. MJll Stack Module Set
   A. Organization
   B. Logic Operation
   C. Example

XXXXVIII. Troubleshooting Laboratory

References: MJll Memory System Maintenance Manual: Ch. 4.

Reading Assignment: MJll Memory System Maintenance Manual: Ch. 4.
PDP-11/70 MJ11 MEMORY OPTIONS

Minimum Configuration
CPU Cabinet with CPU
1 Memory Cabinet
1 Memory Box with Controller and Transceiver
64K words

Maximum Configuration
CPU Cabinet with CPU
2 Memory Cabinets
8 Memory Boxes with Controller and Transceiver in each box
1024K words
Figure 1-5 Word and Byte Addresses
### Figure 1-6 Main Memory Addresses

<table>
<thead>
<tr>
<th>WORD 1</th>
<th>WORD 0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BYTE 3</strong></td>
<td><strong>BYTE 2</strong></td>
</tr>
<tr>
<td>00 000 003</td>
<td>00 000 002</td>
</tr>
<tr>
<td>00 000 007</td>
<td>00 000 006</td>
</tr>
<tr>
<td>00 000 010</td>
<td>00 000 000</td>
</tr>
<tr>
<td>00 777 767</td>
<td>00 777 766</td>
</tr>
<tr>
<td>00 777 773</td>
<td>00 777 772</td>
</tr>
<tr>
<td>00 777 777</td>
<td>00 777 776</td>
</tr>
</tbody>
</table>

**Note:** The table and diagram illustrate the memory address layout with byte values from 00 000 000 to 00 777 774.
PDP-11/70 SYSTEM ADDRESS

17 777 776 Unibus
17 000 000
16 777 776

Non Existent Memory

17 760 000
17 757 776

Unibus Map
124K

17 000 000

10 000 000
07 777 776

Maximum 1M

Core Memory

00 377 776
00 000 000

Minimum 64K

17 777 776 Processor Status
17 777 774 Stack Limit
17 777 772 Program Interrupt Request
17 777 770 Microprogram Break
17 777 766 CPU Error
17 777 764 System ID
17 777 762 System Size Hi
17 777 760 System Size Lo
17 777 762 Hit/Miss
17 777 750 Maintenance
17 777 746 Control
17 777 744 Memory System Error
17 777 742 High Error Address
17 777 740 Low Error Address

System Registers
Figure 1-7 Address Paths
Figure 1-10  18-Bit Mapping
Figure 1-11  22-Bit Mapping
Figure 2-1 Block Diagram Data Paths
PROCESSOR CONTROL REGISTERS / ADDRESSES

Figure 3-1 CPU Error Register

Figure 3-2 Program Interrupt Register

Figure 3-3 Stack Limit Register

Figure 3-4 Processor Status Word

Lower Size Register

System ID Register

(TMCD) 17 777 766

(FPDRD) 17 777 772

(PDRC) 17 777 774

(IRCH,PDRD) 17 777 776

Lower Size Register

System ID Register

(SCCN) 17 777 760

(SCCN) 17 777 764
Figure 1-1 BLOCK DIAGRAM
Figure 4-6 Time States
Figure 4-7 Timing Generator & Pauses
<table>
<thead>
<tr>
<th>Table 4-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ring Counter Stop and Pause Conditions</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STOP IN T2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Bus Pause</td>
</tr>
</tbody>
</table>
| Stop: SAPN NOT CACHE ADRS H  
  TIGA PAUSE H (UBSD = 2 or 3)  
  TIGA S0 (0) H or TIGA S1 (0) H |
| Restart: S0 and S1 count to 3 (90 ns). |
| Unibus Pause CPU Control Registers |
| Stop: Same as Internal Bus Pause |
| Restart: Same as Internal Bus AND UBCB TIG RESTART H (BUS SSYN) |
| Interrupt Pause |
| Stop: UBSD = 1 (INTR Pause)  
  UBCD EXT BRQ H |
| Restart: UBCB TIG RESTART H (Passive Release or BUS INTR) |
| Single ROM Cycle |
| Stop: TIGE ROM+UPB (1) H |
| Restart: CONTINUE or MAINTENANCE (XMAA S4) switches |

<table>
<thead>
<tr>
<th>STOP IN T5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache Pause</td>
</tr>
</tbody>
</table>
| Stop: TMCF CACHE ADRS H  
  TIGA PAUSE H (UBSD = 2 or 3)  
  No Aborts (not TMCC ABORT H) |
| Restart: TIGA MEMSYNC (1) H |
| Single Bus Cycle |
| Stop: TIGE SINGLE CY L  
  TIGA PAUSE H |
| Restart: CONTINUE or MAINTENANCE (XMAA S4) switches |
Figure 1-4  ROM Timing
Figure 1-3  Flow Chart Symbols (P/O Flows 2)
PDP11/70 DIAGNOSTICS

Each diagnostic test assumes successful completion of preceding tests.

Diagnostics should be run in the following sequence, otherwise errors will
not be detected or error messages will be misleading.

| MD-11-DEKBH-A | Diagnostic ROM (M9301-YC) |
| MD-11-DEKBA-A | CPU - Part 1              |
| MD-11-DEKBB-A | CPU - Part 2              |
| MD-11-DEKBC-A | Cache - Part 1            |
| MD-11-DEKBD-A | Cache - Part 2            |
| MD-11-DEKBE-A | Memory Management         |
| MD-11-DEKBF-A | Unibus Map                |
| MD-11-DEKBG-A | Power Fail                |
| MD-11-DEMJA-A | Main Memory               |
| MD-11-DEQKC-A | Test T15                  |

| MD-11-DERHA-A | RH-70 Masbus Control     |
| MD-11-DZTUA-A | TU16                      |
| thru DZTUF-A  |                           |
| MD-11-DERSA-A | RS03/RS04                |
| thru DERSD-A  |                           |
| MD-11-DERPK-A | RP04                     |
| thru DERPN-A  |                           |
| and DERPS-A   |                           |
| thru DERPV-A  |                           |

PDP11/70 Diagnostics are stored on two disks
MAINDEC 11-DZZA-A-HB
MAINDEC 11-DZZB-A-HB

MD-11-DEKBI-A is a paper tape diagnostic to check the M9301-YC.
NOTES:

1. Set CP BUSY if -(INPR + NPC + SACK + DSACK + ABORT + BBUSY).

2. CP BUSY is not cleared if DATIP cycle. It is cleared on DATO portion of DATIP/ DATO.

3. Used to start DATO address deskew on DATIP/DATO operation.

4. 75 ns data deskew is obtained by 2 stage synchronizer on TIGA. Unibus data is loaded into PDRH buffer register at T3.

5. Address & control are deskewed from T3 to T1. PDRH buffer register loaded to BR at T1.

Figure 5-2 Unibus Data Transfers
## Positive Multiplicand, Positive Multiplier

**MUL %0, 2**

R0 = 005

R2 = 003

<table>
<thead>
<tr>
<th>UADR</th>
<th>NEXT UADR</th>
<th>SC</th>
<th>SR</th>
<th>ALU</th>
<th>SHFR</th>
<th>BR</th>
<th>DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>MUL.10</td>
<td>MUL.20</td>
<td>6</td>
<td>00 000 011</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00 000 101</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.30</td>
<td>5</td>
<td>00 000 011</td>
<td>00 000 011</td>
<td>00 000 001</td>
<td>00 000 001</td>
<td>10 000 001</td>
</tr>
<tr>
<td>MUL.30</td>
<td>MUL.20</td>
<td>4</td>
<td>00 000 011</td>
<td>00 000 001</td>
<td>00 000 000</td>
<td>00 000 000</td>
<td>11 000 000</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.30</td>
<td>3</td>
<td>00 000 011</td>
<td>00 000 011</td>
<td>00 000 001</td>
<td>00 000 001</td>
<td>11 100 000</td>
</tr>
<tr>
<td>MUL.30</td>
<td>MUL.30</td>
<td>2</td>
<td>00 000 011</td>
<td>00 000 001</td>
<td>00 000 000</td>
<td>00 000 000</td>
<td>11 110 000</td>
</tr>
<tr>
<td>MUL.30</td>
<td>MUL.30</td>
<td>1</td>
<td>00 000 011</td>
<td>00 000 000</td>
<td>00 000 000</td>
<td>00 000 000</td>
<td>01 111 000</td>
</tr>
<tr>
<td>MUL.30</td>
<td>MUL.30</td>
<td>0</td>
<td>00 000 011</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00 111 100</td>
</tr>
<tr>
<td>MUL.30</td>
<td>MUL.40</td>
<td>-</td>
<td>00 000 011</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00 011 110</td>
</tr>
<tr>
<td>MUL.40</td>
<td>MUL.60</td>
<td>-</td>
<td>00 000 011</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00 001 111</td>
</tr>
<tr>
<td>MUL.60</td>
<td>FET.</td>
<td>-</td>
<td>00 000 011</td>
<td>00 001 111</td>
<td>00 001 111</td>
<td>0</td>
<td>00 001 111</td>
</tr>
</tbody>
</table>
NEGATIVE MULTIPLICAND, NEGATIVE MULTIPLIER

MUL %0, 2

R2 = 375 (-3)  \quad -3
R0 = 376 (-2)  \quad \underline{+6}

<table>
<thead>
<tr>
<th>UADR</th>
<th>NEXT</th>
<th>SC</th>
<th>SR</th>
<th>ALU</th>
<th>SHFR</th>
<th>BR</th>
<th>DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>MUL.10</td>
<td>MUL.30</td>
<td>6</td>
<td>11 111 101</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>01 111 111</td>
</tr>
<tr>
<td>MUL.30</td>
<td>MUL.20</td>
<td>5</td>
<td>11 111 101</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00 111 111</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.20</td>
<td>4</td>
<td>11 111 101</td>
<td>11 111 101</td>
<td>11 111 110</td>
<td>11 111 110</td>
<td>10 011 111</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.20</td>
<td>3</td>
<td>11 111 101</td>
<td>11 111 011</td>
<td>11 111 101</td>
<td>11 111 101</td>
<td>11 001 111</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.20</td>
<td>2</td>
<td>11 111 101</td>
<td>11 111 010</td>
<td>11 111 101</td>
<td>01 111 101</td>
<td>01 100 111</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.20</td>
<td>1</td>
<td>11 111 101</td>
<td>11 111 010</td>
<td>11 111 101</td>
<td>11 111 101</td>
<td>00 110 011</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.20</td>
<td>0</td>
<td>11 111 101</td>
<td>11 111 010</td>
<td>11 111 101</td>
<td>11 111 101</td>
<td>00 011 001</td>
</tr>
<tr>
<td>MUL.20</td>
<td>MUL.50</td>
<td>-</td>
<td>11 111 101</td>
<td>11 111 010</td>
<td>11 111 101</td>
<td>11 111 101</td>
<td>00 001 100</td>
</tr>
<tr>
<td>MUL.50</td>
<td>MUL.60</td>
<td>-</td>
<td>11 111 101</td>
<td>00 000 000</td>
<td>00 000 000</td>
<td>00 000 000</td>
<td>00 000 110 STORE BR</td>
</tr>
<tr>
<td>MUL.60</td>
<td>FET.00</td>
<td>-</td>
<td>11 111 101</td>
<td>00 000 110</td>
<td>00 000 110</td>
<td>00 000 000</td>
<td>00 000 110 STORE DR</td>
</tr>
</tbody>
</table>
DIVIDE BLOCK DIAGRAM

NOTES:
At completion of divide
DR = Quotient
BR = Remainder
SR = Unchanged

SIGNS = \(A - B\)
SIGNS = \(A + B\)
DIV. R2, R1

| t1 | BA ← PCB |
| t2 | SHFR ← SR-SR |
| t3 | BUST CLEAR FLAGS |
| t6 | IR ← SHFR |

ICLASS
DAC
BSOPI

2000/DIV R2, R1

FET. ØØ

| t1 | BA ← PCB |
| t2 | SHFR ← PCB+2 |
| t3 | BRQ STROBE BUS PAUSE |
| t5 | PCA ← PCB+2 |
| t6 | IR ← BUS BR ← BUS PCB ← PCA 1RD.ØØ |

FET.1Ø

| t1 | BA ← PCB |
| t2 | SHFR ← PCB |
| t3 | CONDITIONAL BUST |
| t5 | PCA ← PCB+2 |
| t6 | SF7: SR ← GS(SF) SR ← R2 -DF: DR ← GD(DF) DR ← R1 |

R1 = 76
R2 = 77
R3 = 71

BA = 2000
BCØ & BC1 = Ø
SHFR = 2002
PCA = 2002
IR = DIV R2, R1
BR = DIV R2, R1
PCB = 2002

BA = 2002
BCØ & BC1 = Ø
SHFR = 2002

PCA = 2004
SR = 77
DR = 76

DIV * DMØ

DVS. ØØ
t1 \( \langle BA \leftarrow PCB \rangle \)  
\( t2 \) SHFR\( \leftarrow \) DR  
\( t3 \) BEND  
\( t6 \) BR \( \leftarrow \) SHFR

**DIV.00**

\( t1 \) BA \( \leftarrow \) DR  
\( BC \leftarrow \) BSQPI  
\( t2 \) SHFR\( \leftarrow \) BR  
\( t6 \) SR \( \leftarrow \) SHFR  
\( DR \leftarrow \) GD(SF)  
\( DR \leftarrow \) R2  
CCLD4  
N=1, Z=\( \emptyset \), V&C=\( \emptyset \)

**DIV.10**

\( t1 \) \( \langle BA \leftarrow SR \rangle \)  
\( t2 \) SHFR\( \leftarrow \) DR  
\( t6 \) CCLD4  

\( N=1, Z=\emptyset, V&C=\emptyset \)

,  
-\( Z \)  
:

**DIV.20**

\( t1 \) \( \langle BA \leftarrow DR \rangle \)  
\( t2 \) \( \langle SHFR \leftarrow SR \rangle \)  

,  
\( N \)  
:

**DVN.00**

\( t1 \) \( \langle BA \leftarrow DR \rangle \)  
\( t2 \) \( \langle SHFR \leftarrow SR \rangle \)  
\( t3 \) CLEAR DR  
\( t6 \) SR\( \leftarrow \) GS(SFV1)  
SR\( \leftarrow \) R3

**DVN.10**

\( t1 \) \( \langle BA \leftarrow DR \rangle \)  
\( t2 \) SHFR\( \leftarrow \) DR-SR  

**BA = 2002**  
**SHFR = 76**  
**BUS CYCLE END**  
**BR = 76**  
**DIVISOR**

**BA = 76**  
**BC = DATI**  
**SHFR = 76**  
**SR = 76**  
**DR = 77**  
**HI ORDER DIVIDEND**

**BA = 76**  
**SHFR = 76**

,  
-\( Z \)  
:

**BA = 77**  
**SHFR = 76**

,  
\( N \)  
:

**BA = 77**  
**SHFR = 76**  
**DR = \emptyset \emptyset**  
**SR = 71**

**BA = \emptyset \emptyset**  
**DR = 000000**  
**SR_2 = 000111**  
**SHFR = 000111**
t5 \ GR(SFV1) \rightarrow SHFR \\
\ R3 \leftarrow SHFR \\
\ DVN.2Ø \\
\ t1 \ \langle BA \leftarrow DR \rangle \\
\ t2 \ \ SHFR \leftarrow DR-SR \\
\ t6 \ \ DR \leftarrow LEFT (DR) \\
\ DVN.3Ø \\
\ t1 \ \langle BA \leftarrow DR \rangle \\
\ t2 \ \ SHFR \leftarrow DR-1 \\
\ t6 \ \ SR \leftarrow GS(SF) \\
\ SR \leftarrow R2 \\
\ DR \leftarrow SHFR \\
\ DVN.4Ø \\
\ t1 \ \langle BA \leftarrow DR \rangle \\
\ t2 \ \ SHFR \leftarrow DR-SR \\
\ t5 \ \ GR(SF) \leftarrow SHFR \\
\ R2 \leftarrow SHFR \\
\ t6 \ \ DR \leftarrow SHFR \\
\ CCLD4 \\
\ N=Ø, \ Z=1, \ V&C=Ø \\
\ DVN.5Ø \\
\ t1 \ \langle BA \leftarrow DR \rangle \\
\ t2 \ \ SHFR \leftarrow BR \\
\ t6 \ \ SR \leftarrow SHFR \\
\ \cdot \\
\ \cdot \\
\ -N \\
\ \cdot \\
\ DVN.6Ø \\
\ t1 \ \langle BA \leftarrow DR \rangle \\
\ t2 \ \ SHFR \leftarrow DR \\
\ t6 \ \ BR \leftarrow SHFR \\
\ R3 = Ø7 \\
\ BA = ØØ \\
\ DR = 000000 \\
\ SR^2 = 000111 \\
\ SHFR = 000111 \\
\ DR = ØØ \\
\ BA = ØØ \\
\ DR = 000000 \\
\ -1 = 111111 \\
\ SHFR = 111111 \\
\ COUT15 = Ø \\
\ SR = 77 \ HI ORDER DIVIDEND \\
\ DR = 77 \\
\ BA = 77 \\
\ DR = 111111 \\
\ SR^2 = 000001 \\
\ SHFR = 000000 \\
\ R2 = ØØ \\
\ DR = ØØ \\
\ BA = ØØ \\
\ SHFR = 76 \ DIVISOR \\
\ SR = 76 \\
\ BA = ØØ \\
\ SHFR = ØØ \\
\ BR = ØØ
DVN. 7Ø (9)

\[
\begin{align*}
t1 & \quad BA \leftarrow DR \\
t2 & \quad SHFR \leftarrow DR \\
t3 & \quad SC \leftarrow \emptyset \\
t6 & \quad DR \leftarrow GD(SFV1) \\
& \quad DR \leftarrow R3 \\
& \quad CCLD4
\end{align*}
\]

BA = 7Ø
SHFR = 77
SC = 5Ø
DR = 77 LOW ORDER DIVIDEND

N=1, Z=Ø, V&C=Ø

DIV.3Ø

\[
\begin{align*}
t1 & \quad BA \leftarrow DR \\
t2 & \quad SHFR \leftarrow ALUS \quad BR+BR+DR15
\end{align*}
\]

BA = 77
BR = 000000
BR = 000000
DR15 = 0
SHFR = 000000
BR=7Ø

N=1, C,V&2=1

SR15(1)

DIV.50

\[
\begin{align*}
t1 & \quad BA \leftarrow DR \\
t2 & \quad SHFR \leftarrow BR+SR \\
t3 & \quad SC \leftarrow SC-1 \\
t6 & \quad BR \leftarrow SHFR \\
& \quad DR \leftarrow LEFT(DR) \\
& \quad (ALU CARRY INSERTED) \\
& \quad CCLD6
\end{align*}
\]

BA = 77
BR = 000000
SR = 111110
SHFR = 111110 COUT15 = 0
SC=04
BR = 76
DR = 001110

N=Ø, Z=Ø, C=1 & V=1

DIV.60

\[
\begin{align*}
t1 & \quad BA \leftarrow DR \\
t2 & \quad SHFR \leftarrow BR
\end{align*}
\]

BA = 16
SHFR = 76

-DIV QUIT

z=1 ∧ SR15(1)

DIV.7Ø
t1  <BA ← DR>  

BA = 16  
BR = 111110  
BR = 111110  
DR15 = 0  
SHFR = 111100  

BR = 74  

COUT15 = Ø  SR15(1) FROM DIV.50

DIV SUB

DIV.8Ø

BA = 001110  
BR = 111100  
SR2 = 000010  
SHFR = 111110  

COUT15 = Ø  
BR = 76  
DR = 011100

DIV.7Ø

BA = 34  
BR = 111110  
BR = 111110  
DR15 = 0  
SHFR = 111100  

BR = 74  

COUT15=Ø∧SR15(1)

DIV SUB

DIV.8Ø

BA = 34  
BR = 111100  
SR2 = 000010  
SHFR = 111110  

SC = Ø2  COUT15 = Ø  
BR = 76  
DR = 111000

DIV.70

BA = 70  
BR = 111110  
BR = 111110  
DR15 = 1  
SHFR = 111101  

BR = 75
DIV SUB

DIV. 8Ø

t1 <BA ← DR>
t2 SHFR ← BR-SR

t3 SC ← SC-1
t6 BR ← SHFR
  DR ← LEFT(DR)

DIV. 7Ø

BA = 70
  BR = 111101
  SR² = 000010
  SHFR = 111111
  COUT15 = Ø
SC = Ø
  BR = 111111
  DR = 110000

BA = 110000
  BR = 111111
  DR = 111111
  DR15 = 1
  SHFR = 111111
  BR = 77

DIV SUB

DIV. 8Ø

BA = 110000
  BR = 111111
  SR² = 000010
  SHFR = 000011
  COUT15 = 1
SC = Ø
  BR = 000001
  DR = 100001

BA = 41
  BR = 000001
  DR = 000001
  DR15 = 1
  SHFR = 000011
  BR = 03

BA = 41

DIV. 9Ø

t1 <BA ← DR>
t2 \text{SHFR} \leftarrow \text{BR} + \text{SR} \quad \text{BR} = \text{000011}, \text{SR} = \text{111110}, \text{SHFR} = \text{0000011}

t3 \text{SC} \leftarrow \text{SC} - 1 \quad \text{SC} = \text{77}

t6 \text{BR} \leftarrow \text{SHFR} \quad \text{BR} = \text{0000010}, \text{SHFR} = \text{000011}

t6 \text{DR} \leftarrow \text{LEFT (DR)} \quad \text{DR} = \text{000011}

\text{DVC.} \emptyset \emptyset

\text{N}

\text{DVC.} \text{60}

t1 \langle \text{BA} \leftarrow \text{DR} \rangle \quad \text{BA} = \text{03}

t2 \text{SHFR} \leftarrow \text{-BR} \quad \text{SHFR} = \text{01}, \text{BR} = \text{0000110}

t6 \text{BR} \leftarrow \text{SHFR} \quad \text{BR} = \text{111110}

\text{DVC.} \text{70}$

\text{t1} \langle \text{BA} \leftarrow \text{-DR} \rangle \quad \text{BA} = \text{03}

t2 \text{SHFR} \leftarrow \text{BR} + 1 \quad \text{BR} = \text{1111101}, \text{SHFR} = \text{1111111}

t5 \text{GR (SFV) \leftarrow SHFR} \quad \text{R3} = \text{77}

\text{DVC.} \text{70}$

\text{t1} \langle \text{BA} \leftarrow \text{-DR} \rangle \quad \text{BA} = \text{03}

t2 \text{SHFR} \leftarrow \text{DR} \quad \text{SHFR} = \text{03}

t3 \text{BRQ STROBE} \quad \text{BR} = \text{03}

t5 \text{GR (SF) \leftarrow SHFR} \quad \text{R2} = \text{03}

t6 \text{CCLD4} \quad \text{R2} = \text{03}

\text{N} = \emptyset, \text{Z} = \emptyset, \text{V&C} = \emptyset
Figure 6-1 Examples of Stack Limit
Figure 6-3 Stack Error Aborts
<table>
<thead>
<tr>
<th>Order</th>
<th>Condition</th>
<th>Input</th>
<th>Output*</th>
<th>Result*</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>console flag</td>
<td>UBCF STOP L</td>
<td>TMCA CONF (1) H</td>
<td>do console control function</td>
</tr>
<tr>
<td>2</td>
<td>cache parity</td>
<td>CCBJ PARITY TRAP H</td>
<td>TMCB PART L</td>
<td>trap (114)</td>
</tr>
<tr>
<td>3</td>
<td>memory management traps</td>
<td>SSRD MEM MGMNT TRAP L</td>
<td>TMCB SEGT L TMCB HONOR SEGT H</td>
<td>trap (250)</td>
</tr>
<tr>
<td>4</td>
<td>warning stack violation</td>
<td>TMCD SL YEL</td>
<td>TMCB HONOR SLY H</td>
<td>trap (4)</td>
</tr>
<tr>
<td>5</td>
<td>power fail</td>
<td>UBCE PDNF (1) H</td>
<td>TMCB HONOR PWRF L</td>
<td>trap (24)</td>
</tr>
<tr>
<td>6</td>
<td>floating-point exception trap CP LEV 7</td>
<td>FRIH FF EXC TRAP L</td>
<td>TMCB HONOR FPTRAP L</td>
<td>trap (224)</td>
</tr>
<tr>
<td>7</td>
<td>priority interrupt request PIRQ7</td>
<td>PDRD PIR15 (1) H</td>
<td>TMCB HONOR PIR7 L</td>
<td>trap (240)</td>
</tr>
<tr>
<td>8</td>
<td>bus request, level 7 interrupt CP LEV 6</td>
<td>BUS BR7 L</td>
<td>TMCB HONOR BR7 L</td>
<td>interrupt</td>
</tr>
<tr>
<td>9</td>
<td>priority interrupt request PIRQ6</td>
<td>PDRD PIR14 (1) H</td>
<td>TMCB HONOR PIR6 L</td>
<td>trap (240)</td>
</tr>
<tr>
<td>10</td>
<td>bus request, level 6 interrupt CP LEV 5</td>
<td>BUS BR6 L</td>
<td>TMCB HONOR BR6 L</td>
<td>interrupt</td>
</tr>
<tr>
<td>11</td>
<td>priority interrupt request PIRQ5</td>
<td>PDRD PIR13 (1) H</td>
<td>TMCB HONOR PIR5 L</td>
<td>trap (240)</td>
</tr>
<tr>
<td>12</td>
<td>bus request, level 5 interrupt CP LEV 4</td>
<td>BUS BR5 L</td>
<td>TMCB HONOR BR5 L</td>
<td>interrupt</td>
</tr>
<tr>
<td>13</td>
<td>priority interrupt request PIRQ4</td>
<td>PDRD PIR12 (1) H</td>
<td>TMCB HONOR PIR4 L</td>
<td>trap (240)</td>
</tr>
<tr>
<td>14</td>
<td>bus request, level 4 interrupt CP LEV 3</td>
<td>BUS BR4 L</td>
<td>TMCB HONOR BR4 L</td>
<td>interrupt</td>
</tr>
<tr>
<td>15</td>
<td>priority interrupt request PIRQ3</td>
<td>PDRD PIR11 (1) H</td>
<td>TMCB HONOR PIR3 L</td>
<td>trap (240)</td>
</tr>
<tr>
<td>16</td>
<td>priority request PIRQ2 CP LEV 2</td>
<td>PDRD PIR10 (1) H</td>
<td>TMCB HONOR PIR2 L</td>
<td>trap (240)</td>
</tr>
<tr>
<td>17</td>
<td>priority request PIRQ1 CP LEV 1</td>
<td>PDRD PIR09 (1) H</td>
<td>TMCB HONOR PIR1 L</td>
<td>trap (240)</td>
</tr>
<tr>
<td>18</td>
<td>T bit set and not RTT CP LEV 1</td>
<td>PDRD PS04 (1) H and - (IRCQ RTT L)</td>
<td>TMCB HONOR T L</td>
<td>trap (14)</td>
</tr>
</tbody>
</table>

* Only if no higher priority request has been received.
Figure 6-9  INTR Sequence
Figure 6-11  Power-Up

*NOTE*: Power-up subroutine executed during this time.
UBCE PNF (1) H cannot be set
DC power coming up.
Figure 6-10  Power-Down
Figure 2-1 22-Bit Byte Address Breakdown (2 Words per Block, 256 Sets of Blocks)

Figure 2-2 Fast Data Memory Organization
Figure 2-3 Address Memory Organization
Figure 2-4 PDP-11/70 Cache Simplified Data Path Diagram
Table 2-1
Example Program
(all numbers in octal notation)

<table>
<thead>
<tr>
<th>Address</th>
<th>Machine Code</th>
<th>Index Field</th>
<th>Address Field</th>
<th>Mnemonics</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>001000</td>
<td>013737</td>
<td>200</td>
<td></td>
<td>MOV #5000</td>
<td>This program moves the INC instruction at address 5000 to address 3000, then jumps to address 3000, performs the INC instruction, and HALTS</td>
</tr>
<tr>
<td>001002</td>
<td>005000</td>
<td>201</td>
<td>00000</td>
<td>3000</td>
<td></td>
</tr>
<tr>
<td>001004</td>
<td>003000</td>
<td>202</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001006</td>
<td>000137</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001010</td>
<td>003000</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001012</td>
<td>177776</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>003000</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>003002</td>
<td>001012</td>
<td>200</td>
<td></td>
<td></td>
<td>HALT</td>
</tr>
<tr>
<td>003004</td>
<td>000000</td>
<td>201</td>
<td>0001</td>
<td></td>
<td></td>
</tr>
<tr>
<td>005000</td>
<td>005237</td>
<td>200</td>
<td></td>
<td>INC # #</td>
<td></td>
</tr>
</tbody>
</table>

Table 2-2
Summary of Cache Operations Example

<table>
<thead>
<tr>
<th>Processor</th>
<th>Random Bit (Assumed)</th>
<th>Hit / Miss</th>
<th>Fast Data Memory</th>
<th>Address Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>REF PC</td>
<td>Operation</td>
<td>Block</td>
<td>Contents</td>
<td>Address Memory</td>
</tr>
<tr>
<td>1 1000</td>
<td>Fetch (1000) = 013737</td>
<td>0</td>
<td>Read Miss</td>
<td>0000</td>
</tr>
<tr>
<td>2 1002</td>
<td>Fetch (1002) = 005000</td>
<td>1</td>
<td>Hit on Read Miss</td>
<td>0002</td>
</tr>
<tr>
<td>3 1004</td>
<td>Fetch (5000) = 005237</td>
<td>0</td>
<td>Read Miss on Miss Write Miss</td>
<td></td>
</tr>
<tr>
<td>4 1004</td>
<td>Fetch (1004) = 003000</td>
<td>1</td>
<td>Hit on Read Miss</td>
<td></td>
</tr>
<tr>
<td>5 1006</td>
<td>Write 005237 into 3000</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 1006</td>
<td>Fetch (1006) = 000137</td>
<td>1</td>
<td>Hit on Read Miss</td>
<td></td>
</tr>
<tr>
<td>7 1010</td>
<td>Fetch (1010) = 003000</td>
<td>0</td>
<td>Read Miss on Miss Write Miss</td>
<td></td>
</tr>
<tr>
<td>8 3000</td>
<td>Fetch (3000) = 005237</td>
<td>1</td>
<td>Read Miss on Miss Write Miss</td>
<td></td>
</tr>
<tr>
<td>9 3002</td>
<td>Fetch (3002) = 001012</td>
<td>0</td>
<td>Read Miss on Miss Write Miss</td>
<td></td>
</tr>
<tr>
<td>10 3004</td>
<td>Fetch (001012) = 177776</td>
<td>1</td>
<td>Hit on Read Miss</td>
<td></td>
</tr>
<tr>
<td>11 3004</td>
<td>Write 177777 into 001012</td>
<td>0</td>
<td>Hit on Read Miss</td>
<td></td>
</tr>
<tr>
<td>12 3004</td>
<td>Fetch (3004) = 000000</td>
<td>1</td>
<td>Read Miss on Miss Write Miss</td>
<td></td>
</tr>
</tbody>
</table>

Remarks: Fetch MOV instruction, Fetch source address, Fetch contents at source address, Fetch destination address, MOV contents of source to destination address, Fetch JMP instruction, Fetch destination address, JUMP: Fetch INC instruction, Fetch destination address, Fetch contents of destination address (DATIP), INC and restore (DATO), Fetch and execute HALT instruction.
Figure 4-1 Cache Clock Waveforms

Figure 4-2 Cache Timing Sequence

Figure 4-3 Power-Up Sequence Timing Diagram
Table 4-2
Cache Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Address</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low Error Address</td>
<td>17 777 740</td>
<td>Read only</td>
</tr>
<tr>
<td>High Error Address</td>
<td>17 777 742</td>
<td>Read only</td>
</tr>
<tr>
<td>Memory System Error</td>
<td>17 777 744</td>
<td>Read/selective clear</td>
</tr>
<tr>
<td>Control</td>
<td>17 777 746</td>
<td>Read/write</td>
</tr>
<tr>
<td>Maintenance</td>
<td>17 777 750</td>
<td>Read/write</td>
</tr>
<tr>
<td>Hit/Miss</td>
<td>17 777 752</td>
<td>Read only</td>
</tr>
</tbody>
</table>

Figure 4-8 Low Error Address Register

Figure 4-9 High Error Address Register

Figure 4-10 Memory System Error Register
Figure 4-11 Control Register

Figure 4-12 Maintenance Register

Figure 4-13 Hit/Miss Register
Figure 4-14  Register Logic Block Diagram
CACHE OPERATION ON HIT AND MISS

<table>
<thead>
<tr>
<th>Processor or Unibus Map</th>
<th>READ</th>
<th>WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>HIT</td>
<td>MISS</td>
</tr>
<tr>
<td>MISS</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>WRITE</td>
<td>HIT</td>
<td>MISS</td>
</tr>
<tr>
<td>HIT</td>
<td>Update</td>
<td>No Change</td>
</tr>
<tr>
<td>MISS</td>
<td>Update</td>
<td>Update</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>RH-70 Massbus Controller</th>
<th>READ</th>
<th>WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>HIT</td>
<td>MISS</td>
</tr>
<tr>
<td>HIT</td>
<td>No Change</td>
<td>Update</td>
</tr>
<tr>
<td>MISS</td>
<td>No Change</td>
<td>Update</td>
</tr>
<tr>
<td>WRITE</td>
<td>HIT</td>
<td>MISS</td>
</tr>
<tr>
<td>HIT</td>
<td>Invalidate</td>
<td>Update</td>
</tr>
<tr>
<td>MISS</td>
<td>No Change</td>
<td>Update</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>What Happens In:</th>
<th>CACHE</th>
<th>MAIN MEMORY</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIT</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>MISS</td>
<td>Update</td>
<td>Update</td>
</tr>
<tr>
<td>HIT</td>
<td>Update</td>
<td>Update</td>
</tr>
<tr>
<td>MISS</td>
<td>No Change</td>
<td>Update</td>
</tr>
<tr>
<td>HIT</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>MISS</td>
<td>No Change</td>
<td>No Change</td>
</tr>
<tr>
<td>HIT</td>
<td>Invalidate</td>
<td>Update</td>
</tr>
<tr>
<td>MISS</td>
<td>No Change</td>
<td>Update</td>
</tr>
</tbody>
</table>

TR-1021
Figure 3-8 Processor Read Hit

*The processor time states are intended as a frame of reference only for events which occur in the processor.
Figure 3-12 Unibus Map Read Hit
Figure 3-11 Processor Burst-Bend Cycle

*The processor time states are intended as a frame of reference only for events which occur in the processor.
Figure 3-15  Register Read and Write
Figure 1-2  Construction of PA
Figure 1-3  Relocation
Figure 2-4 MM Relocation Function
PDP-11/70 MEMORY MANAGEMENT FAMILIARIZATION LAB

1. Set up the appropriate PAR's to complete each of the following steps.

   a. Map all virtual page zero addresses to the entire upper 4K section of memory in your processor for Kernel, User and Super modes. (do not map into the device register address range).

   b. Use I Space control at this time.

2. What is the memory size of the processor you are working on _______________ K.


5. Enable the memory management relocation logic for 18 bit mapping.

   a. How was this done?

   __________________________________________

   __________________________________________

6. Load address with zero in the switch register.

   a. Which function or functions has the memory management performed during Load Address? Explain:

   __________________________________________

   __________________________________________

   __________________________________________

   __________________________________________
6. b. Select Kernel I with the address select switch, depress the Examine key.

(1) What address is displayed ______________8
(2) Is this the virtual or physical address?

______________________________

c. Select Program Physical display. What address is displayed? _________________8
Explain: ________________________

______________________________

7. Repeat steps 6, 6b, and 6c using the User I and Super I controls.

a. Notice the mode control lights change on the console (top center) as the new mode is entered and operated on.

8. Repeat step 6. This time load address with the value 10008.

a. Explain what happens this time.

______________________________

______________________________

9. Repeat step 6 again. This time load address with 21,0008.

a. Explain what happens now. ________________________

______________________________

10. Turn the memory management relocation logic off. Look up the address of the TTY or LA30, printer data buffer; what is it? _________________8.

For the PDP-11/70 this address must be prefixed by a 178.

a. If you deposit the ASCII code of a valid character into this address, the character will print one time.

(1) Try this operation.
11. Enable the memory management logic again. The virtual address of the buffer is 177566. Load this address. Select Kernel I and deposit the character.

a. What happens, and why? 

b. Which PAR and PDR must be set up?

(1) PAR = 

(2) PDR = 

c. Do what has to be done to make it work with Memory Management on.

d. There are actually several PAR values which will cause the printer data buffer address to be output from memory management. When using 18 bit mapping an address is defined as a Unibus address if bits are all 1's. If this is true, the bits 21:18 are forced to 1's, even though they might have contained some other value after relocation. In a sense, Unibus addressing may be relocated twice; once to the upper 4K of the 18 bit addressing space, and once to the upper 4K of the 22 bit addressing space. To verify this, load Kernel I PAR7 with the constant required to relocate Kernel I address 177566 to physical address 00777566.

Kernel I PAR7 = 

Deposit the code for an ASCII character in that address. Note that the character is printed. Select PROG PHY, and note the 22 bit address displayed.

22 bit address = 

12. Twenty two bit mapping is enabled by setting bit 4 of memory management register 3. (Refer to the KBL1B Processor Manual, Section IV, Figure 9-6) For memory addresses in the range 0-124K, there is no difference between 18 bit mapping and 22 bit mapping. Valid addresses above 124K were relocated to the 4K device addresses under 18 bit mapping. Under 22 bit mapping, addresses up to 1920K are treated as memory addresses. The 128K addresses with address bits 21:18 equal to all 1's are treated as Unibus addresses. The upper 4K
of these are the device addresses, the remaining 124K address the Unibus Map. After relocation; the address is determined to be a Unibus address, the leading 1's are stripped off and bits 17:00 are used as the 18 bit Unibus address.

a. Enable 22 bit mapping.

b. Repeat step 6 again. Is the operation different from the previous execution of step 6? 

---

c. Repeat step 11. Is the printer data buffer addressed? The value loaded into PAR7 in step 1101 causes the memory management output to be a non-Unibus address. Change it so that the buffer register will be addressed.

13. To use D-Space memory management register three must be set up to specify the mode.


b. Explain what happens and why? 

---

c. Correct the problem, and see that Kernel D-Space works.

14. Analyze the following simple program. Deposit it into the specified location. Do what is needed to make it work with the memory management enabled.

```
2000008  MOV#1,@#777572
2  000001
4  177572
6  BR
```
ANSWERS TO QUESTIONS

<table>
<thead>
<tr>
<th>STEP NUMBER</th>
<th>ANSWERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>Core Range PAR's</td>
</tr>
<tr>
<td></td>
<td>32K- 1600g</td>
</tr>
<tr>
<td></td>
<td>40K- 2200g</td>
</tr>
<tr>
<td></td>
<td>48K- 2600g</td>
</tr>
<tr>
<td></td>
<td>56K- 3200g</td>
</tr>
<tr>
<td></td>
<td>64K 3600g</td>
</tr>
<tr>
<td>4</td>
<td>PDR's = 0774068</td>
</tr>
<tr>
<td>5</td>
<td>Deposit a one into SR0 bit 0</td>
</tr>
<tr>
<td>6a</td>
<td>None; KT11-C only deals with address from the BAMX.</td>
</tr>
<tr>
<td>6b(1)</td>
<td>Zero</td>
</tr>
<tr>
<td>6b(2)</td>
<td>Virtual PAR+O: This is the physical address after the PAR0 and the virtual addresses were added.</td>
</tr>
<tr>
<td>6c</td>
<td>The virtual address is 1000. This address is mapped to the specified physical address range.</td>
</tr>
<tr>
<td>8a</td>
<td>Memory Management abort. The virtual address is in page two. Page two hardware is not set up.</td>
</tr>
<tr>
<td>9a</td>
<td>7775668</td>
</tr>
<tr>
<td>10</td>
<td>Memory Management abort. Virtual page 7 is referenced and the hardware is not set up. Kernel PAR7 and PDR7.</td>
</tr>
<tr>
<td></td>
<td>PAR = 177600g.</td>
</tr>
<tr>
<td></td>
<td>PDR = 0774068.</td>
</tr>
<tr>
<td></td>
<td>17:13</td>
</tr>
<tr>
<td></td>
<td>Kernel I PAR7 = 007600g 22 bit address = 17777566</td>
</tr>
<tr>
<td>12b</td>
<td>No</td>
</tr>
<tr>
<td>12c</td>
<td>No</td>
</tr>
<tr>
<td>13</td>
<td>Memory Management abort. The Kernel D PAR and PDR are not set up correctly.</td>
</tr>
</tbody>
</table>
Figure 8-1 Traps and Aborts
Figure 8-2  Trap Timing
Figure 3-1  Addressing of PAR/PDR
Figure 4-10  Generation of Physical Address
Figure 9-1 MMR0
Figure 9-2  Clocking of MMR0
Figure 9-3  MMR0 Write Timing
Figure 9-4  MMR1

Figure 9-5  MMR2

Figure 9-6  MMR3
Figure 1-1  Construction of the PA
Figure 2-1  Unibus Map Flowchart
Figure 2-2 Unibus Map Block Diagram
Figure 2-3  Unibus Map Interface
Figure 2-4  Cache/Unibus Transactions
Figure 3-1 Addressing of UB Map Register
Figure 3-2 UB Map Register Read/Write
HYSTERESIS LOOP FOR CORE

INHIBIT OR READ HALF SELECT

FLUX STORED OR SWITCHED

UNDISTURBED

DISTURBED

WRITE FULL SELECT

DRIVE CURRENT

I WRITE

FLUX CHANGE FOR I AT READ TIME

READ FULL SELECT

"O" DISTURBED

"O" UNDISTURBED

FLUX CHANGE AT READ TIME FOR A "O". NOTE NO SWITCHING TAKES PLACE.

HALF SELECT WRITE

"O" OUTPUT COMES DURING I RISE TIME AND IS A FUNCTION OF IT AND CURRENT AMPLITUDE.

"O" OUTPUT \( \propto \frac{I}{T} \) OR \( \propto \frac{4I}{3T} \)

\( \approx 40 \text{ MV} \)

\( \approx 20 \text{ MV} \)

"I" OUTPUT SWITCHES AT THE CORE TIME CONSTANT AND IS PRIMARILY DEPENDENT ON CURRENT AMPLITUDE. IT WILL SWITCH FASTER AND GROW AS RISE TIME IS DECREASED.

DOTTED LINES SHOW HOW OUTPUTS WOULD BEHAVE WITH DIFFERENT CURRENTS

Figure 4-2 Hysteresis Loop for Core
Figure 4-3  Three-Wire, 3D Memory – Four Mats of a 16-Word by 4-Bit Memory
MJ11 MEMORY OPTIONS

MJ11-AE: 32K words

MJ11-AA: Memory Box with Controller and Transceiver, 32K words, 110 V.
        AB: Memory Box with Controller and Transceiver, 32K words, 220 V.

MJ11-AG: Memory Box with Controller and Transceiver, 128K words, 110 V.
        AH: Memory Box with Controller and Transceiver, 128K words, 220 V.

MJ11-AC: Memory Cabinet and one Memory Box with Controller and Transceiver, 128K words, 110 V.
        AD: Memory Cabinet and one Memory Box with Controller and Transceiver, 128K words, 220 V.

Maintenance Spares (not for expansion purposes)

MJ11-AM: 16K words

TR-0916
NOTES:
BIT 9 of DATA BYTES 3 and 1 are implemented on the MAIN MEMORY BUS but are not used in the PDP-11/70.
BIT 8 of each DATA BYTE is the byte parity bit in PDP-11/70 applications.

Figure 1-1  Data Word Organization
Figure 1-9  MJ11 Simplified Block Diagram
TOP OF MODULE

- D10 MISMATCH ERROR
- D9 CONFIGURATION ERROR
- D8 PARITY ERROR
- D5 BUSY

MBI48 MEMORY CONTROL AND
TIMING MODULE EDGE VIEW
FROM FRONT OF MEMORY FRAME.

Figure 3-3 Location of Memory Controller Status LED Indicators
Figure 2-2 Write Operation – Main Memory Bus Protocol

Figure 2-3 Read Operation – Main Memory Bus Protocol
Figure 3-1 Memory Controller Operation -- Simplified Flowchart
Figure 3-5 Buffered Outputs of Read Timing Delay Line
Figure 3-6 Write Operation Timing Control Signals
Figure 3-7  Read Operation Timing Control Signals
Figure 4-4  Operation of Drivers and Switches
NOTE:
A matrix this size would be used in a system having 16 Y drive lines. The MJ11 16K stack contains 128 Y drive lines on an 8 x 16 matrix.

SWITCHES

33R
33W
32R
32W
31R
31W
23R
23W
22R
22W
13R
13W
12R
12W
O3R
O3W
O2R
O2W
O1R
O1W
OR
OW

DRIVERS

YNRD3
YPWD3
YNRD2
YPWD2
YNRD1
YPWD1
YNRDO
YPWD0

NUMBER OF CORES DEPENDS ON NUMBER OF WORDS AND WORD LENGTH

Y-AXIS 4x4 SECTION (16 LINES)

Figure 4-5  Simplified Y Line Selection Stack Diode Matrix
Figure 4-6 Typical Y Line Read/Write Switches and Drivers
Figure 4-7 Example of Address Decoding (Non-interleaved)
Figure 4-8  Interconnection of Internal Bus, Data Register, Sense Amplifier and Inhibit Driver
Figure 4-9 Sense Operation Timing Diagram
Figure 4-10 Bias Current Supply and Read X Current Generator
NOTE:
Refer to logic schematic STKA

Figure 4-13 Stack Charge Circuits