VA 38
20μs CHARACTER GENERATOR
INSTRUCTION MANUAL
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VA38 20 μs CHARACTER GENERATOR
VA38 20-μs Character Generator
CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The VA38 20 μs Character Generator (frontispiece) is an option to the Type 338 or the Type 339 Programmed Buffered Display manufactured by Digital Equipment Corporation of Maynard, Massachusetts. The VA38-338 and VA39-339 systems evolve when the option is used with the 338 and 339 displays, respectively. The contents of this manual pertain to both cases. The option is used to generate ASCII (American Standard Code for Information Interchange) character information for the display. This document and the documents referenced herein provide the information necessary for installation, operation and maintenance of the option. The level of discussion assumes that the user is familiar with the display.

1.2 SPECIFICATIONS

The following specifications pertain to the VA38 20 μs Character Generator.

1.2.1 Performance

Character format is fixed by the nature of the read-only memory and cannot be changed by the user. The character-generation-speed of 20 μs per character allows the display of 1600 flicker-free ASCII characters.

1.2.2 Physical

The VA38 consists of a DEC standard 1943 Mounting Panel of FLIP-CHIP modules and a read-only memory. Both units mount in preassigned locations in the display as shown in Figure 2-1.

1.2.3 Power Requirements

The VA38 obtains all necessary operating power from the display with which it is used.

1.3 RELATED DOCUMENTATION

The documents listed in Table 1-1 contain information which supplements the information provided in this manual.

1.4 ENGINEERING DRAWING REFERENCES

VA38 control logic engineering drawings will be referenced by an abbreviated drawing number code. As an example, drawing D-BS-VA38-0-1, sheet 1, will be referenced as [VA-1(1)]. A complete VA38 control logic engineering drawing list is contained in Chapter 7 of this manual.

Table 1-1
Reference Documents

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<tr>
<th>Title</th>
<th>Document Number</th>
<th>Description</th>
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<td>DIGITAL Logic Handbook</td>
<td>C-105</td>
<td>Specifications and descriptions of most FLIP-CHIP modules used in the VA38</td>
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<tr>
<td>338 Programmed Buffered Display Instruction Manual</td>
<td>DEC-08-H6AA-D</td>
<td>Operation and programming information for the Type 338 Programmed Buffered</td>
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<td>Display</td>
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<td>Addendum to the 338 display manual, describing modifications of the 338 to</td>
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<td>the 339 display</td>
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<td>Operation and maintenance information for the read-only memory.</td>
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<td>Instruction Manual</td>
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1-1
CHAPTER 2
INSTALLATION

The VA38 installation should be attempted only by a DEC Field Engineer. Before proceeding with the following installation procedures, display operation should be checked by all display diagnostic programs.

VA38 installation consists of the procedures described in the following paragraphs, and requires the following equipment.

- Electric drill*
- 1/4 in. bit*
- 10-32 Rivnut gun
- Wire wrap gun
- Standard field service tool kit
- 10-32 x 3/4 in. machine screws (6)*
- 10-32 external tooth lockwashers (6)*
- 10-32 Rivnuts (6)*
- B117 NAND/NOR Gate module (1)
- 4698 Intensity Amplifier module (1)
- Power jumpers
- Wire wrap wire
- R/C Terminator (0.01 μF capacitor and 100Ω resistor)
- MAINDEC-08-D8MA tape and write-up
- Copy of ECO 338-00003
- Copy of ECO 338-00004
- Set of 338 engineering drawings containing ECO 338-00004

2.1 MECHANICAL

The VA38 control logic and read-only memory mount in the relative display locations shown in Figure 2-1. The read-only memory is attached to the vertical supporting members of display bay 1, below the table assembly bracket. When properly installed, the memory proper should be near the back of bay 1 with the plated connector pins facing the front of the display.

Displays with serial numbers of 45 and greater have mounting holes for the VA38 read-only memory. The supplied screws and washers are used to secure the memory to the display. Displays with serial numbers less than 45 do not have these holes. The memory must be positioned against the vertical supporting members of bay 1, the hole locations marked and drilled out with a 1/4 inch bit and the Rivnuts installed. The memory is then secured to the vertical supporting members with the supplied hardware.

The VA38 control logic modules are contained by a DEC Type 1943 Mounting Panel. Three mounting panel covers are located directly below the 338 Display CRT. To install the control logic, remove the middle panel cover and replace with the control logic. Secure the 1943 panel with the four screws that previously held the panel cover.

Figure 2-1 VA38-338 Installation Diagram

*Required only for displays with serial numbers less than 45.
2.2 ELECTRICAL

Electrical installation of the VA38 involves connecting power wiring between the display and the control logic, and interface cables between the control logic, the read-only memory and the display.

The VA38 obtains operating and marginal power from the logic mounting panel above the display CRT. Power is supplied by jumper wires connected between the control logic and the mounting panel.

Four cables interface the VA38 control logic, the read-only memory and the 338 display. Figure 2-2 and Table 2-1 provide all necessary interface cabling information. It should be noted that the plated connector pins of the memory are arranged in two groups, P1 and P2, and are designated as such on the memory. When the memory is properly installed, P2 will be above P1. The 80-pin cable connectors can attach to the plated pins correctly or upside down. When correctly attached the connector end stamped "50-90" will face upward.

![VA38 Cables](image)

**Figure 2-2 VA38 Cables**

**Table 2-1**
VA38-338 Cabling Information

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<th>No.</th>
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<th>Location</th>
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2.3 DISPLAY MODIFICATIONS

Incorporation of a VA38 20 μs Character Generator into a 338 Programmed Buffered Display requires the modifications described in the following paragraphs.

a. The following Engineering Change Orders (ECO) must be executed. ECO 338-00004 which pertains only to the display should be incorporated first and checked by all 338 diagnostic programs. When installation proves correct, ECO 338-00003, which pertains only to the VA38/39, should be executed. The wire list for ECO 338-00004 is provided in Table 2-2; ECO 338-00003 is provided in Table 2-3. These wire lists should be used.

b. Two modules are also required for VA38 implementation. A B117 NAND/NOR Gate must be inserted in display location R26, and the 4688 Intensity Amplifier found in display location Z02 must be replaced by the supplied high-speed 4698 Intensity Amplifier which is described in Section 6.2.

Following installation of the 4698 module, the high voltage interlock switches, located at the back of both display bays, should be placed in the OFF position until the intensity time delay is set as described below.

c. Two display delays require changes: The Break Request delay, location S07V, must be increased to 500 ns; the Intensify Time delay, location M25F must be decreased from 300 ns to 100 ns.

Table 2-2
Wire List for ECO 338-00004

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<td>N10D</td>
<td>L30F</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>L30F</td>
<td>L07T</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>R25V</td>
<td>R25U</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Signal Name</td>
<td>From Pin</td>
<td>To Pin</td>
<td>Components</td>
<td>Add</td>
<td>Del.</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
<td>---------</td>
<td>------------</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td>R25U</td>
<td>L09F</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>L09F</td>
<td>L09E</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>R13U</td>
<td>L09D</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>S14S</td>
<td>S15F</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>S03P</td>
<td>S04M</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>P25D</td>
<td>K26U</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>N07T</td>
<td>N10H</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>N09L</td>
<td>N29K</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>L25M</td>
<td>L25S</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>L26U</td>
<td>L26V</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>L30P</td>
<td>GND</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>F05E</td>
<td>F14U</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>F14U</td>
<td>F14V</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>H18H</td>
<td>H24U</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>H24U</td>
<td>H24V</td>
<td></td>
<td></td>
<td>x</td>
<td></td>
</tr>
</tbody>
</table>

Add B117 Module in Location R26 in the 338 Logic.
CHAPTER 3
OPERATION AND PROGRAMMING

The VA38 is completely under the control of the display with which it is used. No controls or indicators are found on the VA38.

3.1 PROGRAMMING

The character generator is accessed by a mode instruction containing an enter mode 7, enter data state command 1171. Mode 7 is reserved for the character generator. The words read from PDP-8 memory are decoded as two characters per word. Special character ESC (escape), described in Section 4.11, allows the display to leave the data state and enter the control state. The next word in the display file is interpreted as a control word.

The sample program below illustrates the program simplicity of the VA38. Figure 3-1 illustrates the five character sets (320 characters) produced by such a program.

```
0200 7200 BEGIN, CLA /PROGRAM START
0201 1215 TAD PTR
0202 6135 SPDP /SET THE PUSH DOWN POINTER
0203 7200 CLA
0204 1216 TAD IC
0205 6145 SIC /SET THE INITIAL CONDITIONS
0206 7200 CLA
0207 1217 TAD BF
0210 6155 LBF /LOAD THE BREAK FIELD
0211 7200 CLA
0212 1220 TAD SA
0213 6165 INIT /INITIALIZE THE DISPLAY
0214 5214 JMP
0215 4000 PTR, 4000
0216 0004 IC, 0004
0217 4000 BF, 4000
0220 0221 SA, FILE
0221 0517 FILE, SC1 INT7 /PARAMETER WORD
0222 1107 POINT EDS /POINT WORD
0223 1700 1700
0224 4000 4000
0225 2010 PJMP /JUMP TO SUBROUTINE
0226 0241 CHAR /THAT CONTAINS THE
0227 2010 PJMP /CHARACTER SET
0230 0241 CHAR
0231 2010 PJMP
0232 0241 CHAR
0233 2010 PJMP
0234 0241 CHAR
0235 2010 PJMP
0236 0241 CHAR
0237 2000 DJMP /JUMP TO START OF
0240 0221 FILE /THE DISPLAY FILE
```

/FIVE CHARACTER SETS

3-1
CHAR, CHARM EDS /MODE COMMAND TO
/ENTER CHARACTER
/GENERATOR
/TWO CHARACTER CODES PER WORD

SPDP=6135
SIC=6145
LBF=6155
INIT=6165
SC1=0500
INT7=0017
POINT=1106
EDS=1001
PJMP=2010
DJMP=2000
CHARM=1170
POP=3000

BEGIN 0200
BF 0217
CHAR 0241
CHARM 1170
DJMP 2000
EDS 1001
FILE 0221
Figure 3-1  Sample Program Characters
CHAPTER 4
PRINCIPLES OF OPERATION

4.1 GENERAL

The VA38 20 μs Character Generator consists of control logic and a read-only memory. Figure 4-1 illustrates the relationship between these units and the 338 Programmed Buffered Display with which it is used.

Basically, characters are generated from a series of 6-bit character words stored in the read-only memory (ROM). To initiate generation of a character, the ASCII code for the character desired is applied to the VA38 control logic. It is combined with an internally produced 4-bit word to provide the 10-bit address required by the ROM. Under control of the 338 display, the character generator control logic produces a START CYCLE pulse to read a character word out of the rope memory and into the ROM output data register. The word is then jam transferred into the VA38 control logic where it is decoded. While this character word is being incremented in preparation for the next word of the character, the current word provides character information for the display. After this word has been completely decoded, an XFER INIT pulse is produced again and the 6-bit word at the incremented address is jam transferred into the control logic. The address is again incremented during this time. This chain continues until the end of the character is sensed.

4.2 ASCII CHARACTER SET

Figure 4-2, ASCII Character Set, provides the character code, ROM address and character words for all ASCII characters capable of being generated by the VA38. Before proceeding, it should be noted that the ROM requires a 10-bit address consisting of 6 high-order bits from the ASCII character code and 4 low-order bits from the internal VA38 MCTR (memory counter). The high-order portion of the address remains fixed throughout a given character while the MCTR is incremented and the low-order portion changes.

The character "D" will serve as an example in explaining the use of the table. D has the ASCII code of 04. The code comprises 6 bits of the 10-bit address. The remaining 4 bits are obtained from the content of the MCTR which is cleared at the beginning of a character.
Thus the initial 10-bit ROM address will be

```
000 100 0000
```

ASCII MCTR
CODE

Converted to octal, the address becomes 1008. Character word 728 is obtained from this address. The word is jam transferred into the VA38 CH REGISTER, from which it is decoded, as explained in Section 4.6, CH Register, and Section 4.7 Character Information Utilization.

While the current word is being decoded, the MCTR is incremented and the address becomes 101. This cycle continues until the end of the character is sensed via 06. The MCTR is then cleared.

A maximum of 64 ASCII characters can be produced by the VA38. Of these, three are termed "special", they are CR (carriage return), LF (line feed) and ESC (escape) and they replace $, %, and &, respectively.

The usual characters will be termed common and will be explained as a group since the operations they initiate are basically the same. The special characters will be explained separately.

4.3 COMMON CHARACTER GENERATION

Section 4.4 and 4.5, Common Character Signal Flow and Character End Signal Flow, respectively, illustrate the timing chain for all common characters. Section 4.4 illustrates the operations which serve to condition the VA38 control logic, address the read-only memory and decode the character words from memory. Reference should also be made to Section 4.6 and 4.7 as they contain information regarding specific character word decoding and resultant functions.

Section 4.5 illustrates the operations that result when the completion of the character is sensed.

<table>
<thead>
<tr>
<th>Code</th>
<th>Character</th>
<th>Code</th>
<th>Character</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>@</td>
<td>40</td>
<td>SPC</td>
</tr>
<tr>
<td>01</td>
<td>A</td>
<td>41</td>
<td>1</td>
</tr>
<tr>
<td>02</td>
<td>B</td>
<td>42</td>
<td>#</td>
</tr>
<tr>
<td>03</td>
<td>C</td>
<td>43</td>
<td>$</td>
</tr>
<tr>
<td>04</td>
<td>D</td>
<td>44</td>
<td>CR</td>
</tr>
<tr>
<td>05</td>
<td>E</td>
<td>45</td>
<td>%</td>
</tr>
<tr>
<td>06</td>
<td>F</td>
<td>46</td>
<td>LF</td>
</tr>
<tr>
<td>07</td>
<td>G</td>
<td>47</td>
<td>&amp;</td>
</tr>
<tr>
<td>08</td>
<td>H</td>
<td>50</td>
<td>ESC</td>
</tr>
<tr>
<td>09</td>
<td>I</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>J</td>
<td>52</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>K</td>
<td>53</td>
<td>+</td>
</tr>
<tr>
<td>12</td>
<td>L</td>
<td>54</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>M</td>
<td>55</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>N</td>
<td>56</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>O</td>
<td>57</td>
<td>/</td>
</tr>
<tr>
<td>16</td>
<td>P</td>
<td>60</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>Q</td>
<td>61</td>
<td>1</td>
</tr>
<tr>
<td>18</td>
<td>R</td>
<td>62</td>
<td>2</td>
</tr>
<tr>
<td>19</td>
<td>S</td>
<td>63</td>
<td>3</td>
</tr>
<tr>
<td>20</td>
<td>T</td>
<td>64</td>
<td>4</td>
</tr>
<tr>
<td>21</td>
<td>U</td>
<td>65</td>
<td>5</td>
</tr>
<tr>
<td>22</td>
<td>V</td>
<td>66</td>
<td>6</td>
</tr>
<tr>
<td>23</td>
<td>W</td>
<td>67</td>
<td>7</td>
</tr>
<tr>
<td>24</td>
<td>X</td>
<td>70</td>
<td>8</td>
</tr>
<tr>
<td>25</td>
<td>Y</td>
<td>71</td>
<td>9</td>
</tr>
<tr>
<td>26</td>
<td>Z</td>
<td>72</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>[</td>
<td>73</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>\</td>
<td>74</td>
<td>&lt;</td>
</tr>
<tr>
<td>29</td>
<td>]</td>
<td>75</td>
<td>=</td>
</tr>
<tr>
<td>30</td>
<td>?</td>
<td>76</td>
<td>&gt;</td>
</tr>
<tr>
<td>31</td>
<td></td>
<td>77</td>
<td>?</td>
</tr>
</tbody>
</table>

Special characters include control words which may be decoded to implement the functions:

- CR
- LF
- ESC

(The LF word forces a reference to R/O MEM LOC 0014. This section contains coding for execution of LF.)

Figure 4-2 VA38 ASCII Character Set
Figure 4-2 VA38 ASCII Character Set (Cont)
Prior to character generation, GENERAL CLR conditions the VA38 control logic. The pulse is the OR condition of CHARM or B PWR CLR or IOT 164. CHARM is produced when the display enters the character mode. B PWR CLR is produced when power is first applied to the system or when the computer START key is actuated. IOT 164, Resume After Stop Code, is usually executed following the raising of an internal display stop flag.

Following logic conditioning operations, CHARM will be produced when the display enters the character mode. The level conditions an internal VA38 DCD gate which is strobed by DY LEFT DATA AVAIL. The result is CODE AVAIL which initiates character generation.

CODE AVAIL is gated with CHAR DONE (1) to produce START CYCLE. This pulse conditions the read-only memory (ROM) sense amplifiers and output data register and also allows the 10-bit memory address access to the ROM address decoding circuitry.

START CYCLE, delayed 400 ns, is READ DELAY. The delay allows sufficient time to read the 6-bit character word of the current ROM address out of the rope memory and into the output data register.

Delay termination results in a -3V~0V transition which strobes a DCD gate conditioned by ENABLE which is the result of CHAR DONE (1). The result, XFER INIT, clears CHAR DONE and increments the MCTR.

XFER INIT triggers a 100 ns delay to produce BUFFER STROBE (100 ns, -3V level) and BUFFER DELAY at the termination of the delay. BUFFER DELAY allows the current 6-bit character word (bit 1 through bit 6), held in the ROM output data register, to be jam transferred into the VA38 CH REGISTER.

The contents of the CH REGISTER are applied to a binary to octal decoder where a SPECIAL of a SPECIAL condition is determined. All common character words will produce a SPECIAL condition because CH0 ^ CH1 ^ CH2^0. The decoder will be disabled and no LCn levels will be produced. BUFFER DELAY will not produce any Cn pulses.

NOTE: n is 0 through 7

BUFFER DELAY and SPECIAL produce XFER DELAY DONE which, in turn, produces a second START CYCLE pulse. This enables the 6-bit character word of the incremented ROM address to be read out of the rope memory and into the output data register. ENABLE is not present because of CHAR DONE (0), therefore no further action is taken on this character word.
RO WORD AVAIL (0) and \( \overline{\text{FLAG}} \) are gated to produce \( \text{STEP TIME} \). \( \text{FLAG} \) is the result of \( \text{LP} (0) \land \text{OVFLO} \land \text{EXT STOP} (0) \) from the display.

If CH1 and CH2/0, producing COUNT ZERO, \( \text{STEP TIME} \) will generate \( \text{STEP} \) to complement CH2. \( \text{STEP TIME} \) also sets the FLASH NEXT flip-flop and triggers a 400 ns delay to produce \( \text{STEP TIME DELAY} \) (400 ns, 0V level) which complements CH1. Thus, the number-of-moves counter consisting of CH1 and CH2 is decremented by one.

\( \text{STEP TIME DELAY} \) clears the \( \text{STEP NEXT flip-flop} \). \( \text{STEP TIME PULSE} \) occurs 400 ns after \( \text{STEP TIME} \) and is gated with \( \text{FLAG} \) to trigger a second 400 ns delay.

If COUNT ZERO is true, indicating that the current character word is completed, XFER INIT will be produced via COUNT ZERO \( \land \) CHAR DONE (0) \( \land \) STEP TIME DONE D. If COUNT ZERO is true, indicating that the current word has not been completed, the \( \text{STEP NEXT flip-flop} \) will be set and the word will be cycled through until COUNT ZERO is true. Assuming the end of the character is not sensed, a new 6-bit character word will be jam transferred into the CH REGISTER.

\( \text{STEP TIME DONE-P} \) is produced with \( \text{STEP TIME DONE} \). This pulse triggers a 100 ns intensity delay. If CH0, the intensity bit, is in the 1 state, INT TIME will be produced for 100 ns. This -3V level is utilized by the display intensity circuitry. Termination of the delay results in the production of FLASH TIME DONE. FLASH TIME DONE and \( \text{STEP NEXT} (1) \) produce \( \text{STEP TIME} \) which, in turn, is gated with COUNT ZERO to produce \( \text{STEP} \).

The 338 display is provided with three types of character information for character display. Namely, intensity information, specified by INT TIME, number of moves, specified by the number of times a given character word is cycled through and direction of moves, described in Section 4.7.
4.5 END CHARACTER SIGNAL FLOW

Referring to Figure 4-2, ASCII Character Set, it is observed that all characters terminate with character word 06. When this word is sensed, logic operations result which signal the display that the current character has been fully decoded.

Completion of the character word preceding 06 produces an XFER INIT pulse to produce BUFFER STROBE. BUFFER STROBE jam transfers 06 from the ROM output data register into the VA38 CH REGISTER.

CH0, CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC6 to be produced from the remaining CH bits. LC6 is gated with BUFFER DELAY (XFER INIT delayed 100 ns) to produce C6. C6, in turn, sets the CHAR DONE flip-flop to produce BYTE DONE. This signals the display that another ASCII character code may be sent to the VA38 control logic.

4.6 CH REGISTER

The VA38 CH REGISTER is essentially a storage register from which character words are decoded. The register format is as follows:

<table>
<thead>
<tr>
<th>CH 0</th>
<th>CH 1</th>
<th>CH 2</th>
<th>CH 3</th>
<th>CH 4</th>
<th>CH 5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intensity</td>
<td>Number of Moves</td>
<td>Direction</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CH0 and VA38 control signals are used to generate INT TIME which is used by the display to intensify a point.

A maximum of three moves can be specified by a single character word. The initial content of CH1 and CH2 dictates the number of times the current word will be cycled through.

Any of eight directions can be specified via the content of CH3 - CH5. The content/direction relationship is as shown:

```
0 1 2 3
5 4 6 7
```
4.7 CHARACTER INFORMATION UTILIZATION

As previously stated, INT TIME is sent to the display to intensify the dot. Number-of-moves information is sent to the display via CX (COUNT X) and CY (COUNT Y) pulses. These pulses count the X- and Y-position registers. Direction information is applied to the display via CHARM LEFT and CHARM DOWN. Combinations of CHARM LEFT, CHARM DOWN, CX and CY are illustrated in Table 4-1.

4.8 SPECIAL CHARACTER GENERATION

As previously stated, the VA38 character repertoire contains a number of SPECIAL characters. Namely:

<table>
<thead>
<tr>
<th>ASCII Character</th>
<th>SPECIAL Character</th>
</tr>
</thead>
<tbody>
<tr>
<td>$</td>
<td>CR (Carriage Return)</td>
</tr>
<tr>
<td>%</td>
<td>LF (Line Feed)</td>
</tr>
<tr>
<td>&amp;</td>
<td>ESC (Escape)</td>
</tr>
</tbody>
</table>

4.9 CR (CARRIAGE RETURN) SIGNAL FLOW

CR is a SPECIAL character which move the dot and further information to be displayed to the left edge of the display CRT.

When CR (octal code 44) is executed, logic operations similar to those of common character generation address the ROM and jam transfer the first character word into the CH REGISTER. CH0 and CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC3 to be produced from the remaining CH bits. LC3 is gated with BUFFER DELAY (XFER INIT delay 100 ns) to produce C3.

C3 produces CLR X which clears the display X-Position Register (refer to drawing BS-D-338-0-6, sheet 1).

C3 and CHARM trigger 35 μs CR DELAY necessary for worst case (right edge to left edge) dot return. The termination of the delay produces CR DONE which, in turn, sets the CHAR DONE flip-flop to produce BYTE DONE.

Table 4-1
Direction Information

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;</td>
<td>CR DOWN (0V)</td>
</tr>
<tr>
<td>&lt;</td>
<td>CR DOWN (-3V)</td>
</tr>
<tr>
<td>&lt;</td>
<td>CR LEFT (0V)</td>
</tr>
<tr>
<td>&lt;</td>
<td>CR LEFT (03V)</td>
</tr>
<tr>
<td>&lt;</td>
<td>CR, CY LEFT (0V) and DOWN (0V)</td>
</tr>
<tr>
<td>&lt;</td>
<td>CR, CY LEFT (-3V) and DOWN (-3V)</td>
</tr>
<tr>
<td>&lt;</td>
<td>CR, CY LEFT (-3V) and DOWN (0V)</td>
</tr>
<tr>
<td>&lt;</td>
<td>CR, CY LEFT (0V) and DOWN (-3V)</td>
</tr>
</tbody>
</table>

Diagram of signal flow and logic operations.
4.10 LF (LINE FEED) SIGNAL FLOW

LF is a SPECIAL character which moves the dot and further information to be displayed down one line on the display CRT.

When LF (octal code 45) is executed, logic operations similar to those of common character generation address the ROM and jam transfer the first character word into the CH REGISTER. CH0 and CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC4 to be produced from the remaining CH bits. LC4 is gated with BUFFER DELAY (XFER INIT delayed 100 ns) to produce C4.

C4 clears the MCTR, sets the SPECIAL LF flip-flop and triggers a 0.5 μs delay.

By clearing the MCTR and then setting MCTR1 and MCTR2, the ROM address 0014 is specified.

Referring to Figure 4–2, ASCII Character Set, common character words can be seen at the specified address.

The termination of the 0.5 μs delay produces START CYCLE. Operations continue as with common character generation with the exception that CHAR DONE (0) is true. ENABLE, necessary for the continuation of the timing chain, is now produced by C4 rather than by CHAR DONE (1).

4.11 ESC (ESCAPE) SIGNAL FLOW

ESC is a SPECIAL character which allows the display to leave character mode.

When ESC (octal code 46) is executed, logic operations similar to those of common character generation address the ROM and jam transfer the first character word into the CH REGISTER. CH0 and CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC5 to be produced from the remaining CH bits. LC5 is gated with BUFFER DELAY (XFER INIT delayed 100 ns) to produce C5.

C5 and CHARM produce OP DONE to clear the MCTR. C5 also sets the CHAR DONE flip-flop to produce BYTE DONE.

OP DONE becomes OP DONE D in the display (refer to drawing B5–338–0–20) and is gated with LC5 to produce SET CYC 1.
CHAPTER 5
MAINTENANCE

Preventive and corrective maintenance of the VA38 is simplified by the use of diagnostic program techniques. The following procedure can be used in both instances.

a. Connect the VA38 - 338 cables according to the information provided in Figure 3-2 and Table 3-1 in Section 3 of this manual.

b. Check for +5V at pin B02J.

c. Set the reset break request delay to 500 ns. Set the INTENSIFY TIME delay M25 to 100 ns. These are all found in the 338.

d. Load MAINDEC-08-D8MA. Run Section 00.

e. Temporarily ground pin A25V (VA38). The graphic timing chain will be inhibited to allow the checking of single read only memory bytes.

f. Check the following pulses: CODE AVAIL, START CYCLE, READ DELAY, XFER INIT, BUFFER STROBE, and BUFFER DELAY. Sync at pin B31M.

g. Check memory inputs at the following pins: A31-H, M, F, E, P, D, N, T, R and S. The following pattern should be found:

<table>
<thead>
<tr>
<th>0V</th>
<th>5V</th>
<th>5V</th>
<th>0V</th>
<th>0V</th>
<th>5V</th>
<th>5V</th>
<th>5V</th>
<th>5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>6</td>
<td>0V</td>
<td>1</td>
<td>5V</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

h. Check the START CYCLE pulse at pin A31J. Sync at pin B11F.

i. Check for the pattern (46) described in Step g at CH0 through CH5. Sync at pin B12F.

j. Check CH5 for proper decoding. NOTE: With SW0 = 0 and SW1 = 1. If the character generator is operating properly, the Y REGISTER and the X REGISTER of the 338 should contain 1000 and 1070, respectively. A visual check can be made via the indicator lights.

k. Run Section 01 of MAINDEC-08-D8MA.

l. Remove the temporary ground at pin A25V. Toggle 56g into the last six bits of the PDP-8 SWITCH REGISTER.

m. Check for proper number of steps and direction decoding.

n. Check all characters. Place emphasis on the SPECIAL characters 44 and 45, carriage return and line feed, respectively.

o. Run Sections 10 and 11 of MAINDEC-08-D8MA.

p. Rerun Section 10 of MAINDEC-08-D8MA. Determine the total time to generate one complete character set by measuring the time pin B31M remains continuously at ground. Divide this time by 68. The resulting time must not exceed 21.5 μs

q. Rerun Section 01 of MAINDEC-08-D8MA. Measure the time between pulses at pin B26F. This is STEP TIME and must not exceed 1.1 μs.
6.1 MODULES

Table 6-1 contains DEC module quantity, description and type information.

Table 6-1
Module List

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Description</th>
<th>Type</th>
<th>Page</th>
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<td>R001</td>
<td>7-2</td>
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<td>R111</td>
<td>7-3</td>
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<td>R602</td>
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6.2 SPECIAL MODULE

6.2.1 Type 4698 Intensity Amplifier

The VA38 option contains a DEC Type 4698 Intensity Amplifier module which is a high speed replacement of the 4688 Intensity Amplifier used in 338 and 339 display systems. Use of the 4698 permits about 20% faster incremental plotting speed and individual adjustment of each of the eight intensity levels. The 4698 is required in 338/339 systems having a VA38/VA39 and is optional in other 338/339 systems.

The 4698 allows a decrease in the intensity time from 300 ns to 100 ns allowing a total incremental point to point decrease from 1.1 μs to .9 μs. This decrease allows about 20% more information to be displayed. The 4698 also features individual adjustment of the light output on each of the eight programmable intensity levels. An advantage of this feature for example would be to have intensity level 7 (brightest), very bright for highly responsive light pen operation, but a smooth gray scale from intensity 6 to intensity 0.

6.2.2 Circuit Description

Transistors T2, T3, T4 serve to convert the single rail inputs from the intensity register to double rail signals needed to drive the binary to octal converter. Transistor T1 is a simple inverter driving a "totem-pole" type output stage comprised of transistors T13 and T14. Transistor T13 is normally biased off. The leading edge of the input pulse turns T13 on and T14 off, causing a fast fall time at the output port, Pin 8. When the trailing edge is encountered, transistor T13 is turned off and T14 on. A faster rise time results than is possible with a passive load on T13. Rise and fall times are about 40 ns for a 40V pulse.

Transistors T5 through T12 serve as a binary to octal decoder, selecting one of eight resistors corresponding to each of the eight intensity levels. Transistor T15 forms a constant current source and, when used in conjunction with the selected resistor from the binary to octal converter, develops a unique voltage corresponding to one of the eight intensity levels. This voltage then references the diode D40 with the power gain of transistor T16. As the output pulse attempts to go more negative than this reference voltage, the diode D40 acts as a clamp and holds the output pulse to the reference value.

The network made up by D39 and R27 serves to DC restore the output pulse. This pulse is then coupled to the CRT cathode causing the spot to be intensified.

6.2.3 Adjustment Procedure

Load and start "Lots of Little Pictures" at address 107. Place the oscilloscope probe on the yellow wire terminal found on the display component plate. Adjust the intensity level pulse to approximately +20V. Adjust the intensity level setting on the 1705 CRT Bias module, display location Z02, to obtain a minimum intensity level (0). CRT light output should be minimum at this point. Readjust the gain potentiometer on the 4698 module for an even grey scale; minor adjustment should be required.

Figure 6-1 is a photograph of the 4698 Intensity Amplifier module and serves to illustrate the position of the gain control and the eight resistors responsible for the setting of the eight discrete intensity steps of the display. A circuit schematic of the module is shown in Figure 6-2.
Figure 6-1  4698 Intensity Amplifier Module
Figure 6-2  4698 Intensity Amplifier
## CHAPTER 7
ENGINEERING DRAWINGS

<table>
<thead>
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<th>Drawing Number</th>
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<td>20 μs Character Generator</td>
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<td>Utilization Module List</td>
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<td>External Components List</td>
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RO01 Diode Network

RO02 Diode Cluster
R107 Inverter

R111 Diode Gate
UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639-0
RESISTORS ARE 1/4W, 5%
DIODES ARE D662

R113 Diode Gate

UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639-0
RESISTORS ARE 1/4W, 5%
DIODES ARE D662

R123 Diode Gate
R603 Pulse Amplifier

B104 Inverter
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE 56 MFD
TRANSISTORS ARE DEC 2894-18

B105 Inverter

UNLESS OTHERWISE INDICATED:
CAPACITORS ARE 56 MFD
RESISTORS ARE 1/4W, 10%
TRANSISTORS ARE DEC 2894-18
RESISTORS ARE 100Ω, 5%

B123 Inverter
B124 Inverter

B301 Delay (One Shot)
B681 Power Inverter

W005 Clamped Load
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 15%
DIODES ARE 0664
TRANSISTORS ARE OEC3639B

W512 Positive Level Converter

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
DIODES ARE 0664
TRANSISTORS ARE OEC3009B

PARTS LIST A-PL-W603-0-0

W603 Positive Level Amplifier

7-11
NOTE:
Q1 IS MOUNTED ON A WAKEFIELD HEAT SINK 660-.75K

W704 Power Supply

UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W,±5%
DIODES ARE 0-664
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC2894-1B

B204 Quadruple Flip-Flop
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<th>NO. REQD.</th>
<th>DESCRIPTION</th>
<th>ITEM</th>
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<th>MFG.</th>
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A-PL-VA38-0-0 20 μs Character Generator
NOTES:
1. CONNECTIONS ON ITEMS "1" & "2" TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BOARD.
2. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
3. USE YELLOW WIRE (ITEM "3") FOR MACHINE WRAPPED & BLUE WIRE (ITEM "4") FOR HAND WRAPPED WIRING.
4. MODULE SLOTS BOX, A28, A29, A30 WILL BE CONNECTED TO FIXED POWER ONLY.
<table>
<thead>
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<th>NO. REQD.</th>
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<th>STOCK SIZE—CAT. NO.</th>
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SEE ML REF WIRE LIST (VA-39)

SEE ML REF EXTERNAL COMPONENTS LIST (VA-3P)

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**ASS'Y, D-UA-VA38-0-0**

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A-CP-VA38-0-7 External Components List