D-216
16-BIT
MSI computer.

DIGITAL COMPUTER CONTROLS INC
The D-216.
It's plug, program,
and mechanically interchangeable
with "11" Series Minicomputers.

Our new 16-BIT minicomputer is a general purpose MSI unit that incorporates the latest in solid-state components and electronic packaging. It's plug, program and mechanically interchangeable with the latest models in the "11" Series Minicomputers. Software requirements are identical. And you can physically substitute a D-216 for an "11" mainframe without mechanical adjustments.

Memory expansion to 32,768 words
The D-216 incorporates the latest MSI integrated circuit TTL components in a main console capable of receiving core or solid state memory up to a maximum of 32,768 words. The chassis is compact (10-1/2" x 19" x 23"). The front panel is only 8-3/4" high. And the unit can be rack mounted (on tilt and lock chassis slides), or table mounted in a stand-alone version.

Expand your system without complicating it
The D-216 DATA-BUS is configured to allow physical and electrical modularity. And that means unlimited system expansion. Without sacrificing either the simplicity of the system or the ease of its maintenance.

With DATA-BUS, instructions operate directly on register information. Data is transferred from input to output, and the CPU is bypassed. The devices themselves are modular subsystems that electrically attach to the DATA-BUS in parallel. I/O instructions are no longer required because of the memory-identity given to a device on the DATA-BUS. Instructions for I/O are accomplished on a word or byte basis in a manner directly comparable to moving data from one location in core to another.

A repertoire of more than 400 specific instructions
Although the Central Processor connects to the DATA-BUS like an I/O device, it controls the assignment of DATA-BUS to the subsystems and performs logical operations, including instruction decoding by utilizing Arithmetic
Accumulators, Index Registers, Auto Increment and Auto Decrement Registers. This gives greater flexibility than ever before, and provides an inherent repertoire of more than 400 specific instructions. Addressing modes of the CPU include direct register addressing, sequential addressing, full address incrementing and full address decrementing. In addition, both single and double address order codes are applied on either a byte or word basis.

**More power for your money**

The power of the D-216 Central Processing unit is demonstrated by features like single-line, multi-level interrupts, an unlimited number of DMA devices attached to the DATA-BUS, stack handling on a last-in, first-out basis with general register stack pointing, direct memory access (with maximum priority during instruction execution in order to store or acquire data at memory cycle speed), and a structural concept which allows you to use it in applications once confined to larger systems.

All this, at a very realistic price.

**Compare and decide**

Our D-216 16-BIT general purpose computer compares quite favorably with everything else on the market. Compare the speed, the flexibility, and the expansion capability. Then compare the total cost effectiveness (both initially and on a long-term basis).

**FUNCTIONAL CHARACTERISTICS**

**Read/Write Memory**
- Cycle Time: 1.2 microseconds
- Access Time: 400 nanoseconds
- Word Length: 16-BITS
- Core Memory Size: 4096 words, expandable to 32,768 words

**Read-Only-Memory**
- Access Time: 300 nanoseconds
- Word Length: 16-BITS

Increments of 1024 words available with additional options of Read/Write or Read-Only-Memory.

**Direct Memory Access**
- Rate: 2,500,000 words per second max.
- Maximum Latency: 3.5 microseconds for highest priority device
- Multiple device capability without multiplexer
- DATA-BUS Rate: 2,500,000 words per second

**Automatic Priority Interrupts**

One main level is incorporated initially with optional expansion to 4 main levels with any quantity of sublevels for each main level.

**Response Time**
7.2 microseconds including storage of existing program counter and status word insertion of new program counter.

**Restore Time**
4.5 microseconds for restoration of status word and program counter.

**General Registers**

Eight high-speed Flip-Flop Registers within the Central Processor which can be employed as Accumulators, 16-BIT Index Registers, Auto Increment or Auto Decrement Registers. The eight registers are available as stack pointers while register 6 is specifically utilized as the CPU Stack Pointer. Register 7 is always used as the Program Counter.

**Instructions**

400 hard-wired instructions through use of the General Register Address Modes.

- 65,576 Bytes or 32,768 words Machine Addressable.

**PHYSICAL CHARACTERISTICS**

**Table-Top Model:**
- Dimensions: 11" H x 20" W x 24" D
- Weight: 60 lbs. (4096 words of core)

**Rack-Mounted Model:**
- Dimensions: 10-1/2" H x 19" W x 23" D with Tilt and Lock Chassis slides
- Weight: 60 lbs (4096 words of core)
ELECTRICAL CHARACTERISTICS
Power Requirements:
115/230 volts ±10%, Single Phase, 47-63 Hz, 4 Amperes (4096 words of core)
DATA-BUS Logic Levels:
Ground and +3 Volts
Logic:
Integrated Circuitry TTL and Medium Scale Integration.

SYSTEM CONFIGURATION/OPTIONS
The basic system D-216 consists of:
Central Processor, Power Supply, Mounting Box, w/Tilt slides
Add-On Features/Options:
216/PC Programmers Console with
Switch Register, Remote Controllable, Key Actuated Panel
216/PF Power Failure Detection and
Auto Restart
216/TTC Teletypewriter Control
216/PI Four Level Priority Interrupt
216/EA Extended Arithmetic
ASR-33TU Modified Teletypewriter ASR-33TU
216/MM-4C 4096 Word Memory Module, 1.2 usec Core
216/MM-4S 4096 Word Memory Module, 0.9 usec Semiconductor RAM
216/MM-2S 2048 Word Memory Module, 0.9 usec Semiconductor RAM
216/MM-1S 1024 Word Memory Module, 0.9 usec Semiconductor RAM
216/MM-1R 1024 Word Memory Module, 0.35 usec Read-Only-Memory (ROM)
216/RTC-4 Real Time Clock, Power Line Frequency

In addition to the basic options that can be incorporated in the main frame there exists an extensive line of peripherals that can be utilized to extend system storage capability, on-line communications facility or methods for inserting data into a D-216. The following is a brief listing of these optional peripherals:
Single & Multiple Line Communications Interface Equipment
Remote Display Terminals
A/D-D/A Converters
Line Printers
Industry Compatible Magnetic Tape
High-Speed Paper Tape Reader or Punch
Teletypewriters
Magnetic Disk Systems

INSTRUCTIONS*
DOUBLE OPERAND GROUP:
OPR src, dst
MOV (B) MOVE (Byte)
ADD ADD
SUB SUBtract
CMP(B) COMPare (Byte)
BIT(B) Bit Test (Byte)
BIC(B) Bit Clear (Byte)
BIS(B) Bit Set (Byte)

SINGLE OPERAND GROUP:
OPR dst
CLR(B) CLeaR (Byte)
COM(B) COMplement (Byte)
INC(B) INCrement (Byte)
DEC(B) DECrement (Byte)
NEG(B) NEGate (Byte)
ADC(B) ADDt Add Carry (Byte)
SBC(B) SuBtract Carry (Byte)
TST(B) TeST (Byte)
ROL(B) ROtate Right (Byte)
ROL(B) ROtate Left (Byte)
ASR(B) Arithmetic Shift Right (Byte)
ASL(B) Arithmetic Shift Left (Byte)
JMP JuMP
SWAB SWAp Bytes
XEC eXECute

* Append B for byte instruction;
i.e., MOV B is MOVB Byte

CONDITIONAL BRANCHES:
B -- loc
(location = (offset x 2) + current address
to address + 2)
BR Branch always
BNE Branch if Not Equal (zero)
BEQ Branch if Equal (zero)
BGE Branch if Greater or Equal (zero)
BLT Branch if Less Than (zero)
BGT Branch if Greater Than (zero)
BLE Branch if Less or Equal (zero)
BPL Branch if Plus
BMI Branch if Minus
BHI  Branch if Higher
BLO S  Branch if LOwer or Same
BVS  Branch if oVerflow Set
BCC  Branch if Carry Clear
     or BHIS  Branch if Hlgher than
     or Same
BVC  Branch if oVerflow Clear
BCS  Branch if Carry Set
     or BHI  Branch if Hlgher

OPERATE GROUP: OPR
HALT   HALT
WAIT   WAit for InTerrupt
RTI    ReTurn from Interrupt
IOT    Input/Output Trap
     (Vector at 20)
RESET  RESET
EMTxxx EMulate Trap
     (Vector at 30)
TRAPxxx TRAP
     (Vector at 34)
Note: xxx  8-bit trap code

CONDITION CODES
OPERATOR: OPR
Instructions clear and set condition codes
in status word
CLC  CLear Carry (c)
SEC  SEt Carry(c)
CLV  CLear oVerflow(v)
SEV  SEt oVerflow(v)
CLZ  CLear Zero(z)
SEZ  SEt Zero(z)
CLN  CLear Negative(n)
SEN  SEt Negative(n)

ADDRESSING MODES
Source or
Destination
Symbolic  Description
R  register
@R or (R)  register deferred
(R)+  autoincrement
(R)−  autodecrement
@−(R)  autodecrement deferred
x(R)  indexed
@ x(R)  indexed deferred
(x is the index word)
#n  immediate (n = data)
@ #A  absolute (A = address)
A  relative
@ A  relative deferred

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