USER MANUAL FOR
DATA TRANSLATION, INC.
DEC DUAL HEIGHT
ANALOG INPUT SYSTEMS
DT2762        DT2765
DT2764        DT2765-T

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TABLE OF CONTENTS

CHAPTER 1

1.1 Options 1-1
1.1.1 DT2762 1-1
1.1.2 DT2764 1-1
1.1.3 DT2765 1-1

CHAPTER 2

DT2762 High Level Input System Specifications 2-1
2.1 Analog Inputs 2-1
2.2 Number of Analog Inputs 2-1
2.2.1 Selection of SE/DI 2-1
2.3 Input Range 2-1
2.4 Input Protection 2-1
2.5 Input Impedence 2-1
2.6 Input Bias Current 2-1
2.7 Maximum Input Signal 2-1
2.8 Common Mode Rejection Ratio 2-1
2.9 A/D Specifications 2-1
2.9.1 Resolution 2-1
2.9.2 Linearity 2-2
2.9.3 Inherent Quantizing Error 2-2
2.9.4 Stability 2-2
2.10 Sample and Hold Specifications 2-2
2.10.1 Aperature Uncertainty 2-2
2.11 System Specifications 2-2
2.11.1 System Accuracy 2-2
2.11.2 System Throughput 2-2
2.11.3 Input Noise 2-2
2.12 Power Requirements 2-2
2.13 System Compatibility 2-2
2.14 Physical 2-2

CHAPTER 3

DT2764 Wide Range Input System Specifications 3-1
3.1 Analog Inputs 3-1
**TABLE OF CONTENTS**

<table>
<thead>
<tr>
<th>CHAPTER 3 (cont.)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3.2</td>
<td>Number of Analog Inputs 3-1</td>
</tr>
<tr>
<td>3.2.1</td>
<td>Analog Input Range 3-1</td>
</tr>
<tr>
<td>3.2.2</td>
<td>Analog Input Configuration 3-1</td>
</tr>
<tr>
<td>3.2.3</td>
<td>Input Protection 3-1</td>
</tr>
<tr>
<td>3.2.4</td>
<td>Input Impedence 3-1</td>
</tr>
<tr>
<td>3.2.5</td>
<td>Input Bias Current 3-1</td>
</tr>
<tr>
<td>3.2.6</td>
<td>Maximum Input Signal 3-1</td>
</tr>
<tr>
<td>3.2.7</td>
<td>Common Mode Rejection Ratio 3-1</td>
</tr>
<tr>
<td>3.3</td>
<td>A/D Specifications 3-1</td>
</tr>
<tr>
<td>3.3.1</td>
<td>Resolution 3-1</td>
</tr>
<tr>
<td>3.3.2</td>
<td>Linearity 3-2</td>
</tr>
<tr>
<td>3.3.3</td>
<td>Inherent Quantizing Error 3-2</td>
</tr>
<tr>
<td>3.3.4</td>
<td>Stability 3-2</td>
</tr>
<tr>
<td>3.4</td>
<td>Sample and Hold Specification 3-2</td>
</tr>
<tr>
<td>3.4.1</td>
<td>Aperture Uncertainty 3-2</td>
</tr>
<tr>
<td>3.5</td>
<td>System Specification 3-2</td>
</tr>
<tr>
<td>3.5.1</td>
<td>System Accuracy 3-2</td>
</tr>
<tr>
<td>3.5.2</td>
<td>Throughput Rates 3-2</td>
</tr>
<tr>
<td>3.5.3</td>
<td>Input Noise 3-2</td>
</tr>
<tr>
<td>3.6</td>
<td>Power Requirements 3-2</td>
</tr>
<tr>
<td>3.6.1</td>
<td>DT2764 3-2</td>
</tr>
<tr>
<td>3.7</td>
<td>System Compatibility 3-2</td>
</tr>
<tr>
<td>3.8</td>
<td>Physical 3-3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CHAPTER 4</th>
<th>DT2765 Isolated Wide Range Input System Specifications 4-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.0</td>
<td>General 4-1</td>
</tr>
<tr>
<td>4.1</td>
<td>Input Specifications 4-1</td>
</tr>
<tr>
<td>4.2</td>
<td>Amplifier 4-1</td>
</tr>
<tr>
<td>4.3</td>
<td>A/D Converter 4-1</td>
</tr>
<tr>
<td>4.4</td>
<td>Power Requirements 4-2</td>
</tr>
<tr>
<td>4.5</td>
<td>DT2765-T Thermocouple Input 4-2</td>
</tr>
<tr>
<td>4.6</td>
<td>System Compatibility 4-2</td>
</tr>
<tr>
<td>4.7</td>
<td>Physical 4-2</td>
</tr>
</tbody>
</table>
# TABLE OF CONTENTS

## CHAPTER 5

<table>
<thead>
<tr>
<th>Section</th>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.1</td>
<td>DT2762 and DT2764 Programming</td>
<td>5-1</td>
</tr>
<tr>
<td>5.1.1</td>
<td>Modes of Operation</td>
<td>5-1</td>
</tr>
<tr>
<td>5.1.2</td>
<td>Device Address</td>
<td>5-1</td>
</tr>
<tr>
<td>5.1.3</td>
<td>Interrupt Vector Address</td>
<td>5-1</td>
</tr>
<tr>
<td>5.1.4</td>
<td>Control and Status Register</td>
<td>5-1</td>
</tr>
<tr>
<td>5.1.5</td>
<td>A/D Data Buffer Register (ADCSR) (Read Only)</td>
<td>5-2</td>
</tr>
<tr>
<td></td>
<td>CSR Bit Description</td>
<td>5-3</td>
</tr>
<tr>
<td>5.2</td>
<td>DT2765 Programming</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.1</td>
<td>Modes of Operation</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.2</td>
<td>Program I/O</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.3</td>
<td>Interrupt Operation</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.4</td>
<td>Device Address</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.5</td>
<td>Interrupt Vector Address</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.6</td>
<td>Control and Status Register</td>
<td>5-4</td>
</tr>
<tr>
<td>5.2.7</td>
<td>A/D Data Buffer Register (ADDBR) (Read Only)</td>
<td>5-5</td>
</tr>
<tr>
<td></td>
<td>CSR Bit Description</td>
<td>5-6</td>
</tr>
</tbody>
</table>

## CHAPTER 6

<table>
<thead>
<tr>
<th>Section</th>
<th>Topic</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1</td>
<td>Base Address Selection (DT2762, DT2764, DT2765)</td>
<td>6-1</td>
</tr>
<tr>
<td>6.2</td>
<td>Vector Address Selection</td>
<td>6-1</td>
</tr>
<tr>
<td></td>
<td>DT2764, DT2765</td>
<td>6-2</td>
</tr>
<tr>
<td>6.3</td>
<td>Analog Configuration</td>
<td>6-3</td>
</tr>
<tr>
<td></td>
<td>DT2762</td>
<td>6-2</td>
</tr>
<tr>
<td>6.3.1</td>
<td>Ranges</td>
<td>6-2</td>
</tr>
<tr>
<td>6.3.1.1</td>
<td>PG Option</td>
<td>6-2</td>
</tr>
<tr>
<td>6.3.2</td>
<td>Data Notation</td>
<td>6-3</td>
</tr>
<tr>
<td>6.4</td>
<td>Analog Configuration</td>
<td>6-3</td>
</tr>
<tr>
<td></td>
<td>DT2764</td>
<td>6-3</td>
</tr>
<tr>
<td>6.4.1</td>
<td>DT2764 Single Ended or Differential Input</td>
<td>6-3</td>
</tr>
<tr>
<td>6.4.2</td>
<td>Gain Configuration</td>
<td>6-4</td>
</tr>
<tr>
<td>6.4.3</td>
<td>Unipolar/Bipolar Selection</td>
<td>6-4</td>
</tr>
<tr>
<td></td>
<td>DT2764</td>
<td>6-4</td>
</tr>
</tbody>
</table>
# TABLE OF CONTENTS

## CHAPTER 6

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.4.4</td>
<td>Data Notation</td>
<td>6-5</td>
</tr>
<tr>
<td>6.5</td>
<td>Analog Configuration</td>
<td>6-5</td>
</tr>
<tr>
<td>6.5.1</td>
<td>Number of Channels</td>
<td>6-5</td>
</tr>
<tr>
<td>6.5.2</td>
<td>Bipolar - Unipolar Selection</td>
<td>6-5</td>
</tr>
<tr>
<td>6.5.3</td>
<td>Data Notation</td>
<td>6-6</td>
</tr>
<tr>
<td>6.5.4</td>
<td>Gain Configuration - DT2765</td>
<td>6-6</td>
</tr>
<tr>
<td>6.5.5</td>
<td>Programmable Gain Option</td>
<td>6-7</td>
</tr>
<tr>
<td></td>
<td>Figure 6</td>
<td>6-8</td>
</tr>
</tbody>
</table>

## CHAPTER 7

### Connection of Analog Inputs

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.1</td>
<td>Single Ended Inputs - 16 Channels</td>
<td>7-1</td>
</tr>
<tr>
<td>7.2</td>
<td>Pseudo - Differential Inputs - 16 Channels</td>
<td>7-2</td>
</tr>
<tr>
<td>7.3</td>
<td>Differential Inputs - 8 Channels</td>
<td>7-3</td>
</tr>
<tr>
<td>7.4</td>
<td>Isolated Analog Inputs - DT2765</td>
<td>7-4</td>
</tr>
<tr>
<td>7.5</td>
<td>Avoiding Spurious Signals</td>
<td>7-5</td>
</tr>
<tr>
<td>7.5.1</td>
<td>Twisted Pair Input Lines</td>
<td>7-5</td>
</tr>
<tr>
<td>7.5.2</td>
<td>Shielded Input Lines</td>
<td>7-5</td>
</tr>
<tr>
<td>7.5.3</td>
<td>Input Settling with High Source Impedance</td>
<td>7-5</td>
</tr>
<tr>
<td>7.6</td>
<td>Common Mode Rejection Ratio - (CMRR)</td>
<td>7-5</td>
</tr>
<tr>
<td>7.7</td>
<td>User Connections</td>
<td>7-6</td>
</tr>
<tr>
<td>7.7.1</td>
<td>CONN J1 - Channel Expansion - RTCIN</td>
<td>7-6, 7-7</td>
</tr>
<tr>
<td>7.7.2</td>
<td>DT2765/DT2765-T User Inputs</td>
<td>7-8</td>
</tr>
<tr>
<td>7.8</td>
<td>External Trigger and RTC Inputs</td>
<td>7-8</td>
</tr>
<tr>
<td>7.8.1</td>
<td>Input Signal Characteristics</td>
<td>7-8</td>
</tr>
<tr>
<td>7.8.1.1</td>
<td>EP050 REVD</td>
<td>7-8</td>
</tr>
<tr>
<td>7.8.1.2</td>
<td>EP050 REV E</td>
<td>7-9</td>
</tr>
</tbody>
</table>

## CHAPTER 8

### Calibration and Testing

<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1</td>
<td>Equipment and System Requirements</td>
<td>8-1</td>
</tr>
<tr>
<td>8.2</td>
<td>Loading SP0023 from</td>
<td></td>
</tr>
<tr>
<td>TABLE OF CONTENTS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>-------------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CHAPTER 8</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><em>(Cont.)</em></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8.2.1</td>
<td>Loading Floppy Disk</td>
<td>8-2</td>
</tr>
<tr>
<td>8.3</td>
<td>Using SP0023</td>
<td>8-2, 8-3</td>
</tr>
<tr>
<td>8.4</td>
<td>Test Descriptions</td>
<td>8-3</td>
</tr>
<tr>
<td>8.5</td>
<td>SP0023 Program</td>
<td></td>
</tr>
<tr>
<td>Description</td>
<td>8-4</td>
<td></td>
</tr>
<tr>
<td>8.6</td>
<td>SP0023 Tests</td>
<td>8-5</td>
</tr>
<tr>
<td>8.6.1</td>
<td>Test Description</td>
<td>8-5</td>
</tr>
<tr>
<td>8.6.2</td>
<td>Modes of Operation</td>
<td>8-5</td>
</tr>
<tr>
<td>8.6.3</td>
<td>Calibration</td>
<td>8-6</td>
</tr>
<tr>
<td>8.6.3.1</td>
<td>Calibration of Analog</td>
<td></td>
</tr>
<tr>
<td>Inputs</td>
<td>8-6</td>
<td></td>
</tr>
<tr>
<td>8.6.3.2</td>
<td>Calibration of Analog</td>
<td></td>
</tr>
<tr>
<td>Inputs with Programmable</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Amplifier</td>
<td>8-6</td>
<td></td>
</tr>
<tr>
<td>8.7</td>
<td>Adjustment Values</td>
<td>8-7</td>
</tr>
<tr>
<td>8.7.1</td>
<td>Notes on Full Scale</td>
<td>8-7</td>
</tr>
<tr>
<td>8.7.2</td>
<td>Computing Calibration</td>
<td></td>
</tr>
<tr>
<td>Values</td>
<td>8-7</td>
<td></td>
</tr>
<tr>
<td>8.7.3</td>
<td>A/D Offset Adjustment</td>
<td></td>
</tr>
<tr>
<td>Values</td>
<td>8-7</td>
<td></td>
</tr>
<tr>
<td>8.7.4</td>
<td>A/D Range Adjustment</td>
<td></td>
</tr>
<tr>
<td>Values</td>
<td>8-8</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>APPENDIX A</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>4-20mA Input Options</td>
</tr>
<tr>
<td>A.1</td>
</tr>
<tr>
<td>A.2 Coding</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>APPENDIX B</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Compensation Circuit</td>
</tr>
<tr>
<td>for DT2765-T</td>
</tr>
<tr>
<td>Ambient Temperature Compensation</td>
</tr>
<tr>
<td>Circuit</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>APPENDIX C</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>SP-0023 Program Listings</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th><strong>APPENDIX D</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic Drawings</td>
</tr>
</tbody>
</table>
CHAPTER 1

PRODUCT DESCRIPTION

DT2762 - High level Analog input system with 16 single-ended or 8 differential input channels on a standard DEC dual height card.

DT2772 - High level input expander - Expands the DT2762 to 64 single ended or 32 differential inputs: Packaged on a standard DEC dual height card.

DT2764 - Wide range analog input systems with 16 single ended or 8 differential input channels as a standard DEC dual input card. Ranges are resistor selectable from 10mV FSR to 10V FSR.

DT2774 - Wide range input expander - Expands the DT2764 to 64 single ended or 32 differential input. Packaged on a standard DEC dual height card.

DT2765 - Isolated Wide Range analog inputs system containing 4 channels of isolated analog inputs with dry reed relay flying capacitor multiplexing. Packaged on a standard DEC dual height card.

DT2775 - Isolated input expander - Expands the DT2765 to 20 channels of analog inputs in groups of eight channels. Packaged on a standard DEC dual height card.

1.1 Options

1.1.1 DT2762 - optional features are as follows:

PG - programmable gain amplifier, gain controlled via software with gains of 1, 2, 4 and 8.

C - 100KHz data acquisition module provides 100KHz analog acquisition and concession throughput.

1.1.2 DT2764

R - resistor gain selection bit provides resistor for setting gains of 100, 200, 10, 2, 1.

1.1.3 DT2765

PG - Programmable gain amplifier, gains controlled via software with gains of 1, 10, 100 and 500.

T - Thermocouple input version, provides input for cold reference junction compensation.
CHAPTER 2
DT2762 HIGH LEVEL INPUT SYSTEM SPECIFICATIONS

2.1 Analog Inputs
The DT2762 utilizes the DT5701 data acquisition module. This module will accept up to 16 single ended inputs or 8 differential inputs with 12 bit resolution. Expansion channels may be added by the addition of the DT2772 expander module for up to 64 single ended or 32 differential inputs.

2.2 Number of Analog Inputs
- 8 channels Differential input (DI)
- 16 channels Single Ended inputs (SE)
- 32 channels Differential (DI)
- 64 channels Single Ended (SE)

2.2.1 Selection of SE/DI
Selection of SE or DI must be specified by the user and cannot be changed except by the factory.

2.3 Input Range
0-5V, ±5V, 0-10V, ±10V twos compliment, or offset binary notation.

2.4 Input Protection
Inputs are current limited and protected to ±35V overvoltage without damage.

2.5 Input Impedence
100 MOHM, 10pF - "OFF" Channels
100 MOHM, 100pF - "ON" Channels

2.6 Input Bias Current
15nA @ 25°C

2.7 Maximum Input Signal
±10.5V Signal & Common Mode Voltage

2.8 Common Mode Rejection Ratio
80db @ 5V range
100db @ 10mV range

2.9 A/D Specifications
2.9.1 Resolution
12-bits Unipolar
11-bits + Sign Bipolar
2.9.2 Linearity
\( \pm \frac{1}{2} \) LSB

2.9.3 Inherent Quantizing Error
\( \pm \frac{1}{2} \) LSB

2.9.4 Stability
\( \pm 25 \text{ppm/}^\circ \text{C} \) FSR

2.10 Sample and Hold Specification

2.10.1 Aperature Uncertainty
Less than 10nS

2.11 System Specifications

2.11.1 System Accuracy
\( \pm 0.03\% \) FSR

2.11.2 System Throughput
The throughput is defined as the time interval from a start A/D convert to an A/D Done bit set. It does not include overhead of program to retrieve data.

Throughput = 35KHz or 28.5 uSEC
            = 100KHz or 10 uSEC optional

2.11.3 Input Noise
2uV RMS R.T.I.

2.12 Power Requirements
+5V @ 1.5A, 5%

2.13 System Compatibility
Standard DEC QBus compatible. DC Bus load = 1

2.14 Physical
Contained on a standard DEC dual height card for compatibility LSI-11, LSI-11/2 and LSI-11/23 systems.
CHAPTER 3

DT2764 WIDE RANGE INPUT SYSTEM SPECIFICATIONS

3.1 Analog Inputs
The DT2764 products utilize the Data Translation DT5702 12-bit data acquisition module. Expansion beyond 16 channels SE or 8 channels DI is accomplished with the DT2774 expander boards.

3.2 Number of Analog Inputs
DT2764 - 8 Channels DI, 16 Channels SE
DT2764 with DT2774 - Up to 32 Channels DI, 64 Channels SE

3.2.1 Analog Input Range
DT2764 - From 10mV to 10V Full Scale
From ±10mV to ±10V Full Scale
Ranger selectable via external resistor.

3.2.2 Analog Input Configuration
Analog inputs may be user selectable for Single Ended or Differential Input configuration. This selection is via jumpers on the board.

3.2.3 Input Protection
Inputs are current limited and protected to ±15V overvoltage without damage.

3.2.4 Input Impedence
100 MOHM, 10pF - "OFF" Channels
100 MOHM, 100pF - "ON" Channels

3.2.5 Input Bias Current
15nA @ 25°C

3.2.6 Maximum Input Signal
±10.5V Signal & Common Mode Voltage

3.2.7 Common Mode Rejection Ratio
80db @ 10V range
100db @ 10mV range

3.3 A/D Specifications

3.3.1 Resolution
12-bits Unipolar
11-bits + Sign Bipolar

3-1
3.3.2 Linearity

±¼ LSB

3.3.3 Inherent Quantizing Error

±¼ LSB

3.3.4 Stability

±25ppm/°C FSR

3.4 Sample and Hold Specification

3.4.1 Aperture Uncertainty

10nSec

3.5 System Specification

3.5.1 System Accuracy

The system accuracy is dependent upon the gain of the system as follows:

<table>
<thead>
<tr>
<th>GAIN</th>
<th>ACCURACY (BIPOLAR)</th>
<th>THROUGHPUT (KHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>±0.03%</td>
<td>31</td>
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<td>2</td>
<td>±0.03%</td>
<td>31</td>
</tr>
<tr>
<td>4</td>
<td>±0.03%</td>
<td>31</td>
</tr>
<tr>
<td>10</td>
<td>±0.03%</td>
<td>31</td>
</tr>
<tr>
<td>100</td>
<td>±0.05%</td>
<td>16.75</td>
</tr>
<tr>
<td>200</td>
<td>±0.07%</td>
<td>11.1</td>
</tr>
<tr>
<td>400</td>
<td>±0.08%</td>
<td>7.1</td>
</tr>
<tr>
<td>1000</td>
<td>±0.1%</td>
<td>3.7</td>
</tr>
</tbody>
</table>

(Table 3.5.1 Gain Parameters)

3.5.2 Throughput Rates

The system throughput is again dependent upon the gain of the system. Table 3.5.1 shows the throughput versus gain. This throughput is set via an external capacitor by the user.

3.5.3 Input Noise

2uV RMS

3.6 Power Requirements

3.6.1 DT2764 - +5V @ 1.5A, 5%

3.7 System Compatibility

Standard DEC Q-Bus compatible, DC Bus load =1.

3-2
3.8 **Physical**

Contained on a standard DEC dual height card for compatibility with LSI-11, LSI-11/2 and LSI-11/23 systems.
CHAPTER 4

DT2765 ISOLATED WIDE RANGE INPUT SYSTEM SPECIFICATIONS

4.0 General

The DT2765 series systems are Q-BUS compatible isolated wide range analog input systems. The input multiplexer is isolated via a flying capacitor technique utilizing dry reed relays. The system uses a DT5703 4 channel isolated data acquisition module. Expansion to 20 channels accomplished using the DT2775 expansion card.

4.1 Input Specification

4.1.1 Number of Analog Inputs

4 Differential, 12 channels with expander card.

4.1.2 Common mode voltage range

+250V DC max

4.1.3 Common mode rejection ratio

126db @ 60Hz with 1k unbalance

4.1.4 Input impedance

Power On

10 Megohms

Power Off

100 Megohms

4.1.5 Zero offset channel to channel

+10uV

4.1.6 Input filter

1.5Hz

4.1.7 Throughput Rate

Random Mode

20 conversions per sec.

4.1.8 Differential Input Voltage

15V DC max, or 100V for 10mS max.

4.2 Amplifier

4.2.1 Offset voltage

Adjustable to Zero

4.2.2 Offset voltage TC

+3uV/°C

4.2.3 Gain TC

+10ppm/°C

4.2.4 Gain Range

Gain of 1 to 1000 where, G = 1 + \frac{20,000}{R_{ext.}}

4.2.5 Bias Current

@ 25°C

50pA

@ 70°C

1.2nA

4.2.6 Input Noise

@ 15KHz BW

5uV rms

4.3 A/D Converter
4.3.1 Resolution 12 bits
4.3.2 Linearity ±1/4 LSB
4.3.3 Quantizing Error ±1/4 LSB
4.3.4 Range
   - Unipolar: 0 to +5V or 0 to 10V
   - Bipolar: ±5V ±10V
DT2725/15V
4.3.5 Temperature Coefficient
   - Zero Full Scale
   - ±20µV/°C
   - ±30ppm/°C
4.4 Power Requirements
4.4.1 DT2765 +5V @ 1.5A 5%
4.5 DT2765-T Thermocouple Input
4.5.1 Compensation Input Specification - DT2765-T
   The DT2765-T version allows connection of a compensation circuit for providing thermocouple cold junction compensation.
4.5.2 Input Connection
   The compensation inputs are connected at connector
   J1 Pins 15 COMP IN HI
   16 COMP IN LO
4.5.3 Input Impedence - 100 Ohms
4.5.4 Compensation Requirements
   - Type J IRON/CONSTANTINE 50µV/°C
   - Type T COPPER/CONSTANTINE 40µV/°C
   - Type K Chrome1/Alumel 40µV/°C
   For application circuit see Appendix
4.6 System Compatibility - Standard DEC
   Q-Bus compatible
   DC Bus Load - 1
4.7 Physical
   Standard DEC dual height card for compatibility with LSI-11, LSI-11/2 or LSI-11/23 systems.
CHAPTER 5
PROGRAMMING SPECIFICATIONS

Data Translation interfaces are designed to meet the requirements of standard DEC interfaces. As such they are structured around a Control and Status register for complete software control of the interface.

5.1 DT2762 and DT2764 Programming.

5.1.1 Modes of Operation.

This series can operate in a number of operating modes, as follows:

Program I/O - In this mode standard LSI-11 instructions can access and control the A/D components on the interface. A start A/D conversion can be accomplished by two ways:

1. Set A/D Start Bit (Bit 0) ADCSR

2. External Triggers or Real Time Clock input.

Interrupt - In many real time applications the program does not want to dedicate itself to taking analog measurements. In this case the interface can be enabled to produce a program interrupt on the condition A/D Done. An interrupt may also be produced on the Error bit (Bit 15 ADCSR).

5.1.2 Device Address

The DT2762 device address is selectable via a dip switch. Device address may be assigned between 1700000 and 1777748. The order of address is as follows, once a base address has been set in the switch:

A/D Control and Status Register (ADCSR) - Base
A/D Data Buffer Register (ADDBR) - Base + 2 (Read Only)

5.1.3 Interrupt Vector Address

The vector address is set via a dip switch pack, they are selectable in increments of 108. There are two Interrupts A/D DONE, and ERROR. (See 5.1.4 CSR descriptions).

A/D DONE = BASE VECTOR
ERROR = BASE VECTOR + 4

5.1.4 Control and Status Register

![Diagram of Control and Status Register](image-url)
5.1.5 A/D DATA BUFFER REGISTER (ADDBR) (READ ONLY)

This location contains the A/D data, the format is as follows:

```
  15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
```

MSB ←→ MSB

A/D Data → LSB
CSR BIT DESCRIPTIONS:

<table>
<thead>
<tr>
<th>BIT #</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
</table>
| 15    | ERROR                 | READ/WRITE - Indicates an error set by one of the following conditions.  
|       |                       | 1. Attempting an external start or clock start during MUX settling.  
|       |                       | 2. Attempting a start while conversion in process.  
|       |                       | 3. Attempting any start while the A/D Done bit is set.  
|       |                       | Cleared by Processor and Init. |
| 14    | ERROR INT.            | READ/WRITE - When set enables an Interrupt on Error Bit. Cleared by INIT. |
|       | ENABLE                |             |
| 13-8  | MULTIPLEXER ADDRESS   | READ/WRITE - Six MUX channel address bits for addressing up to 64 channels. |
| 7     | A/D DONE              | READ ONLY - Set by end of conversion reset by read A/D data. Cleared by INIT. |
| 6     | DONE INT.             | READ/WRITE - When set will enable interrupts from A/D done. Cleared by INIT. |
|       | ENABLE                |             |
| 5     | RTC ENB               | READ/WRITE - Real time clock enable when set this bit allows start conversion from the real time clock |
| 4     | EXT TRIG ENB          | READ/WRITE - When set this bit allows start conversion from an external trigger source. |
| 3-2   | GAIN SELECT           | READ/WRITE - These bits provide the gain select information. |
|       |                       | \begin{tabular}{|c|c|c|}
<table>
<thead>
<tr>
<th>BIT 3 (GS1)</th>
<th>2 (GS0)</th>
<th>GAIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ø</td>
<td>A/D START</td>
<td>WRITE/ONLY - Initiates a conversion when set, cleared by internal logic after start conversion, will always read back as Ø.</td>
</tr>
</tbody>
</table>
5.2 DT2765 Programming

5.2.1 Modes of Operation
The DT2765 can operate in a number of operating modes, as follows.

5.2.2 Program I/O
In this mode standard LSI-11 instructions can access and control the A/D on the interface. Start A/D conversion is accomplished by loading the MUX channel in the CSR.

5.2.3 Interrupt Operation
In many real time applications the computer does not want to be dedicated to taking analog measurements. Then the Interrupt on A/D done bit is utilized.

5.2.4 Device Address
The DT2765 device address is selectable via a dip switch. Device Address may be assigned between 1700000_8 and 177774_8. The order of the address is as follows, once a base address has been set in A/D Control and Status Register (ADCSR) - Base A/D Data Buffer Register (ADDBR) - Base + 2 (Read only).

5.2.5 Interrupt Vector Address
The vector address is set via a dip switch pack, and are selectable in increments of 10_8. There are two interrupts: A/D DONE, and ERROR.

\[
\begin{align*}
A/D \text{ DONE} &= \text{BASE VECTOR} \\
\text{ERROR} &= \text{BASE VECTOR + 4}
\end{align*}
\]

5.2.6 Control and Status Register

[Diagram of control and status register]

- EN Error Int
- Multiplexer ADDR
- A/D Done
- ENB Interrupt Enable
- GSI, GS0

(Note Used on DT2765)
5.2.7 A/D DATA BUFFER REGISTER (ADDBR) READ ONLY

This location contains the A/D data, the format is as follows:

```
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

MSB ←  MSB ←  LSB

A/D Data
### CSR BIT DESCRIPTIONS

**NOTE:**

<table>
<thead>
<tr>
<th>BIT #</th>
<th>NAME</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ERROR (NOT USED IN DT2765)</td>
<td>Cleared by INIT</td>
</tr>
<tr>
<td>14</td>
<td>ERROR INT. ENABLE</td>
<td>READ/WRITE - When set Enables an Interrupt on Error Bit. Cleared by INIT</td>
</tr>
<tr>
<td>13-8</td>
<td>MULTIPLEXER ADDRESS</td>
<td>READ/WRITE - Six MUX channel address bits for addressing up to 64 channels. Will start an A/D conversion upon loading new MUX channel.</td>
</tr>
<tr>
<td>7</td>
<td>A/D DONE</td>
<td>READ ONLY - Set by end of conversion reset by read A/D data. Cleared by INIT.</td>
</tr>
<tr>
<td>6</td>
<td>EN INTERRUPT DONE</td>
<td>READ/WRITE - When set will enable interrupts from A/D done. Cleared by INIT.</td>
</tr>
<tr>
<td>5,4</td>
<td>NOT USED ON DT2765</td>
<td>READ/WRITE - These bits provide the gain select information:</td>
</tr>
<tr>
<td>3-2</td>
<td>GAIN SELECT</td>
<td></td>
</tr>
<tr>
<td>1,0</td>
<td>NOT USED</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** All instructions that modify the upper Byte of the CSR will cause a start A/D conversion.
6.1 Base Address Selection (DT2762, DT2764, DT2765)

The Base Address which is the I/O address assigned to the Control-Status Register (CSR) is user selectable by means of DIP switches SW1 and SW2 located near the bus interface logic as shown in Appendix E. The A/D Data Buffer Register address is then two locations greater than the CSR (Base) address. The DIP switches allow the user to set the base address anywhere in the 170000<sub>8</sub> - 170000<sub>8</sub> address space in increments of 4<sub>8</sub>. The recommended base address for the DT2760 series is 170000<sub>8</sub> and is the address set at the factory. Figure 6.1 shows how switches SW1 and SW2 must be set to generate this base address.

![Diagram of DIP switches and bit mapping]

**Figure 6.1**
Switch Setting for Base Address of 170000<sub>8</sub>

As shown in Figure 6.1 a switch in the "ON" position represents a "1" in the corresponding bit location and a switch in the "OFF" position represents a "0" in the corresponding bit location.

6.2 Vector Address Selection - DT2764, DT2765

The DT2760 series systems are capable of generating two distinct interrupt vectors to the LSI-11 processor. These interrupts can occur when:

1. A/D Done is set
2. Error is set

Each of these two events can generate a unique interrupt to the
6.2 processor with the internal priority being arranged such that the A/D Done interrupt has the higher priority of the two if both occur simultaneously and are both enabled. The interrupt vector address in the 000\textsubscript{8} - 770\textsubscript{8} vector address space in 10\textsubscript{8} increments. The interrupt vector of the Error Interrupt is then always 4\textsubscript{8} locations higher than the A/D Done interrupt vector address. The recommended interrupt vector address for the DT2760 series is 130\textsubscript{8} and is set to that value at the factory. Figure 6.2 shows how switch SW2 must be set to generate this address.

![Diagram of switch settings](image)

Figure 6.2
Switch Setting for Vector Address of 130\textsubscript{8}

6.3 Analog Configuration DT2762
Factory Supplied Range - ±10V FSR 2's Complement Notation.

6.3.1 Ranges
The DT2762 is a high level system only and can be configured for the following ranges and data formats. The ranges are selectable via wire wrap posts and ±10V 2's complement is installed in etch on the board.

<table>
<thead>
<tr>
<th>RANGE</th>
<th>CONNECT JUMPER</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-10V</td>
<td>1 and 2</td>
</tr>
<tr>
<td>±10V</td>
<td>2 and 4</td>
</tr>
<tr>
<td>0-5V</td>
<td>3 and 4</td>
</tr>
<tr>
<td>±5V</td>
<td>1 and 3</td>
</tr>
</tbody>
</table>

**NOTE:** The user must cut the jumpers which are already etched at pins 2, 4, 5 to change ranges from the factory supplied ±10V, 2's complement.

**NOTE:** The jumpers are located at the handle end of the board. Installing a jumper requires wire wrapping across a pair of pins as marked in Fig. 6.

6.3.1.1 PG Option
When the programmable gain option is installed the DT2762 must be set for ±10V or 0 to 10V coding only.
6.3.1.1 PG Option
(Cont.) Thus the ranges with PG option are:

\[
\begin{align*}
\text{GAIN} & = 1 - 10\text{V} \\
& = 2 - 5\text{V} \\
& = 4 - 2.5\text{V} \\
& = 8 - 1.25\text{V}
\end{align*}
\]

6.3.2 Data Notation
Parallel digital outputs are provided in binary code. A unipolar input (0 to 10V, 0 to 5V) signal should be jumpered to produce a straight binary output. A Bipolar input (±5V, ±10V) can be jumpered to produce offset binary coding or 2's complement code.

CODING JUMPERS

BINARY NOTATION - CONNECT JUMPER 6
2's COMPLEMENT - CONNECT JUMPER 5

<table>
<thead>
<tr>
<th>CODE</th>
<th>10V FULL SCALE</th>
<th>20V FULL SCALE</th>
<th>16 BIT OUTPUT CODE (OCTAL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BINARY</td>
<td>+9.9976V</td>
<td>-9.9976V</td>
<td>007777</td>
</tr>
<tr>
<td></td>
<td>0.0000V</td>
<td>0.0000V</td>
<td>000000</td>
</tr>
<tr>
<td>OFFSET</td>
<td>+4.9976V</td>
<td>+4.9976V</td>
<td>007777</td>
</tr>
<tr>
<td>BINARY</td>
<td>0.0000V</td>
<td>0.0000V</td>
<td>000000</td>
</tr>
<tr>
<td></td>
<td>-5.0000V</td>
<td>-10.0000V</td>
<td>000000</td>
</tr>
<tr>
<td>2'S COMP.</td>
<td>+4.9976V</td>
<td>+4.9976V</td>
<td>003777</td>
</tr>
<tr>
<td>COMPLEMENT</td>
<td>0.0000V</td>
<td>0.0000V</td>
<td>000000</td>
</tr>
<tr>
<td></td>
<td>-5.0000V</td>
<td>-10.0000V</td>
<td>174000</td>
</tr>
</tbody>
</table>

CODING TABLE

6.4 Analog Configuration DT2764

Factory Supplied - ±10mv FSR 2's Complement notation differential inputs.

6.4.1 DT2764 Single Ended or Differential Input
The DT2764 can be user configured for SE or DI operation as follows:

<table>
<thead>
<tr>
<th>JUMPERS</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SE (16 channels)</td>
<td>P1 to P2</td>
</tr>
<tr>
<td>DI (8 channels)</td>
<td>P2 to P3, P4 to P5</td>
</tr>
</tbody>
</table>

NOTE: The user must cut the jumper in etch at P2 to P3, P4 to P5 to change from DI operation to SE operation
6.4.2 Gain Configuration - DT2764 - Gains from 1 to 1000

The INSTRUMENTATION AMPLIFIER may be programmed for a gain between 1 and 1000. Because the A/D has an input voltage range of either 0 to +10V volts, or ±10 volts, the gain of the INSTRUMENTATION AMPLIFIER will determine the input signal voltage range to be digitized. At a gain of 1000, the input signal range for full scale would be 10mV. For a gain of 1, no external resistor need be added, since the instrumentation amplifier has been set to this gain internally. The gain equation for the INSTRUMENTATION AMPLIFIER is:

\[ G = 1 + \frac{20,000}{R_G} \quad \text{or} \quad \frac{R_G}{R_G} = 20,000 \]

The table shows a chart of resistors and capacitors for setting the gain and timing.

<table>
<thead>
<tr>
<th>INPUT RANGE</th>
<th>GAIN</th>
<th>Rg (Ohms)</th>
<th>Cf</th>
<th>SETTLING TIME</th>
<th>ACCURACY THROUGHPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±10mV</td>
<td>1000</td>
<td>20.02</td>
<td>0.015uf</td>
<td>250us</td>
<td>±0.1%</td>
</tr>
<tr>
<td>±25mV</td>
<td>400</td>
<td>50.13</td>
<td>6800pf</td>
<td>120us</td>
<td>±0.08%</td>
</tr>
<tr>
<td>±50mV</td>
<td>200</td>
<td>100.5</td>
<td>3300pf</td>
<td>70us</td>
<td>±0.07%</td>
</tr>
<tr>
<td>±100mV</td>
<td>100</td>
<td>202.0</td>
<td>150pf</td>
<td>40us</td>
<td>±0.05%</td>
</tr>
<tr>
<td>±1.0 Volt</td>
<td>10</td>
<td>2222</td>
<td>None</td>
<td>12us</td>
<td>±0.03%</td>
</tr>
<tr>
<td>±2.5 Volts</td>
<td>4</td>
<td>6667</td>
<td>None</td>
<td>12us</td>
<td>±0.03%</td>
</tr>
<tr>
<td>±5.0 Volts</td>
<td>2</td>
<td>20.0K</td>
<td>None</td>
<td>12us</td>
<td>±0.03%</td>
</tr>
<tr>
<td>±10.0 Volts</td>
<td>1</td>
<td>None</td>
<td>None</td>
<td>12us</td>
<td>±0.03%</td>
</tr>
</tbody>
</table>

NOTE: THROUGHPUT = AMP SETTLING TIME + 20 USEC A/D CONVERSION TIME.

6.4.3 Unipolar/Bipolar Selection - DT2764

The DT2764 can be configured for Unipolar (0 to F.S.) on Bipolar (+F.S.) operation.

<table>
<thead>
<tr>
<th>CONNECT JUMPERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNIPOLAR 0 TO F.S.</td>
</tr>
<tr>
<td>BIPOLAR ± F.S.</td>
</tr>
</tbody>
</table>

NOTE: The user must cut the jumper in etch at 2 and 4 to change the range from Bipolar to Unipolar.
6.4.4 Data Notation

Parallel digital outputs are provided in binary code. A unipolar input (0 to F.S.) should be jumpered to produce a straight binary output. A Bipolar input (±F.S.) can be jumpered to produce offset binary coding or 2's complement coding.

CODING JUMPERS

BINARY NOTATION - CONNECT JUMPERS 6
2's COMPLEMENT - CONNECT JUMPER 5

<table>
<thead>
<tr>
<th>CODE</th>
<th>RANGE</th>
<th>16 BIT BINARY CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Binary</td>
<td>+ F.S.</td>
<td>007777</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>000000</td>
</tr>
<tr>
<td>Offset Binary</td>
<td>+ F.S.</td>
<td>007777</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>004000</td>
</tr>
<tr>
<td></td>
<td>- F.S.</td>
<td>000000</td>
</tr>
<tr>
<td>2's Complement</td>
<td>+ F.S.</td>
<td>003777</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>000000</td>
</tr>
<tr>
<td></td>
<td>- F.S.</td>
<td>174000</td>
</tr>
</tbody>
</table>

6.5 Analog Configuration

DT2765 isolated wide range analog input system.

Factory Supplied ±10mV F.S.R. 2's complement notation unless PG option is installed then range is set by program control.

6.5.1 Number of Channels

The DT2765 is strictly a 4 channel isolated analog input system. The inputs are fully isolated via a flying capacitor dry reed multiplexer. Expansion beyond 4 channels is accomplished by the addition of the DT2775 dual height expander module. All inputs are fully differential.

6.5.2 Bipolar - Unipolar Selection

The DT2765 can be configured for Bipolar (±F.S.) or Unipolar (0 to F.S.) operation.

<table>
<thead>
<tr>
<th>UNIPOLAR 0 to F.S.</th>
<th>1 and 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIPOLAR ±F.S.</td>
<td>2 and 4</td>
</tr>
</tbody>
</table>

NOTE: The user must cut the jumper in etch at 2 and 4 to change the range from Bipolar to Unipolar.

6-5
6.5.3 Data Notation

Parallel digital outputs are provided in binary code. A Unipolar input should be jumpered to produce a straight binary output. A Bipolar input (±F.S.) can be jumpered to produce offset binary coding or 2's complement coding.

CODING JUMPERS

BINARY NOTATION - CONNECT JUMPER 6
2's COMPLEMENT - CONNECT JUMPER 5

<table>
<thead>
<tr>
<th>CODE</th>
<th>RANGE</th>
<th>16 BIT BINARY CODE (OCTAL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>BINARY</td>
<td>+F.S.</td>
<td>007777</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>000000</td>
</tr>
<tr>
<td>OFFSET</td>
<td>+F.S.</td>
<td>007777</td>
</tr>
<tr>
<td>BINARY</td>
<td>0</td>
<td>004000</td>
</tr>
<tr>
<td></td>
<td>-F.S.</td>
<td>000000</td>
</tr>
<tr>
<td>2's COMPLEMENT</td>
<td>+F.S.</td>
<td>003777</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>000000</td>
</tr>
<tr>
<td></td>
<td>-F.S.</td>
<td>174000</td>
</tr>
</tbody>
</table>

6.5.4 Gain Configuration - DT2765 - Gains from 1 to 1000

The INSTRUMENTATION AMPLIFIER may be programmed for a gain between 1 and 1000. Because the A/D has an input voltage range of either 0 to +10V volts, or ±10 volts, the gain of the INSTRUMENTATION AMPLIFIER will determine the input signal voltage range to be digitized. At a gain of 1000, the input signal range for full scale would be 10mV. For a gain of 1, no external resistor need be added, since the instrumentation amplifier has been set to this gain internally. The gain equation for the INSTRUMENTATION AMPLIFIER is:

\[
G = 1 + \frac{20,000}{R_G} \quad \text{or} \quad R_G = \frac{20,000}{G-1}
\]
The table shows a chart of resistors for setting the gain.

<table>
<thead>
<tr>
<th>INPUT RANGE</th>
<th>GAIN</th>
<th>OHMS</th>
<th>SYSTEM ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>±10mV</td>
<td>1000</td>
<td>20.02</td>
<td>+0.1%</td>
</tr>
<tr>
<td>±25mV</td>
<td>400</td>
<td>50.13</td>
<td>+0.08%</td>
</tr>
<tr>
<td>±50mV</td>
<td>200</td>
<td>100.5</td>
<td>+0.07%</td>
</tr>
<tr>
<td>±100mV</td>
<td>100</td>
<td>202.0</td>
<td>+0.05%</td>
</tr>
<tr>
<td>±1.0 Volt</td>
<td>10</td>
<td>2222</td>
<td>+0.03%</td>
</tr>
<tr>
<td>±2.5 Volts</td>
<td>4</td>
<td>6667</td>
<td>+0.03%</td>
</tr>
<tr>
<td>±5.0 Volts</td>
<td>2</td>
<td>20.0K</td>
<td>+0.03%</td>
</tr>
<tr>
<td>±10.0 Volts</td>
<td>1</td>
<td>None</td>
<td>+0.03%</td>
</tr>
</tbody>
</table>

6.5.5 Programmable gain option.

The DT2765 can be configured with a programmable gain amplifier. In this case the range must be set for 10V and the gains can be programmed as follows:

<table>
<thead>
<tr>
<th>GAIN</th>
<th>RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10V</td>
</tr>
<tr>
<td>10</td>
<td>1V</td>
</tr>
<tr>
<td>100</td>
<td>100mV</td>
</tr>
<tr>
<td>500</td>
<td>20mV</td>
</tr>
</tbody>
</table>
CHAPTER 7
CONNECTION OF ANALOG INPUTS

Table 7.1 shows the various models and the connection schemes available.

<table>
<thead>
<tr>
<th>MODEL</th>
<th>SE/DI JUMPER SELECTABLE</th>
<th>NUMBER OF INPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DT2762-SE</td>
<td>NO</td>
<td>16</td>
</tr>
<tr>
<td>DT2762 - DI</td>
<td>NO</td>
<td>8</td>
</tr>
<tr>
<td>DT2764</td>
<td>YES</td>
<td>16 SE</td>
</tr>
<tr>
<td>DT2765</td>
<td>NO</td>
<td>8 DI</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4 DI (ISOLATED)</td>
</tr>
</tbody>
</table>

7.1 Single Ended Inputs - 16 Channels

Single ended analog inputs - Single ended connections are those which have a common side that is referenced back to analog common of the system. The advantage of this scheme is that the user gets twice the number of channels in the same space. The major disadvantage is that the user gives up any common mode rejection he might obtain from a differential system.

Recommendations:

High level inputs, greater than 1V.
Short lead lengths, less than 15 ft.

\[ \text{VIN} = \text{VS} + \text{VCM} \]

Fig 7.1 Single Ended Inputs
Fig. 7.1 Single Ended Inputs (continued)

Where $V_{CM} = $ Common Mode Voltage

7.2 Pseudo - Differential Inputs - 16 Channels.

Pseudo - Differential mode can be utilized with a single ended system if the user has all input sensors referenced to a common ground point. In this manner the input instrumentation amplifier can reject common mode noise. This is possible since the AMP LO input is brought out to connector J1 for user connection. The following diagram illustrates -

Recommendation:

Input Ranges: 100mV to 10V
Lead Lenghths- less than 25 ft.

VIN = $V_S + CMRR (VCM)$

Fig. 7.2 PSEUDO-DIFFERENTIAL
7.3 **Differential Inputs - 8 Channels**

Differential Inputs - when the differential input scheme is utilized, there are two switches per channel, thus the number of channels are cut in half. The benefits are that common mode voltages, i.e. voltages appearing on both sides of the source simultaneously can be rejected by the differential input instrumentation amplifier. This CMR accounts for a much quieter system. The amount of CMRR depends on how well balanced the instrumentation amplifier is.

**Recommendations:**

- **Input Ranges:** 10mV to 10V
- **Lead Lengths:** As required by user
- **Lead Type:** Twisted Pair (Low Level) Shielded Input line.

---

**Fig. 7.3 DIFFERENTIAL INPUT CONNECTION**

---
7.4 Isolated Analog Inputs - DT2765

The DT2765 provides four (4) isolated input channels via a dry reed flying capacitor multiplexer. Since the inputs are isolated there need not be any connection of system ground to input signal reference.

V_S

VCM = 250V p-p

Fig 7.4 Isolated Analog Input.
7.5  Avoiding Spurious Signals
In order to obtain the best performance from a system, certain
guidelines in connecting analog signals to the system should
be utilized. These guidelines and precautions will minimize
the pickup of electrical noise by measuring circuits.

7.5.1  Twisted Pair Input Lines
The effects of magnetic coupling on the input signals may
be reduced for differential input configuration by twisting
the signal and return lines. This is effective since the
inductive pickup voltages on the two lines tend to match, thus
not having an effect on the measurement. This is not the
case for a ground referenced single ended system.

7.5.2  Shielded Input Lines
The effects of electrostatic coupling may be reduced by shield-
ing the input lines. This becomes important if the source has a
high impedance. The shield should only be tied to ground at the
instrument end. This will prevent ground loop currents.

7.5.3  Input Settling with High Source Impedance
Solid state multiplexers inject a small amount of charge into
the input lines when channels are switched. This can cause
a transient error due to the input source impedance time
constants. All Data Translation systems allow for input set-
tting upon new channel selection. The settling time varies for
the different input systems available.

Normally, the control logic allows sufficient time for this
charge to settle to less than \( \frac{1}{2} \) LSB of error (nine time con-
tants to 0.012 percent). However, more time may be needed
when the multiplexer is switching an input channel with high
source impedance, particularly when large amounts of shunt
capacitance exists in the interconnecting cables. Source
impedance/cable shunt capacitance products greater than 1 uSec
(1K-1000PF) on 30KHz units should be avoided for less than
\( \frac{1}{2} \) LSB error. Assuming a twisted pair cable capacitance of
50 PF/foot and 1K ohm source impedance this translates into a
maximum run of twenty feet on 30KHz models. Note also that
settling errors can be minimized by increasing the internal
time out with an external capacitor \( C_t \) (\( \approx 60PF \) per uSec).

7.6  Common Mode Rejection Ratio - (CMRR)
The CMRR of a system is defined as the ratio of output voltage
from the instrumentation amplifier to the voltage which is
common to both sides of the differential input amplifier. This
ratio is given in units of decibels.

7-5
7.6 For example, the specification for CMRR on Data Translation's wide range interface is 100db at 60HZ at a gain of 1000. Thus with a CMV of 10 volts, the V out of the amplifier at a gain of 1000 should be:

\[ CMRR = 20 \log_{10} \left( \frac{CMV}{VOUT/A} \right) \]

Where CMRR = common mode rejection in db
CMV = common mode voltage
VOUT = The change in the amplifier output voltage due to the CMV.
A = Amplifier gain

\[ 100 = 20 \log_{10} \left( \frac{CMV}{VOUT/A} \right) \]

\[ \text{Antilog} (100) = \frac{10^4}{20} \frac{VOUT}{1000} \]

\[ 10^5 = \frac{10^4}{VOUT} \]

\[ VOUT = 10^{-1} V. \]

Thus with a CMV of 10 volts, the output of the instrumentation amplifier is 100 millivolts.

7.7 User Connections

User connections are via a 20 pin connector. Mass terminated connections can be made to either flat ribbon cable or twisted pair cable.

7.7.1 CONN J1 - Channel Expansion - RTCIN

Connector J1 is utilized for expansion of input channels via expander loads DT2772, DT2774 and DT2775. Also contained on this connector is the Real Time Clock input RTCINL.
### J1 Connector - Expansion Connector

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Pin</th>
<th>Signal Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MX0H</td>
<td>2</td>
<td>MX1H</td>
</tr>
<tr>
<td>3</td>
<td>MX2H</td>
<td>4</td>
<td>MX3H</td>
</tr>
<tr>
<td>5</td>
<td>MX4H</td>
<td>6</td>
<td>MX5H</td>
</tr>
<tr>
<td>7</td>
<td>MXENB</td>
<td>8</td>
<td>SE/DI</td>
</tr>
<tr>
<td>9</td>
<td>RTC INL</td>
<td>10</td>
<td>D GND</td>
</tr>
<tr>
<td>11</td>
<td>DGND</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>AGND</td>
<td>14</td>
<td>A GND</td>
</tr>
<tr>
<td>15</td>
<td>MXOUT HI</td>
<td>16</td>
<td>MXOUT LO</td>
</tr>
<tr>
<td>17</td>
<td>AGND</td>
<td>18</td>
<td>-15V</td>
</tr>
<tr>
<td>19</td>
<td>AGND</td>
<td>20</td>
<td>+15V</td>
</tr>
</tbody>
</table>

#### 7.7.2 CONN - J2 Analog Inputs

**CONN J2 - DT2762/DT2764 Single Ended Inputs**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CH0</td>
<td>11</td>
<td>CH5</td>
</tr>
<tr>
<td>2</td>
<td>CH8</td>
<td>12</td>
<td>CH13</td>
</tr>
<tr>
<td>3</td>
<td>CH1</td>
<td>13</td>
<td>CH6</td>
</tr>
<tr>
<td>4</td>
<td>CH9</td>
<td>14</td>
<td>CH14</td>
</tr>
<tr>
<td>5</td>
<td>CH2</td>
<td>15</td>
<td>CH7</td>
</tr>
<tr>
<td>6</td>
<td>CH10</td>
<td>16</td>
<td>CH15</td>
</tr>
<tr>
<td>7</td>
<td>CH3</td>
<td>17</td>
<td>AGND</td>
</tr>
<tr>
<td>8</td>
<td>CH11</td>
<td>18</td>
<td>AMPLO</td>
</tr>
<tr>
<td>9</td>
<td>CH4</td>
<td>19</td>
<td>EXT TRIG L</td>
</tr>
<tr>
<td>10</td>
<td>CH12</td>
<td>20</td>
<td>D. GND.</td>
</tr>
</tbody>
</table>

**CONN J2 - DT2762/DT2764 Differential Inputs**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CH0</td>
<td>11</td>
<td>CH5</td>
</tr>
<tr>
<td>2</td>
<td>RET0</td>
<td>12</td>
<td>RET5</td>
</tr>
<tr>
<td>3</td>
<td>CH1</td>
<td>13</td>
<td>CH6</td>
</tr>
<tr>
<td>4</td>
<td>RET1</td>
<td>14</td>
<td>RET6</td>
</tr>
<tr>
<td>5</td>
<td>CH2</td>
<td>15</td>
<td>CH7</td>
</tr>
<tr>
<td>6</td>
<td>RET2</td>
<td>16</td>
<td>RET7</td>
</tr>
<tr>
<td>7</td>
<td>CH3</td>
<td>17</td>
<td>AGND</td>
</tr>
<tr>
<td>8</td>
<td>RET3</td>
<td>18</td>
<td>AMPLO</td>
</tr>
<tr>
<td>9</td>
<td>CH4</td>
<td>19</td>
<td>EXT TRIG L</td>
</tr>
<tr>
<td>10</td>
<td>RET4</td>
<td>20</td>
<td>D. GND.</td>
</tr>
</tbody>
</table>
7.7.2 DT2765/DT2765-T - User Inputs
(Cont.)

<table>
<thead>
<tr>
<th>CONN J2 - ISOLATED DIFFERENTIAL INPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin</td>
</tr>
<tr>
<td>-----</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>8</td>
</tr>
<tr>
<td>9</td>
</tr>
<tr>
<td>10</td>
</tr>
</tbody>
</table>

7.8 External Trigger and RTC Inputs

This series of analog interfaces allow the user to externally trigger the conversion. Thus allowing synchronization of conversion to real word or a real time clock input. Data Translation can supply the user with a KWV11-A equivalent module, the DT2769 real time clock module.

7.8.1 Input Signal Characteristics

7.8.1.1 EP050 REVD.

For this revision the RTCIN inputs and the EXT TRIG inputs are different.

**EXT TRIG L Input** - CONN J2 PIN 19

**DIGITAL GROUND** - CONN J2 PIN 20

- TTL compatible, 1 unit LOAD
- Positive pulse, 100 MSEC to 2JSEC duration.
- Trigger on high to low transition.

**RTC INL INPUT** - CONN J1 PIN 9

**DIGITAL GROUND** - CONN J1 PIN 10

7-8
7.8.1.1
(Cont.)
- TTL or CMOS input compatible
- Source current $\lesssim 10\mu\text{A}$
- Sink current $\lesssim 10\mu\text{A}$
- LO THRESHOLD $\lesssim 0.8\text{V}$
- HI THRESHOLD $\geq 2.4\text{V}$
- MAX HI VOLTAGE 11V MAX.
- Pulse input - Hi to low pulse duration 200nSEC to 2μSEC.
- Trigger on LO to HI transition.

7.8.1.2 EPO50 REV E
This revision has both inputs with identical electrical characteristics.

Electrical Characteristics
- TTL or CMOS compatible
- Source current, less than 10μA
- Sink current, less than 10μA
- LOW THRESHOLD, less than 0.8V
- HIGH THRESHOLD, greater than 2.4V
- MAX. HIGH VOLTAGE, 11V
- Pulse input, High to low pulse with a duration between 200nSEC and 2μSEC.
- Trigger on Low to High transition.

Connections
RTCINL - CONN J1 PIN 9, or Wire Wrap Pin (see appendix E)
EXTTRIGL - CONN J2 PIN 19, or Wire Wrap Pin (see appendix E)
A special wire is supplied with every DT2769 real time clock board to allow easy connection between the DT2769 output and the DT2760 series analog input board.
CHAPTER 8
CALIBRATION AND TESTING

8.1 Equipment and System Requirements

In order to assist the user in testing the operation of the DT2760 series interfaces, Data Translation has developed a comprehensive software diagnostic aid designated SP0023. This software is provided in either of the two media: Paper tape for minimum, paper tape based LSI-11 Systems, or Floppy Disks for more sophisticated RT-11 Systems. The system and test equipment requirements for this software are given below:

SP0023 - DT2762
     DT2764
SP0029 - DT2765

Sp0023/SP0029 System Requirements

Paper Tape:
KD11-F (LSI-11) processor, ECO #10 or greater
or
KD11-HA (LSI-11/2) processor
Minimum of 4K words RAM
Serial Interface at Standard DEC console address
Paper tape reader
Data Translation DT2760 series interface.

Floppy Disk
KD11-F (LSI-11) processor, ECO #10 or greater
or
KD11-HA (LSI-11/2) processor
Minimum of 8K words RAM
System console terminal at standard DEC console address
DEC compatible dual floppy disc drive system
RT-11 operating system (Version 2 or Version 3)
Data Translation DT2760 series interface

Test Equipment Requirements

10MHz or greater bandwidth oscilloscope
Laboratory quality voltage standard.

8.2 Loading SP0023/SP0029 from Paper Tape

This software is supplied in PDP-11 absolute loader format. To load this release into memory the following steps must be taken:

1. Load the LSI-11 absolute loader (see DEC documentation for information on this.)
2. Place the paper tape in the paper tape reader.
3. Start the absolute loader at location XXX500 where XXX is determined by the following table: (See 8-2)
8.2 Loading SP0023/SP0029 from Paper Tape

(Cont.)

<table>
<thead>
<tr>
<th>SYSTEM MEMORY SIZE</th>
<th>XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>4K</td>
<td>017</td>
</tr>
<tr>
<td>8K</td>
<td>037</td>
</tr>
<tr>
<td>12K</td>
<td>057</td>
</tr>
<tr>
<td>16K</td>
<td>077</td>
</tr>
<tr>
<td>20K</td>
<td>017</td>
</tr>
<tr>
<td>24K</td>
<td>137</td>
</tr>
<tr>
<td>28K or greater</td>
<td>157</td>
</tr>
</tbody>
</table>

Following this procedure will cause SP0023 to be loaded into memory and executed.

8.2.1 Loading Floppy Disk

The SP0023 on SP0029 diskette contain an RT-11 memory image file called SP0023.SAV. This is a linked and executable version of SP0023. To load and execute SP0023 the user should boot up RT-11 in the usual way with the system disk in drive 0. When RT-11 comes up the user should insert the SP0023 disk into drive 1 and type the following command string to the RT-11 monitor:

```
.RUN DX1:SP0023 (Return)
```

This will cause SP0023 to be loaded and executed, at this time the SP0023 monitor will have control of the system and RT-11 will be prevented from interfacing.

8.3 Using SP0023/SP0029

SP0023/SP0029 is a stand-alone software diagnostic package that allows the user to test Data Translation's dual-height series of LSI-11 interface cards. The test program does not need RT-11 once it has been loaded and in fact it flushes RT-11 from the system after it has loaded. To allow the user to control the testing procedure a monitor has been included that interfaces to the user. When SP0023/SP0029 is brought up this monitor is automatically entered. On start up the resident monitor prints out the directory of the various Data Translation interface boards that can be tested followed by the monitor prompt character ">`" (a right angle-bracket). At this point the user should set the desired model number to be tested using the MODEL command, for example:

```
>`Model (Space) DT2762 (Return)
```

would set up the program to test the DT2762 Analog Input Board. The monitor would then invoke all the necessary initialization routines to test this board and confirm the board model by printing out a confirmation message followed by the default base and vector addresses that will be used. These base and vector addresses have
been preset at the factory and need not be changed. If for 
.some reason however a change in the base or vector address 
is required the user can modify locations 542 (base address) 
and 544 (vector address) to the new address. In order to easily 
facilitate this change the SP0023/SP0029 monitor also has some subset 
capabilities of ODT. In particular the user can use the slash 
and back-slash characters to open and modify memory locations 
just as in ODT. Therefore if the user needs to change any location 
he should type the address followed by a slash (/) or back-slash (\), 
the monitor will then open that location just as in ODT. The user 
can roll up or down sequentially in memory by using the line feed 
or carat (^) keys. The SP0023/SP0029 monitor is reentered from the ODT 
mode by typing a carriage return. Like ODT a memory location will 
only be modified if a valid octal number is typed before any of 
the ODT terminator characters. For example, to change the base and 
vector address of the DT2762 tests one would type:

```
>542/17700 170400 (line-feed)
 000544/000300 400 (return)
> 
```
to change the base address to 170400 and vector address to 400. 
Note that this change is only temporary and the default addresses 
will be reloaded if the model number is retyped or if SP0023 is 
reloaded. In addition to these commands the SP0023 test executive 
allows the user to ask for the model directory, to start 
tests, to loop or halt on tests or even to reboot RT-11. The 
commands available to the user under the SP0023 test executive 
are listed on the following page.

Example: User wants to run a scope loop on Test 2 because an 
error is encountered. Type:

```
>IL TEST(Space) 2
```

In this case the program will loop on Test 2 and inhibit error 
printouts.

If a test is run and no errors occur the test will return to 
the SP0023 command level without any other messages. If however, 
an error does occur then the test will print out the test number 
and error code. The user may look up the meaning of each error 
code in the program listings given in Appendix A.

8.4 Test Descriptions

All descriptions of the tests and the set up requirements needed 
for any particular test are described in detail in the program 
listings at the beginning of each test.
8.5 SP0023/SP0029 Program Description

SP0023/SP0029 consists of two groups of tests. The first group contains
a series of tests which test all the logic of the interface board.
These tests contain scope loops for debug purposes and will provide
an error message if a problem exists. The second set of tests test
the analog operation and calibration of the boards.

A listing of all the tests for testing DT2760 series boards can
be found at the beginning of the program listings.

Note that the user can run all the logic tests by using the
monitor ALL command. Calibration tests, however, must be run
individually.

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALL</td>
<td>Runs all logic tests that are present for current device. Generates an error if there is no current device.</td>
</tr>
<tr>
<td>BOOT</td>
<td>Jumps to the standard hardware bootstrap (173000). Generates an error if there is no bootstrap present.</td>
</tr>
<tr>
<td>DIRECTORY</td>
<td>Displays the contents of the current directory.</td>
</tr>
<tr>
<td>EXIT</td>
<td>Halts the processor</td>
</tr>
<tr>
<td>MODEL</td>
<td>Displays the parameters associated with the current device. Generates an error if there is no current device.</td>
</tr>
<tr>
<td>MODEL (space) DTXXX</td>
<td>Searches the current directory for the given model number. If found, makes that model the current device. Generates an error if there is no current directory or if the model number cannot be found.</td>
</tr>
<tr>
<td>TEST</td>
<td>Runs the last test executed.</td>
</tr>
<tr>
<td>TEST (space) &lt;octal&gt;</td>
<td>Runs the indicated test</td>
</tr>
</tbody>
</table>

Test Command prefixes - The following command prefixes are to be used with the TEST command to control the execution of the various tests.
COMMAND PREFIXES TO TEST EXECUTION COMMANDS

R  (TEST command only)       repeat this test continuously
L  (both TEST and ALL)       loop on this test if an error
                               is detected.
H  (both TEST and ALL)       halt test stream if an error
                               is detected.
I  (both TEST and ALL)       inhibit error printout

A control-C will terminate any test.

Example: User wants to run a scope loop on Test 2 because an error is encountered. Type:

ILTEST (space) 2

In this case the program will loop on test 2 and inhibit error printouts.

SP0023/SP0029 Error Codes - SP0023/SP0029 will print an error code when a specific error is encountered. All codes are in the program listing and show the error and what test the program was in when a failure occurred. Use the table of contents printed at the front of the listing to quickly find the pages in the listing associated with the test that generates the error.

8.6  SP0023 Tests

Logic Tests

| TEST 10: A/D CALIBRATION | TEST 11: A/D INPUT CHANNEL SCAN | TEST 12: A/D INPUT GAIN/CHANNEL SCAN |

SP0029 TESTS

| TEST 10: A/D INPUT CHANNEL SCAN | TEST 11: A/D INPUT GAIN/CHANNEL SCAN |

8.6.1 Test Description

All description of tests are located in the program listing at the beginning of each test.

8.6.2 Modes of Operation

Test 10, 11 and 12 will ask for a MODE input when they are called. This MODE input is the lower byte of the CSR.
8.6.2 When a user wants to run an interface under RTC control or 
(Cont.) EXT TRIG he can set these bits when the program asks for MODES. 
If a user wants to run under EXT TRIG he will set the MODES 
as 208.

```
  7 6 5 4 3 2 1 0
RTC EN GSI G50
```

MODE BITS FOR USE IN TEST 10, 11 AND 12.

8.6.3 Calibration

Calibration of the system requires a voltage standard for highly 
accurate analog inputs and a DVM for calibration of analog 
inputs.

Equipment Required:

Voltage standard - EDC Model MV-100 or equivalent 
- Data Technology Model 40 or equivalent.

8.6.3.1 Calibration of Analog Inputs

Configuration ±10V FS, 2's complement notation:

1. Connect a Voltage Standard to CH0 input
2. Set standard to -2.4mV
3. Start A/D Calibration test at CH0, Mode 0.
4. Adjust A/D offset for the printout between 177777 and 000000
5. Set voltage standard to +9.9927V
6. Adjust A/D range control for printout between 003776 and 003777

NOTE: For ±10mV systems (DT2765, DT2764) divide above voltage values 
by 1000. (Octal values remain the same.)

8.6.3.2 Calibration of Analog Inputs with Programmable Gain Amplifier

1. Adjust the A/D offset and range as in section 8.4.3.1
2. Set voltage standard to -600mV
3. Start A/D Calibration Test at CH0 Mode 148
4. Adjust the Programmable gain offset pot for a printout 
between 177777 and 000000

For other ranges please see 8.0 Adjustment Values.
8.7 Adjustment Values

8.7.1 Notes on Full Scale (FS)

Full Scale (FS) is the amount of input voltage required to turn on all the bits of the A/D converter. For a D/A converter, the inverse is true: Full Scale is the voltage that results when all bits of the converter are turned on.

In a 12 bit converter there are 4096 possible states ($2^{12}$). Because one of these states is given to zero, the converter lacks one state at its high or positive FS end. Hence even though the converter is rated at 10 volts Full Scale, the positive Full Scale value will actually be 1 state (1 least significant bit value) below 10 volts. For example, a 0-10 volt range converter has a least significant bit value of 2.44 mV (10 volts / 4096 states). The positive Full Scale will be reached at 10 volts -2.44 mV or 9.99756 volts. The negative full scale (in this instance taken to mean the voltage associated with all converter bits OFF) will be 0 volts.

The Full Scale Range is the difference in voltage between positive Full Scale (all converter bits ON) and negative full scale (all converter bits OFF). Thus a 0-10 volt converter has a Full Scale Range of 10 volts while a ±10 volt converter has a FSR of 20 volts.

8.7.2 Computing Calibration Values

(Note: LSB (least significant bit) = FSR ÷ 4096

8.7.3 A/D Offset Adjustment Values

<table>
<thead>
<tr>
<th>Unipolar Ranges</th>
<th>0-n Volts, n ≤ 10</th>
<th>Adjust for Printout Between</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Range</td>
<td>Input Voltage</td>
<td>Low Value</td>
</tr>
<tr>
<td>any</td>
<td>+½LSB</td>
<td>0</td>
</tr>
<tr>
<td>any, Octal output</td>
<td>+½LSB</td>
<td>0000</td>
</tr>
<tr>
<td>0-10</td>
<td>+1.2207mV</td>
<td>0000</td>
</tr>
<tr>
<td>0-5V</td>
<td>+0.6104mV</td>
<td>0000</td>
</tr>
<tr>
<td>0-10mV</td>
<td>+1.220mV</td>
<td>0000</td>
</tr>
</tbody>
</table>
### Bipolar Ranges

<table>
<thead>
<tr>
<th>Input Range</th>
<th>Input Voltage</th>
<th>Low Value</th>
<th>High Value</th>
<th>Adjust for Printout Between</th>
</tr>
</thead>
<tbody>
<tr>
<td>any, OCTAL output</td>
<td>Φ volts -½ LSB</td>
<td>Φ volts -1 LSB</td>
<td>Φ volts</td>
<td></td>
</tr>
<tr>
<td>±10V</td>
<td>-2.4414mV</td>
<td>177777</td>
<td>000000 (two's complement)</td>
<td></td>
</tr>
<tr>
<td>±5V</td>
<td>-1.2207mV</td>
<td>008777</td>
<td>004000 (offset binary)</td>
<td></td>
</tr>
<tr>
<td>±10mV</td>
<td>-2.4414μV</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Unipolar Ranges

<table>
<thead>
<tr>
<th>Input Range</th>
<th>Input Voltage</th>
<th>Low Value</th>
<th>High Value</th>
<th>Adjust for Printout Between</th>
</tr>
</thead>
<tbody>
<tr>
<td>any, OCTAL output</td>
<td>+FS-1½ LSB</td>
<td>+FS-2 LSB</td>
<td>+FS-1 LSB</td>
<td></td>
</tr>
<tr>
<td>±10</td>
<td>+9.9963V</td>
<td>007776</td>
<td>007777</td>
<td></td>
</tr>
<tr>
<td>±5V</td>
<td>+4.9982V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>±10mV</td>
<td>+9.9963mV</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Bipolar Ranges

<table>
<thead>
<tr>
<th>Input Range</th>
<th>Input Voltage</th>
<th>Low Value</th>
<th>High Value</th>
<th>Adjust for Printout Between</th>
</tr>
</thead>
<tbody>
<tr>
<td>any, OCTAL output</td>
<td>+FS - 1½ LSB</td>
<td>+FS - 2 LSB</td>
<td>+FS - 1 LSB</td>
<td></td>
</tr>
<tr>
<td>±10V</td>
<td>+9.9927</td>
<td>003776</td>
<td>003777 (two's complement)</td>
<td></td>
</tr>
<tr>
<td>±5V</td>
<td>+4.9964</td>
<td>007776</td>
<td>007777 (offset binary)</td>
<td></td>
</tr>
<tr>
<td>±10mV</td>
<td>+9.9927mV</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
APPENDIX A

4-20MA INPUT OPTIONS
THERMOCOUPLE

ANALOG INPUT

HI
LO

COPPER

MOUNTED ON OR NEAR BARRIER STRIP

LT5600 NATIONAL

COPPER/CONSTANTAN

ambiNTemperature Compensation Circuit

THERMOCOUPLE COLD JUNCTION Compensation Circuit

R = \left( \frac{10 \text{ mV/°C}}{\text{COMP}} - 1 \right) \times 100

50 \text{ mV/°C} 19.9K
40 \text{ mV/°C} 24.9K
40 \text{ mV/°C} 29.4K
A.1 4-20 mA Inputs are supplied on the DT2762 and DT2765 by ordering (4-20). This option is configured by Data Translation by adding precision 250 ohm resistor on the interface board. A modified data acquisition module is also utilized providing a 1 to 5V input - thus the user just supplies us current input and will receive full 12 bit resolution of his signal.

DT2762 (4-20)  -  8 Channels input
DT2765 (4-20)  -  4 channels input
<table>
<thead>
<tr>
<th>DT2765</th>
<th>DT2762</th>
<th>VIN(V)</th>
<th>IiN (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>7777</td>
<td>1.000</td>
<td>4.000</td>
</tr>
<tr>
<td>0001</td>
<td>7776</td>
<td>1.0010</td>
<td>4.004</td>
</tr>
<tr>
<td>0002</td>
<td>7775</td>
<td>1.0020</td>
<td>4.008</td>
</tr>
<tr>
<td>0004</td>
<td>7773</td>
<td>1.0039</td>
<td>4.015</td>
</tr>
<tr>
<td>0010</td>
<td>7767</td>
<td>1.0078</td>
<td>4.031</td>
</tr>
<tr>
<td>0020</td>
<td>7757</td>
<td>1.0156</td>
<td>4.062</td>
</tr>
<tr>
<td>0040</td>
<td>7737</td>
<td>1.0313</td>
<td>4.125</td>
</tr>
<tr>
<td>0100</td>
<td>7577</td>
<td>1.0625</td>
<td>4.250</td>
</tr>
<tr>
<td>0200</td>
<td>7577</td>
<td>1.1250</td>
<td>4.500</td>
</tr>
<tr>
<td>0400</td>
<td>7377</td>
<td>1.2500</td>
<td>5.000</td>
</tr>
<tr>
<td>1000</td>
<td>6777</td>
<td>1.5000</td>
<td>6.000</td>
</tr>
<tr>
<td>2000</td>
<td>5777</td>
<td>2.0000</td>
<td>8.000</td>
</tr>
<tr>
<td>4000</td>
<td>3777</td>
<td>3.0000</td>
<td>12.000</td>
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<tr>
<td>6000</td>
<td>1777</td>
<td>4.0000</td>
<td>16.000</td>
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<tr>
<td>7000</td>
<td>0777</td>
<td>4.5000</td>
<td>18.000</td>
</tr>
<tr>
<td>7400</td>
<td>0377</td>
<td>4.7500</td>
<td>19.000</td>
</tr>
<tr>
<td>7600</td>
<td>0177</td>
<td>4.8750</td>
<td>19.500</td>
</tr>
<tr>
<td>7700</td>
<td>0077</td>
<td>4.9375</td>
<td>19.750</td>
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<td>7740</td>
<td>0037</td>
<td>4.9688</td>
<td>19.875</td>
</tr>
<tr>
<td>7760</td>
<td>0017</td>
<td>4.9844</td>
<td>19.938</td>
</tr>
<tr>
<td>7770</td>
<td>0007</td>
<td>4.9922</td>
<td>19.969</td>
</tr>
<tr>
<td>7774</td>
<td>0003</td>
<td>4.9961</td>
<td>19.984</td>
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<tr>
<td>7776</td>
<td>0001</td>
<td>4.9980</td>
<td>19.992</td>
</tr>
<tr>
<td>7777</td>
<td>0000</td>
<td>4.9990</td>
<td>19.996</td>
</tr>
</tbody>
</table>
APPENDIX B

TEMPERATURE COMPENSATION CIRCUIT

FOR

DT2765-T
AMBIENT TEMPERATURE COMPENSATION CIRCUIT

When the thermocouple wire is connected to copper wire at the barrier strip an additional thermocouple is made with an output that would cancel the measurement thermocouple's output if the barrier strip was at the same temperature.

To compensate for this error a National Semiconductor LX5600 temperature transducer should be mounted on the center of the barrier strip or near the most critical thermocouple connection. The output at pin 1 as shown is -10 millivolts per degree Kelvin. Following this the amplifier is utilized to remove the -2.7 volt offset due to ambient temperature and reference the output to 0 millivolts for 0°C with +10 millivolts per + degree C and -10 millivolts per -degree C.

The millivolts per degree C can now be scaled by calculating the value of R to produce the correct compensation voltages for the thermocouple utilized. Note that once a thermocouple has been compensated it will remain compensated through the entire gain range with the PG option. (PG = programmable gain).

To calibrate the system place the thermocouple in a beaker of crushed ice and adjust the 20K ohm potentiometer for zero volts out of the system. Now transfer the thermocouple into a known high temperature medium and adjust the fullscale scale of the DT5703-T for the appropriate reading.
APPENDIX C
SP-0023 PROGRAM LISTINGS
SP-0029 PROGRAM LISTINGS
1-  9  GENERAL INFORMATION
2-  1  LIST OF CHANGES
3-  1  TEST PARAMETER BLOCK (TPB)
4-  1  INITIALIZATION
5- 25  DISPLAY PARAMETERS
6-  1  ERROR REPORTERS
7-  1  MODEL TESTING INFORMATION
8-  1  LOGIC TESTS
9-  2  TEST 1: BRPLY FROM ALL REGISTERS
 10- 1  TEST 2: CHECK ADCSR BITS
 11- 1  TEST 3: BINITL ACTION
 12- 1  TEST 4: BYTE OPERATION OF ADCSR
 13- 1  TEST 5: A/D DONE BIT AND INTERRUPT
 14- 1  TEST 6: ERROR BIT AND INTERRUPT
 15- 1  TEST 7: END OF LOGIC TESTS
16- 14  CALIBRATION INITIALIZATION
17-  1  DISPLAY A/D DATA
18- 20  TEST 10: A/D CALIBRATION
 19- 1  TEST 11: A/D INPUT CHANNEL SCAN
 20- 1  TEST 12: A/D INPUT GAIN/CHANNEL SCAN
SETTL  GENERAL INFORMATION

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DIGITAL INTERFACE BOARDS.

VERSION V03-01

EDWIN KROEKER 6-JAN-79
PHILLIP MARTINEZ 17-AUG-79

THIS PROGRAM MODULE CONTAINS ROUTINES TO TEST AND
CALIBRATE DTI DT2760 SERIES ANALOG INTERFACE SYSTEMS
FOR THE LSI-11. A COMPLETE LISTING OF THE MODELS
TESTED BY THIS CODE MODULE WILL BE FOUND ON THE
FOLLOWING PAGES. THIS MODULE IS DESIGNED TO OPERATE
UNDER TST-11 SUPERVISION.
DESCRIPTION OF CHANGES:

THE DIFFERENCES BETWEEN V02-01 AND V03-01 ARE:

1). THE 2765 BOARD TESTS HAVE BEEN TAKEN OUT

2). TEST 10 HAS BEEN CHANGED TO ALLOW ODD MUX
   ADDRESSES

3). THE TEST NOW COMPUTES ITS OWN TIME DELAY
   FOR DIFFERENT SPEED MODULES

.LIST BIN
SBTTL TEST PARAMETER BLOCK (TPB)

; TEST-11 DECLARATION

; MCALL TST11
TST11

; ADDITIONAL PARAMETERS USED BY THIS DIAGNOSTIC

000546 DELAY =546 ; A/D DELAY COUNT STORAGE

000522 ERRCNT =522 ; ERROR COUNTER

; TEST PARAMETER BLOCK

; NLIST BIN

000000 TPB: .WORD PARAM ; ADDRESS OF PARAMETER

000002 .BYTE 377 ; PRINT-OUT ROUTINE

000003 .BYTE 12 ; # OF TESTS

; TEST ADDRESS TABLE FOR USE BY TST-11

000004 .WORD TEST1,PR7

000010 .WORD TEST2,PR7

000014 .WORD TEST3,PR7

000020 .WORD TEST4,PR7

000024 .WORD TEST5,PR7

000030 .WORD TEST6,PR7

000034 .WORD TEST7,PR7

000040 .WORD TEST10,0

000044 .WORD TEST11,0

000050 .WORD TEST12,0

; LIST BIN
```
1 5760 TST-11 MODULE  MACRO V03.0E  31-AUG-79 03:27:32 PAGE 4

2
3 000054 005037  INIT62: CLR  @#SWR  ; INPUT ONLY MODEL.
   000540
4 000060 012727  MOV  @400, @#DELAY  ; SET DELAY CONSTANT
   000620  000546
5 000066 000406  BR  INIT  ; GO TO COMMON INIT.
6
7 000070 012727  INIT64: MOV  @BIT4, @#SWR  ; LOW LEVEL INPUT ONLY
   000620  000540
8 000076 012727  MOV  @800, @#DELAY  ; SET LOW LEVEL DELAY
   000620  000546
9
10
11 000104  INIT: PRINT  <# OF A/D INPUT CHANNELS (IN OCTAL): >
12 000154  GETOCT  ; GET OCTAL INPUT
13 000166 103352  BCC  INIT  ; NO CR - ASK AGAIN
14 000160 105737  TSTB  @#ODTACC  ; ZERO?
15 000164 001747  BEO  INIT  ; ASK AGAIN
16 000166 113737  MOV  @#ODTACC, @#SWR+1
17 000174 012737  MOV  @177000, @#BASE  ; SET DEFAULT ADDRESS
   177000  000542
18 000202 012737  MOV  @130, @#VECTOR  ; SET DEFAULT VECTOR
   000130  000544
19 000210 000207  RETURN  ; ALL DONE
```
T2760   TST-11 MODULE    MACRO V03.0B    31-AUG-79 03:27:32 PAGE 5

INITIALIZATION

1 0000212 QUERY: PUSH R1 ; SAVE POINTER
2 0000214 PRINTS ; PRINT PROMPT
3 0000216 PRINT < (Y OR N)? >
4 0000234 TTYIN
5 0000236 127200 CMPB #"Y", R0 ; A "Y"?
   000131
6 0000242 001427 BEO 2$ ;
7 0000244 127200 CMPB #"N", R0 ; A "N"?
   000116
8 0000250 001422 BEO 1$ ; YES
9 0000252 CRLF
10 0000254 PRINTC <SEE MANUAL FOR ASSISTANCE>
11 0000312 POP R1 ; RESTORE POINTER
12 0000314 000736 BR QUERY
13
14 0000316 000261 1$: SEC ; SET CARRY FLAG
15 0000320 000401 BR 3$ ;
16 0000322 000241 2$: CLC ; CLEAR CARRY FLAG
17 0000324 3$: TTYOUT ; ECHO CHARACTER
18 0000326 CRLF
19 0000330 POP R1 ; RESTORE R1
20 0000332 000207 RETURN

;SBTL DISPLAY PARAMETERS

; THIS ROUTINE DISPLAYS THE CURRENT SETTING
; OF 'BASE' AND 'VECTOR' ON THE TERMINAL.

31 0000334 PARAM: PRINT < BASE ADDRESS = >
32 0000360 013700 MOV @#BASE,R0 ; GET BASE ADDRESS
   000542
33 0000364 OCT16 ; DISPLAY
34 0000366 CRLF
35 0000370 PRINT <VECTOR ADDRESS = >
36 0000414 013700 MOV @#VECTOR,R0 ; GET VECTOR ADDRESS
   000544
37 0000420 OCT16 ; DISPLAY
38 0000422 CRLF
39 0000424 000207 RETURN ; ALL DONE
.SBTTL  ERROR REPORTERS

; THIS ROUTINE PROVIDES ERROR REPORTING FOR BUS
; TIME-OUT ERRORS (NO BRPLY FROM INTERFACE).

000426  MOV R1, R0
000428  OCT16 ; DISPLAY ADDRESS
00042A  CRLF
00042C  RETURN ; DONE

; THIS ROUTINE PROVIDES ERROR REPORTING FOR REGISTER
; BIT ERRORS (ONE OR MORE INCORRECT BITS IN A REGISTER)

000502  PRINTC <REGISTER ERROR>
000504  PRINT <ADDRESS: >
000506  PUSH R0 ; SAVE R0
000508  MOV R1, R0 ; GET ADDRESS
00050A  OCT16
00050C  CRLF
00050E  PRINT <EXPECTED: >
000510  MOV R2, R0 ; GET EXPECTED VALUE
000512  OCT16 ; DISPLAY
000514  CRLF
000516  PRINT <FOUND:  >
000518  MOV (SP), R0 ; GET BAD BITS
00051A  XOR R2, R0 ; GENERATE SNAPSHOT
00051C  OCT16 ; DISPLAY
00051E  CRLF ; FORMATTING
000520  PRINT <BITS: >
000522  POP R0 ; GET ERROR BITS
000524  OCT16 ; DISPLAY
000526  CRLF
000528  RETURN ; DONE
; THIS CODE MODULE CONTAINS THE ROUTINES NECESSARY
; TO TEST THE FOLLOWING DT1 INTERFACE MODELS:

DT2762 : HIGH LEVEL ANALOG INPUT

I2762  == INIT62
T2762  == TPB

DT2764 : LOW LEVEL ANALOG INPUT

I2764  == INIT64
T2764  == TPB

; SOFTWARE SWITCH REGISTER BIT RESERVATIONS

; BITS 13-8:  # OF A/D CHANNELS
; BIT 6-5:    UNUSED
; BIT 4:      DT5702 A/D MODULE PRESENT
; BIT 3:      UNUSED
; BITS 2-0:   RESERVED
SBTTL LOGIC TESTS
SBTTL TEST 1: BRPLY FROM ALL REGISTERS

; THIS TEST VERIFIES THAT THE INTERFACE SYSTEM RESPONDS
; WITH A BUS REPLY SIGNAL DURING A BUS DATIO BUS CYCLE
; ALL REGISTERS AVAILABLE ON THE BOARD ARE CHECKED

TEST1: MOV SP, R2 ; SAVE SP
RELMOV #3$, R0 ; SET UP TRAP TO 4
MOV R0, @#4

MOV @#BASE, R1 ; GET ADDRESS

SCOPE ; DECLARE LOOP POINT
CLR <R1> ; DATIO BUS CYCLE
ADD #2, R1 ; NEXT REGISTER

SCOPE ; DECLARE LOOP POINT
CLR <R1> ; DATIO BUS CYCLE
EXIT

; ***************************************************
; ERROR CODE 1 - BUS TIMEOUT

; ***************************************************

MOV <SP>, R3 ; GET OFFENDING PC
MOV R2, SP ; RESTORE STACK
ERROR 1, NORPLY ; REPORT ERROR
JMP <R3> ; CONTINUE TEST
; SBTTL TEST 2: CHECK ADCSR BITS
; THIS TEST CHECKS MOST OF THE BITS IN ADCSR.
; BITS ARE CHECKED FOR BOTH SET AND RESET CAPABILITY.
; BITS THAT ARE NOT CHECKED ARE THE A/D DONE BIT
; AND THE ERROR BIT (BOTH CHECKED IN OTHER TESTS).

; TEST2: MOV @#BASE, R1 ; GET ADDRESS
;        CLR R2          ; INIT TEST REG
;        MOV #40, R3     ; SET # OF STATES

; SCOPE
; MOV R2, (R1) ; DECLARE LOOP POINT
; MOV (R1), R0 ; SET BITS
; BIC #177600, R0 ; GET BITS
; XOR R2, R0 ; IGNORE HIGH BYTE
; BEQ 2$ ; TEST BITS
; NO ERROR - SKIP

; ERROR CODE 2 - BIT ERROR, ADCSR
; BITS 0-6

; ERROR 2, REG ; REPORT ERROR
; ADD #4, R2 , ; NEXT STATE
; SUB R3, 1$ ; LOOP UNTIL DONE
; CLR R2 ; INIT TEST REG.
; MOV #200, R3 ; SET # OF STATES

; SCOPE
; MOV R2, (R1) ; DECLARE LOOP POINT
; MOV (R1), R0 ; SET BITS
; BIC #100377, R0 ; GET BITS
; XOR R2, R0 ; IGNORE LOW BYTE
; BEQ 5$ ; TEST BITS
; NO ERROR - SKIP

; ERROR CODE 3 - BIT ERROR, ADCSR
; BITS 8-14

; ERROR 3, REG ; REPORT ERROR
; ADD #400, R2 ; NEXT STATE
; SUB R3, 4$ ; LOOP UNTIL DONE

; EXIT
.SBTTL TEST 3: BINITL ACTION

; THIS TEST VERIFIES THAT THE BINITL SIGNAL-clears
; THE PROPER ADCSR BITS.

TEST3: MOV @#BASE, R1 ; GET ADDRESS
       MOV #40101, (R1) ; SET BITS
       MOV @#DELAY, R0 ; WAIT FOR A/D DONE
       SUB R0, .2$ ; SET ERROR BIT
       CLR R2 ; CLR TEST REG.
       SCOPE ; DECLARE LOOP POINT
       RESET ; ISSUE BINITL
       MOV (R1), R0 ; GET BITS
       BIC #37476, R0 ; IGNORE SOME BITS
       XOR R2, R0 ; TEST BITS
       BEQ 3$ ; OK - SKIP ERROR

; ************************************************************
; ERROR CODE 4 - PROPER BIT(S) NOT CLEARED
; BY BINITL
; ************************************************************

ERROR 4, REG ; REPORT ERROR

3$: EXIT ; ALL DONE
.SETTL TEST 4: BYTE OPERATION OF ADCSR

; THIS TEST VERIFIES HIGH AND LOW BYTE OPERATIONS
; INVOLVING THE ADCSR.

7 001062 013701 TEST4: MOV @#BASE.R1 ; GET ADDRESS
    000542
8 001066 005011 CLR (R1) ; CLEAR ADCSR
9 001070 005002 CLR R2 ; INIT. TEST REGISTER
10 001072 SCOPE
11 001074 112711 MOVb #-1,(R1) ; SET R/W BITS
    177777
12 001100 001100 MOV (R1),R0 ; GET ADCSR AS WORD
13 001102 042700 BIC #100377,R0 ; IGNORE LOW BYTE
    100377
14 001106 074200 XOR R2,R0 ; TEST BITS
15 001110 001402 BEQ 1$ ; OK - SKIP ERROR

; ERROR CODE 5 - HIGH BYTE LOADED DURING
; A LOW BYTE OPERATION

24 001112 005011 1$: CLR (R1) ; CLEAR ADCSR
25 001116 005002 CLR R2 ; INIT. TEST REGISTER
26 001122 005201 INC R1 ; POINT TO HIGH BYTE
27 001124 SCOPE
28 001126 112711 MOVb #-1,(R1) ; SET R/W BITS
    177777
29 01132 016100 MOV -1(R1),R0 ; GET ADCSR AS WORD
    177777
30 001136 042700 BIC #177600,R0 ; IGNORE HIGH BYTE
    177600
31 001142 074200 XOR R2,R0 ; TEST BITS
32 001144 001402 BEQ 2$ ; OK - SKIP ERROR

; ERROR CODE 6 - LOW BYTE LOADED DURING
; A HIGH BYTE OPERATION

36 38 001146 ERROR 6,REG ; REPORT ERROR
40 41 001152 2$: EXIT
TST-11 MODULE MACRO V03.0B 31-AUG-79 03:27:32 PAGE 12

5: A/D DONE BIT AND INTERRUPT

1 SBTTL TEST 5: A/D DONE BIT AND INTERRUPT

; THIS TEST VERIFIES THAT THE A/D DONE BIT CAN
; BE SET PROPERLY AND THAT THE INT ENB BIT
; FUNCTIONS PROPERLY.

8 001154 013701 TEST5: MOV @#BASE,R1 ; GET ADDRESS

9 001160 013702 MOV @#VECTOR,R2 ; GET VECTOR ADDRESS

10 001164 005761 TST 2(R1) ; CLEAR A/D DONE BIT

11 001170 005011 CLR (R1) ; CLEAR ADCSR

12 001172 SCOPE (R1) ; DECLARE LOOP POINT

13 001174 105211 INCB (R1) ; SET A/D DONE BIT

14 001176 013700 MOV @#DELAY,R0 ; WAIT FOR A/D DONF

15 001202 077001 1$: SOB R0,1$ ; IS BIT SET?

16 001204 105711 TSTB (R1) ; YES - SKIP ERROR

17 001206 100402 BMI 2$ ; ERROR CODE 7 - A/D DONE BIT NOT SET

; ERROR CODE 7 - A/D DONE BIT NOT SET

18 001210 ERROR 7 ; REPORT ERROR

19 001212 000460 BR 8$ ; CAN'T CONTINUE

20 001214 2$ ; SCOPE 8$ ; DECLARE LOOP POINT

21 001216 005761 TST 2(R1) ; READ ADDBR

22 001222 105711 TSTB (R1) ; DONE BIT CLEAR?

23 001224 100002 BPL 3$ ; YES - SKIP ERROR

24 001226 100002 ; ERROR CODE 10 - A/D DONE BIT NOT CLEARED

; ERROR CODE 10 - A/D DONE BIT NOT CLEARED

; AFTER A/D DATA WAS READ

34 001230 000451 ERROR 10 ; REPORT ERROR

35 001232 000460 BR 8$ ; CAN'T CONTINUE
1 001232 005003 3$: CLR R3 ; PREPARE STATUS WORDS
2 001234 012704 MOV #PR7,R4
3 001240 000340
4 001246 010012 RELMOV #5$,R0 ; GET ISR ADDRESS
5 001250 010462 MOV R0,(R2) ; STORE
6 001254 000002 MOV R4,2(R2) ; STORE STATUS TOO
7 001256 105211 SCOPE \(R1\) ; DECLARE LOOP POINT
8 001260 013700 INC\(B\) (R1) ; SET A/D DONE
9 001264 000546 MOV @#DELAY,R0 ; WAIT FOR DONE
10 001266 077001 4$: SOB R0,4$ ; ENABLE INTERRUPTS
11 001272 106403 BIS #100,(R1) ; ENABLE CPU INTERRUPTS
12 001274 000100 MPS R3 ;STALL TIME
13 001276 106404 MPS R4 ; TURN OFF CPU

;******************************************************************************
; ERROR CODE 11 - NO INTERRUPT ON A/D DONE
;******************************************************************************
21 001300 000424 ERROR 11 ; REPORT ERROR
22 001302 00424 BR 8$ ; CAN'T CONTINUE
23 ;
24 001304 062706 5$: ADD #4,SP ; ADJUST STACK
25 001310 000004 000004
26 001312 005761 SCOPE \(R1\) ; DECLARE LOOP POINT
27 001316 105711 TST \(R1\) ; READ ADBBR
28 001320 100002 TSTB \(R1\) ; A/D DONE CLEAR?
29 ;
30 ;******************************************************************************
; ERROR CODE 12 - A/D DONE BIT NOT CLEARED
; AFTER A/D DATA WAS READ
;******************************************************************************
31 32 ;
33 34 ;
35 36 ;
37 001322 ERROR 12 ; REPORT ERROR
38 001324 000413 BR 8$ ; CAN'T CONTINUE
D:\760 \TST-11 MODUO MACRO V03.0B 31-AUG-79 03:27:32 PAGE 14

1 001326
2 001330 005761
     000002
3 001334 005011
4 001336 005211
5 001340 013700
     000546
6 001344 077001
7 001346 005711
8 001350 100001
9  
10 6$: SCOPE
11 TST 2(R1)
12 ; DECLARE LOOP POINT
13 ; CLEAR DONE
14 7$: CLR (R1)
15 INC (R1)
16 MOV @#DELAY, R0
17 ; CLEAR ADCSR
18 ; START CONVERSION
19 ; WAIT -
20 8$: SOF R0, 7$
21 TST (R1)
22 ; ERROR BIT SET?
23 ; NO - EXIT
24  
25 9$: ; ERROR CODE 13 - ERROR BIT SET AFTER NORMAL
26 ; A/D TRIGGERING SEQUENCE
27  10$: ERROR 13
28 ; REPORT ERROR
29 11$: CLR (R1)
30 12$: CLR R0
31 ; INITIALIZE COUNTER
32 13$: INC (R1)
33 ; START CONVERSION
34 14$: INC R0
35 ; BUMP COUNTER
36 15$: TSTB (R1)
37 ; WAIT FOR DONE
38 16$: BPL 9$
39 17$: ASL R0
40 ; FORM NEW DELAY
41 18$: ASL R0
42 19$: ASL R0
43 20$: MOV R0, @#DELAY
44 ; STORE NEW DELAY
45 21$: TST 2(R1)
46 ; CLEAR DONE
47 22$: CLR (R1)
48 ; EXIT
49 23$:
.SB TTL TEST 6: ERROR BIT AND INTERRUPT

; THIS TEST VERIFIES THAT THE ERROR BIT CAN BE SET
; PROPERLY AND THAT THE ERR INT ENB BIT FUNCTIONS
; CORRECTLY.

; TEST 6:
MOV @#BASE, R1       ; GET ADDRESS

MOV @#VECTOR, R2    ; GET VECTOR ADDRESS

ADD #4, R2          ; ADJUST VECTOR

TST 2(R1)            ; CLEAR A/D DONE BIT

SCOPE                ; DECLARE LOOP POINT
CLR (R1)             ; CLEAR ADCSR
TST (R1)             ; ERROR CLEAR?
BPL 1$                ; YES - SKIP ERROR

; ERROR CODE 14 - ERROR BIT NOT CLEAR

; ERROR CODE 15 - ERROR BIT NOT SET

ERROR 14             ; REPORT ERROR
BR 5$                 ; CAN'T CONTINUE

1$: SCOPE             ; DECLARE LOOP POINT
INCB (R1)             ; SET A/D DONE BIT
MOV @#DELAY, R0      ; WAIT FOR A/D DONE

2$: SOB R0, 2$         ; SET ERROR BIT
INCB (R1)             ; IS BIT SET?
TST (R1)              ; YES - SKIP ERROR

3$                      ;

ERROR 15             ; REPORT ERROR
BR 5$                 ; CAN'T CONTINUE
1 001476 005003 3$: CLR R3 ; PREPARE STATUS WORDS
2 001500 012704 MOV #PR7, R4
000340
3 001504 RELMOV #4$, R0 ; GET ISR ADDRESS
4 001512 010012 MOV R0, (R2) ; STORE
5 001514 010462 MOV R4, 2(R2) ; STORE STATUS TOO
000002
6 001520 SCOPE
7 001522 052711 BIS #40000,(R1) ; DECLARE LOOP POINT
040000 ; ENABLE INTERRUPTS
8 001526 106403 MTPS R3 ; ENABLE CPU INTERRUPTS
9 001530 000240 NOP ; STALL TIME
10 001532 106404 MTPS R4 ; TURN OFF CPU
11
12 ;******************************************************************************
13 ; ERROR CODE 16 - NO INTERRUPT ON ERROR
14 ;******************************************************************************
15 16 001534 ERROR 16 ; REPORT ERROR
19 001536 000407 BR 5$ ; CAN'T CONTINUE
20 ;
21 001540 062706 ADD #4, SP ; ADJUST STACK
000004
22 001544 SCOPE
23 001546 005011 CLR (R1) ; DECLARE LOOP POINT
24 001550 005711 TST (R1) ; CLEAR ERROR BIT
25 001552 100001 BPL 5$ ; CHECK BIT
26 ; CLEAR - SKIP ERROR
27
28 ;******************************************************************************
29 ; ERROR CODE 17 - ERROR BIT NOT CLEAR
30 ;******************************************************************************
31 32 001554 ERROR 17 ; REPORT ERROR
34 35 001556 005761 5$: TST 2(R1) ; CLEAR DONE
000002
36 001562 005011 CLR (R1) ; CLEAR ADCSR
37 001564 EXIT
; TEST 7: END OF LOGIC TESTS

; THIS TEST IS PRESENT TO INFORM THE TST-11 MONITOR
; THAT THERE ARE NO MORE ADDITIONAL LOGIC TESTS
; TO BE EXECUTED WHEN THE "ALL" COMMAND IS USED.
; THIS TEST WILL FORCE A RETURN TO THE COMMAND
; LEVEL OF TST-11 WHEN THE TEST SEQUENCER REACHES
; THIS TEST.

; TEST7: ESCAPE

; SBTTL CALIBRATION INITIALIZATION

; THIS ROUTINE PERFORMS INITIALIZATION FUNCTIONS
; FOR SOME OF THE CALIBRATION TESTS.

20 001570 GETCH: PRINT <CHANNEL? > ; OUTPUT PROMPT
21 001604 GETOCT ; GET VALUE
22 001606 103422 BCS 1$ ; CR AT END - CONT.
23 001610 PRINTC <ENTER AN OCTAL CHANNEL ADDRESS. >
24 001652 000746 BR GETCH ; TRY AGAIN
25
26 001654 013701 1$: MOV @#BASE, R1 ; GET ADDRESS
27 001660 013702 000542
28 001664 000302 MOV @#ODTACC, R2 ; GET VALUE
29 001666 2$: SWAP R2 ; ADJUST
30 001704 GETOCT ; GET VALUE
31 001706 103420 BCS 3$ ; CR AT END - CONT.
32 001710 PRINTC <ENTER AN OCTAL BYTE VALUE. >
33 001746 000747 BR 2$;
34
35 001750 042702 3$: BIC #377, R2 ; CLEAR LOW BYTE, R2
36 001754 013700 000377 MOV @#ODTACC, R0 ; GET VALUE
37 001760 042700 000514 BIC #177400, R0 ; CLEAR HIGH BYTE, R0
38 001764 177400 ADD R0, R2 ; ADD IN MODE BYTE
39 001766 05766 000002 TST 2(R1) ; CLEAR DONE
40 001772 005011 CLR (R1) ; CLEAR BOARD
41 001774 000207 RETURN
MACRO v03.06  31-aug-79 03:27:32 page 18

. SBTTL DISPLAY A/D DATA

; THIS ROUTINE TAKES THE DATA FROM ADDER AND DISPLAYS IT FOR THE USER AS A 16 BIT OCTAL VALUE.

6 001776 016100 DISPLY:  MOV    2(R1),R0 ; GET DATA
  000002
   OCT16   PRINT
   OCT16   (R1) ; ERROR BIT SET?
   BPL    1$ ; NO - RETURN
   MOVB  #E,R0 ; PRINT 'E'

11 002014 TTYOUT
12 002016 042711 BIC    #40000,(R1) ; CLEAR ERROR BIT
  040000
13 002022 005237 INC    @#ERRCNT ; INC. COUNT
  005222
14 002026 005737 TST    @#ERRCNT ; OVERFLOW?
  005222
15 002032 001003 BNE    1$ ; NO - SKIP
16 002034 012777 MOV    #-1,@#ERRCNT ; YES - FORCE VALUE
  177777
  000002
   1$: RETURN

. SETTL TEST 10: A/D CALIBRATION

; THIS TEST ACCEPTS A CHANNEL ADDRESS FROM THE USER AND DISPLAYS THE DATA FROM THAT CHANNEL CONTINUOUSLY

26 002044 TEST10: PRINTC <A/D CALIBRATION>
27 002066 004767 CALL    GETCH ; GET CHANNEL ADDRESS
  177476
28 002072 KBEXIT
29 002074 042702 BIC    #140303,R2 ; CLEAR SOME BITS
    140303
30 002100 032702 BIT    #60,R2 ; EXTERNAL?
  000000
31 002104 001002 BNE    1$ ; YES - NO START BIT
32 002106 052702 BIS    #1,R2 ; SET START BIT
  000001
33 002112 112704 1$: MOVB   #10,R4 ; LINE COUNTER
  177777
  000000
34 002116 CRLF
35 002120 010211 2$: MOV    R2,(R1) ; START CONVERSION
  10211
36 002122 105711 3$: TSTB   (R1) ; WAIT FOR DONE
  105711
37 002124 100376 BPL    3$ ; DISPLAY DATA
38 002126 004767 CALL    DISPLAY
  177644
39 002132 105304 DECB   R4 ; LINE OVER?
40 002134 001766 BEQ    1$ ; YES - NEW LINF
41 002136 TAB
42 002140 000767 BR    2$ ; NEXT CONVERSION
TEST 11: A/D INPUT CHANNEL SCAN

002142 TEST11: PRINTC <A/D INPUT CHANNEL SCAN>
002174 KBEXIT
002176 MOV 000002
002180 000542
000542
002182 TST 2(R1)
002184 CLR (R1)
002186 CLR R2
002188 INIT. CHANNEL COUNT
002190 MOVB #10, R3
002194 102000 PRINT <CH=>
002198 OCT R2 R0
00219C MOV R2 R0
0021A0 SWAB R0
0021A4 MOV R0, R(R1)
0021A8 INCB R(R1)
0021AA TSTB R(R1)
0021B0 TSTB R(R1)
0021B4 BPL 3$
0021B8 CALL DISPLAY
0021C2 100376 R3
0021CC 105211 DECB R3
0021D0 105303 BNE 2$
0021D4 001370 BNE 2$
0021D8 005202 INC R2
0021DC 123702 CMPB 000541
002208 000002 BNE 1$
00220C 000746 CRLF
002210 000010 CRLF
002214 112703
TEST 12: PRINTC <A/D INPUT GAIN/CHANNEL SCAN>

KBEXIT
MOV @#BASE,R1 ; SET UP KEYBOARD

TST 2(R1) ; CLEAR DONE

CLR (R1) ; CLEAR CSR
CLR R2 ; INIT. CHANNEL COUNT
CLR R3 ; INIT. GAIN

CRLF
MOVB #7,R4 ; LINE COUNTER

PRINT <CH=>

MOV R2,R0 ; DISPLAY ADDRESS

OCT8
MOVB #',R0 ; DISPLAY GAIN

TTYOUT

MOVB #`,R0

BIT #10,R3 ; GS1 SET?

BEQ 2$ ; NO - SKIP

INCB R0

TTYOUT

MOVB #`,R0 ; DISPLAY BIT

BIT #4,R3 ; GS0 SET?

BEQ 3$ ; NO - SKIP

INCB R0

TTYOUT ; DISPLAY BIT
TST-11 MODULE  MACRO V03.0B

1 002436 010200 MOV R2, R0 ; GET CHANNEL ADDRESS
2 002440 000300 SWAB R0 ; PUT IN HIGH BYTE
3 002442 050300 BIS R3, R0 ; SET GAIN BITS
4 002444 010011 MOV R0, (R1) ; SET UP CHANNEL
5 002446 105211 4$ ; TRIGGER CONVERTER
6 002450 105711 5$ ; WAIT FOR DONE
7 002452 100376 BPL 5$ ;
8 002454 TAE
9 002456 004767 CALL DISPLAY ; DISPLAY DATA
     177314
10 002462 105304 DECB R4 ; LINE DONE?
11 002464 001370 BNE 4$ ; NO - CONTINUE
12 002466 005202 INC R2 ; INC. CHANNEL
13 002470 062703 ADD #4, R3 ; INCREMENT GAIN
     000004
14 002474 042703 BIC #177763, R3 ; CLEAR EXTRA BITS
     177763
15 002500 123702 CMPB @#SWR+1, R2 ; END OF RANGE?
16 002504 001323 BNE 1$ ; NO - CONTINUE
17 002506 005002 CLR R2 ; YES
18 002510 CRLF
19 002512 000720 BR 1$ ;
20 . END
<table>
<thead>
<tr>
<th>SYMBOL TABLE</th>
</tr>
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<tbody>
<tr>
<td>BASE = 000542</td>
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<tr>
<td>BIT0 = 000001</td>
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<td>BIT1 = 000002</td>
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<td>BIT10 = 002000</td>
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<td>BIT11 = 004000</td>
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<tr>
<td>BIT12 = 010000</td>
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<td>BIT13 = 020000</td>
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<td>BIT14 = 040000</td>
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<tr>
<td>BIT15 = 100000</td>
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<tr>
<td>BIT2 = 000004</td>
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<td>BIT3 = 000010</td>
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<td>BIT4 = 000020</td>
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<td>BIT6 = 000100</td>
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<td>BIT7 = 000200</td>
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<td>BIT8 = 000400</td>
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<tr>
<td>BIT9 = 001000</td>
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<tr>
<td>BITL = 000015</td>
</tr>
<tr>
<td>BTLC = 000003</td>
</tr>
<tr>
<td>BTRLl = 000011</td>
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<td>BS = 000000</td>
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<td>BS = 0000</td>
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<td>CS = 01776R</td>
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<td>ERRCNT = 00052</td>
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<td>ERROR = 000540</td>
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<td>FF = 000014</td>
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<td>GETCH = 001570R</td>
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<td>HLTERM = 000004</td>
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<td>INHERR = 000100</td>
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<td>INIT = 00104R</td>
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<td>INIT6 = 000054</td>
</tr>
<tr>
<td>INIT64 = 000070R</td>
</tr>
<tr>
<td>I2762 = 000054RG</td>
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<tr>
<td>LF = 000012</td>
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<td>LPERR = 000002</td>
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<td>LPTST = 000001</td>
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<td>NEWFLG = 010000</td>
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<td>NORMIAL = 00426R</td>
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<tr>
<td>ODTACC = 000514</td>
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<tr>
<td>PARAM = 000334R</td>
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<td>PR7 = 000340</td>
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<tr>
<td>QUERY = 000212R</td>
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<tr>
<td>RBUF = 177562</td>
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<td>RCSR = 177560</td>
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<td>RSVP = 000546</td>
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<td>TSC = 000002R</td>
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<td>TSTALL = 000010</td>
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<td>TSTCSR = 000500</td>
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<td>TSTNUM = 000520</td>
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<td>TSTONE = 000040</td>
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<td>TSTSE0 = 000020</td>
</tr>
<tr>
<td>TSTSE = 000000RG</td>
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<tr>
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<td>XCSR = 177564</td>
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VIRTUAL MEMORY USED: 2128 WORDS (9 PAGES)

VMK MEMORY AVAILABLE FOR 67 PAGES

1: 2760. = DX0: TST11. ML/M, DX1: 2760. V01
<table>
<thead>
<tr>
<th>SECTION</th>
<th>ADDR</th>
<th>SIZE</th>
<th>GLOBAL VALUE</th>
<th>GLOBAL VALUE</th>
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<td>001000</td>
<td>000060</td>
<td>(RW, I, LCL, REL, CON)</td>
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<tr>
<td>DIRECT</td>
<td>001000</td>
<td></td>
<td></td>
<td></td>
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<td>001060</td>
<td>002514</td>
<td>(RW, I, LCL, REL, CON)</td>
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<td>T2762</td>
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<td>T2764</td>
<td>001060</td>
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<td>001150</td>
<td>001154</td>
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<td>003342</td>
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<td>003574</td>
<td>12769</td>
<td>003574</td>
<td>003740</td>
</tr>
<tr>
<td>TST11</td>
<td>007136</td>
<td>006434</td>
<td>(RW, I, LCL, REL, CON)</td>
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<tr>
<td>START</td>
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</table>

TRANSFER ADDRESS = 007136, HIGH LIMIT = 015572 = 3517. WORDS
<table>
<thead>
<tr>
<th>Section</th>
<th>Addr</th>
<th>Size</th>
<th>Global Value</th>
<th>Global Value</th>
<th>Global Value</th>
</tr>
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<tbody>
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<td>001000</td>
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<td>TST11</td>
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<td>(RW,I,LCL,REL,CON)</td>
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<td>P0029</td>
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<td>T2765</td>
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<td>002234</td>
<td>(RW,I,LCL,REL,CON)</td>
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<td></td>
</tr>
</tbody>
</table>

Transfer address = 001000, High limit = 011730 = 2540 words
<table>
<thead>
<tr>
<th>Page</th>
<th>Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>General Information</td>
</tr>
<tr>
<td>3</td>
<td>Test Parameter Block (TPR)</td>
</tr>
<tr>
<td>4</td>
<td>Initialization</td>
</tr>
<tr>
<td>5</td>
<td>Display Parameters</td>
</tr>
<tr>
<td>6</td>
<td>Error reporters</td>
</tr>
<tr>
<td>7</td>
<td>Model testing information</td>
</tr>
<tr>
<td>8</td>
<td>Logic Tests</td>
</tr>
<tr>
<td>8</td>
<td>Test 1: BRPLY from all registers</td>
</tr>
<tr>
<td>9</td>
<td>Test 2: check ADCSR bits</td>
</tr>
<tr>
<td>10</td>
<td>Test 3: BIT/ITL action</td>
</tr>
<tr>
<td>11</td>
<td>Test 4: byte operation of ADCSR</td>
</tr>
<tr>
<td>12</td>
<td>Test 5: A/D DONE bit and interrupt</td>
</tr>
<tr>
<td>15</td>
<td>Test 6: End of logic tests</td>
</tr>
<tr>
<td>15</td>
<td>Calibration initialization</td>
</tr>
<tr>
<td>16</td>
<td>Display A/D data</td>
</tr>
<tr>
<td>16</td>
<td>Test 7: A/D Calibration</td>
</tr>
<tr>
<td>17</td>
<td>Test 10: A/D input channel scan</td>
</tr>
<tr>
<td>18</td>
<td>Test 11: A/D input gain/channel scan</td>
</tr>
</tbody>
</table>
.LIST TTM
.ENABL LC
.TITLE DT2765 TST-11 module
.IDENT /V01.02/
.PSECT DT2765

000000

.NLIST BIN

.SBTTL General Information

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the use of any portion of this software for other than
its intended diagnostic purpose in calibrating and
testing Data Translation manufactured analog and
digital interface boards.

Version 01-02

Phillip Martinez 19-Apr-79
Edwin Kroeker 6-Jan-79
Phillip Martinez 16-Aug-79

This program module contains routines to test and
calibrate DTI DT2765 series analog interface systems
for the LSI-11. A complete listing of the models
tested by this code module will be found on the
following pages. This module is designed to operate
under TST-11 supervision.
The differences between V01-01 and V01-02 are as follows.
1). test 7 now supports even and odd mux addresses.
2). general cleanup of various small inconsistent coding sequences.
.LIST BIN
.SRTL  Test Parameter Block (TPB)

; Test-11 Declaration

.MCALL TST11

TST11

; Additional parameters used by this diagnostic

000046  DELAY  =546  ; A/D delay count storage

000522  ERRCTR  =522  ; error counter

; Test Parameter Block

.NLIST BIN

; Test Address Table for use by TST-11

000000  TBP:  .WORD  PARAM:  ; address of parameter

000002  .BYTE  377  ; print-out routine

000003  .BYTE  11  ; reserved

000004  .WORD  TEST1,PR7

000010  .WORD  TEST2,PR7

000014  .WORD  TEST3,PR7

000020  .WORD  TEST4,PR7

000024  .WORD  TEST5,PR7

000030  .WORD  TEST6,PR7

000034  .WORD  TEST7,0

000040  .WORD  TEST10,0

000044  .WORD  TEST11,0

; .LIST BIN
.SBTTL Initialization

4 000050 012737 INIT65: MOV #BIT3, @S'TR ; isolated module
000010 000540
5 000056 012737 MOV $21000, @DELY ; big delay
051040 000546
6
7 000064 INIT: PRINT <# of A/D input channels (in octal): >
8 000134 GETOCT ; get octal input
9 000136 103352 BCC INIT ; no CR - ask again
10 000140 105737 TSTB @ODTACC ; zero?
000514
11 000144 001747 BEO INIT ; ask again
12 000146 113737 MOV @ODTACC, @S'TR+1
000514 000541
13 000154 012737 MOV $177000, @BASE ; set default address
177000 000542
14 000162 012737 MOV $130, @VECT ; set default vector
000130 000544
15 000170 000207 RETURN ; all done
.SBTTL Display Parameters

This routine displays the current setting of 'BASE' and 'VECTOR' on the system console terminal.

PARA!: PRINT <Base address = >
    MOV @#BASE,R0 ; get base address
    OCT16
    CRLF
    PRINT <Vector address = >
    MOV @#VECTOR,R0 ; get vector address
    OCT16
    CRLF
    RETURN ; all done
.SRTTL  Error reporters

; This routine provides error reporting for bus
; time-out errors (no BRPLY from interface).

NORPLY: PRINT  <No BRPLY when accessing location >
          MOV   R1,R0
          OCT16
          CRLF
          RETURN
          ; done

; This routine provides error reporting for register
; bit errors (one or more incorrect bits in a register).

REG: PRINTC  <Register Error>
      PRINT  <Address: >
      PUSH   R0
      MOV    R1,R0
      OCT16
      CRLF
      PRINT  <Expected:>
      MOV    R2,R0
      OCT16
      CRLF
      PRINT  <Found: >
      MOV    (SP),R0
      XOR    R2,R0
      OCT16
      CRLF
      PRINT  <Bits: >
      POP     R0
      OCT16
      CRLF
      RETURN
      ; done

; This routine provides for house keeping upon
; leaving a routine.

WAIT: MOV    @#DELAY,R0
000546
S:   SOB    R0,1S
TST    2(R1)
000002
RETURN
000207
Model testing information

This code module contains the routines necessary to test the following DTI interface models:

DT2765 Isolated wide range input

I2765 == INIT65
T2765 == TPB

Software switch register bit reservations

bits 13-8: # of A/D channels
bit 6: DT5710 A/D module present
bit 5: DT5701 A/D module present
bit 4: DT5702 A/D module present
bit 3: DT5703 A/D module present
bits 2-0: reserved
LOGIC TESTS

000514 010602 TEST1: MOV SP, R2 ; save SP
000516 010037 REL:MOV $3$, P0 ; set up trap to 4
000524 000004 MOV R0, @4
000530 013701 2$: MOV @BASE, R1 ; get address
000534 000542 SCOPE
10 10 5011 CLRB (R1) ; DATIO bus cycle
15 000540 062701 ADD #2, R1 ; next register
16 000540 000002 SCOPE
17 000546 005011 CLR (R1) ; DATIO bus cycle
18 000550 004767 CALL WAIT
19 000554 177724 EXIT

** Error Code 1 - Bus timeout **

3$: MOV (SP), R3 ; get offending PC
28 000560 010206 MOV R2, SP ; restore stack
29 000562 ERROR 1, NORPLY ; report error
30 000566 000113 JMP (R3) ; continue test
SBTTL Test 2: check ADCSR bits

; This test checks most of the bits in ADCSR.
; Bits are checked for both set and reset capability.
; Bits that are NOT checked are the A/D DONE bit
; and the ERROR bit (both checked in other tests).

TEST2: MOV @BASE,R1  ; get address
CLR R2               ; init test reg.
MOV $40,R3           ; set # of states
SCOPE
MOV $177600,R0       ; declare loop point
ignore high byte
XOR R2,R0            ; test bits
BEQ 2$                ; no error - skip

; Error Code 2 - bit error, ADCSR
; bits 0-6

ERROR 2,REG           ; report error
ADD $4,R2             ; next state
SOB R3,1$             ; loop until done
CLR R2                ; init test reg.
MOV $200,R3           ; set # of states
SCOPE
MOV (RL),R0           ; declare loop point
get bits
BIC $100377,R0        ; get bits
ignore low byte
XOR R2,R0             ; test bits
BEQ 5$                ; no error - skip

; Error Code 3 - bit error, ADCSR
; bits 8-14

ERROR 3,REG           ; report error
ADD $400,R2           ; next state
SOB R3,4$             ; loop until done
CALL WAIT
EXIT
**SBTTL Test 3: BINITL action**

This test verifies that the BINITL signal clears the proper ADCSR bits.

```
TEST3: MOV @#BASE, R1 ; get address
       MOV $40100,(R1) ; set bits
       MOV @#DELAY,R0 ; wait for A/D DONE

2$: SUB R0, 2$ ; set error bit
    BIS $0,(R1)

CLR R2 ; clr test reg.
SCOPE
RESET ; declare loop point
MOV (R1), R0 ; issue BINITL
BIC $37476, R0 ; ignore some bits

XOR R2, R0 ; test bits
BEQ 3$ ; OK - skip error

;********************************************************************
; Error Code 4 - proper bit(s) not cleared by BINITL
;********************************************************************

;********************************************************************
; ERROR 4, REG ; report error
;********************************************************************

3$: CALL WAIT ; all done
EXIT
```
.SBTTL Test 4: byte operation of ADCSR

; This test verifies high and low byte operations
; involving the ADCSR.

TEST4: MOV @#BASE,R1 ; get address
        CLR B (R1) ; clear ADCSR
        CLR R2 ; init. test register
        SCOPE #1,-1,(R1) ; declare loop point
        MOVB #00377, R0 ; set R/′ bits
        MOV (R1), R0 ; get ADCSR as word
        BIC #100377, R0 ; ignore low byte
        XOR R2, R0 ; test bits
        BEQ 1$ ; ok - skip error

;*****************************************************************************

; Error Code 5 - high byte loaded during a low byte operation

;*****************************************************************************

ERROR 5,REG ; report error

1$: CLR B (R1) ; clear ADCSR
    CLR R2 ; init. test register
    INC R1 ; point to high byte
    SCOPE #1,-1,(R1) ; declare loop point
    MOVB #177600, R0 ; set R/′ bits
    MOV -1(R1), R0 ; get ADCSR as word
    BIC #177600, R0 ; ignore high byte
    XOR R2, R0 ; test bits
    BEQ 2$ ; ok - skip error

;*****************************************************************************

; Error Code 6 - low byte loaded during a high byte operation

;*****************************************************************************

ERROR 6,REG ; report error

2$: CALL WAIT

EXIT
SBTTL Test 5: A/D DONE bit and interrupt

; This test verifies that the A/D DONE bit can
; be set properly and that the INT ENB bit
; functions properly.
;
TEST5: MOV @#BASE,R1 ; get address
         MOV @#VECTOR,R2 ; get vector address
         TST 2(R1) ; clear A/D DONE bit
         CLR (R1) ; clear ADCSR
         SCOPE #0,(R1) ; declare loop point
         BIS 0,(R1) ; set A/D DONE bit
         MOV @#DELAY,R0 ; wait for A/D DONE

1$:  SOB R0,1$ ; is bit set?
         TSTB (R1) ; yes - skip error

;********************************************************************
; Error Code 7 - A/D DONE bit not set
;********************************************************************

         ERROR 7 ; report error
         BR 8$ ; can't continue

2$:  SCOPE ; declare loop point
         TST 2(R1) ; read ADDER
         TSTB (R1) ; done bit clear?
         BPL 3$ ; yes - skip error

;********************************************************************
; Error Code 10 - A/D DONE bit not cleared
; after A/D data was read
;********************************************************************

         ERROR 10 ; report error
         BR 8$ ; can't continue
DT2765 TST-11 MODULE MACRO V03.0B 16-AUG-79 14:03:44 PAGE 13

TEST 5: A/D DONE BIT AND INTERRUPT

1 001130 005003 3$: CLR R3 ; prepare status words
    001132 012704 MOV #PR7,R4
    001136 000340

3 001136 RELMOV $50,R0 ; get ISR address
    001144 010012 MOV R0,(R2)
    001146 010462 MOV R4,2(R2)

5 001152 000002 ; store

6 001152 SCOPE ; store status too
    001154 005011 CLR (R1)
    001156 013700 MOV @#DELAY,R0

8 001162 077001 4$: SOB R0,4$ ; declare loop point
    001164 152711 BISB #100,(R1) ; set A/D DONE

10 001164 005100 ; wait for DONE

11 001164 106403 ; enable interrupts

12 001170 000240 ; enable CPU interrupts

13 001174 106404 ; stall time

14 ; turn off CPU

15

16

17

18

19

20 21 001176 ERROR 11 ; report error
    001200 000423 BR 8$

22 001202 062706 5$: ADD #4,SP ; can't continue

23 001206 000004

24 001206 SCOPE ; adjust stack

25 001210 005761 ; declare loop point

26 001210 000002 ; read ADDSR

27 001214 105711

28 001216 100002 TSTB (R1) ; A/D DONE clear?

29 ; yes - exit

30

31

32

33

34

35

36

37 001220 ERROR 12 ; report error
38 001222 000412 BR 8$ ; can't continue

; Error Code 11 - no interrupt on A/D DONE

; Error Code 12 - A/D DONE bit not cleared after A/D data was read
TEST 5: A/D DONE BIT AND INTERRUPT

1 001224  6$: SCOPE
2 001226  005761  TST 2(R1)  ; declare loop point
   000002  ; clear DONE
3 001232  005011  CLR (R1)  ; clear ADCSR
4 001234  013700  MOV #DELAY,R0  ; wait
   000546
5 001240  077001  7$: SOB R0,7$
6 001242  005711  TST (R1)  ; error bit set?
7 001244  100001  BPL 8$  ; no - exit

;***************************************************************
; Error Code 13 - Error bit set after normal
; A/D triggering sequence
;***************************************************************

16 001246  8$: TST 2(R1)  ; report error
17 001250  005761
18 000002  ; clear DONE
19 001254  005011  CLR (R1)
20 001256  004767  CALL WAIT
21 001262  177216  EXIT
.SBTTL Test 6: End of logic tests

; This test is present to inform the TST-11 monitor
; that there are no more additional logic tests
; to be executed. When the "ALL" command is used,
; this test will force a return to the command
; level of TST-11 when the test sequencer reaches
; this test.

; TEST6: ESCAPE

; .SBTTL Calibration initialization

; This routine performs initialization functions
; for some of the calibration tests.

GETCH: PRINT <Channel? > ; output prompt
GETOCT ; get value
BCS 1$ ; CR at end - cont.
PRINTC <Enter an octal channel address.>
BR GETCH ; try again

; MOV @#BASE,R1 ; get address
MOV @#ODTACC,R2 ; get value
SWAB R2 ; adjust
PRINT <Mode bits? > ; output prompt
GETOCT ; get value
BCS 3$ ; CR at end - cont.
PRINTC <Enter an octal byte value.>
BR 2$

; BIC $377,R2 ; clear low byte,R2
MOV @#ODTACC,R0 ; get value
BIC $177400,R0 ; clear high byte,R0
ADD R0,R2 ; add in mode byte
TST 2(R1) ; clear DONE
CLR (R1) ; clear board

RETURN
.SBTTL Display A/D data

; This routine takes the data from ADDBR and displays it for the user as a 16 bit octal value.

DISPLY: MOV 2(R1),R0 ; get data
OCT16 ; print
TST (R1) ; error bit set?
BPL 1$ ; no - return
MOVE '#E,R0 ; print 'E'
TTYOUT
BIC #40000,(R1) ; clear error bit
INC @#ERRCNT ; inc. count
TST @#ERRCNT ; overflow?
BNE 1$ ; no - skip
MOV #-1,@#ERRCNT ; yes - force value

1$: RETURN

; .SBTTL Test 7: A/D Calibration

; This test accepts a channel address from the user and displays the data from that channel continuously.

TEST7: PRINTC <A/D Calibration>
CALL GETCH ; get channel address
KBEXIT ; clearing key board
BIC #140363,R2 ; clear all but gain bit
1$: MOV #10,R4 ; line counter
CRLF
MOV R2,(R1) ; start conversion
TSTB (R1) ; wait for DONE
BPL 3$ ;
CALL DISPLY ; display data
1$: DEC R4 ; line over?
BEQ 1$ ; yes - new line
TAB
BR 2$ ; next conversion
.SBTTL Test 10: A/D input channel scan

; This test scans the input channels while displaying the A/D data on the terminal.

TEST10: PRINTC <A/D Input channel scan>

KBEXIT
MOV @#BASE,R1 ; set up keyboard
MOV 000542 ; get address
TST 2(R1) ; clear DONE
CLR (R1) ; clear CSR
CALL WAIT
CLR R2 ; init. channel count
CRLF
MOVE #10,R3 ; line counter
PRINT <CH=>
MOV R2,R0 ; display address
OCT8
MOV R2,R0 ; get channel address
SUBAB R0
MOV R0,(R1) ; put in high byte
JMP 3$

BIS #0,(R1) ; trigger converter
TSTB (R1)
BPL 3$
CALL DISPLAY ; display data
DEC# R3 ; line done?
BNE 2$ ; no - continue
INC R2 ; inc. channel
CHPB @#SW+1,R2 ; end of range?
BNE 1$ ; no - continue
CLR R2 ; yes
CRLF
BR 1$
.SBTTL Test 11: A/D input gain/channel scan

; This test scans the input channels while
; changing the gain of the converter. The
; A/D data is displayed on the terminal.

TEST11: PRINTC <A/D Input gain/channel scan>

KBEXIT

MOV @BASE,R1

; set up keyboard
; get address

TST 2(R1)

; clear DONE

CLR (R1)

; clear CSR

CLR (R1)

BPL 6$

TST 2(R1)

; init. channel count
; init. gain

CLR R2

CLR R3

MOV #7,R4

; line counter

PRINT <CH->

; display address

MOV R2,R0

OCT8

MOVB #'',R0

; display gain

MOVB #0,R0

; GS1 set?

BIT #10,R3

; no - skip

BEQ 2$

INC# R0

; display bit

MOVB #0,R0

; GS0 set?

BIT #4,R3

; no - skip

BEQ 3$

INC# R0

; display bit

MOVB #0,R0

; display bit

MOVB #0,R0
DT2765  TST-11 MODULE  MACRO V03.0B
TEST 11: A/D INPUT GAIN/CHANNEL SCAN

1  002154  010200
2  002156  000300
3  002160  050300
4  002162
5  002164  011611  4$:
6  002166  105711  5$:
7  002170  100376
8  002172
9  002174  004767  177304
10  002200  105304
11  002202  001370
12  002204
13  002206  005202
14  002210  062703  000004
15  002214  042703  177763
16  002220  123702  000541
17  002224  001322
18  002226  005002
19  002230
20  002232  000717
21
22  000001 ; .END

16-AUG-79 14:03:44 PAGE 19

MOV  R2,R0 ; get channel address
SWAB  R0
BIS  R3,R0 ; set gain bits
PUSH  R0
MOV  (SP),(R1) ; trigger conversion
TSTB  (R1)
BPL  5$
TAB
CALL  DISPLY ; wait for DONE
; display data
DEC B  R4 ; line done?
BNE  4$ ; no - continue
POP  R0
INC  R2 ; inc. channel
ADD  #4,R3 ; increment gain
BIC  #177763,R3 ; clear extra bits
CNPB  @#SUR+1,R2 ; end of range?
BNE  1$ ; no - continue
CLR  R2 ; yes
CLRF  BR  1$
.Symbol Table

<table>
<thead>
<tr>
<th>CASE</th>
<th>000542</th>
<th>ERRCNT= 000522</th>
<th>SWR  = 000540</th>
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<tr>
<td>BIT0</td>
<td>000001</td>
<td>ERRNUM= 000521</td>
<td>TEST1 000514R 002</td>
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<tr>
<td>BIT1</td>
<td>000002</td>
<td>FF  = 000014</td>
<td>TEST10 001636R 002</td>
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<td>BIT10</td>
<td>002000</td>
<td>GETCH 001266R 002</td>
<td>TEST11 002004R 002</td>
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<td>BIT11</td>
<td>004000</td>
<td>HLTER= 000004</td>
<td>TEST2 000570R 002</td>
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<td>BIT12</td>
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<td>INHERR= 000100</td>
<td>TEST3 000676R 002</td>
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<td>BIT13</td>
<td>020000</td>
<td>INIT 000064R 002</td>
<td>TEST4 000752R 002</td>
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<td>040000</td>
<td>INIT65 000050R 002</td>
<td>TEST5 001050R 002</td>
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<td>TEST6 001264R 002</td>
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<td>000004</td>
<td>LF  = 000012</td>
<td>TEST7 001552R 002</td>
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<td>000010</td>
<td>LPERR = 000002</td>
<td>TPB 000000R 002</td>
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<td>000020</td>
<td>LPTST = 000001</td>
<td>TSTALL= 000010</td>
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<td>000100</td>
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<td>TSTONE= 000040</td>
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<td>PR7  = 000340</td>
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<td>RBUF = 177562</td>
<td>VECTOR= 000544</td>
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<td>CTRL</td>
<td>000003</td>
<td>RCSR = 177560</td>
<td>WAIT 000500R 002</td>
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<td>CTRL1</td>
<td>000011</td>
<td>REG 000340R 002</td>
<td>XBUF = 177566</td>
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<tr>
<td>RTL1</td>
<td>000546</td>
<td>SPACE = 000040</td>
<td>XCSR = 177564</td>
</tr>
</tbody>
</table>

ABS. 000000 001
000000 001
02765 002234 002

ERRORS DETECTED: 0

VIRTUAL MEMORY USED: 2128 WORDS ( 9 PAGES)
DYNAMIC MEMORY AVAILABLE FOR 67 PAGES
.DX1:2765,=DX1:TST11.ML/M,DX1:2765.V01
APPENDIX D
SCHEMATIC DRAWINGS