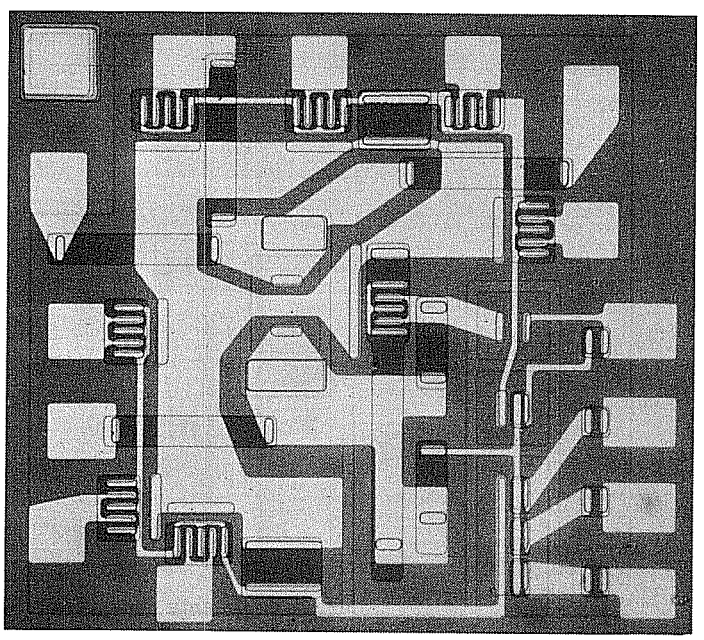
an introduction to
INTEGRATED CIRCUITS



CONTROL DATA
CORPORATION

Initial Printing, March 1967

Pub No. 60202000

by Control Data Corporation

Printed in United States of America

Address comments concerning this manual to:

Control Data Corporation
Technical Publications Department
4201 North Lexington Avenue
St. Paul, Minnesota 55112

or use Comment Sheet in the back of this manual.

FOREWORD

The integrated circuit (IC) is used in many new-generation computer systems for both military and commercial markets. The struggle toward the realization of ever-increasing speed, wherein the transient time of an electron from one circuit element to another becomes a factor of major importance, has forced a gradual reduction in the size of the physical package. The IC offers, at least for the present, the happiest combination of speed, size, and low cost; although with our rapidly advancing technology, few experts would care to predict what further strides will be made.

This manual attempts to give, in as simple language as possible, some insight into what integrated circuits - specifically monolithic circuits - really are.

The usefulness of any training manual is directly related to how accurately it reflects the current "state of the art". Accordingly, it is the author's intention to periodically revise this book as new concepts or advances in manufacturing techniques are revealed.

(The descriptions of some Process Steps in Chapter 3, and the drawings that illustrate them, have been taken from the Production Training Manual put out by Motorola's Semiconductor Division.)

CONTENTS

CHAPTER 1
INTRODUCTION

To understand integrated circuits and their properties, a brief history of the evolution of transistors will be helpful. In this discussion, the kinds of transistors have been arranged according to their chronological development, and a general summary of the manufacturing process for each is presented.

ALLOY TRANSISTOR

Process steps

1. Lightly doped (high-resistivity) P-or N-type material (here we will assume N type for an eventual PNP transistor)
2. Germanium N-type ingot is sliced into wafers about 10 mils thick and 125 mils on a side.
3. P-type indium-aluminum or indium-gallium round dots are melted and alloyed onto each side of material.
4. The metal and semiconductor recrystallizes on cooling and becomes heavily doped (low resistivity) P material ; forms two PN junctions

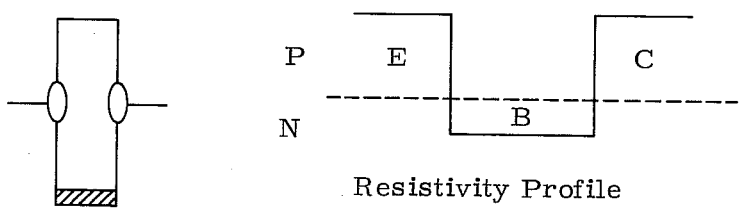


Figure 1-1. Alloy Transistor

Advantages

High gain and low r_{SAT} high avalanche breakdown voltage

Disadvantages

1. Susceptible to "punch through", a phenomenon where the depletion layer spreads into the high restivity base region as reverse voltage across the collector-base junction increases. This reduces the effective base width to zero and a V_{CE} short appears.

   This can be improved with higher concentration base material, but C_{DE} and the base store increases.

2. Process control is also hard, thus limiting $f\tau \approx$ 500 KC. This is due to poor base width control and physically large alloyed junctions.

$$f\tau \propto \frac{1}{W^2} \quad \text{where W = base width}$$

This is improved by the micro-alloy-transistor (MAT) process in which a deep pit is electrochemically etched for the emitter and a shallow pit for the collector. W can be controlled to 10^{-4} inches; $f\tau >$ 2 MHz are obtainable, but due to the narrow base width BV_{CEO} is small (6 volts).

DIFFUSED-BASE ALLOY TRANSISTOR

By not doping the N-type ingot initially, and then doping the ingot by a N-type diffusion, further improvements were made.

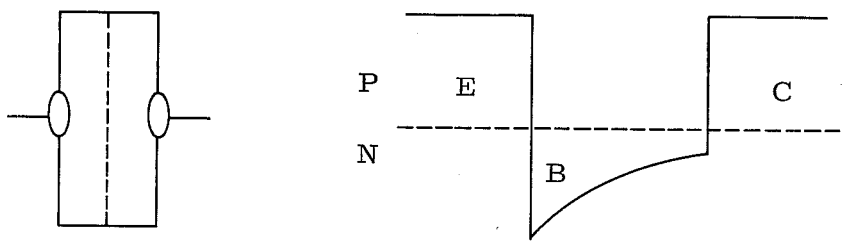
First, diffusing the N-type base causes a graded base resistivity profile as Figure 1-2 illustrates. The resistivity of the base at the emitter junction is lower than at the collector junction. Because of this, the depletion layer penetration is hindered and a higher V_{PT} is obtained. Penalties are: lower β, lower BV_{EBO}, and higher C_{TE} because of the relationship

$$C_{TE} = A\sqrt[2]{\frac{KM}{V_r}}$$

where M is the base concentration. This device, however, offered greatly improved switching speed.

Disadvantages:

Because of the circular area of the emitter, high speeds at high currents are difficult to obtain. The point at which I_E and $f\tau$ are maximum is very important; $f\tau$ is proportional to C_{TE} which is proportional to the emitter area and I_E is proportional to the emitter periphery. A circular emitter, therefore, is the worst possible shape for obtaining high speeds at high currents.



Resistivity Profile

Figure 1-2. Diffused-Base Alloy Transistor Resistivity Profile
Graded Base - Impurity Distribution

MESA TRANSISTOR

This development provided the first large-volume production breakthrough -- now up to 400 transistors could be made at once. The wafers that were sliced from N- or P-type silicon became the collector, not the base. The base was then diffused into the surface. This offered greater control. Emitters were formed by vacuum evaporation of impurities similar to the collector type. The evaporation took place on the surface and through a metal mask in which rectangular emitter openings had been cut. The last step was chemically etching away the base, leaving the "Mesa" as the Figure 1-3 below illustrates. The etching process step was required to reduce the collector-base junction area, and of course, the collector-base capacitance.

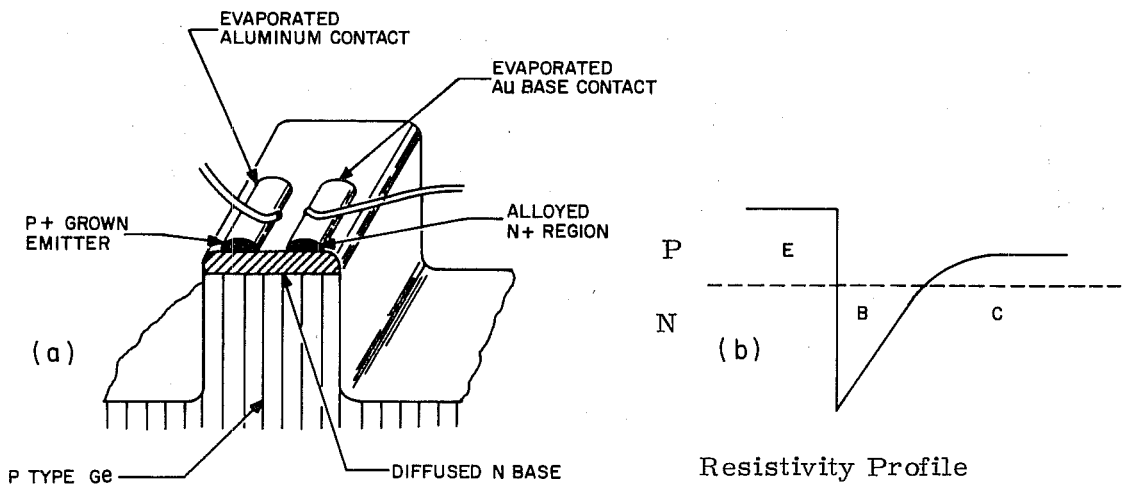


Figure 1-3. Mesa Transistor

The resistivity profile, Figure 1-3(b), offered many advantages:

1. High control gives better overall performance.
2. Graded base means lower C_{TC}.
3. Punch-through means disappears.
4. Higher β due to smaller base widths.
5. Geometry is closer to optimum.
6. Larger collector area for power dissipation.

Limitations

1. High r_{SAT} due to high resistivity collector area. Lower r_{SAT} would mean lower breakdown voltage (BV_{CBO} and BV_{CEO}).
2. Higher storage time due to bulky collector (high resistivity) region.

EPITAXIAL MESA TRANSISTOR

In the Epitaxial process, uniform crystal layers of high resistivity silicon are grown on silicon material of low resistivity.

Advantages of Epitaxial-Mesa Transistor:

1) Compromises in electrical characteristics are overcome.
2) Quality of active semiconductor is improved.
   a) lower dislocation density
   b) greater control
   c) more uniform dopant distribution

To expand Advantage 1:

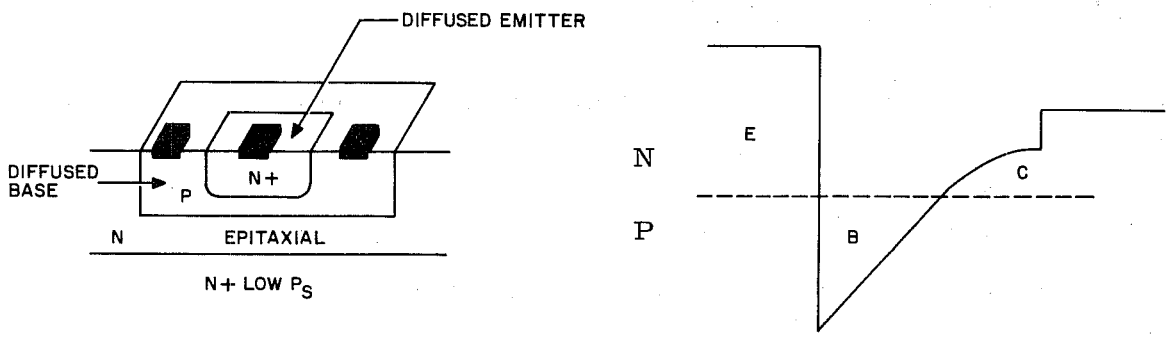
- lower r_{SAT} is possible because of lower resistivity collector material
- higher breakdown due to higher epitaxial layer resistivity
- lower collector excess stored charge. (Lower resistivity material restricts collector charge penetration.)

PLANAR TRANSISTOR

Basic differences between the Mesa and Planar processes are the construction of the junction, as seen by comparing Figures 1-3(a) and 1-4(a), and the method of control. The electrical characteristics are very similar; note especially the diffusion profiles in Figures 1-3(b) and 1-4(b).

Differences lie in the fact that junctions are diffused rather than alloyed and more than 1000 transistors can be built at once. The base and emitter junctions are diffused through selectively etched holes in silicon dioxide layers. This process is the basis for integrated circuits. Note that by double diffusing, the chemical etch of the base-collector junction is not needed.

Table 1-1 illustrates the trade off considerations in transistor design.



Resistivity Profile

Figure 1-4. Planar Epitaxial Transistor

SUMMARY

The trade-off considerations discussed in this chapter are shown again in Table 1-1 and Figure 1-5.

TABLE 1-1. TRADE OFF CONSIDERATIONS IN TRANSISTOR DESIGN

CHANGE	DECREASE	INCREASE	SWITCHING SPEED EFFECT
Decrease Emitter Resistivity	r_E (decrease SV_{CE})	β	
Increase Base Resistivity	V_{PT} C_{Te} C_{Tc}	β V_B (emitter and collector junction) r'_B r_E and r_C	Increase storage time, small increase in other intervals due to r'_B
Increase Collector Resistivity	C_{Tc}	V_B (collector) r_c (increase SV_{CE})	Increase storage time, small decrease in other intervals
Decrease Base Width	C_{De} V_{PT} R_E and r_C	β r'_B $f\tau$	Decrease rise time Decrease fall time Decrease storage time

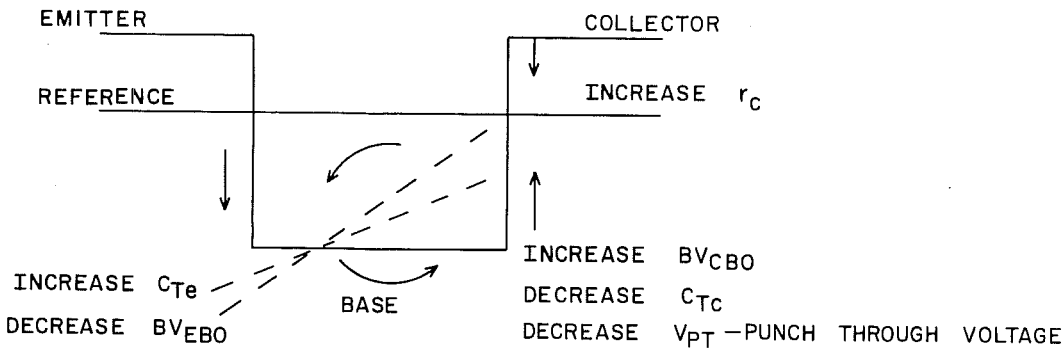
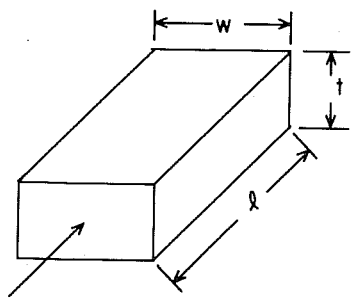


Figure 1-5. Base Resistivity Pivot Effects on Transistor Performance

CHAPTER 2
THE MONOLITHIC PROCESS

WHAT IS THE MONOLITHIC PROCESS?

Carrying the Planar process farther, it can be seen that if other diffusions were placed in the substrate other components could be made. Since the controlled diffusions have a certain resistivity ρ , a resistor can be formed by controlling the length, width and thickness of the diffusion.



$$R = \rho \frac{\ell}{tW}$$

If the resistor is created at the same time that the base is diffused, the thickness (t) is controlled so that the ρ/τ is a fixed number commonly called sheet resistivity ρ_s and therefore the expression for resistance becomes:

$$R = \rho_s \frac{\ell}{W}$$

This is especially helpful because the expression is in terms of the physical dimensions that are masked.

To understand the whys of the various parts of the integrated circuits, let us work out the design of a simple two-input RTL circuit.

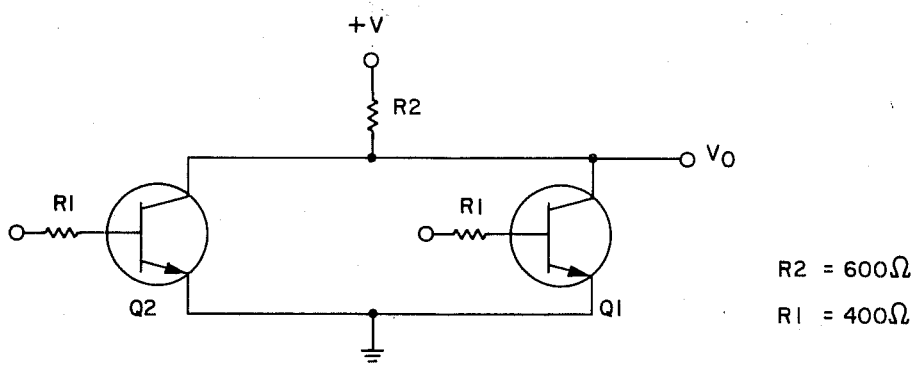


Figure 2-1. Desired Circuit

Using the Planar process the transistors and resistors can be placed as shown below.

Assuming ρ_s = 200 Ω /square, the 1/w ratio for R_2 = 3 and for R_1 = 2. Ignoring contact effects, the first attempt to create the circuit would be as presented below:

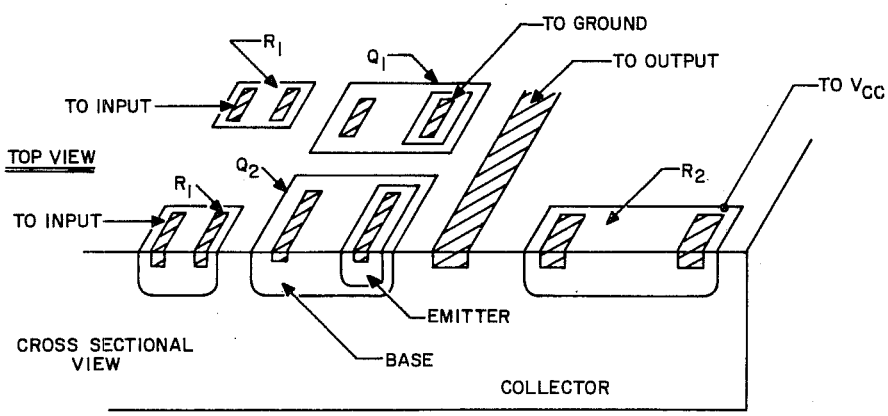


Figure 2-2. Tentative Layout for Figure 2-1

Comments on Layout

1. Since the collectors of the two circuits are common, one stripe of contact can be used for both transistors.

2. Note that the resistors are P-type and are diffused at the same time as the base.

3. Collector contact is brought out at the top.

4. For simplicity, the interconnection pattern is not shown.

To see whether or not the circuit will actually operate, let us examine the collector stripe/R_2 combination in more detail. Actually, between the resistor and the collector a P-N junction exists.

A plot of the voltage versus the current across the diffused 600-Ω resistor shows interesting characteristics (Figure 2-3).

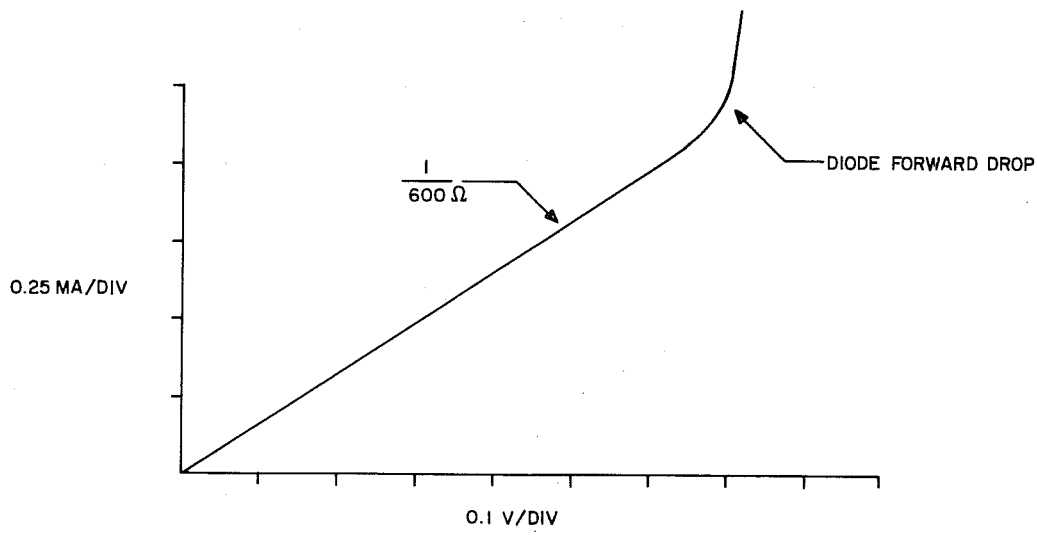


Figure 2-3. VI Characteristics of R_2

This is not a true resistance, however, because it breaks down at approximately 0.7v. To overcome this the "junction isolation" technique is used. A P-type substrate is used as a base for growing the epitaxial N-type material. A P-type diffusion is then placed between the transistors and resistor R_2. The substrate is then biased to the lowest applied potential (ground in this case). The P-type junction then reverse-biases the N-type epitaxial regions. The collector region underneath the resistor is still biased 0.7 volts below the resistor potential, but the current flow is "trapped". Figure 2-4 shows the revised circuit.

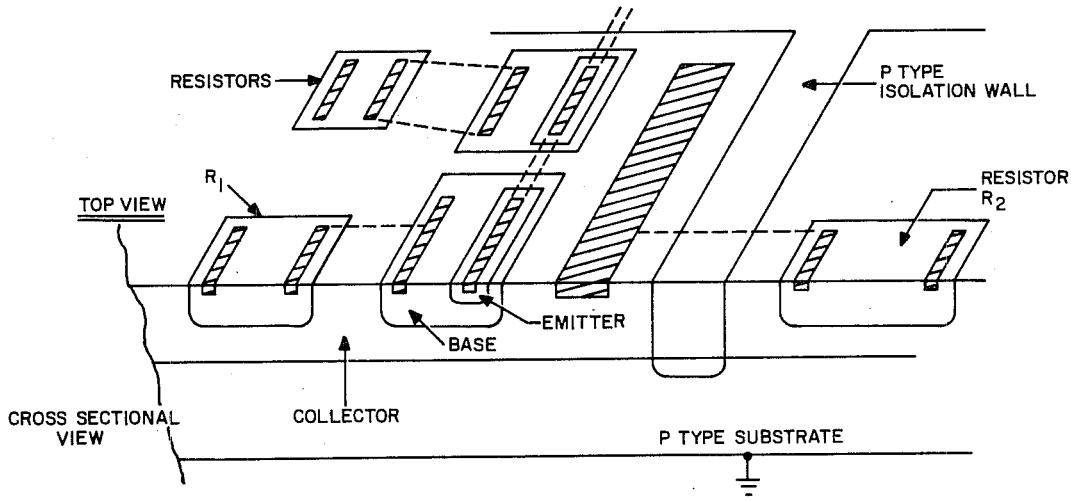


Figure 2-4. Improved RTL Circuit

Note that the collector contact is placed close to the emitter to minimize the transistor-collector current path and keep r_{SAT} as low as possible.

WHY INTEGRATED CIRCUITS?

The answer to this question is discussed in the six points below.

1. Lower Costs - come about because of the number of components per package and the cost per component.

2. Reduced Size and Weight - enable the density of the system to be increased, thus allowing for shorter system paths. This is especially helpful in critical space requirements such as airborne vehicles.

3. Decreased Power Requirements in Most Logic Types - the result of the very small power handling capabilities of the individual integrated circuits.

4. Improved Performance - achieved because of the optimum choice of components for the particular design.

5. Sales Appeal - always helps in user buying decisions. A computer small in size yet large in problem solving capacity is certainly an asset on the industrial market.

6. Improved Reliability (lower system down time) - possible because of the monolithic design - fewer component leads to be broken due to vibration or natural fatigue.

Everyone talks about the increased reliability of integrated circuits. Listed below are some of the reasons and arguments to support this attitude. Proof of these statements will come about by system performance with time. Control Data, among others, will prove or disprove them.

a) Compatibility of Components - All components produced from the same process, therefore all of the circuit has the same reliability. Discrete circuits, on the other hand, are only as reliable as the least reliable part of the circuit.

b) Interconnections - Since the circuit is metalized, only the bonds have possibility of problems. Acts similar to a weld (pressure and temperature). Bonding problems are the least reliable part of a well developed IC.

c) Delicate Surfaces Protection - Hermetic seals, glass passivation and package are three methods used simultaneously to protect chip circuits.

d) Handling Problems - Many automated parts of process reduce human error.

e) Complexity versus Reliability - In IC's, reliability is largely independent of the number of components. For example, assume the reliability of five elements in a discrete component circuit are each 0.95. The circuit reliability is then $[0.95]^5 \approx 77\%$. An equivalent integrated circuit of 80% would therefore be more reliable.

CHAPTER 3
DETAILED FABRICATION PROCESS

An Integrated Circuit has its origin in a CRYSTAL GROWING FURNACE. An INGOT, the silicon crystal about an inch in diameter and four inches long (Figure 3-1), is drawn like taffy from a heated, melted positive type (P-TYPE) impure silicon material.

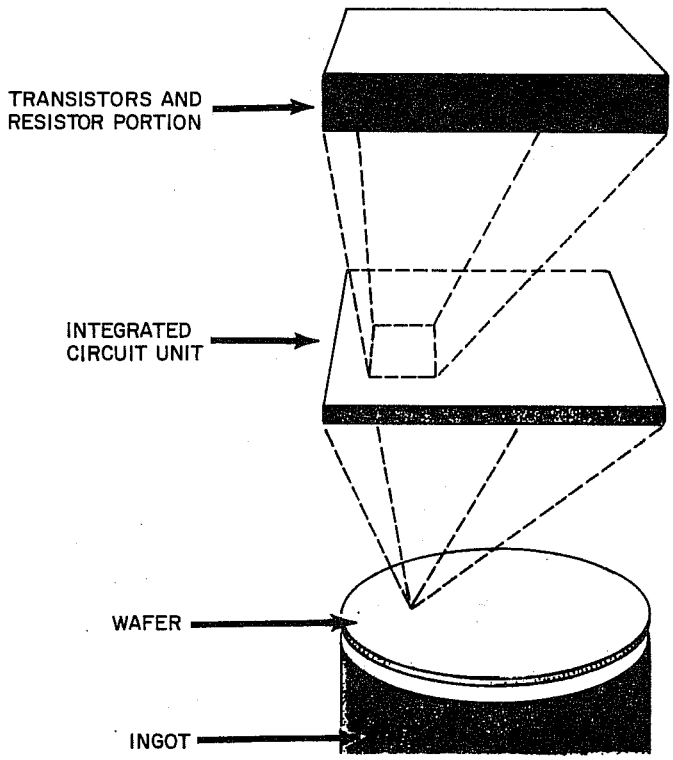


Figure 3-1. Crystal Ingot

When the INGOT is cooled it is sliced into thin wafers, about the thickness of a sheet of paper. After slicing, each WAFER is then ready to receive two additional layers, as shown in Figures 3-2 and 3-3.

The Fabrication Sequence is illustrated more effectively if the cross sectional view is limited to a transistor and resistor portion rather than the whole Integrated Circuit.

A thin layer of N-type impure Silicon is deposited on one surface of the P-type wafer under intense heat. This is what was defined earlier as the epitaxial process.

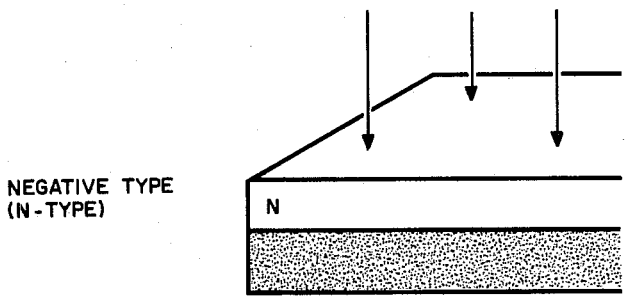


Figure 3-2. Adding N-Type Layer

After the N-type layer is formed, a thin film of oxide (a form of glass) is put over the N-type wafer. The oxide passivates or protects the surface from external contamination.

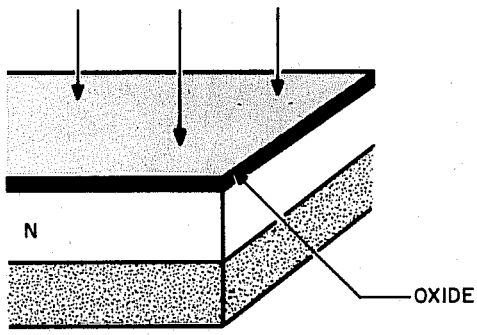
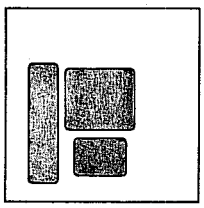


Figure 3-3. Adding Oxide Layer

At this point the wafer material is ready to undergo the first process step in the fabrication of integrated circuits.

FIRST PROCESS STEP - ISOLATION



STEP I

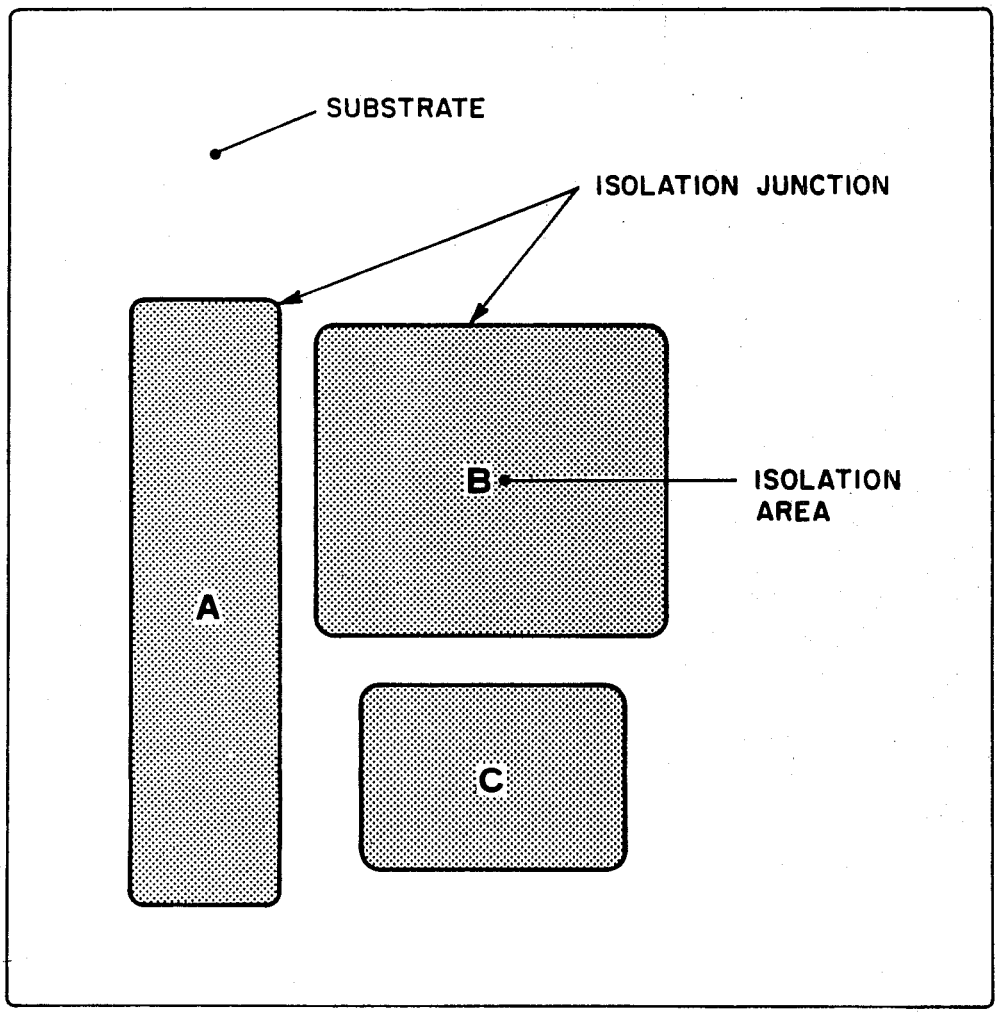


Figure 3-4. First Process Step

STEP 1, ISOLATION (Figure 3-5)

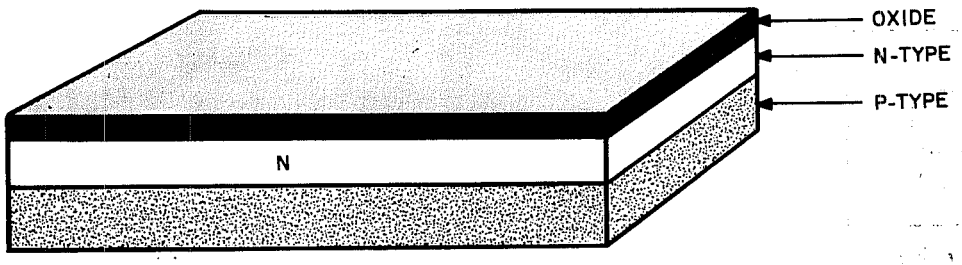


Figure 3-5. Wafer Before Isolation

Upon entering the photo resist room the wafer contains three layers: P-type, N-type, and a layer of oxide. These three layers form the basic starting material for an Integrated Circuit.

STEP 2, SPINNING (Figure 3-6)

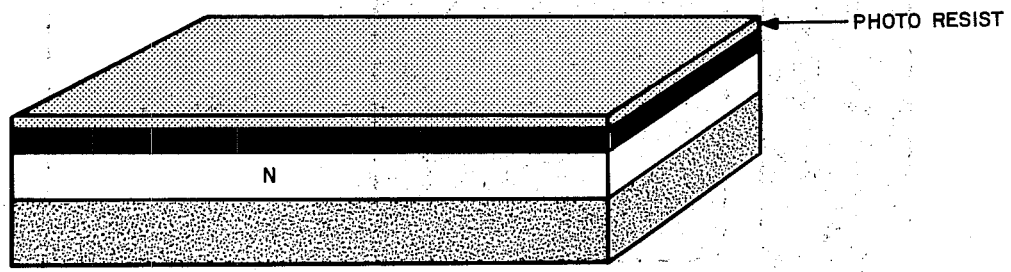


Figure 3-6. Wafer After Spinning

A light-sensitive liquid, photo resist, similar to the emulsion on camera film, is coated over the wafer. A vacuum chuck secures the wafer and the spinning action flattens and smoothes the photo resist to a thin film.

STEP 3, ALIGNMENT AND EXPOSURE (Figure 3-7)

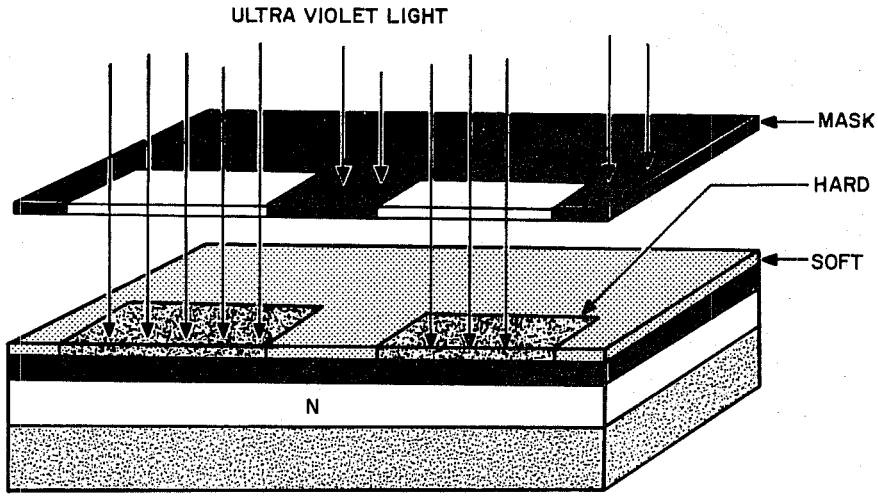


Figure 3-7. Wafer After Alignment and Exposure

The coated wafer is placed on an alignment tool. A mask, carrying a black pattern which is to be reproduced upon the wafer, is correctly oriented over the wafer. The mask and wafer are placed under an ultra violet light. Light going through the clear areas will make the photo resist hard. Light cannot go through the black pattern, so the photo resist under the black pattern remains soft.

STEP 4, DEVELOPING (Figure 3-8)

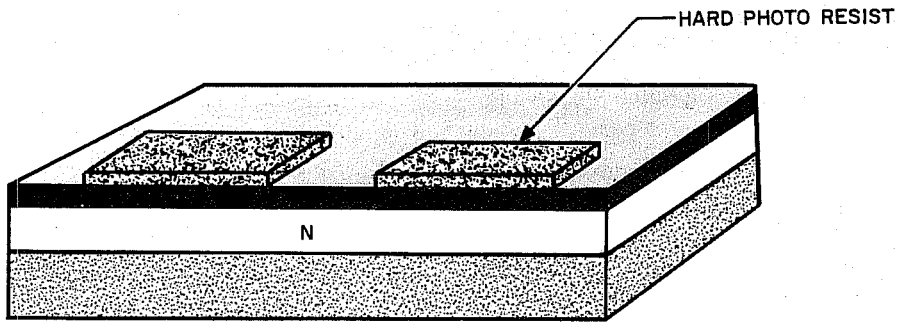


Figure 3-8. Wafer After Developing

A developer solution dissolves or washes away the soft photo resist (area under the black pattern), while the hard photo resist (area exposed to light) remains undisturbed.

STEP 5, ETCHING (Figure 3-9)

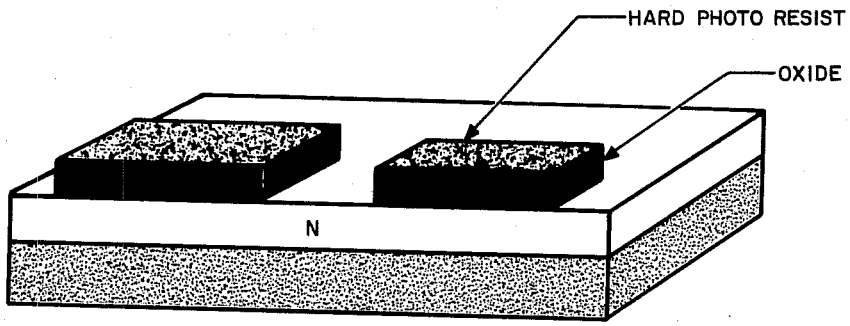


Figure 3-9. Wafer After Etching

Each wafer is submerged in a corrosive acid which eats away (etches) the glass-like oxide. The oxide protected by the hard photo resist remains undisturbed.

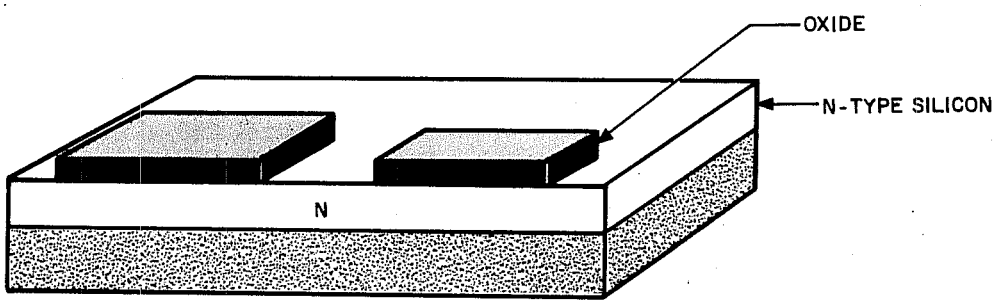


Figure 3-10. Wafer After Cleaning

Each wafer is dipped in another acid solution to wash away the hard photo resist without marring the oxide or N-type silicon.

STEP 7, DIFFUSION (Figures 3-11, 3-12)

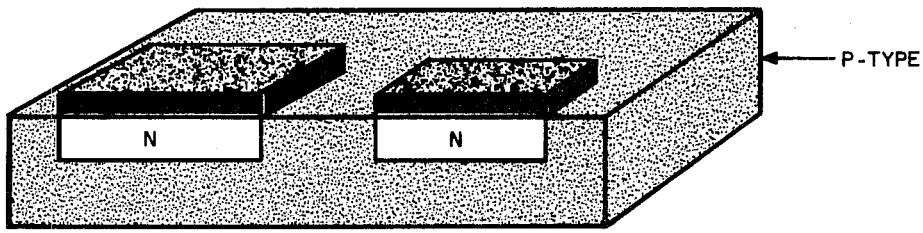


Figure 3-11. Wafer After Diffusion

The first diffusion creates two N-type areas which are isolated from each other by diffusing P-type material through the N-type. This leaves N-type "islands" completely surrounded by P-type material.

To understand how this is done we must first understand the diffusion process. Consider a bucket filled with tightly packed sand. If we pour water into the sand the water will penetrate more or less equally over the entire surface. However, if we cover the surface of the sand with a sheet of glass the water can penetrate the sand only where a crack or hole appears in the glass.

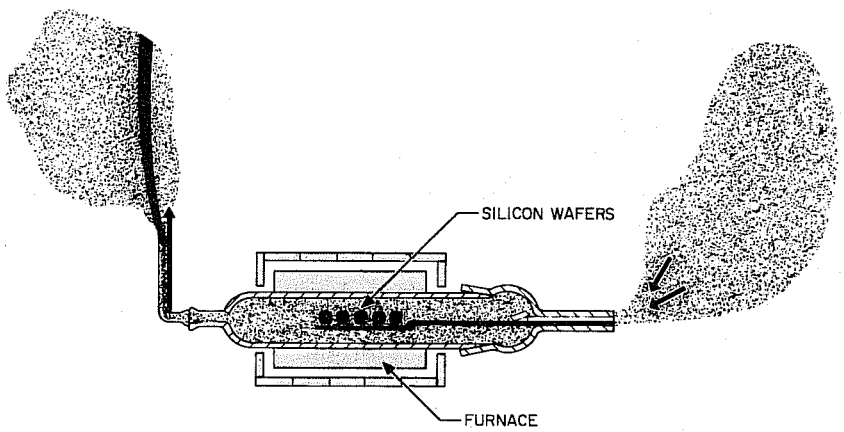


Figure 3-12. Diffusion Process

The diffusion of one type of semiconductor material, say P-type, into a solid wafer of N-type silicon can be done in a manner similar to pouring water into sand. First, silicon wafers are heated red-hot in a furnace. Then a gas containing P-type material flows over the wafers. The wafers, like sand, absorb the P-type material in all areas not covered by glass (oxide). The depth to which the diffusion goes, and the resistivity of the diffusion, depends primarily upon 1) the concentration of impurities, 2) the time span of the diffusion, 3) the temperature and concentration of the material being diffused into.

STEP 8, OXIDATION (Figure 3-13)

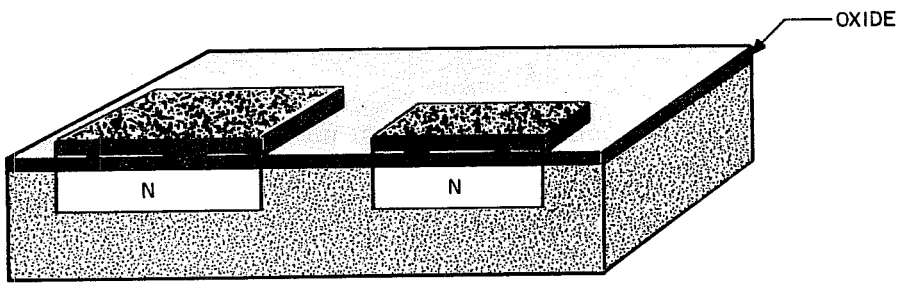
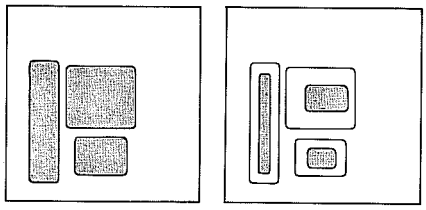


Figure 3-13. Wafer After Oxidation

Upon completion of all diffusion steps another film of oxide is deposited to seal off the entire surface, and to form the basis for the second process step, BASE AND RESISTOR.

SECOND PROCESS STEP - BASE AND RESISTOR



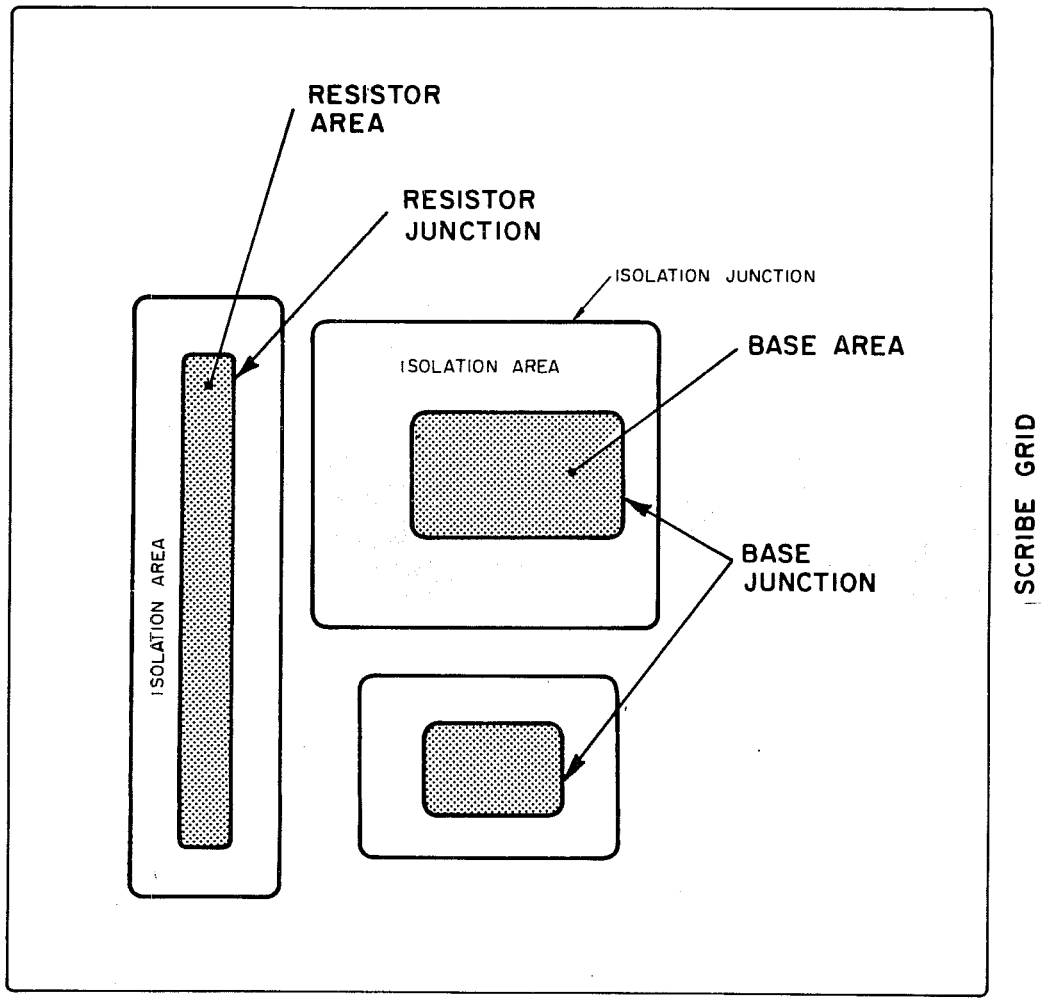


Figure 3-14. Second Process Step

During this process step, base areas are installed inside some of the isolation areas, while long, thin rectangular resistor areas are installed inside the other isolation areas. The base areas and resistor areas are installed at the same time. The dark line around the base area is called the base junction. Similarly, the dark line around the resistor area is called the resistor junction. The scribe grid is also introduced during the base process step. It is the region which separates one integrated circuit from another on a wafer.

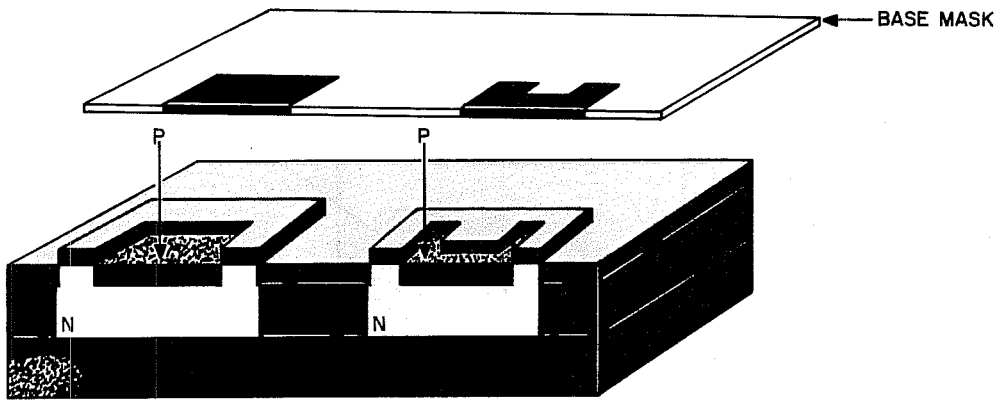
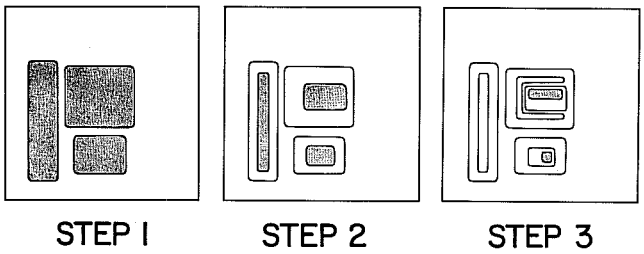


Figure 3-15. Wafer After Adding Base and Resistor Material

Another spinning, masking, developing, and etching step selectively exposes N-type regions (Figure 3-15); then a second diffusion converts these regions to P-type.

THIRD PROCESS STEP - COLLECTOR CONTACT AND EMITTER



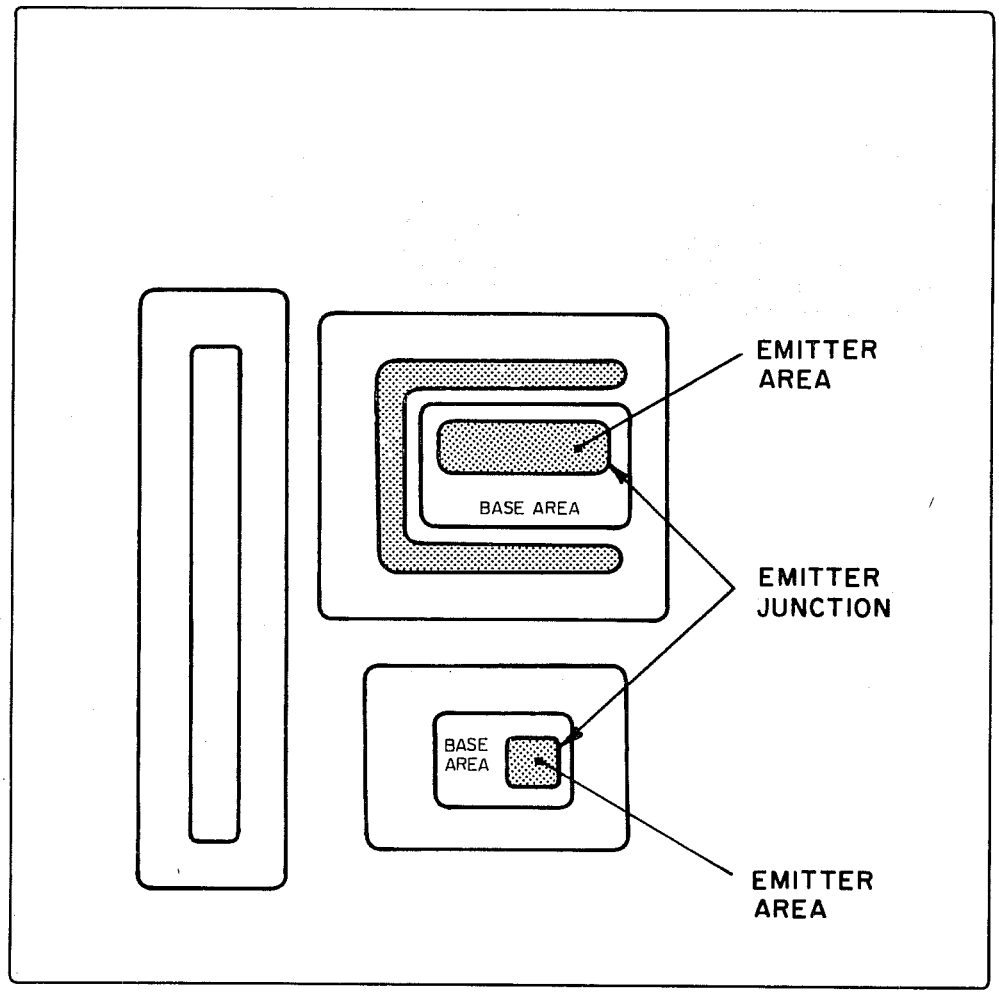


Figure 3-16. Third Process Step

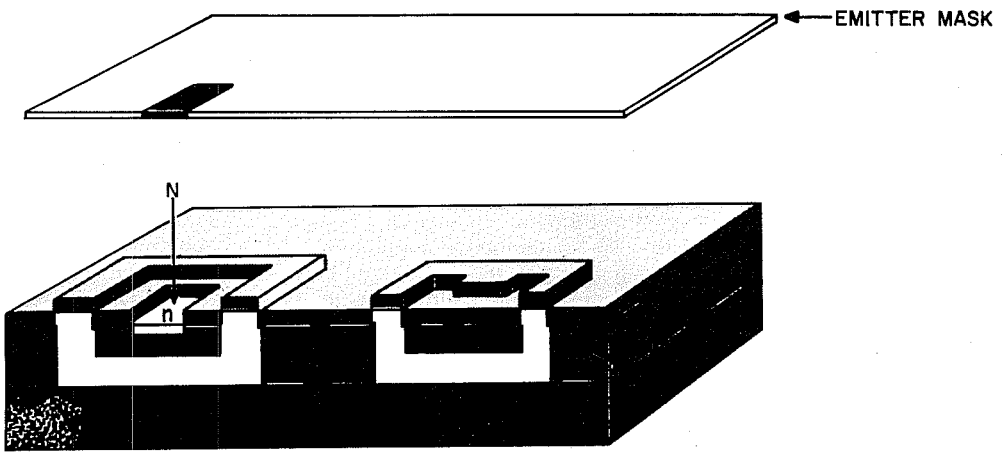
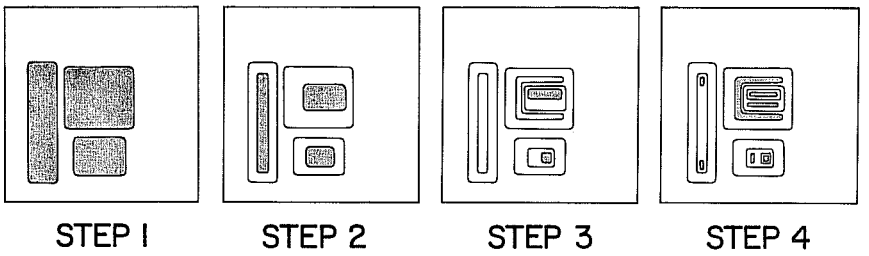


Figure 3-17. Wafer After Emitter Diffusion

Another masking and etching prepares the wafer for the Emitter Diffusion (Figure 3-17). This time the gas carries N-type material which converts P-type regions to N-type. These small regions become the "emitter" of the transistor. Note the region to the right, which will become a resistor, remains sealed off by oxide and thus is not affected by the emitter diffusion.

FOURTH PROCESS STEP - PRE-OHMIC



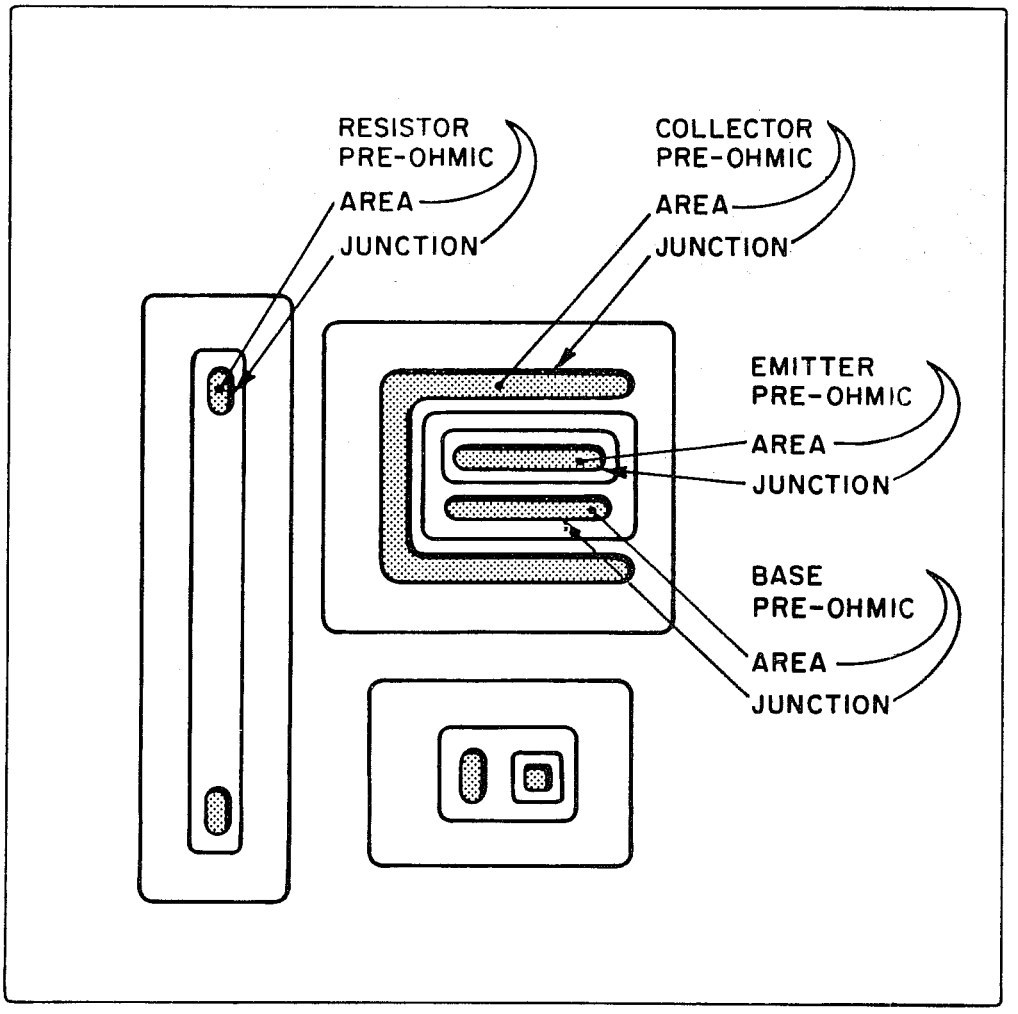


Figure 3-18. Fourth Process Step

The fourth masking and etching step (Figure 3-19) produces a pattern of window-like openings that will enable metal to make contact with the three areas on the transistor (emitter, base, and collector) and two points on the resistor.

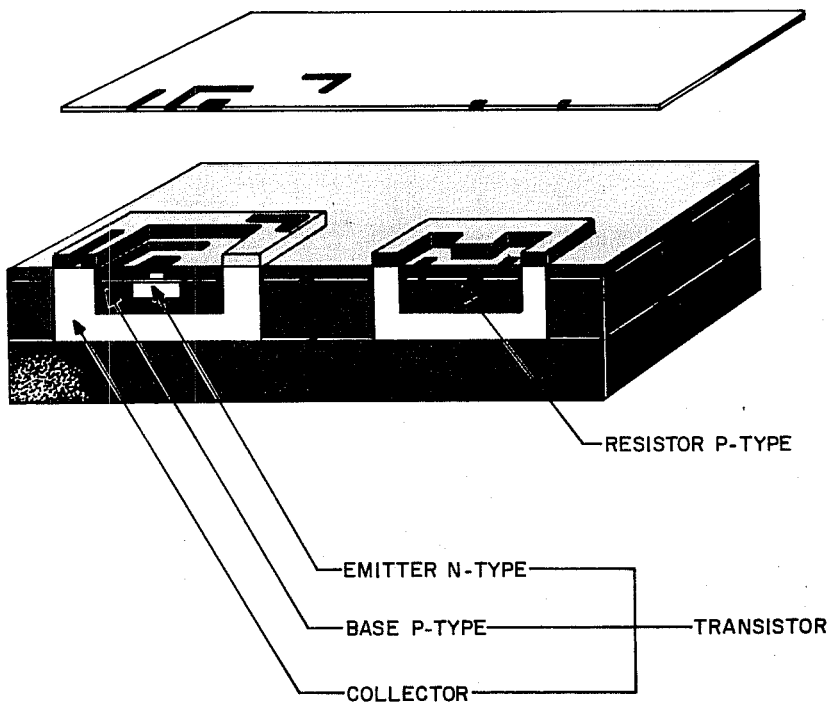
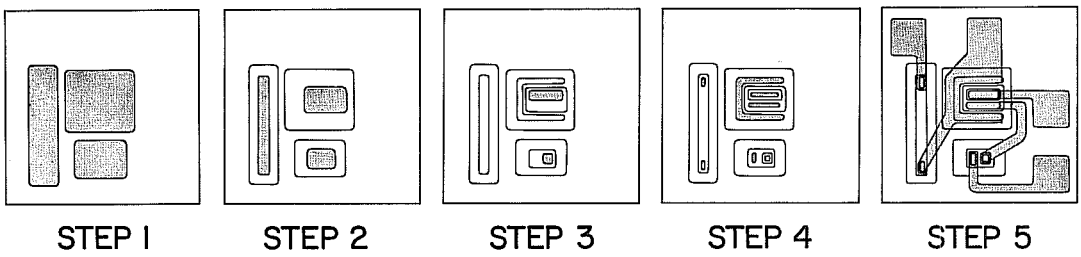


Figure 3-19. Wafer After Pre-Ohmic Process

FIFTH PROCESS STEP - METALLIZATION



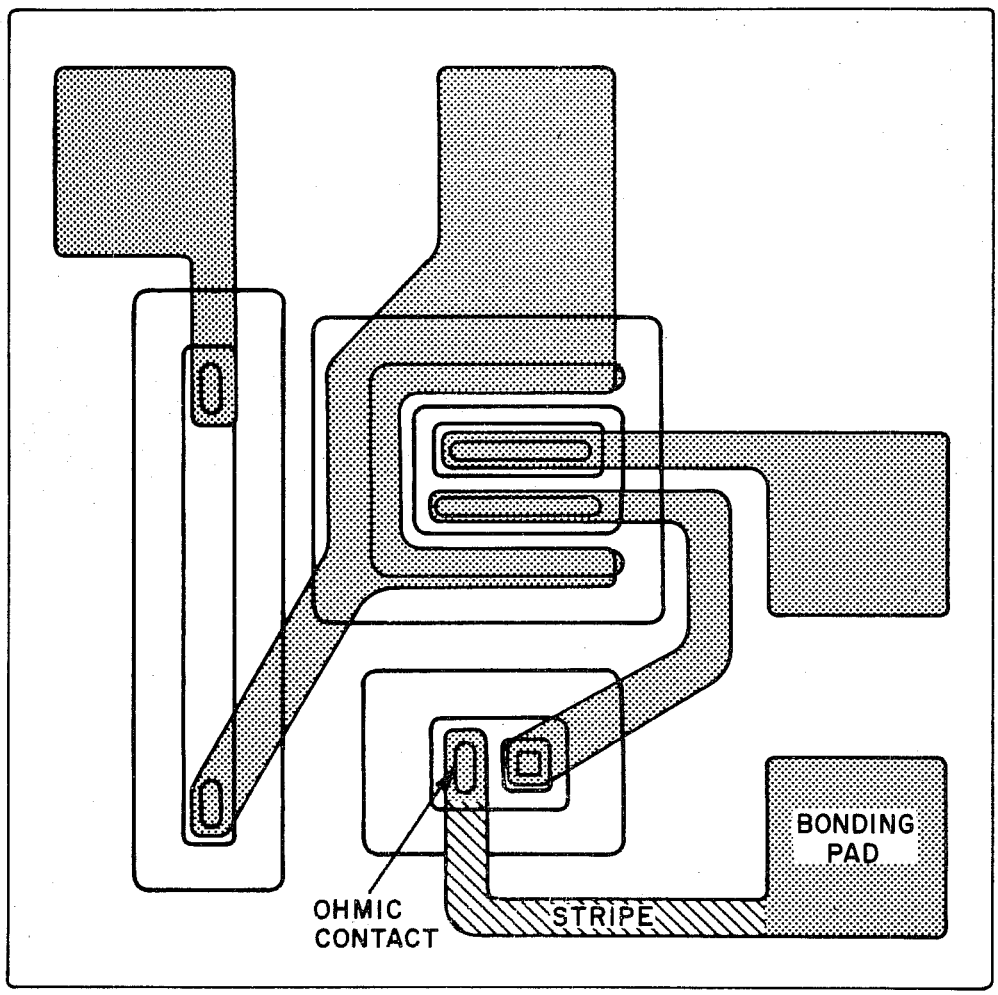


Figure 3-20. Fifth Process Step

STEP 1, EVAPORATION (Figure 3-21)

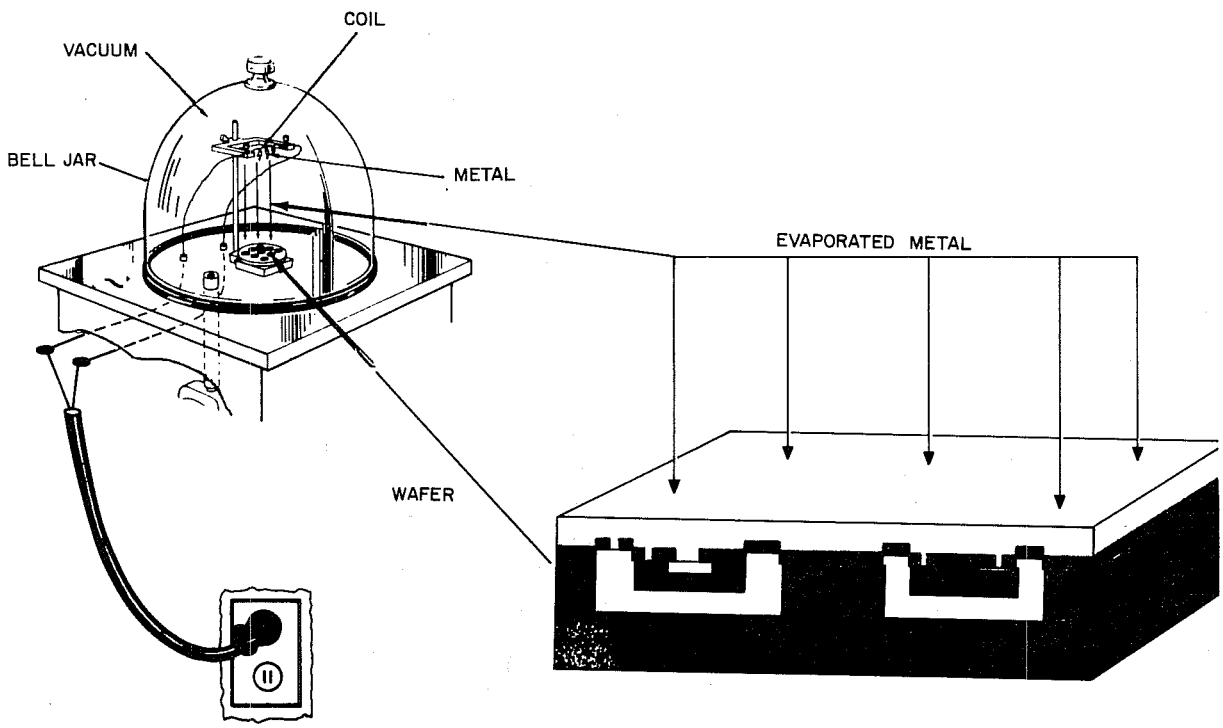


Figure 3-21. Wafer After Metallization Evaporation

Metal contact is made to all areas on the wafer when metal is evaporated over the entire surface. Metal, when heated, evaporates at a boiling point similar to water. Metal evaporation, however, is more complex than water evaporation. When metal is heated by an electric coil in a complete vacuum sealed by a bell jar, the evaporated metal scatters in all directions and accumulates on the surface of the wafer.

STEP 2, MASKING AND ETCHING (Figure 3-22)

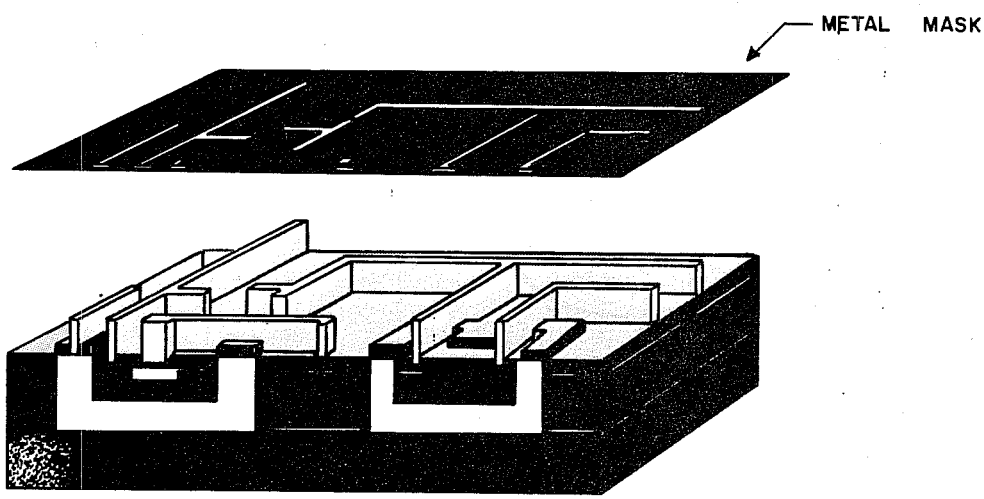


Figure 3-22. Wafer After Metallization Etching

A masking and etching process removes unnecessary metal while the remaining metal creates a network of metal paths that interconnect the various components of the monolithic circuit.

This completes the fabrication of the integrated circuits, and at this point the manufacturing operations take over.

MANUFACTURING OPERATIONS

Testing

At this point each wafer is 100 percent circuit tested; that is, each of the circuits (dies) on every wafer is tested for conformity to dc specifications. If a bad die shows up, a spot of ink or similar identifier is automatically applied to it. This aids in sorting out the bad dies during the scribing operation which follows.

Scribing (Figures 3-23, 3-24)

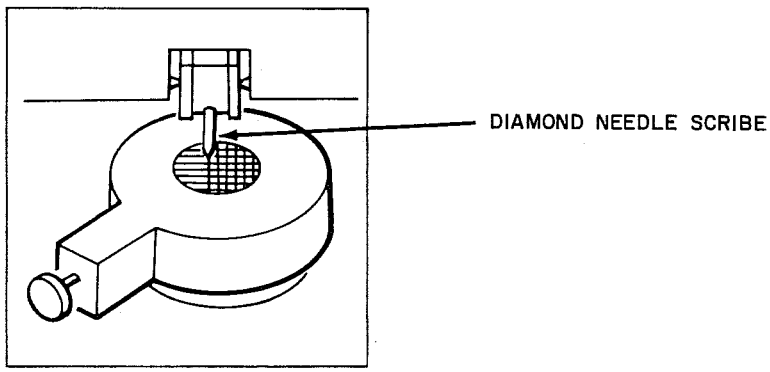


Figure 3-23. Scribing Operation

A diamond needle is used to cut, or scribe, lines into the surface of the wafer, similar to the way a glass cutter is used to cut window panes. The lines weaken the wafer around each integrated circuit, and make it possible to break the wafer into individual integrated circuits, or dies.

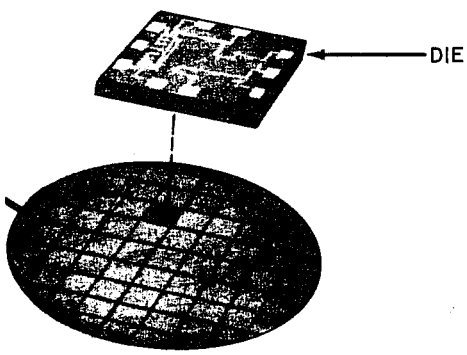


Figure 3-24. Wafer After Scribing

Bonding (Figure 3-25)

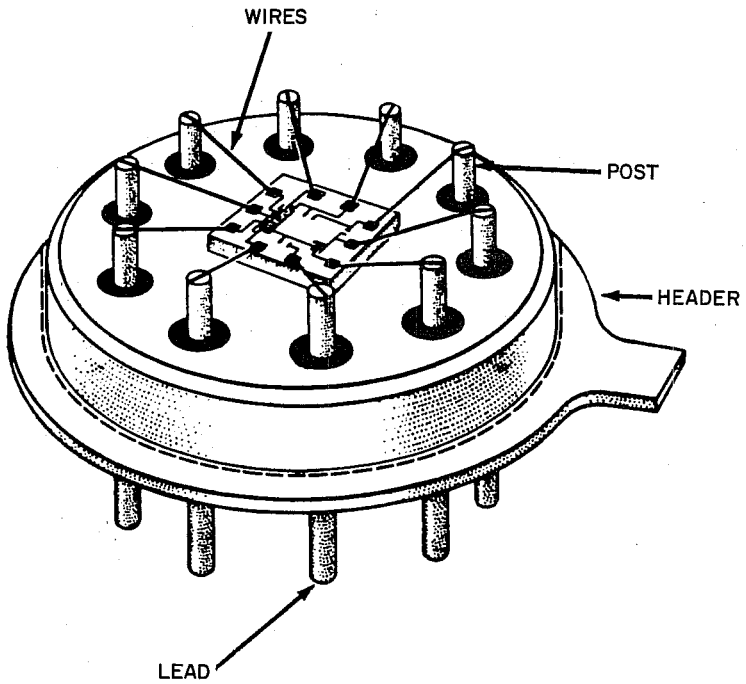


Figure 3-25. Wafer After Bonding

Each integrated circuit, or die, is welded to a container, or header. Fine wires, about 1/3 the thickness of a human hair, are welded from the integrated circuit to each post. Each post goes through the header and forms a lead. Each lead acts as an electrical contact between the integrated circuit and the outside world.

Circuit dies (chips) can, of course, be bonded to flat packages as well as the round can shown in Figure 3-25.

The devices are then sealed, either hermetically or by being encapsulated in a solid plastic. They are then tested to the customer's specifications once again.

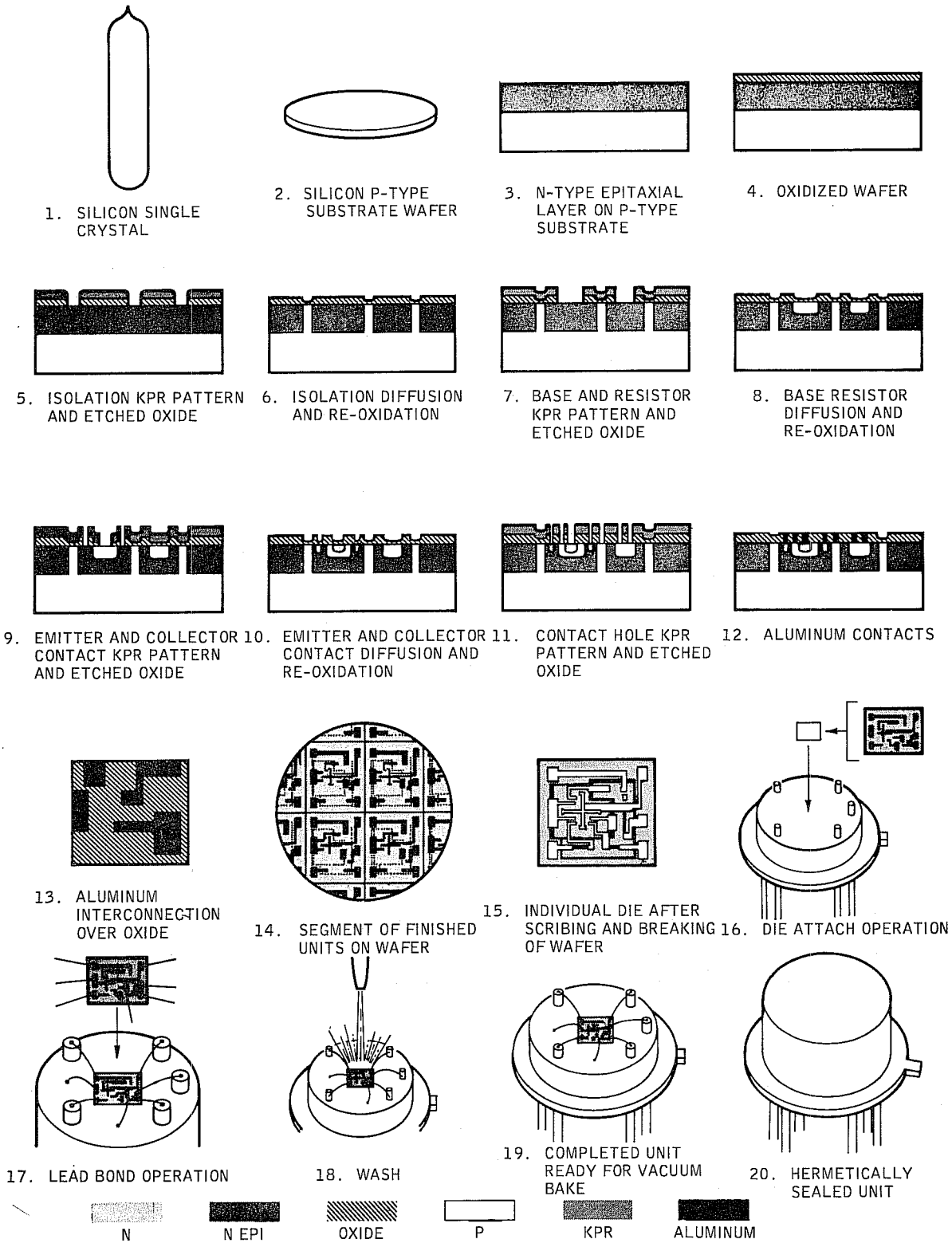


Figure 3-26. Simplified Process Flow Diagram For Integrated Circuit Fabrication

SUMMARY

NOTE

All comments are made with reference to the flow diagram of Integrated Circuit Fabrication, Figure 3-26.

1. Plane that silicon ingot is drawn from is critical - especially for cutting and imperfection count.

2. Sawing, lapping, polishing and etching reduces substrate wafer from 13 mils and 3 mils of imperfections to 5 mils and ≈ less than 0.01 mils of imperfections (this tolerance needed to continue).

3. Approximately 10 microns thick, high resistivity material.

4. Preparation for selecting isolation pattern.

5. All oxide holes are done in the same fashion.

   a. Application of photographic processing material (KPR in flow diagram) usually by spinning process.

   b. Aligning a mask over surface (tolerance less than 0.05 mils).

   c. Taking photograph of mask on silicon.

   d. Etching away oxide to expose window usually acid of HF and catalyst to control process.

   e. Removing all photographic material from oxide.

6. Two-step process

   a. Furnace brought to ≈ 1175°C before impurity concentration is introduced (wet cycle).

   b. Turn off impurity and keep wafer in furnace with heat at the same level (dry cycle).

This drives the P-type material through the epitaxial layer and into the P-type substrate, thereby isolating the epitaxial regions from one another.

Using only the wet cycle causes an erf function distribution gradient of the junction. Using both wet and dry cycles causes the distribution gradient to be Gaussian in nature.

The cycle process used determines, among other things, the value of the exponent "n" in the junction capacitance Formula shown in the Glossary.

7. Repeat 5 for base and resistor holes.

8. Repeat 6 but for significantly shorter time. (Remember isolation material had to be driven in over 10 microns, whereas the base penetration is typically 2-4 microns.)

9. Same as 6.

   Note that collector contacts are also cut now. Strange things happen when aluminum and N-type silicon material are fused together. The combination produces a P-N junction. To avoid this, N+ is diffused at collector contacts.

10. Same as 6, but now only the wet cycle is used. This impurity concentration is driven to within approximately 0.1 - 0.4 microns of the base diffusion thickness to obtain high f_T and high β transistors.

11. Usually the emitter is left exposed and only the base contacts are cut here.

12-13. Present techniques combine these two steps to form a single aluminum interconnection and contact process.

14. Circuits per wafer now run from 200 to 1000.

15. Done with automated diamond tip scribing needle and step-and-repeat machinery.

16. This shows a TO-5 can with six leads. Most circuits are now mounted in flat packages because of handling ease and the number of pins. The package header is heated and the die is "scrubbed in" for proper adherence to the package base.

17. Two categories; three types

    Thermal Compression Bonds

    a. Scissor Bond - in which scissors cut the lead wire after a thermal bond has been made.

    b. Ball Bond - in which a flame cuts the lead wire, producing another "ball" which is ready to be used for the next bonding.

    Ultrasonic Bonding

    c. Vibrations ultrasonically bond the lead wires to the package and the die. The same technique shears the lead after the bond has

been made. This has the advantage of operating under cool temperatures whereas the other two techniques require heat to produce proper bonding.

18. Step done to clean impurities from surface.

19. Stabilizes the circuit and burns off any impurities that have gathered on the surface.

20. Several methods used here, the newest of which is epoxy.

TABLE 3-1. INTEGRATED CIRCUITS, STEP-BY-STEP PRODUCTION YIELD

BASIC OPERATION	AVERAGE YIELD (%)	TYPICAL CAUSES FOR REJECTION	REMAINING CIRCUITS
1. Start	-	-	100
2. Channel Diffusion	95	Poor isolation of epitaxial layer	95
3. Base Diffusion	90	Sheet resistance out of spec.	86
4. Emitter Diffusion	85	"Punch Through" - emitter too deep	72
5. Metallization	90	Breakage - poor handling	66
6. Wafer Testing	75	Devices not to spec.	49
Processing Yield	49	-	-
7. Wafer Scribing	85	Uneven breakage	42
8. Die and Wire Bond	85	Damage in handling; open wires	35
9. Packaging	95	Improper sealing	34
10. Final Testing	75	Circuits not to spec.	25
Assembly Yield	51.5	-	-
Total Yield	25.2	-	25

In Table 3-1, the average yield percentages are given in relation to the number of units processed for any step. For example, in step 8, of the 42 circuits that reach that step, about 35 (or 85%) will be satisfactory. These figures represent yield for a circuit of average difficulty to fabricate in production quantities. Tighter specifications and/or increased number of components would, of course, lower the yield.

CHAPTER 4
DESIGN CONSIDERATIONS

INTEGRATED CIRCUIT RESISTORS

Since the majority of the resistors are made during the transistor base diffusion, considerations must be given to the transistor. Experimentation, calculations and EXPERIENCE, have showed that 100Ω per square to 200Ω per square base sheet resistivity give a good compromise between resistor values and transistor performance. At certain occasions, however, 50 Ω per square base material is used. This indicates to the designer that the 50 Ω should be the lower limit of the resistor size in his design. Due to the fact that price is based to a great extent on physical size, 20 KΩ is a high limit. Although camera reduction and mask-making techniques contribute some element of error in resistor values, diffusion concentrations, gradients and depths contribute the largest tolerance error. If possible, ±20% should be used although ±10% is not unreasonable in modern circuits. Whenever possible, however, the designer should design around ratios of resistor values. The monolithic process lends itself directly toward tight ratio control and here a deviation of ±2% is not unrealistic.

Since parasitic capacitances exist, the resistor size also determines maximum frequencies of circuit operation when the resistor sizes become too large. Since the resistor is laid out in Ω/square, when small resistors are required the length-to-width ratio can be made small by making "fat" resistors. Here, however, the capacitance associated with these resistors also will be large. Temperature coefficients for diffused resistors are positive in the regions where most circuits operate and are usually larger than discrete resistors, or evaporated and sputtered types. A rule of thumb for $\Delta\Omega/C^{o}$ is difficult, for it varies as the sheet resistivity. Rough guide lines are: 100 Ω /square, 0.2 Ω /C^{o}; 200 Ω/square, 0.5 Ω /C^{o}. Since, however, the resistors track, this offers very little difficulty in most designs. Methods of obtaining 2Ω/ square and 3000 Ω / square are also available but both offer ±30 to 250% tolerances. These techniques should be used only when nothing else works or the resistor tolerances are acceptable.

Figure 4-1 shows the equivalent circuit of a resistor and a cross-section of that resistor. Figure 4-2 illustrates two diffusion techniques used to obtain extremely small and extremely large resistors.

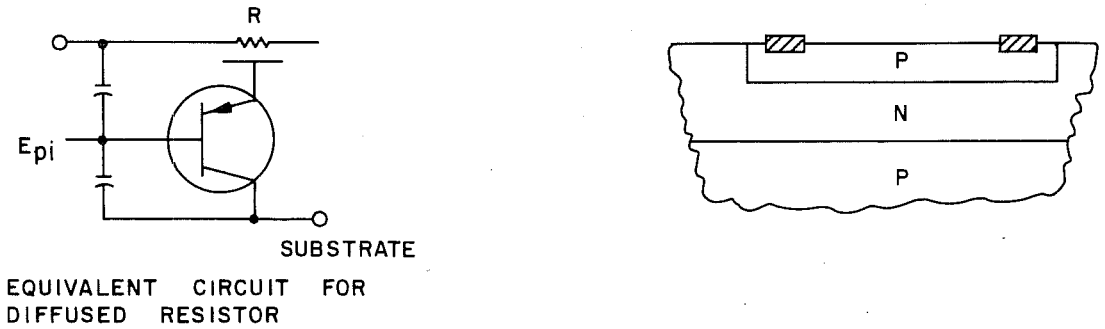


Figure 4-1. Equivalent Circuit of a Resistor

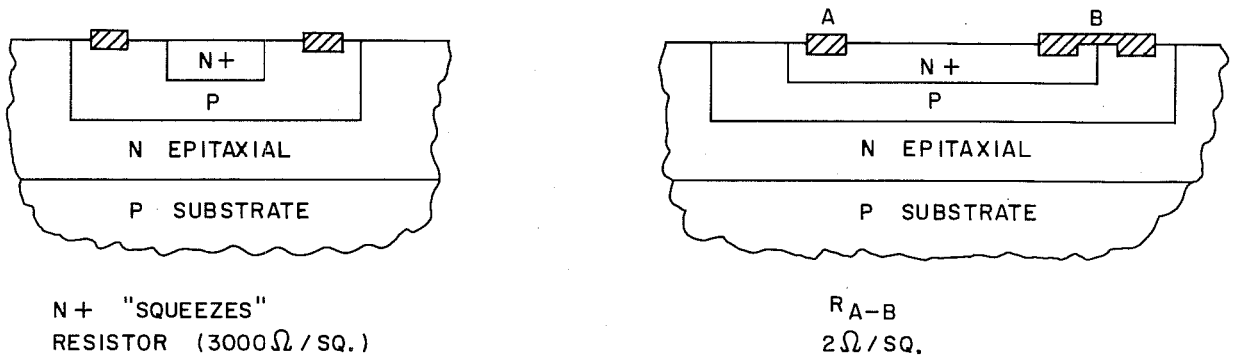


Figure 4-2. Two Diffusion Techniques

NPN versus PNP

To put both NPN's and PNP's on the same chip degrades the optimum performance of each. This is because one type influences the other during diffusions. There are two common types of PNP transistors -- lateral and isolation. Beta values of 10 are typical.

An isolation PNP transistor uses the normal resistor (P) diffusion as its emitter, the epitaxial material (N) for the base, and the P-type substrate as the collector. The collector is always at the most negative voltage of the circuit in this case. Also it is worth noting that W, the effective base width, is the distance between the resistor diffusion and the substrate ($\approx$ 6 - 8 microns). This is the main reason for low f_τ and low beta devices.

The lateral PNP uses two closely diffused resistor diffusions as the emitter and collector. The epitaxial material again is the base. To keep the base width (the distance

between the two resistor diffusions) as narrow as possible, the epitaxial (base) contact is brought out elsewhere. This creates a large r'_b parameter which slows the device down. The base width can be fabricated with 2 to 3 micron base widths, but great alligment and mask precautions must be made. One method used to increase the dc current gain of the lateral PNP is to connect the PNP emitter to an NPN collector and the collector of the PNP to the base of the NPN. The base of the PNP, emitter of the PNP, and emitter of the NPN create an effective PNP with significant dc gain. This, of course, does not improve the high frequency response of the new PNP.

Transistor Design

As pointed out earlier, the transient response of a transistor is directly proportional to the effective junction areas. The emitter current, however, is directly proportional to the effective emitter periphery. The effective emitter periphery is defined as that periphery of the emitter that faces the base contact. A rough, but fairly accurate rule of thumb to abide by in design is 1 to 2 ma of current for every mil of effective emitter periphery.

Figure 4-3 will help clarify this.

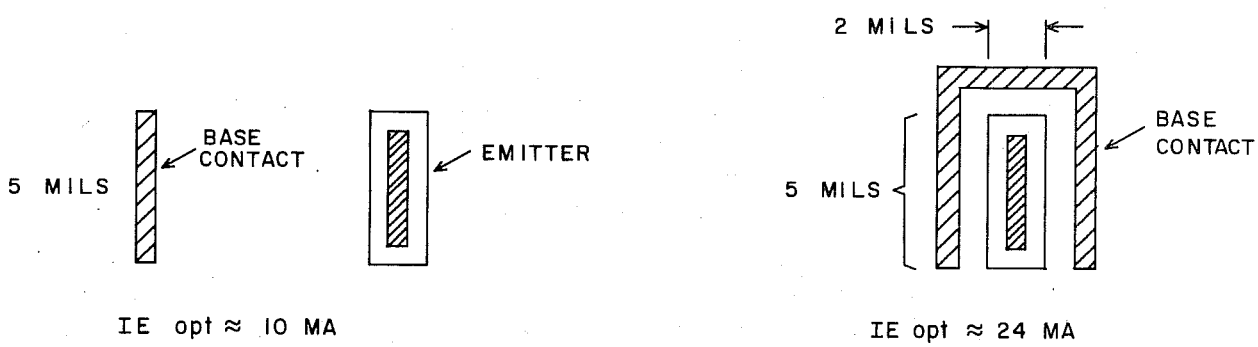


Figure 4-3. Calculating the Emitter Periphery

Figure 4-3(b) has the same emitter-base junction capacitance but uses over 2.2 times of its periphery by wrapping the base contact (interdigitating) around the emitter.

The emitter diffusion should be driven in as close to the collector as BV_{CEO} and the technology allows. This is due to the fact that $f_T \propto \frac{1}{W^c}$, where $W = 1_b - 1_e$, and 1_b and 1_e

are the distances of the respective diffusion depths. Typical thicknesses on high speed transistors are: 0.4μ = W for $f\tau$ 1000 MHz.

To obtain high-speed, high-current transistors, the following ground rules should be the goals:

a) Small r_{SAT} (collector-emitter saturation resistance)

b) Small junction areas, (lower C_{OB}, C_{BE})

c) Long effective emitter periphery

d) Small collector-substrate areas

e) Shallow diffusions

The advantages of IC transistors over discrete components are:

1) Tracking

2) Optimum design for circuit

3) Price per component

The disadvantages include:

1) High r_{SAT} (10 - 100 Ω vs 5 - 10 Ω)

2) Parasitic capacitance degrades the performance of the device.

Resistor versus Diodes and Transistors

Since resistors take up more area than either diodes or transistors, the latter two should be used whenever possible. You pay for area, complexity, testing (yields).

It is possible to make an integrated circuit diode by utilizing either the emitter-base junction or the collector-base junction, as shown in Figure 4-4. These two P-N junctions can be interconnected in several ways to provide different transient characteristics:

1. Emitter-base diode; collector open
2. Emitter-base diode; collector-base short
3. Emitter-base diode; collector-emitter short
4. Collector-base diode; emitter open
5. Collector-base diode; emitter-base short

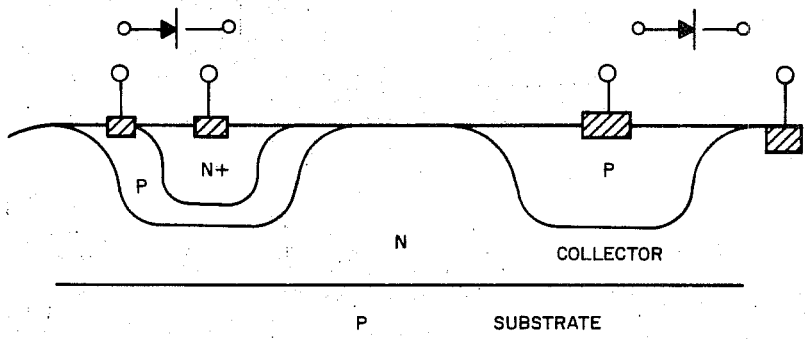


Figure 4-4. P-N Junction Diodes

Capacitors can also be made using P-N junctions. The capacitance is equal to:

$$C = A \sqrt[n]{\frac{KM}{V}} \qquad n = 3 \text{ or } 2 \text{ depending upon junction used.}$$

The maximum capacitance per square mil is $\approx 1\ \mu\mu f$. Therefore, extremely large junctions would be needed to get large capacitors. Another shortcoming of this type of capacitor is that the capacitance value is inversely proportional to the junction potential.

Another technique is the metal-oxide silicon capacitor. This capacitor has a value of 0.2 to 0.5 pf/mil^2 for oxide thicknesses of 500 to 1000 Angstroms. The breakdown voltage of the capacitor is 20 to 40 volts. Figure 4-5 shows this type of capacitor.

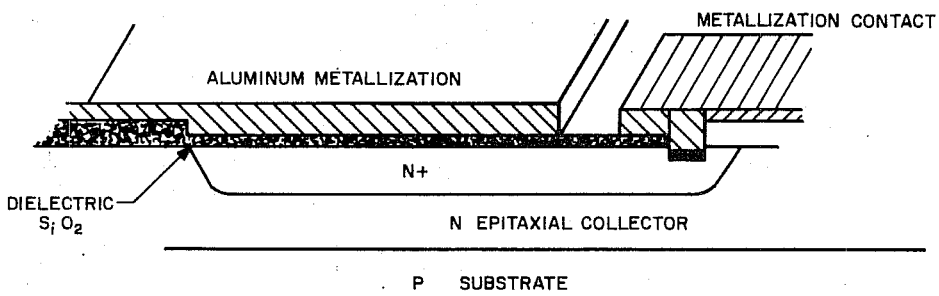


Figure 4-5. Silicon Diode Capacitor

New techniques in oxide control have had success in raising the capacitance value to 1 pf/mil^2. Values of 150 - 200 pf should be considered maximum monolithic values. If bypass or low frequency coupling and/or decoupling capacitors are required, hybrid techniques should be considered; but vendors will then have packaging problems in some cases.

Inductors are to be avoided completely, because of the impossibility (nearly, anyway) to fabricate. To date, only extremely small values with low Q have been obtained. The areas that they occupy are also quite large.

CHAPTER 5
CIRCUIT DESIGN CONSIDERATIONS

To further investigate the advantages and limitations of monolithic circuits used in digital circuit design, four popular types of logic circuits are discussed. Also included in the discussion will be certain design considerations that monolithic manufacturers use to overcome certain inherent limitations in the processes described to date.

DTL (DIODE-TRANSISTOR LOGIC)

Figure 5-1 shows the logic diagram and schematic of a popular DTL logic inverter.

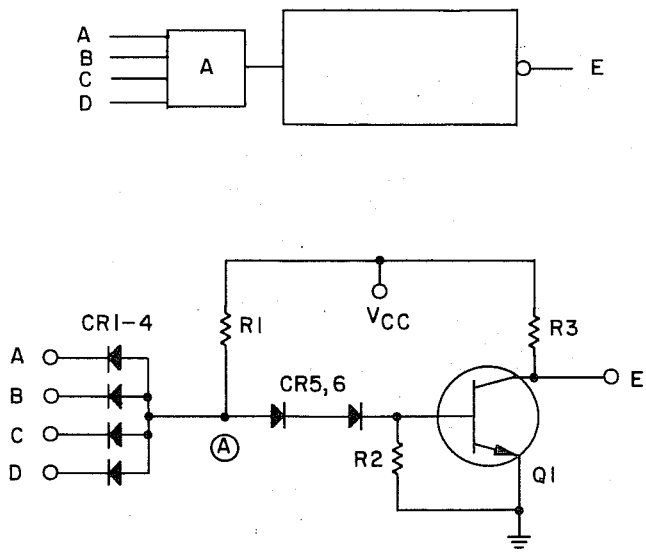


Figure 5-1. DTL Logic

Features of inverter and components:

a) High speed diodes CR1 - CR4
b) Charge storage diodes CR5, CR6
c) Low $V_{CE\ (sat)}$ on Q1 at high fan-out currents
d) High f_T on Q1

e) Low C_{OB} on Q1

f) Low capacitance to ground at point Ⓐ

g) Low t_s storage time

Obtaining Low $V_{CE\ (SAT)}$

As previously discussed, low $V_{CE\ (sat)}$ is a compromise with epitaxial material. A high $V_{CE\ (sat)}$ due to the high resistivity required for low C_{OB} is a compromise which is normally made. To overcome this, a method of maintaining high resistivity around the base diffusion and low resistivity beneath has been developed. This diffusion is performed prior to epitaxial growth into the P-type substrate. The diffusion is made only where the collector contact and base diffusions are made. The resistivity of this diffusion is extremely low (0.01 - 0.05Ω per square). Figure 5-2 illustrates this diffusion. It might also be noted that this diffusion is commonly called "buried layer", or "N + slug" by the industry.

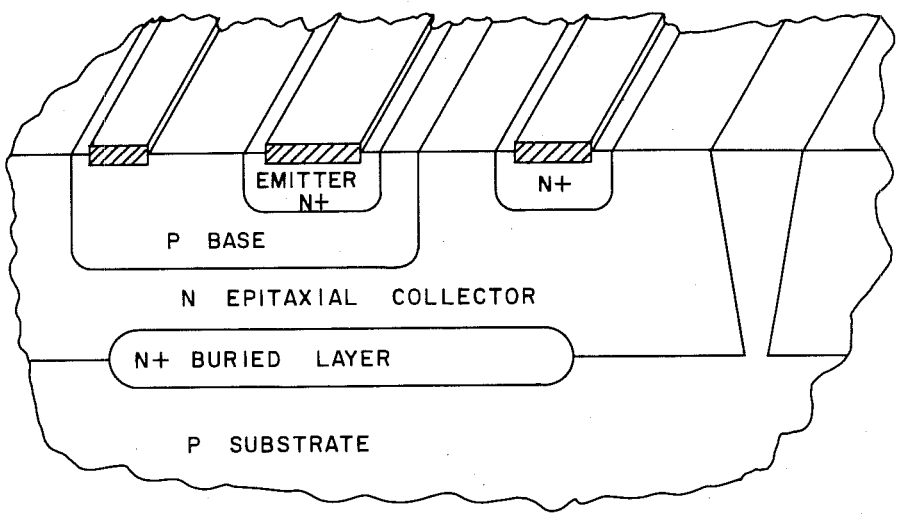


Figure 5-2. Illustration of "N + Slug

Input Diode Considerations

To obtain the fastest input a base-emitter, collector-base short type diode is used because of the effective elimination of the collector-base capacitance by shorting it out. This diode has the lowest reverse breakdown of all types, however ($\approx$ 5-7 volts). Also, since point Ⓐ (Figure 5-1) must have a low capacitance to ground to maintain high speeds, the collector-base short is far from ideal. Figure 5-3 shows the effects of this type of diode design.

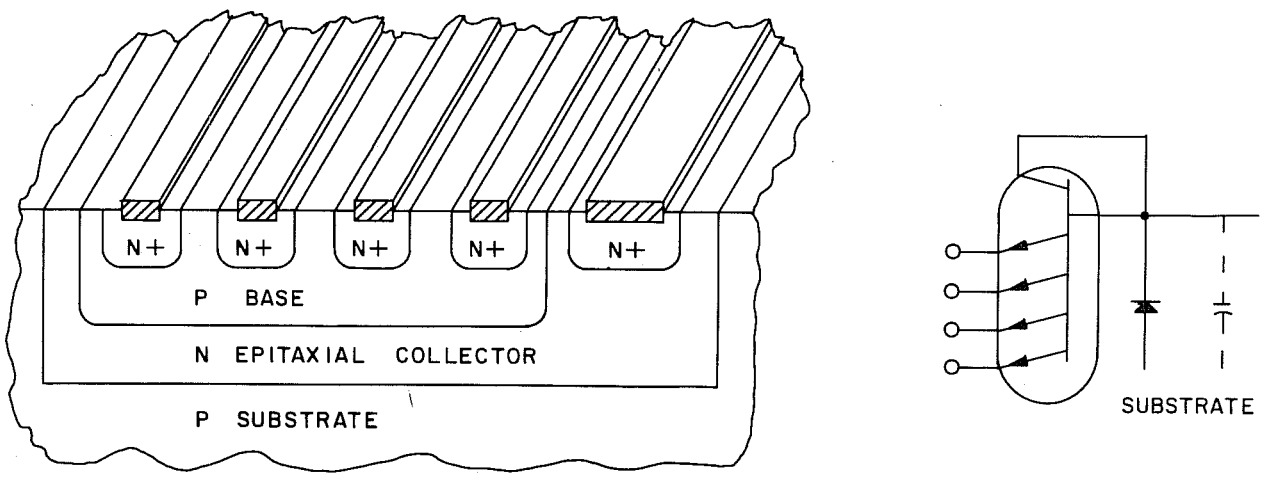


Figure 5-3. Collector Base Short (Emitter-Base Input Diodes)

Note especially that this type of diode cluster creates an extremely high capacitance at point Ⓐ to substrate (ground). By floating the collector and not connecting it to the base region, the collector substrate will be reduced by the series collector-base capacitor. This method is used quite commonly in industry. To maintain high breakdown voltages the collector-base diode must be used at the input. Since the collector junction is N-type, each must be separated by an isolation region. This would then put the collector isolation junction at the output. Figure 5-4 illustrates this type of diode.

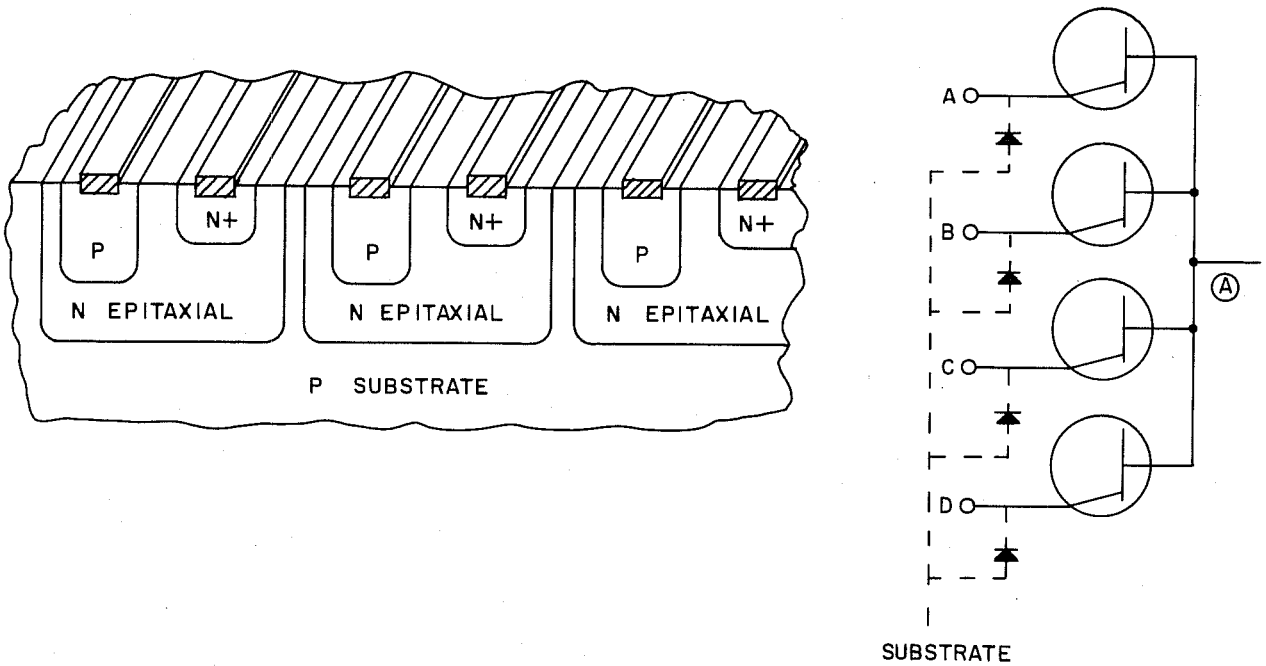


Figure 5-4. Collector-Base Input Diodes

The Level Shift Diodes

CR5 and CR6 (Figure 5-1) are used primarily to produce proper logic levels and obtain improved noise margins. During turn off delay times, however, these diodes must remove excess charge that is stored in the base region to reduce the delay. To accomplish this, a diode that stores charge should be used. This can be accomplished by several techniques. One method would be to use the base-emitter diode and design large junction areas to increase capacitance. This would also increase shunt capacitance to ground, however, and slow the response of the gate. To minimize short capacitance, it would be desirable to place both diodes in one isolation region, if the design trade-offs allow. One method of doing this would be to have CR5 a base-emitter diode and CR6 a collector-base diode. Many designs have used this, but speed limitations have occurred because of the fast turn off times of CR5. Collector-base diodes in separate isolation regions are common.

To further improve the fan-out current/base current ratio, it would be desirable to increase the resistor R_1, and if possible, reduce resistor R_2 to aid in turn-off delay. This is accomplished at no extra cost in a monolithic circuit by replacing CR5 by a transistor and tapping an increased resistance (R_1). Figure 5-5 shows this circuit. The transistor Q_2 has current gain to sufficiently drive the base of transistor Q_1. A decrease in switching time over the conventional DTL gate is achieved along with greater fan-out (loading).

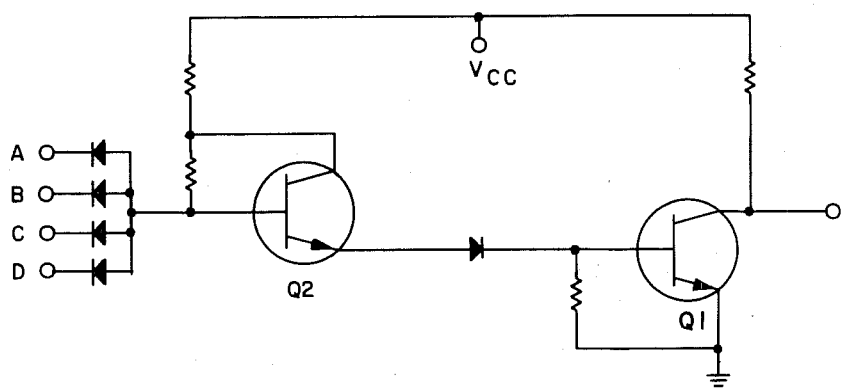


Figure 5-5. Improved DTL Circuit

Figure 5-6 shows the circuit with all of its parasitic diodes. The dashed lines tying to V_{CC} indicate the N portion of the resistor parasitic diodes which result because the resistors are diffused into the epitaxial layer in the same isolation region.

The bar alongside each resistor represents the distributed anode of the parasitic diode created when the P-type resistor (base) is diffused into the N-type epitaxial layer.

The other parasitic diodes are the epitaxial layer substrate diodes inherent in the monolithic process.

Note that the resistor shunting the base-emitter junction of the output transistor is not in the same isolation region as the other resistors.

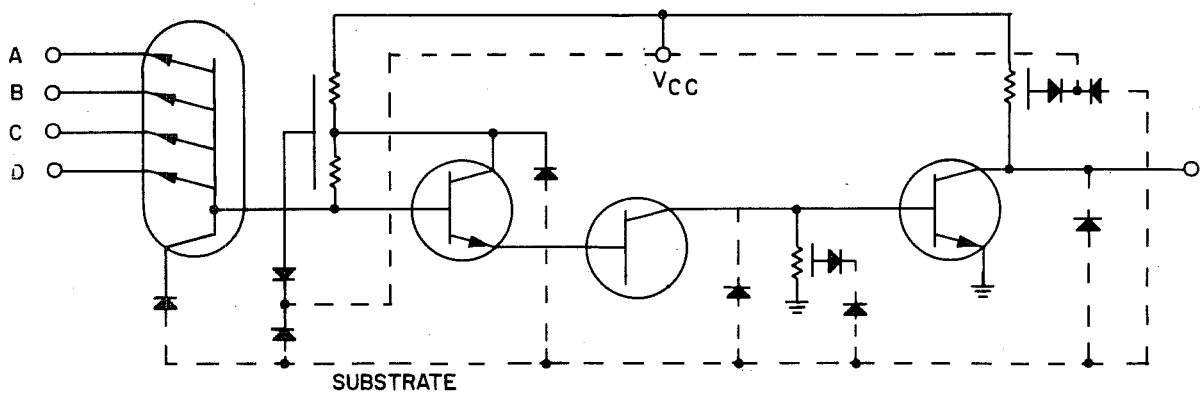


Figure 5-6. Parasitic Diode Effects of Improved DTL Monolithic Circuit

TTL (TRANSISTOR-TRANSISTOR LOGIC)

To obtain faster saturated logic, some sort of device was required to aid the transistor in turn off delay due to: a) the storage problem and b) the capacitance loading problem. To overcome these two difficulties to a great extent and lower delay switching speeds from 15-20 nsec to 7-10 nsec, the circuit in Figure 5-7 is used. (Note that TTL circuitry would be extremely difficult to implement if it weren't for monolithic circuit technology.)

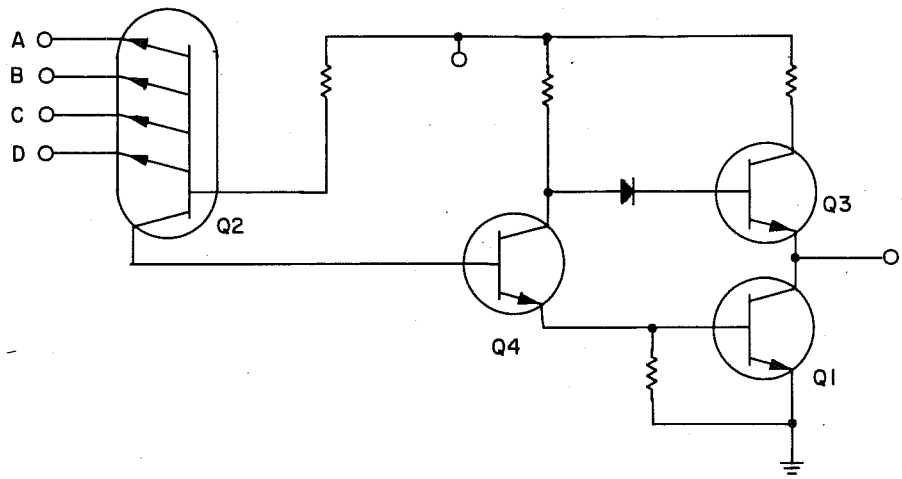


Figure 5-7. TTL Circuit

During turn off delays, (any input drop to a low logic level) the multi-emitter input Q_2 acts as a transistor and removes the charge stored in the base of Q_4 and Q_1. When driving high capacitance loads, the collector voltage at Q_2 can only rise at $R_L C_L$ time constant rate, even though transistor Q_2 begins to turn off. To improve this, transistor Q_3 is placed in a "totem pole" position as shown. This transistor turns on only during the turn off transition and drives current out onto the load line, thus charging the load capacitance. For a very short time, however, both Q_3 and Q_1 are turned on during this transition, and the ground and bus currents become excessive. Since this device has very high noise immunities, this current is usually tolerable. Adequate decoupling of the bus is required, however. This circuit is the fastest high-noise-immunity circuit on the market, and it sells with a complete family of military and commercial circuits including registers, expanders, double level circuitry, buffers and drivers.

CTL (COMPLEMENTARY LOGIC)

Complementary logic is a form of logic mixing PNP and NPN transistors as logical AND elements and inverters to reshape the signal. The circuit types include, AND gates, input buffers, dual rank flip flops and inverter stages. The AND gates have advertised switching times of 3-5 nsec with voltage swings of greater than 2.5 volts.

Construction

To build this unique family of circuits, one new technique has been introduced. A p+-type diffusion is diffused into the p-type substrate prior to epitaxial growth to create the isolation diffusion. During epitaxial growth (base diffusion, and emitter diffusion), the p+ material diffuses into the epitaxial material. The end result is a p-type isolation similar to the triple-diffused techniques. The substrate becomes the collector of the PNP transistors, the epitaxial material is the base, and the p-type resistor diffusion becomes the emitter. The epitaxial material is approximately 5 microns thick and the base (PNP emitter) diffusion is diffused approximately 4 microns. The effective base width (W) is 1μ. This limits the frequence response of the PNP device to less than 40 MHz.

Figure 5-8 illustrates the pre-diffusion technique while Figure 5-9 shows a schematic of the basic AND gate.

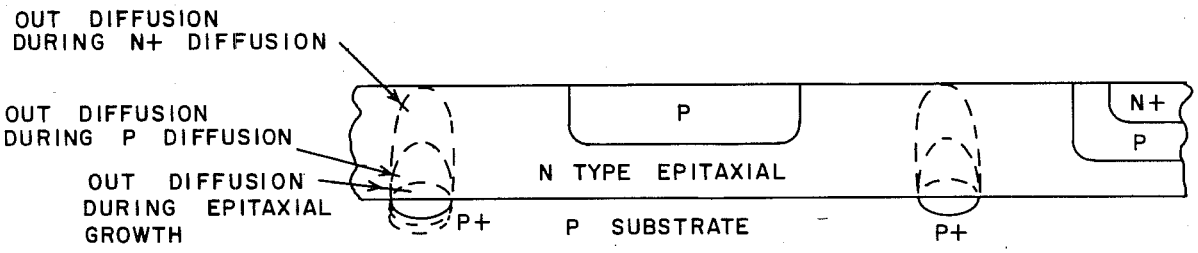


Figure 5-8. Pre-Diffusion For Isolation

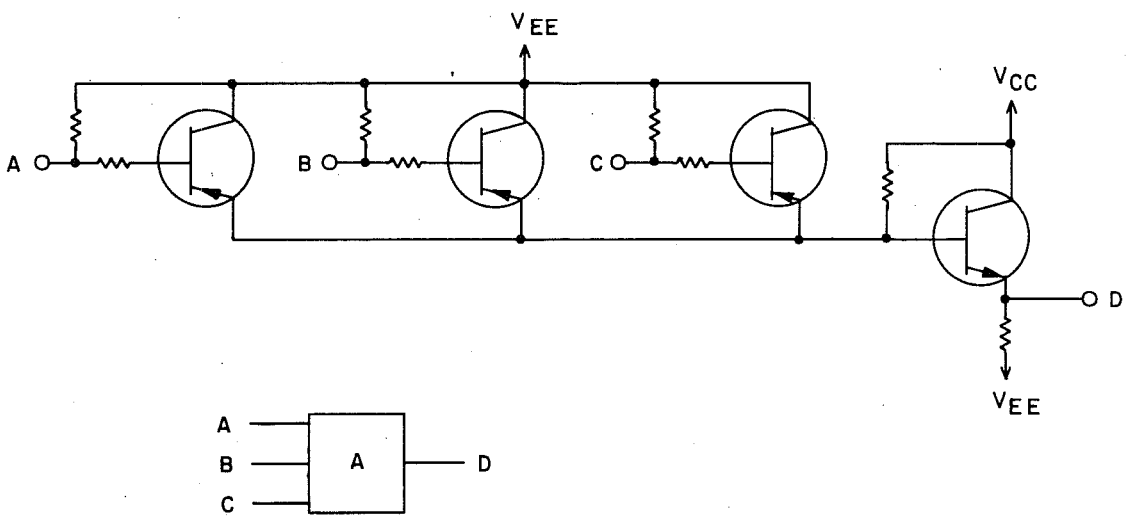


Figure 5-9. Schematic and Logic Diagram of CTL AND Gate

The logic levels for the gate are typically -0.5v to +2.5V. As the fan-out of the gate increases, the V_{BE} drop of the NPN transistor exceeds the V_{BE} of the PNP, thus reducing the gain of the logic gate to less than 1. After several serial delays, the waveform must be reshaped to restore the proper logic levels and maintain adequate noise immunities. To accomplish this, a saturated logic inverter with propagation delays of 9-13 nsec is used.

Figure 5-10 illustrates this schematic.

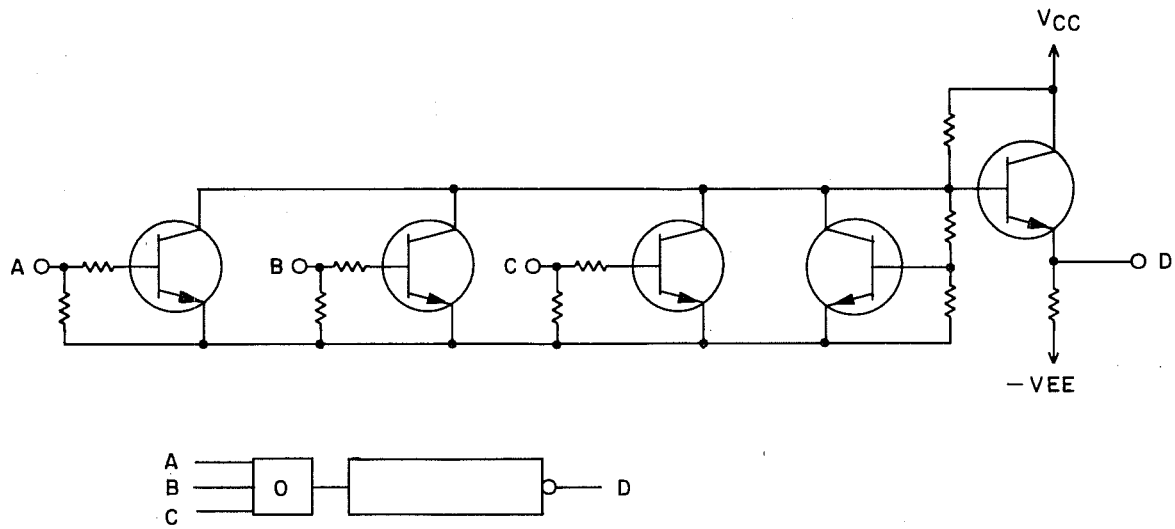


Figure 5-10. Logic Diagram and Schematic of CTL Inverter

This 5-nsec logic utilizes large voltage swings, low input frequency responses, and input termination resistors to guarantee high noise immunities, while using single-layer printed circuit boards and single-ended signal paths (for short lines).

TCS (TRANSISTOR CURRENT SWITCH)

When speeds of less than 5 nanoseconds are required, one must look to a type of circuit that does not saturate. Emitter-coupled or current mode logic is used to accomplish this. Figure 5-11 illustrates the basic current mode gate. The advantages of developing this circuit for high volume production are:

1) Low value resistors (high power)
2) Common collector transistor clusters
3) Dependence on ratios rather than absolute values of resistors.
4) No saturation problems (when logic levels are designed to alleviate this)
5) Small geometries permit more gates/wafer or more complete circuitry per die.

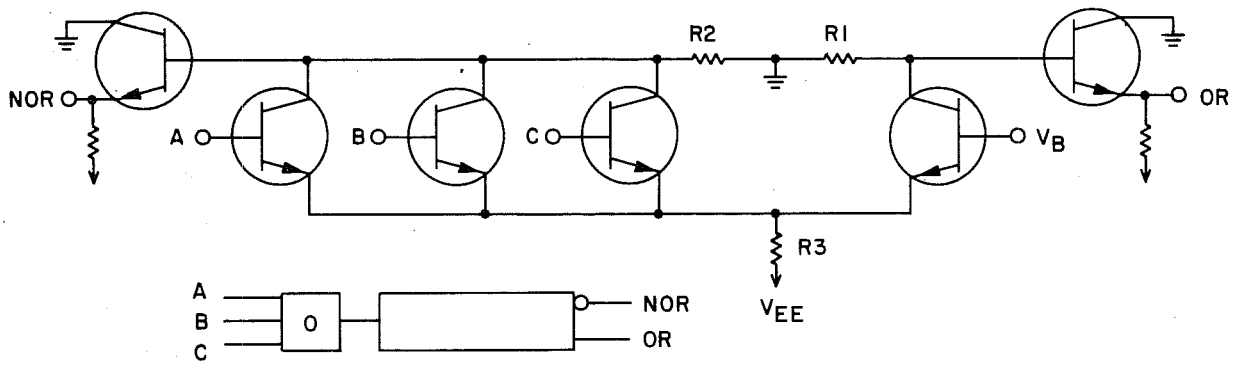


Figure 5-11. TCS Basic Gate and Block Diagram

To acquire 2-nsec to 1-nsec switching times, there are very few "tricks" which can be performed. When designing any integrated circuit, four main problem areas face the designer:

a) mask making
b) photo engraving
c) diffusion
d) metallization

To obtain high speed circuitry, the component dimensions must be made as small as possible to reduce capacitance values. This poses two problems to the designer; smaller masks and shallow diffusions. Of the four main problem areas of integrated circuits, diffusion is the least cumbersome at least up to base widths of 0.1 micron. Mask making, however, is an integral factor in the other two problem areas. Component dimensions and spacings, which are solely dependent upon the tolerances of the camera, dictate the speeds of the device. For example, 0.1 mil spacings produce 2-3 GHz transistor devices when used properly. However, 0.1 mil spacings are considered state-of-the-art for present day production processes; 0.2 mil spacings are as tight as production cares to use presently, due mainly to yield considerations. This type of a transistor will have f_τ characteristics of 700-1000 MHz, and will produce TCS circuitry of 2-3 nsec propagation delays.

Great care must also be given to ac circuit specifications. It must be emphasized that although the dc input impedance of a device is high due to emitter-follower inputs, the ac input impedance during switching can, in fact, be low (200-300Ω). The driving output emitter-follower must therefore have a peak f_T at the maximum fan-out current during switching. This reduces the fan-out a great deal or, reduces the speed at various fan-outs. To obtain high speeds, higher powers are also dissipated. This causes a reduction in the number of functions per package. To overcome this, many manufacturers have costly programs initiated to develop packages capable of handling 1-5 watts of dc power.

The current mode type circuitry is used where high speeds are required and high power dissipations are tolerated. Special packaging of the circuits is required basically because of the speed and the requirement for terminated lines so that the high transient signals are not distorted excessively. The circuit does have the non-inverted and inverted outputs available without additional delay. A complete family of circuits including power drivers, buffers and double-level logic elements can be made by slightly altering the basic configuration shown in Figure 5-11.

CHAPTER 6
MASKS FOR DTL INTEGRATED CIRCUIT

Masks are called the "tools of integrated circuitry". When a solid process has been developed and material is available, one needs only to create a new set of masks to change circuit types and configurations within the guidelines of the process.

This chapter contains drawings which represent a set of masks that might be used to fabricate the circuit shown by the electrical schematic in Figure 6-1. The schematic has the separate isolation regions required dotted in. This drawing, with appropriate positioning with respect to desired pin assignments, would be the first design step. A composite drawing would next be sketched, followed by the individual masks.

The masks illustrated could be used to create a workable DTL circuit. This set of masks was drawn up to illustrate the types required and in no way depicts the "state of the art".

Masks are drawn on precise opaque and/or clear plastic sheets. The accuracies are from $\pm$ 0.010 inch free-hand to $\pm$ 0.001 inch with machines. The masks are drawn 200 to 1000 times finished size; this reduces the 1-mil error to an insignificant amount.

Masks are usually reduced in two steps, the first being a 20 to 1 reduction. The reduction can be made by a fly's eye composite lens, multiple pin-hole plate, multiple lens board, or similar photographic techniques. This pattern (circuit positive or negative) is then reproduced a number of times, as determined by the size of the wafer, onto an "intermediate mask", using a precision, two-dimensional step-and-repeat process. The photo-reduction to finished size is made on glass, which then becomes the "master" for transferring the patterns to the IC wafer.

An alternate method involves a two-step reduction of the original mask to its finished size, after which the step-and-repeat process is performed directly onto the glass master. The second reduction is done using a high quality camera and lens, and a copy illuminator mounted on a vibration-free bed.

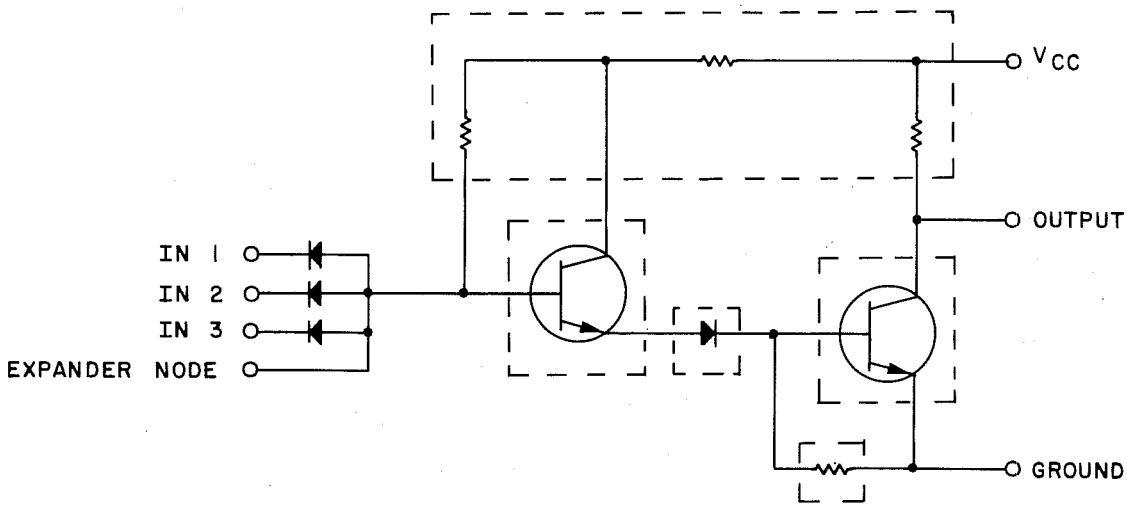


Figure 6-1. DTL Schematic Showing Isolation Areas

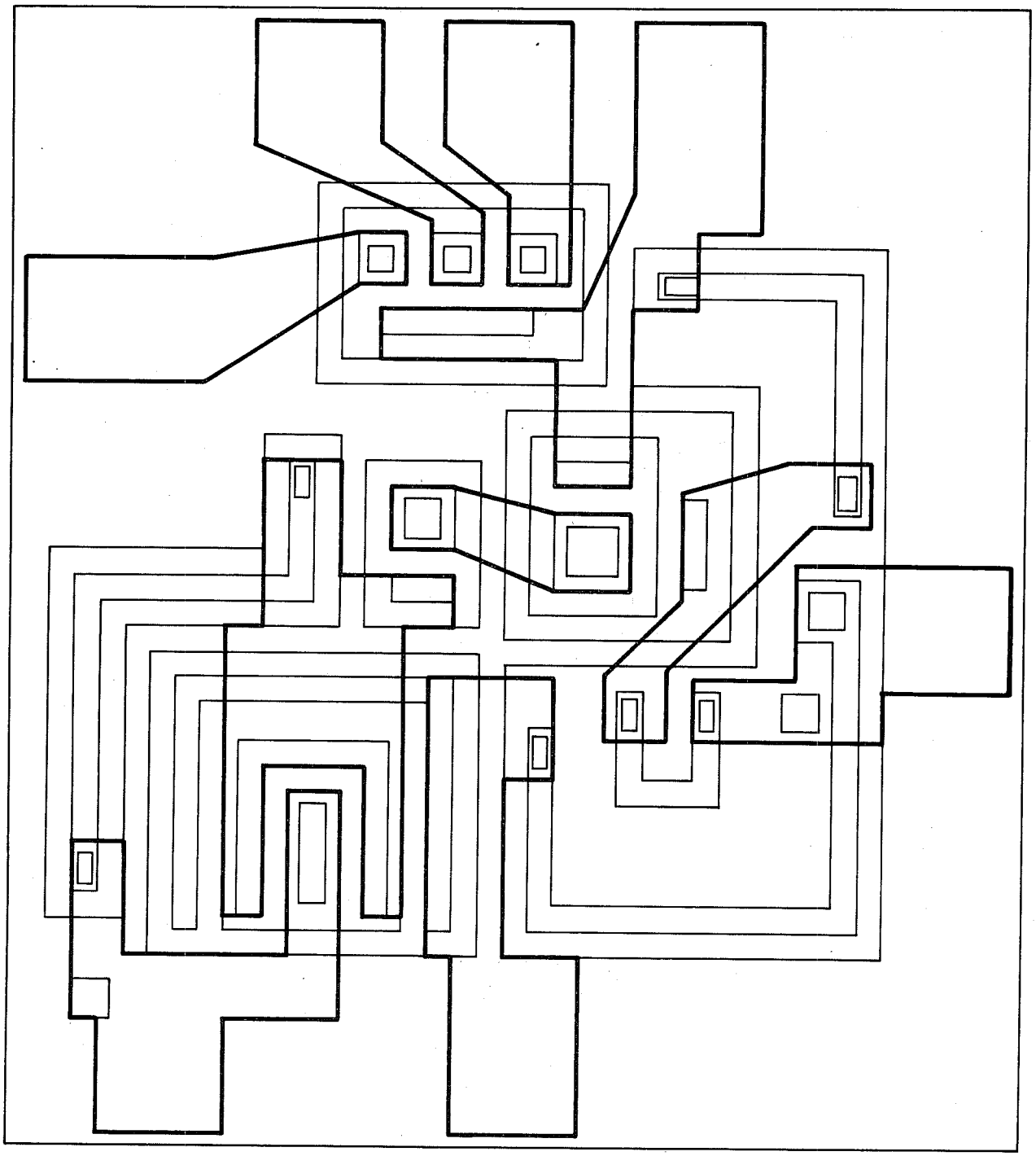


Figure 6-2. Composite Mask

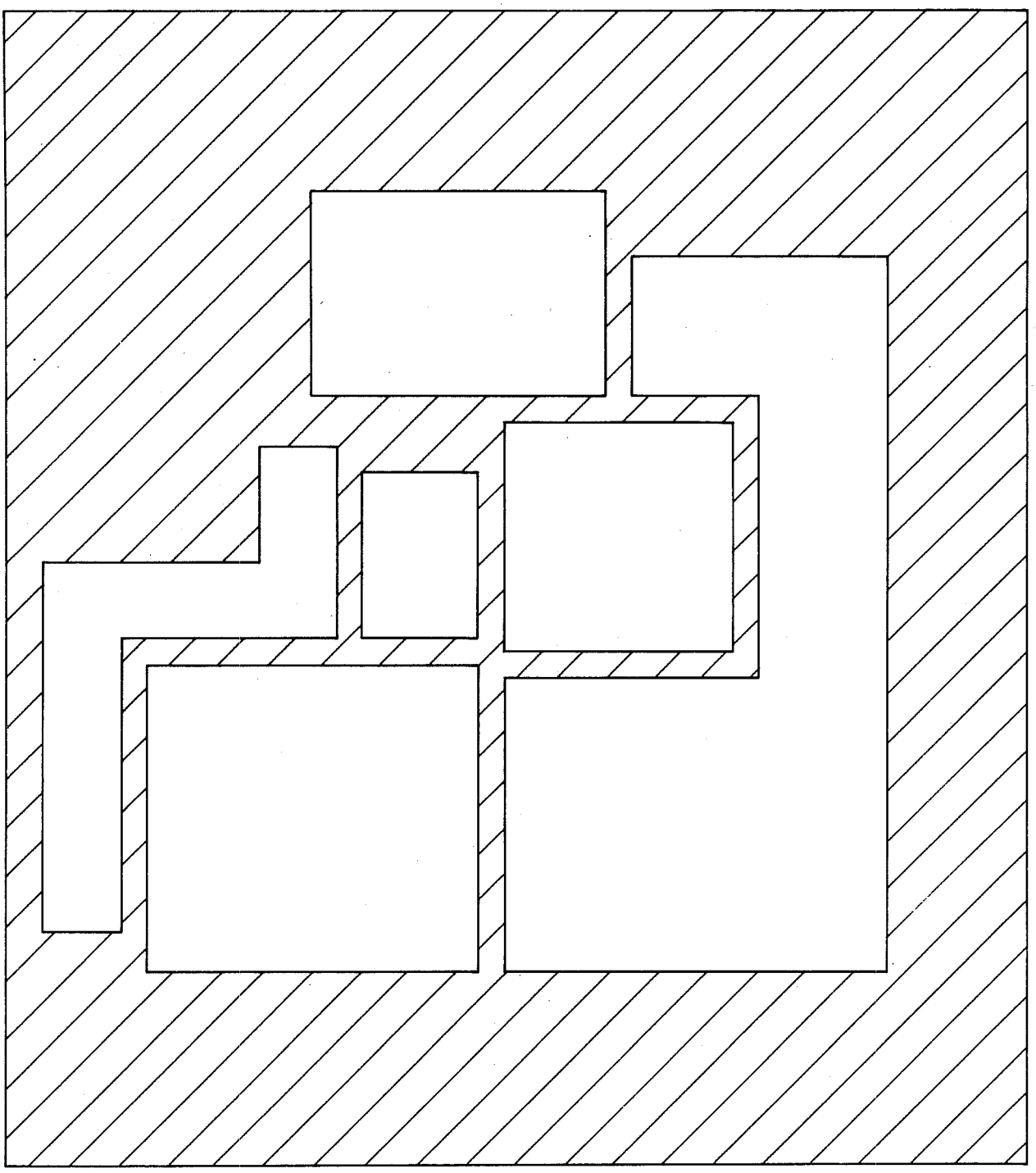


Figure 6-3. Isolation Mask

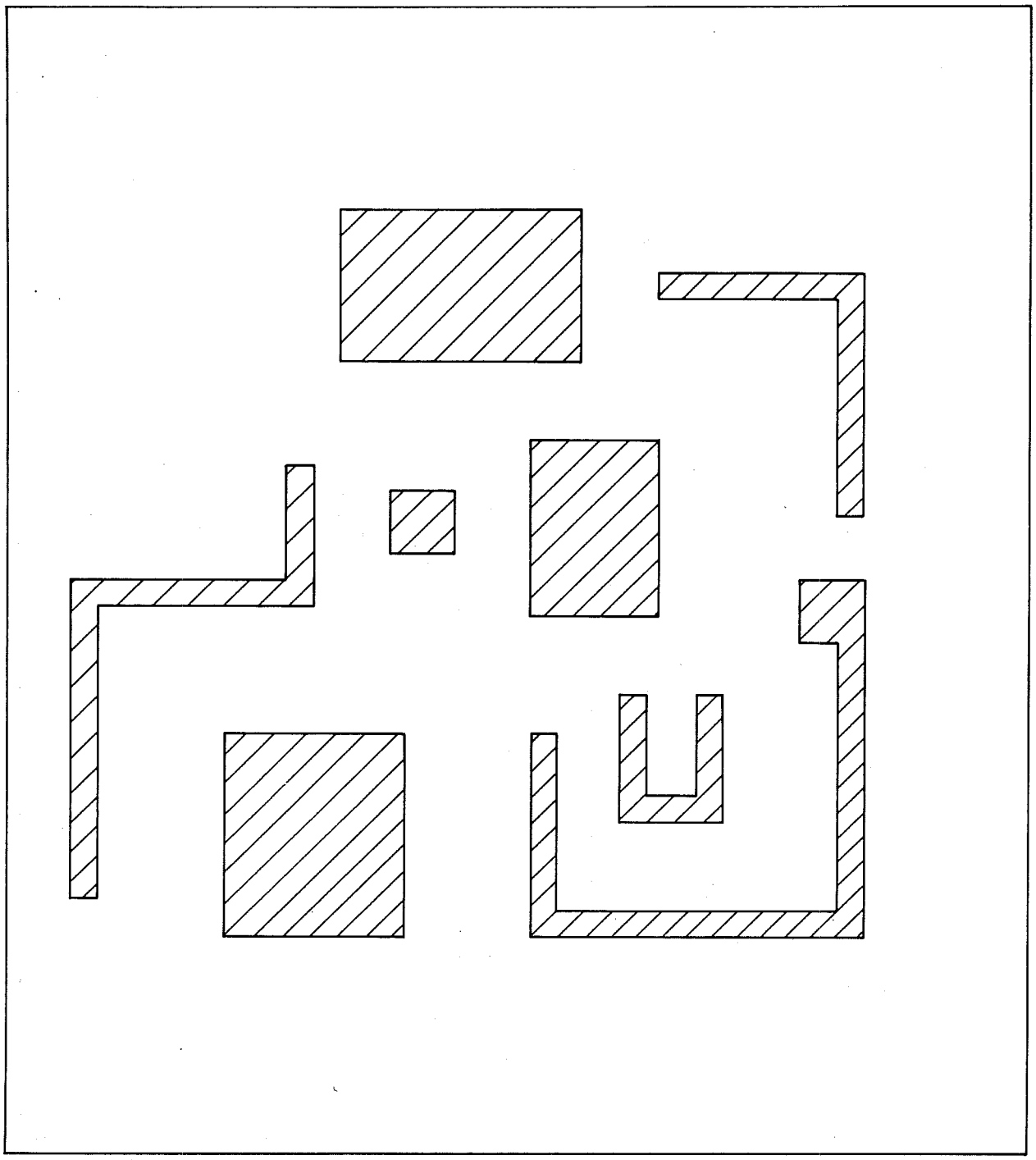


Figure 6-4. Base Mask

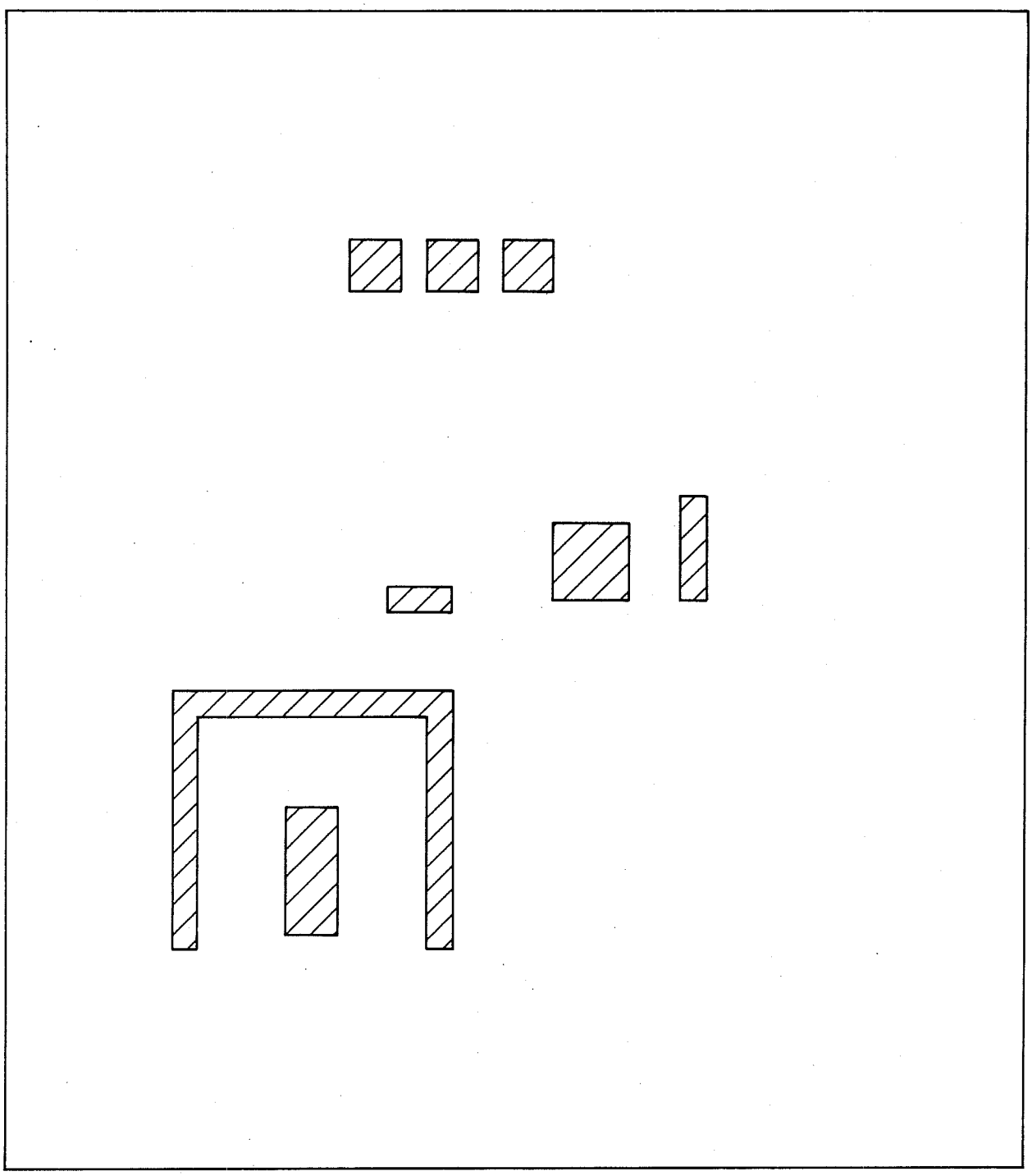


Figure 6-5. Emitter Mask

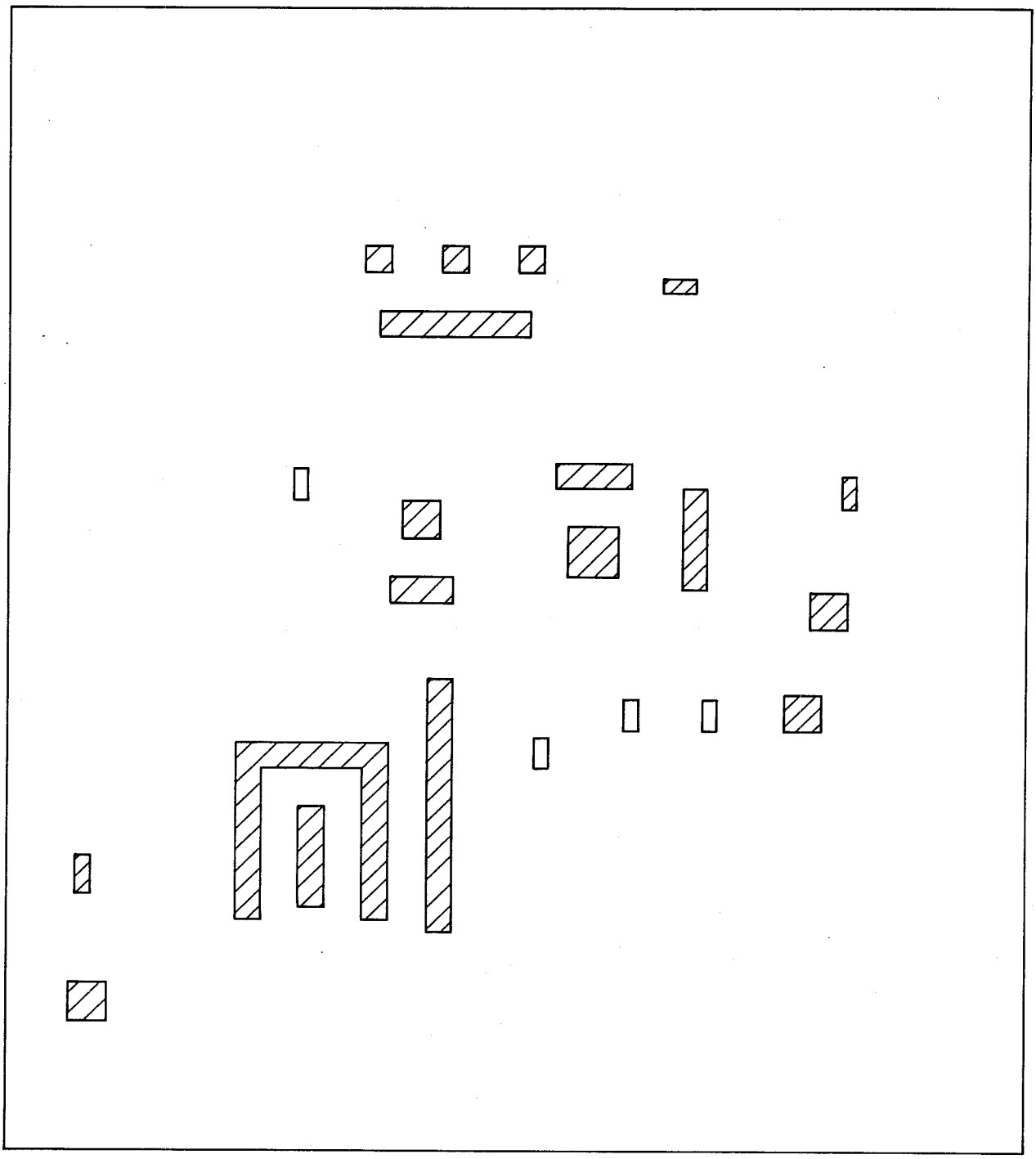


Figure 6-6. Preohmic Mask

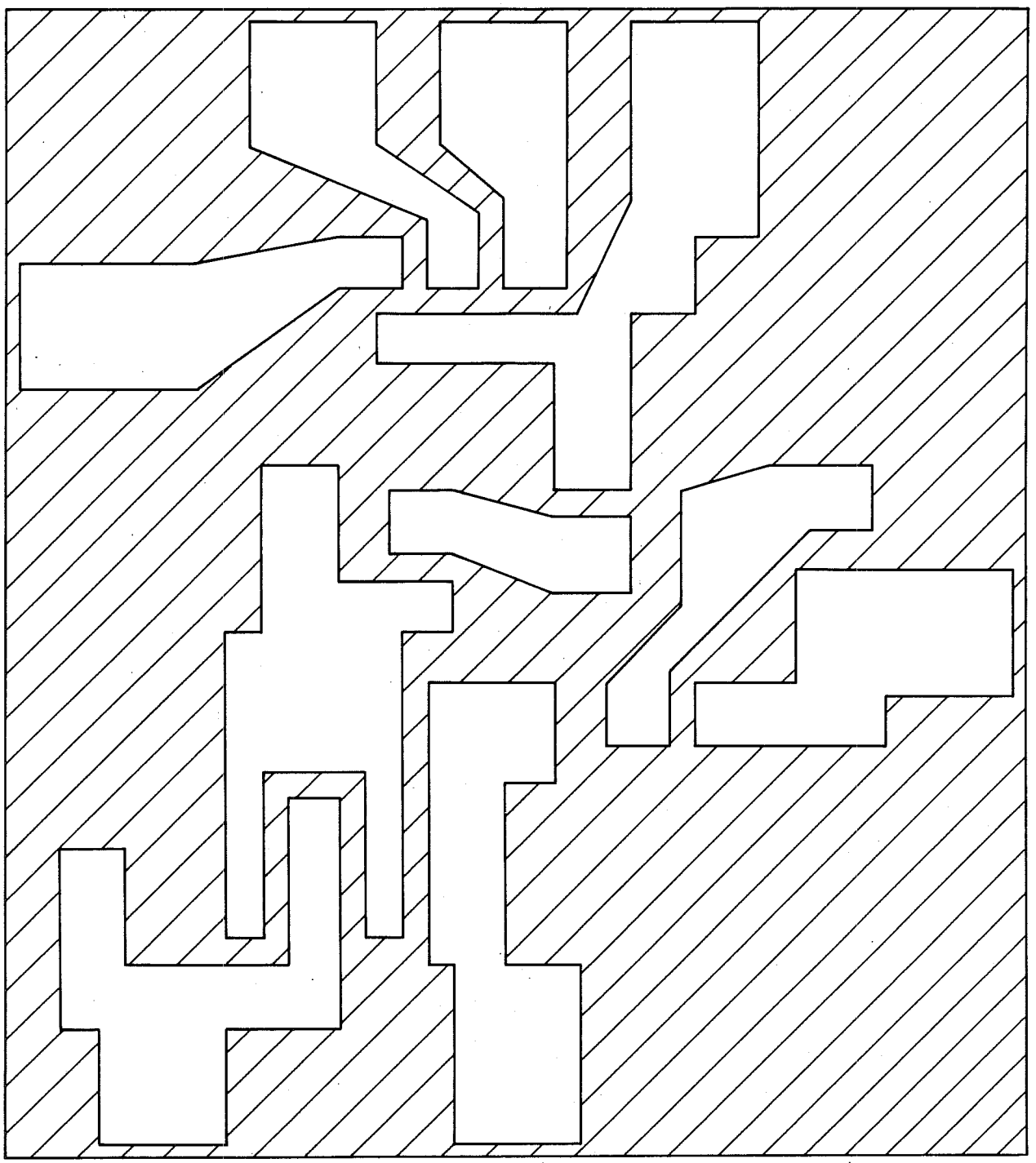


Figure 6-7. Metallization Mask

CHAPTER 7
SPECIFYING AN INTEGRATED CIRCUIT

The following guidelines are presented for consideration when specifying integrated circuits. The do's and don'ts are probably far from complete, but they could save IC users dollars, time, and possibly some embarrassment.

1. Review what is available as standard in the semiconductor IC industry.
2. Cost Considerations
   a) Die size (the most efficient breaking up of the logical functions/package is important).
   b) Specify voltages and currents within prescribed limits of IC components (resistor values, breakdown limits, V_{BE} variations, etc.).
   c) Write tentative speed, fan-in, fan-out, and noise immunity specs; be firm but don't design with these numbers.
   d) Become aware of standard test equipment so that tentative specifications can be written to accommodate them.
   e) If temperature dependent tests must be conducted, try to specify a lot acceptance AQL level rather than a 100% test.
   f) Have each circuit type individually priced, rather than a "package" deal. A package deal masks alternate possibilities that the logical designers might use to overcome high price circuits.
   g) Do not write component specifications - write adequate circuit specs.
   h) Obtain circuit equivalents from the vendor so that you can breadboard the circuit to insure your specification covers all conditions, if possible.
   i) Be sure of the package thermal impedance and also the proper configuration.
   j) Do not specify yourself into a "single vendor" corner, if at all possible.
   k) Let the vendor choose the pin assignment, unless you absolutely need these requirements. (Many times a compromise between circuit layout and printed circuit board layout can be reached.)

l) If possible, specify the maximum voltage that can be applied at each pin. This is not an operating voltage, but a voltage that the circuit can recover from with no change in specified parameters. Transients at times cause large voltages.

m) Power sequencing tests have proved valuable in determining possible faulty junction islation problems. This test should also be examined carefully.

3. Reliability Considerations

a) Obtain all reliability data available from vendor on your circuit type and package, as soon as you can.

b) Die size and number of output pins should be kept to a minimum in high reliability systems. This keeps the number of lead bonds down, the number of pins to a minimum, and the package seal periphery to a minimum.

c) If new packages are used, obtain samples and determine the package quality early in the negotiation period.

d) Write a fair but rigid reliability spec.

e) Compare costs of having vendor doing the tests or you doing them. Also consider if vendor data is needed on purchased lots.

f) Date code the circuits so that problem areas due to faulty processes can be pinpointed more quickly.

g) Require that each and every change in the process be ok'ed prior to using it on your circuits. All changes should be approved and signed off by you.

It is hoped that these recommendations will help when choosing your circuit types and your vendor.

Table 7-1 illustrates a method of determining what circuit type is best for a particular requirement. The most difficult part of the table to determine is the "weighting factor" column. This varies with each computer design and reliability consideration. A thorough analysis of the computer needs can, however, allow the designer to obtain such a column of numbers. After looking at the specification sheets of the circuits that can be used, apply the optimum weighting factor to the best of the circuit types in each category. The ratio of the circuit-type considerations multiplied by the optimum

weighting factor gives the weighting factor for the types:

$$WF_{OPT} \frac{N_{CKT}}{N_{OPT.CKT}} = WF_{CKT}$$

For example, assume circuit A has a propogation delay of 5 nanoseconds. If the optimum Weighting Factor is 30 and the fastest circuit (B) in the group has a $t_{pd} \simeq 2$ nsec, the weighting factors for circuit A is:

$$30\left(\frac{2}{5}\right) = 12$$

Note: If the smallest number is most optimum the expression above becomes:

$$W_F \frac{N_{OPT}}{N_{CKT}} = W_{F_{CKT}}$$

The weighting factor for circuit B, by the way, is the optimum (30), since it is the fastest in the group being compared.

Such considerations as "Packaging and assembly" and "Multi-circuit Source" may also be difficult to assign numbers to. It must be pointed out, however, that this method does give a true comparison of circuit types in an application when used properly.

The weighting factors used in Table 7-1 were chosen to illustrate the example.

TABLE 7-1. UTILIZING WEIGHTING FACTORS IN DETERMINING LOGICAL CIRCUIT TYPES FOR DIGITAL SYSTEMS

CONSIDERATIONS	WEIGHTING FACTOR	DTL 830	DTL CDC	T^2L SuHL	$CT_{\mu}L$	CDC TCS
Propagation Delay	30	3	5	5	12	30
Logical Functions per Package	20	8	20	16	10	18
Cost per Package	20	20	12	10	12	8
Packaging and Assembly	15	12	6	15	9	3
Multi-Circuit Source	10	10	3	8	1	6
Power Dissipation	5	4	2	5	3	1
TOTALS	100	57	48	59	47	66

Primary Consideration for Data Shown

CHAPTER 8
INTEGRATED CIRCUITS NOW AND IN THE FUTURE

GENERAL

Considering the advances in integrated circuits during the past few years, and the advances forseen in the near future, it is wise to review and evaluate the procurement criteria for new integrated circuits.

With improvements in technology and techniques, the semiconductor companies have come from $20.00 prices for 25 nsec propagation delay single function devices in 1962, to $4.00 for 3 nsec propagation delay double function devices in 1966. Several semiconductor companies are currently engaged in the development of 0.5 nsec to 0.1 nsec devices.

Although minor breakthroughs in epitaxial and diffusion processes have accounted for some of the faster transient responses, the main contributor to the "new generation" of speeds is the decrease in geometry size. Because of tighter tolerances on photographic work, the semiconductor companies can now produce more and faster chips per silicon wafer, or, more and faster functions per chip.

Functions Per Chip

To obtain a clear understanding of the term "Functions per chip", consider the expanded double level gate shown in logic form in Figure 8-1. This device (on one chip) performs four AND functions and one OR function -- a total of five functions.

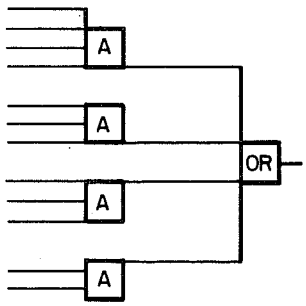


Figure 8-1. Expanded Double Level Gate

Price Versus Function

When requesting high speed integrated circuits, it is especially important for both logic designers and production to know where the circuits are on a "price versus function per package" chart. It is commonly felt that the chart shown in Figure 8-2 illustrates the information needed sufficiently. It will be attempted in the following paragraphs to illustrate that this is not so.

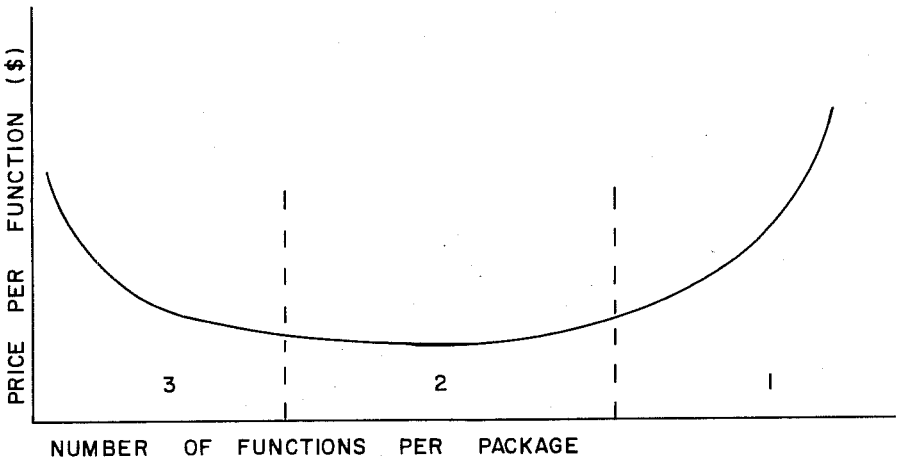


Figure 8-2. Function per Package Versus Price per Circuit

The chart has three definite price regions. Region I is where too many functions/package exist, and the yields are low due to certain limiting specifications and/or complex testing procedures. In Region III, the package cost is the predominant cost of the total circuit. Region II is "Utopia" where the manufacturer obtains the maximum number of circuit functions at the minimum cost and the package costs are optimum for the technology. This chart, however, is only reliable (if it can be accurately obtained at all) for a short period of time. One year at the most is a reasonable estimate.

To obtain a more useful chart, two other variables should be added. One variable is time. Figure 8-3 illustrates a modified version of Figure 8-2 showing time in years. Note especially that the shape of the curves change. The optimum position of each curve shifts right. This is due primarily to increased confidence in the new package. It must be pointed out that the chart, to be accurate, would represent one family of circuits.

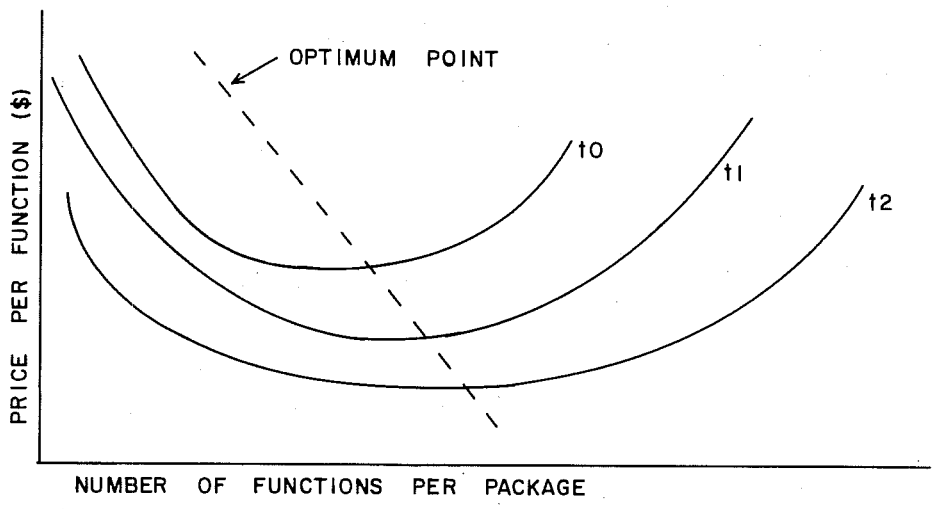


Figure 8-3. Function per Package Versus Price per Circuit (Including Development Progress)

The other pertinent variable is the propagation delay (t_{pd}) per function. An approximation of the effects of t_{pd} on price is illustrated by Figure 8-4(a). This also would vary with time as yields improve and testing is much easier. Figure 8-4(b) illustrates this.

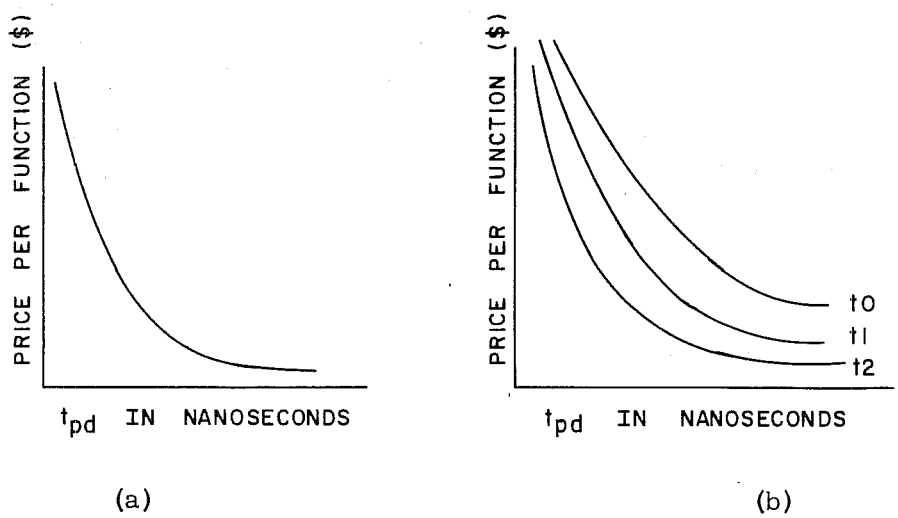


Figure 8-4. Propagation Delay per Function Versus Price per Package

Combining Figures 8-2 and 8-4 into one graph, a three-dimensional representation is obtained (Figure 8-5). On this chart, an estimate of the CDC TCS circuits currently being manufactured is indicated.

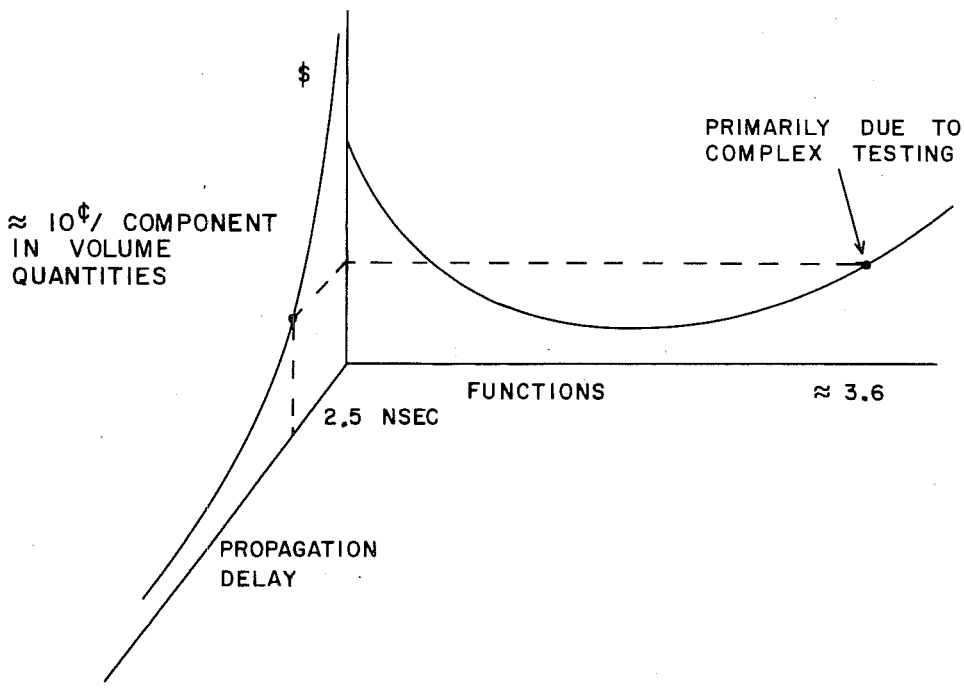
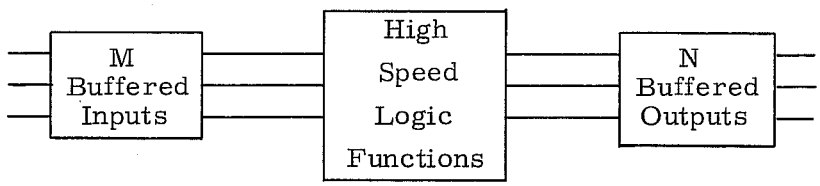


Figure 8-5. Chart for Evaluating Economy of Circuit

The knowledge of price versus functions per package and circuit delay has become a greater necessity with the announcement of subnanosecond circuitry. The size of the circuit chip dictates, to a great extent, the maximum power that the circuit can dissipate. Since improved photo technology generates smaller devices, capacitance effects are greatly reduced. This allows greater speeds to be obtained with much less power dissipation. More power is needed to generate signals outside the package than inside, for higher voltage and current levels must be generated to obtain signals greater than noise generated by the system. Therefore, to utilize the advanced technology and subnanosecond devices, a single circuit should have as many functions per package as economics dictates. Figure 8-6 illustrates how such a package could be arranged.



Total Pins = $M+N+X_{\text{test points}} + 2_{\text{(bus \& gnd.)}}$

Figure 8-6. Block Diagram of Circuit Using High Speed Circuitry, Buffered for High Noise Immunity

This type of circuitry is feasible and is nothing more than an advanced version of the CDC TCS presently being procured.

LARGE SCALE INTEGRATION

Less than five years after digital monolithic integrated logic circuits were first introduced on the military and commercial market, a new term is frequently echoed when speaking of integrated circuits: LSI. LSI stands for large scale integration and is a confusing term that means different things to different people. To better understand LSI, a review of the progress of monolithic circuits would be helpful.

In early 1962, production quantities of monolithic circuits were first introduced to the semiconductor user. Their circuits had logical propagation delays of 20-50 nanoseconds, the number of components ranged from 7 to 10, and the leads per package were 6 to 10.

In 1966, production facilities could produce, in sizable quantities, integrated circuits with the following characteristics: average propagation delays 3 - 5 nsec, number of components 25 - 40, and 16 leads per package. Figures 8-2, 8-3, 8-4, and 8-5 illustrate this improvement in general terms.

Integrated circuits today have more logical functions and switch at much faster rates than the initial versions. This progress has been made primarily because of improvements in the semiconductor process and photolithographic techniques as previously discussed. The semiconductor industry can, perhaps, increase the circuit performance to 1 - 1.5 nanosecond speeds and increase components per package to 60 or 70 with further advances in the above-mentioned processes. To have even higher performance devices, however, the logical voltage levels will have to be reduced and external loading conditions such as connectors, interconnecting lines and package impedance (excluding circuit loading effects) will have to be eliminated wherever possible. For instance, a development circuit displaying propagation delays of 1 nanosecond will probably have 10% to 20% of the delay caused by the package capacitance and the interconnecting length between the monolithic circuit die and the package lead.

A good definition for Large Scale Integration is "the process of achieving large numbers of logical functions on a single silicon die, interconnected together to perform a subsystem requirement". "Large numbers" is a vague term, but is generally considered to be in the order of 50 - 200 logical functions.

Need For LSI

With the need for accurate solutions to large and complex problems, the computer industry has turned to the "super" systems in which thousands of logic circuits are used to create parallel paths to enable problems to be solved in the shortest possible time interval. The 6600 system uses over 500,000 transistors as logic devices. The 7600 system will use over one million transistors to perform logic. Speed is essential and it has already been pointed out that density of logic gates improves the speed performance. Two other considerations in favor of LSI are economy and reliability.

Economic Factors

The economic aspect of LSI stems from the fact that with new and improved production processes, integrated circuit prices have been drastically reduced to somewhere in the order of 25¢ to 50¢ per logic function. One significant cost factor on large volume production units is the cost of encapsulation. This problem has been reduced somewhat with the epoxy and injected molded plastic package. When more logic functions are put on a chip, however, the plastic package is inadequate because of thermal resistance problems. Plastic and epoxy are relatively poor thermal conductors, so a large share of the heat generated within the package as the result of power dissipation must be removed through the package leads. With power of 300 to 500 mw, the package becomes marginal.

Another economic factor is the logic density. Real estate is a concern. The more logic per unit area that can be obtained, the lower the system packaging cost. No matter how many devices a semiconductor has per die, the cost to diffuse, wafer test, scribe, and assemble is relatively constant. Yields, of course, vary with the complexity of the logical function and the difficulty of the specification. With good process control, however, very little difference exists between logic functions throughout the wafer. Since less parts will be handled in manufacturing, the cost per logical function will be reduced.

Reliability Considerations

In semiconductor devices, the least reliable mechanism is lead bonding. For transistors, two lead bonds are used per device. In integrated circuits the number of lead bonds is equal to the number of package leads. Solder joints have proved to be the greatest cause of failures of CDC computers in the field. To date, this failure mode overshadows the component reliability.

To compare the reliability of LSI to discrete components, the following example is illustrated.

The 6600 system uses approximately 5,700 logic modules of which there are 276 types. Each module contains about 50 transistors and 70 resistors. Sixteen of these types, however, account for roughly 40 percent of the total number of modules used. Assuming that the proper IC package could replace one logic module, the comparison shown in

Table 8-1 can be made. The package used to demonstrate the example is a 50-pin package. The number of components in each package is approximately 120. This is a very conservative number when considering large scale integration possibilities.

TABLE 8-1. COMPARISON OF 6600 COMPUTER (LSI MODULES vs. CURRENT 6600 TYPE MODULES)

LOGIC TYPE	NO. OF MODULES	NO. OF MODULE TYPES	NO. OF PARTS	NO. OF SOLDER JOINTS	NO. OF COMPONENT LEAD BONDS
Discrete Components (6600)	2300	16	276, 000	667, 000	345, 000
LSI	2300	16	2, 300	115, 000	115, 000

From the table it is obvious that if an LSI package had up to 1/2 the reliability of the transistor package, it would still be a more reliable means of system design. In fact, if there were two integrated circuit packages per 6600 module, the system would still have 33 percent less solder joints, and 67 percent less lead bonds. When considering the propagation delays, density, and reliability requirements of the 7600 super system, the advantages of LSI are even more apparent.

Manufacturers' Inputs on LSI

Several techniques for creating large scale integration modules have been proposed, and in some cases developed, by manufacturers of integrated circuits. Although the approach varies from company to company, the following considerations and comments are in full agreement by all LSI development groups.

1. The progress made in developing extremely fast (high power) logic blocks will depend upon package development progress. Package development will include the board on which the circuit is mounted, which dictates a close design between user and designer of the LSI package.

2. The number of logic functions per package will range between 50 - 200 to best utilize LSI technique.

3. Multiple interconnection layers, separated by some form of glass, will be required to interconnect the logic functions on the die.
4. The logic types (finished packaged product) will be "special", not standard, parts.
5. Initial "on board" development costs will be expensive. ($100,000 minimum).
6. Semiconductor companies believe that production and development capacity will limit the customers they can supply to two or three. (This has already been the case with present integrated circuits.)
7. To obtain needed logic modules, the user and designer will be forced to closely coordinate their activities.
8. LSI is, in reality, 12 months to 30 months away from being incorporated into large volume computer systems.
9. Many problems have been overcome, yet there are many more to overcome.
10. LSI, however, is a real answer to many system problems.
11. The first usage for LSI will be in flip-flop memory arrays.
12. Computer companies should act soon to obtain the economy, speed, and reliability benefits derived from LSI.
13. Turn-around time on logic modifications is a problem that is being given serious thought.

Development Engineers' Inputs on LSI

Computer development engineers observe LSI from a different view point. Below are listed some of the considerations that logic, circuit, and packaging designers must overcome.

Logic Considerations

With given ground rules on the number and types of logic functions allowed per package, the problem becomes one of organizing the system into logic blocks that have high volume. With the range of 50 - 200 functions per package, and a maximum power dissipation of 4 to 5 watts, the logic designer has significant flexibility in his logic organization.

A second concern to the logic designer is to determine an economical number of functions per package based upon engineering changes and faulty field cards. It is obvious that for changes to be made, the logic function will have to be modified; this means replacing the entire LSI package. Proper organization of the system can reduce these variables and help maintain low inventories on circuit types.

The circuit types will depend to a great extent on the device people and their development capabilities. To guarantee maximum logic density, the circuit configuration should be carefully examined. Serious considerations should be given to having more than one type of logic function per package. This will increase circuit performance per package. One method to be considered would be that of having slow (present speed) buffers with logic levels high enough to overcome system noise on the input and output pins of the package. The logic that communicates only within the package could have smaller logic swings, lower noise immunities, and faster speeds, thus improving system capabilities. This was explained earlier in Chapter 8 -- and see especially Figure 8-6.

The second consideration that the circuit designer is confronted with is the problem of specifying the logic block such that it is feasible to be tested in a manner which guarantees the proper performance of the logic block. Functional and transient testers more complex than used to test 6600 modules will have to be designed and built.

Packaging Considerations

An integrated circuit package must also be developed that will dissipate 4 - 10 watts of power with a thermal resistance of 8 - 10°C per watt. This will mean joint development of a circuit package and the pc board that the circuit is mounted on. The board must be jointly designed because of the required power levels. The board will be a major portion of the heat sink for the circuit package in order to obtain the required low thermal resistance. Cooling methods will have to be investigated and resolved with regard to economy and feasibility.

Development of LSI

Figure 8-7 illustrates one method of obtaining an LSI circuit. This technique utilizes an optical scanner that is controlled by a computer system. The scanner fabricates the pre-ohmic contacts and interconnections directly without the use of masks.

The technique is presently limited to rather large geometric (and therefore slow circuit types).

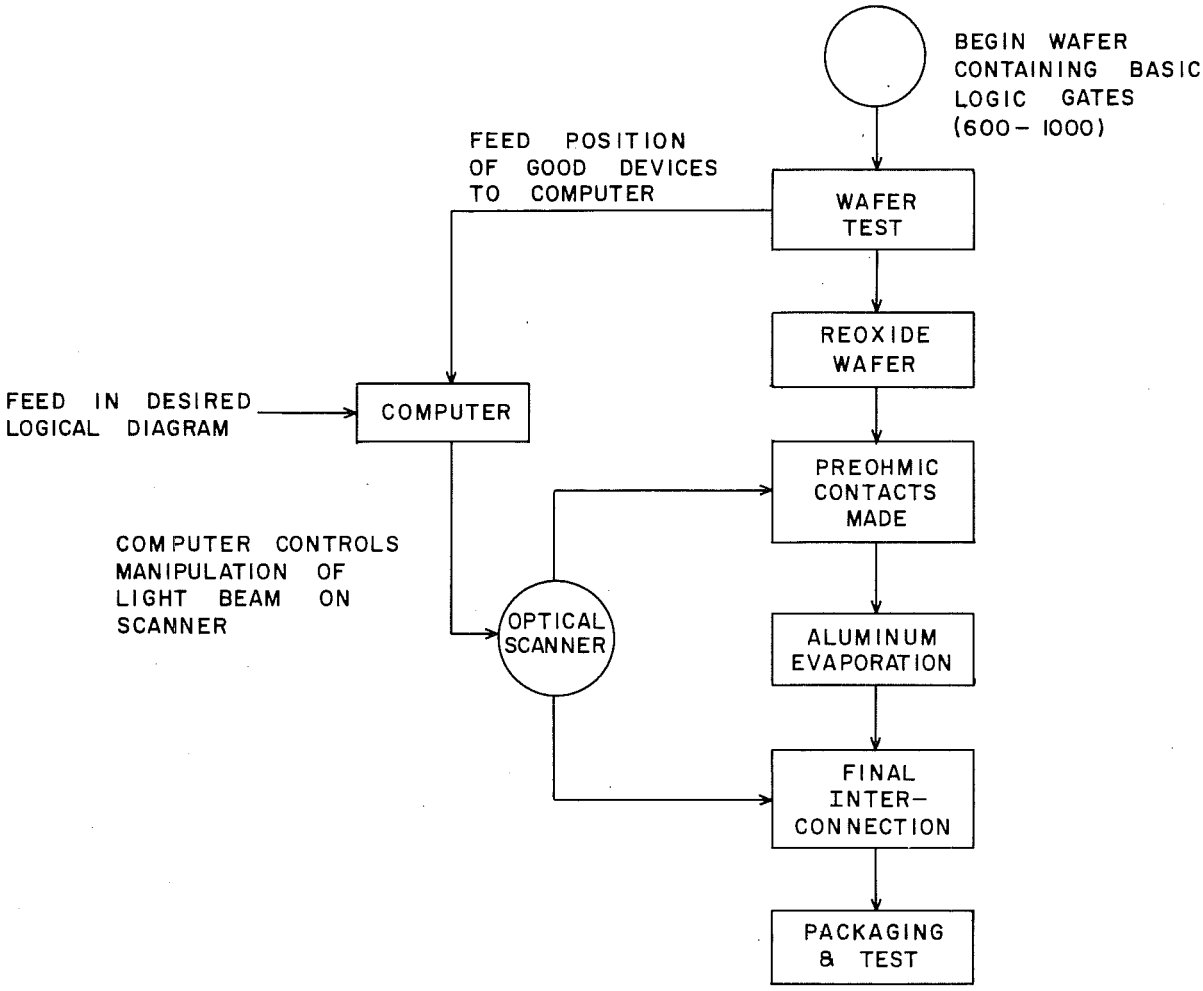


Figure 8-7. One Method of Obtaining LSI (Large Scale Integration) Using An Optical Scanner for Second Metallization Masking.

GLOSSARY OF DEFINITIONS AND REVIEW OF TERMS

Angstrom	Unit of measure: $\mathring{A} = 10^{-8}$ cm.
Beta	DC current gain of common emitter (and effectively common collector) configuration of transistors.
Die	Part of a silicon wafer (or other material) that consists of one monolithic circuit, or one transistor on a transistor wafer.
$f\tau$	Gain bandwidth product of transistor; the frequency at which the common emitter transistor gain = 1.
h_{fe}	High frequency current gain of transistors.
Impurity Concentration	Amount of impurity of N- or P-type material diffused into the semiconductor material, expressed in atoms per cubic centimeter.
Isolation Diffusion	Method in integrated circuits of separating components on a die.
Junction Capacitance	$C = \left(\frac{KM}{V_r}\right)^n A$ Where: n = 1/2 or 1/3, depending on type of junction. K = constant of diffusion materials (permittivity and diffusion constants). M = impurity concentration of lightly doped side of semiconductor junction. A = junction area. V_r = reverse potential of junction.
Logic Types	
CML	Current mode logic (7600 and NPL types).
DTL	Diode-transistor logic (1600/3000 and TVA types).
ECL	Same as CML (emitter-coupled logic).
RTL	Resistor-transistor logic (6600/6400 type).
TCS	Same as CML (transistor current switch).
T^2L (TTL)	Transistor-transistor logic (GSD military computers).
Micron	Unit of measure: $\mu = 10^{-4}$ cm.
Monolithic Circuit	A complete circuit on a single chip; may consist of as many as 150 interconnected components.
Photographic Masks	The topologies used in creating monolithic current layouts; a mask may be photopositive or photonegative.
Resistivity	Measurement of amount of resistance in a semiconductor (or other) material. The symbol is ρ .
Wafer	A silicon slice, usually circular, with a thickness of 5-10 microns and a diameter of 1-1.5 inches; can contain 100 to 1000 integrated circuits (dies), depending upon the circuit type.

Yield

The number of usable items obtained from the total number that were started on a production line. Three main factors affect yield in integrated circuits and transistors:

a) random imperfections,

b) damage during fabrications,

c) failure to meet desired specifications, either electrical or mechanical.

COMMENT SHEET

MANUAL TITLE AN INTRODUCTION TO INTEGRATED CIRCUITS

PUBLICATION NO. 60202000 REVISION

FROM: NAME:

BUSINESS ADDRESS:

COMMENTS:

This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number references and fill in publication revision level as shown by the last entry on the Record of Revision page at the front of the manual. Customer engineers are urged to use the TAR.

CUT ALONG LINE

FORM CA231 REV.1-67 PRINTED IN USA

NO POSTAGE STAMP NECESSARY IF MAILED IN U. S. A.

FOLD ON DOTTED LINES AND STAPLE

STAPLE

STAPLE

FOLD

FOLD

FIRST CLASS
PERMIT NO. 8241

MINNEAPOLIS, MINN.

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

CUT ALONG LINE

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION

8100 34TH AVENUE SOUTH

MINNEAPOLIS, MINNESOTA 55440

ATTN: TECHNICAL PUBLICATIONS DEPT.
PLANT TWO

FOLD

FOLD