60246600

CONTROL DATA CORPORATION

CONTROL DATA®
6600 COMPUTER SYSTEM

6613-D, 6614-D,
CENTRAL MEMORY
CLOCK
EXTENDED CORE STORAGE COUPLER
(SPEC OPT 60080-C/D)
CEJ/MEJ (STD OPT 10104-C/D)
POWER WIRING

DIAGRAMS AND CIRCUIT DESCRIPTION

HARDWARE MAINTENANCE MANUAL

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New features, as well as changes, deletions, and additions to information in the manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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FORM CA 230-2

60246600

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PART 3.	Clock
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PART 1

CENTRAL MEMORY (131 K)

PART 1

CENTRAL MEMORY (131 K)

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KEY TO LOGIC SYMBOLS

(Standard 6000 Series Card Types)

Logic diagrams represent a symbolic approach to electronic schematics. By using symbols to represent building block circuits, the schematic becomes easy to read if the reader understands the function of the symbols. In CONTROL DATA* logic, two signals, a logical "0" and a logical "1" are the possible input or output conditions of a circuit. For example, "1" is considered "up" and "0" is considered "down" on a timing chart. Detailed descriptions of logic symbols and their associated electronic representations are contained in the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700).

STANDARD LOGIC SYMBOLS

Standard logic diagram symbols for Control Data equipment using 6000 Series card types are inverters, test points, flip-flops, twisted pair line drivers, and coaxial cable line drivers.

Inverters

An inverter is a logic element which provides an output that is a negation of its input. When more than one input is provided to an inverter, "0's" take precedence over "1's" and therefore drive the output of the inverter to "1". Because all of the several inputs have to be "1" to drive the output of the inverter to a "0", the inverter may be considered an inverting AND (or NAND) gate when more than one input is present. The basic inverter is shown in the logic diagrams as an arrow into either a circle or a square (Figure 1). Both symbols represent the same electronic circuit and have the same logic interpretation. In a logic sequence of inverters, circle and square symbols are usually alternated as an aid in tracing signals, e.g., a "1" output from a square symbol implies a "1" output from subsequent squares in the logic chain.

Figure 1. Inverter Symbols

Certain card types employ variations of the standard inverter building block. These differences are indicated in the logic diagrams by a dot or a cross in the circle or square (Figure 2). Both the chassis tabs containing the card in question and the Printed Circuit Manual, Cordwood Modules (Pub. No. 60042700) contain electronic schematics of these special variations.

*Registered trademark of Control Data Corporation

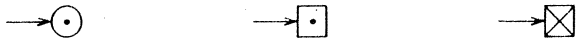


Figure 2. Special Inverters

Acceptable conventions for showing multiple inputs and outputs are given in Figure 3. Note that the output of inverter A is "0" only if inputs X, Y, and Z are all "1". The multiple outputs are identical.

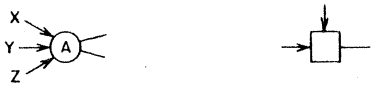


Figure 3. Multiple Inputs/Outputs

Acceptable conventions for showing inverter networks are illustrated in Figure 4. As a general rule, circle inverters alternate with square inverters wherever possible. Because multiple outputs are identical, only one arrow is shown in cases where an inverter (A) serves as the single input to several succeeding inverters. In more complex inverter networks, multiple arrows are used (B to C and D; in this case because B is not the only input to C or D).

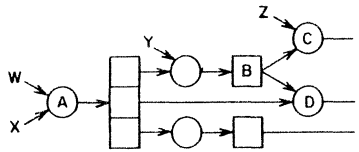


Figure 4. Inverter Networks

Test Points

A test point has no logic function, but is shown in the logic diagrams as a triangle (Figure 5). They are numbered from 1 to 6.

Figure 5. Test Point Symbols

Flip-Flops (FF)

The flip-flop (FF) is a storage device with two stable states--designated as Set and Clear--and is composed of two inverters (Figure 6). The flip-flop is said to be set when the set output (B) is a "1", and clear when it is a "0". Note that the input (A) must be "0" to set the flip-flop and (C) must be "0" to clear it.

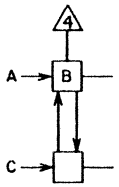


Figure 6. Flip-Flop Symbol

Logic signals are transmitted from one module to another by means of a line driver. Modules on the same chassis are connected with twisted pair lines, and those on separate chassis are connected by coaxial cable.

Twisted Pair Drivers

The twisted pair driver is represented by the standard square or circle. The output of the square or circle, however, is connected to a pin of the module in question and wired from there to a pin on another module (Figure 7). The ground wire of the pair is wired to the connector ground bus of each module. The pins are represented by small circles and are numbered from 1 to 28 (Pins 29 and 30 are ground and +6 volts, respectively, and generally are not shown in logic diagrams). The module location is shown above the card, and the module type is denoted in the upper right corner.

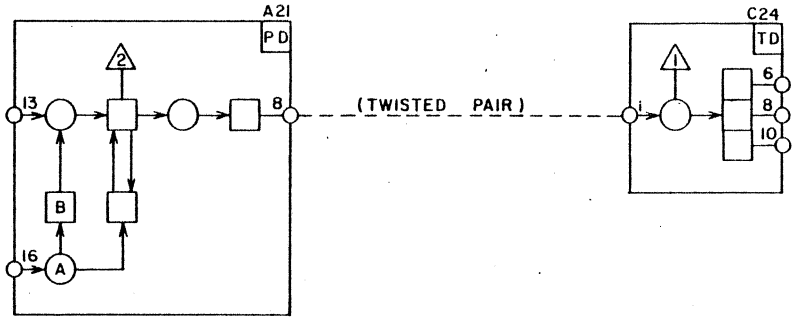


Figure 7. Twisted Pair Line Driver

Coaxial Cable Drivers

The coaxial cable driver is a 25 nsec pulse circuit, and is represented as shown in Figure 8. The pins used are represented by a small double circle.

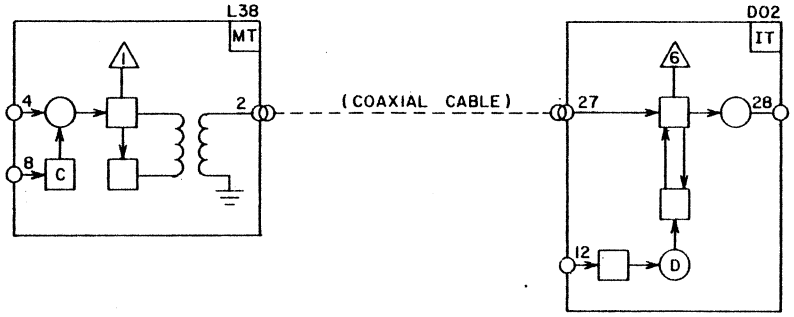


Figure 8. Coaxial Cable Driver

ADDRESSING

The CP programs are stored in CM, and all PPs may use CM for supplementary storage or inter-communication control. Thus CM addresses are generated by the CP and all PPs.

Each processor sends a CM address to a common address clearing house, or stunt box, from where they are sent on to CM. The stunt box can accept addresses from the several sources at 100-nsec intervals (maximum rate) on a priority basis and in turn issue one address every 100 nsec to CM.

An address goes to all banks of CM for decoding, and the referenced bank returns an accept signal to the stunt box if the bank is not busy (free) with a previous reference. The stunt box saves each address that it sends to CM in a hopper mechanism, and, if the address is not accepted, it is recovered from the hopper and re-issued to CM and again saved. The issue-save cycle repeats until an accept is received to void the hopper address. Up to three addresses can be saved in the hopper. However, an address is always accepted within 2000 nsec (worst case because of bank conflict) of the first time it is issued.

DATA DISTRIBUTION

Data to and from CM is distributed from a data distributor. The word from a read reference goes from CM to the data distributor and then to the requesting processor. A word to be stored during a write reference goes from the processor to the data distributor to CM. The distributor can transfer a word to or from CM every 100 nsec. A store word goes to all banks of CM, but separate storage control mechanisms for each bank insure that the word is stored in the proper bank.

The distributor routes data to and from proper origins and destinations as directed by control information or tags received from the stunt box. The tags are entered in the stunt box along with each address and serve to identify the address sender, origin or destination of data, and nature of the address, e.g., read, write, or PP exchange jump. The stunt box sends the tags to the data distributor (and to destinations in the processors for read references) when an address is accepted, and the distributor accomplishes the data transmission. For write references, the data source sends the word to the distributor, where it is held temporarily before it is stored.

STORAGE

The many banks of storage in CM are evenly distributed on 8 chassis in the computer. There are four banks per chassis.

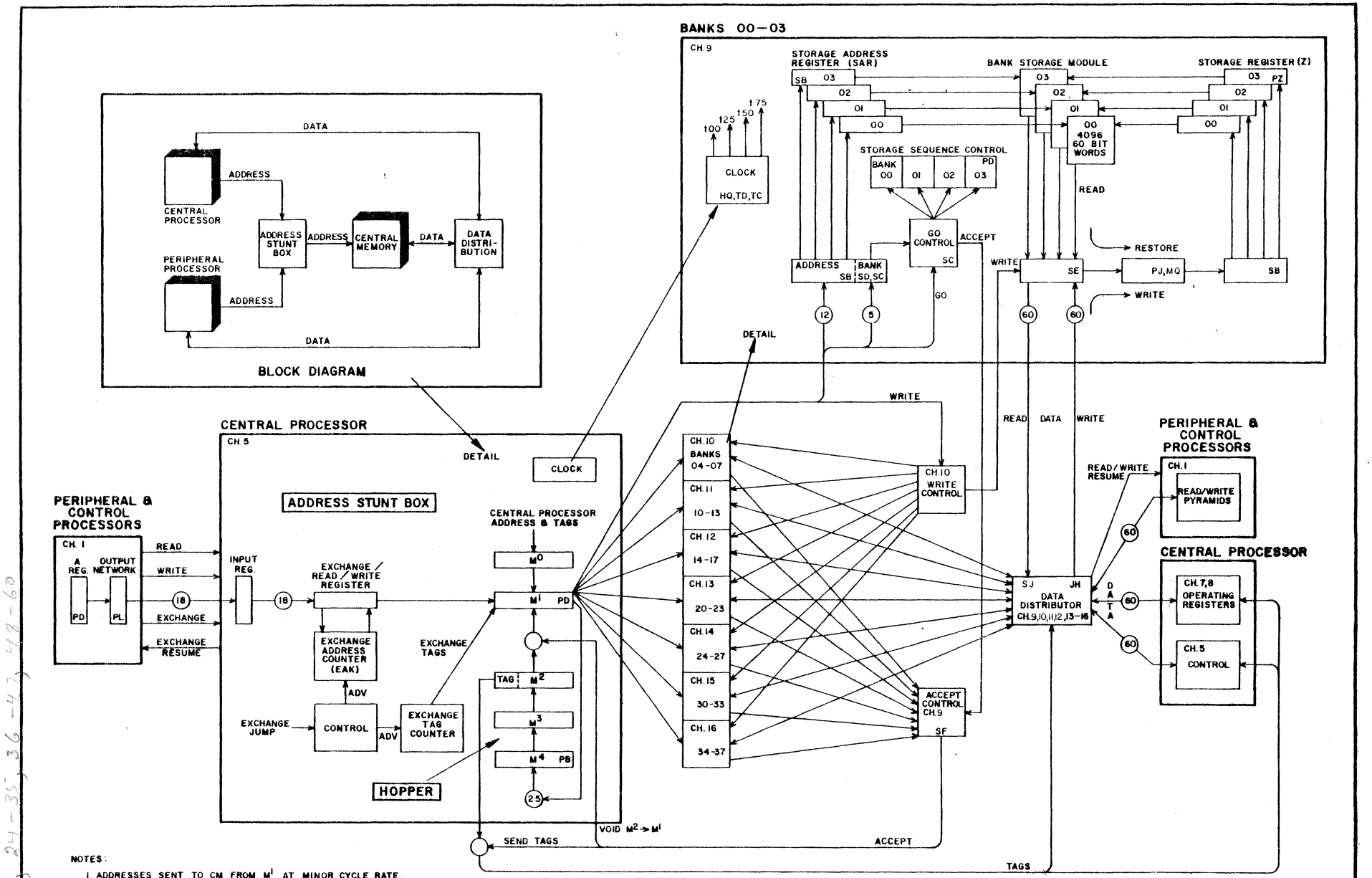
The circuit organization allows the four banks to operate independently and be phased into operation at 100-nsec intervals, which corresponds to the maximum rate at which the stunt box issues addresses. A chassis input register receives the 17-bit address from the stunt box and distributes the 12-bit address to 1 of 4 storage address registers associated with the four banks. Hence 32 consecutive addresses referencing 32 separate banks may be accepted at 32 consecutive minor cycle intervals and result in a data word flowing to or from CM in 32 consecutive minor cycle intervals. The independent controls for each bank and treatment of the address and data word insure that only one bank is in a given time segment of its 1000 nsec storage cycle at any one time. At least one minor cycle separates the storage cycle of all banks.

A word read from any bank is sent to a common temporary storage register and to the data distributor by a common path. A word to be restored is then sent to a write register by way of a buffer register. The write register sends the word to 1 or 4 restoration registers for restoring in the proper bank.

A word from the data distributor during a write reference goes to the temporary storage register on all chassis and then follows the restore path for writing in memory. Only one of the many banks is in the proper time spot in its storage cycle to store the word received, and this bank is the one associated with the write address.

A go signal with each address from the stunt box allows a group of four banks (one chassis) to recognize and translate the bank bits. The referenced bank, if not busy, sends an accept to the stunt box and starts 1 of 4 storage sequence control circuits, which in turn direct the 1000 nsec storage cycle for the selected address.

A write signal may also accompany each address from the stunt box. It distinguishes read and write references and controls the path to the restoration registers. The CM uses the same 12-bit storage module as used in the PPs, but five are driven in parallel to hold the 60-bit word.



NOTES:

1. ADDRESSES SENT TO CM FROM M^1 AT MINOR CYCLE RATE.
2. DATA MOVES TO/FROM CM AT MINOR CYCLE RATE.
3. ADDRESS TAGS DEFINE ORIGIN / DESTINATION OF DATA.
4. TIME FROM $M^1 \rightarrow$ CM TO RESPONSE TO CM ACCEPT IS 200 nSEC.
   a. M^1 STORED IN M^4 AT ISSUE TIME AND MOVES TO M^2 IN TIME SEQUENCE.
   b. ACCEPT VOIDS RE-ISSUE OF ADDRESS FROM HOPPER.

CONTROL DATA CORPORATION	TITLE: CENTRAL MEMORY (131K) ADDRESS - DATA FLOW	PRODUCT: 6613-D	
COMPUTER DIVISION		SIZE: C	DRAWING NO: 60246600 REV: 4
			SHEET: 38 1-1

GO CONTROL (131K)

A go control circuit is associated with each chassis (four banks) of CM. The circuit has several functions.

1. Recognize an address from the stunt box and determine if it is located in an associated bank.
2. Sends an accept to the stunt box if the address is valid and the bank is free.
3. Starts the 1000 nsec storage cycle to read or store the word at the selected address.

No accept is sent to the stunt box if the selected bank is executing a storage cycle from a previously issued address (bank busy case). The address is ignored in this case. The time of address issue from the stunt box and the time the accept should be received back at the stunt box is 200 nsec, and this time is used by the stunt box to determine if the address has been accepted. An accept at the proper time voids reissue of the address; otherwise address reissue continues until the accept is received.

BANK SELECTION

The go signal accompanying each address signals all CM go control circuits to search the bank selection bits and determine if the 12-bit address is located in one of its associated banks. A translator circuit in each go control translates the lower five bits of the address, stores the selection in a FF (one FF for each bank), sends the accept, and starts the storage sequence control circuit to start the storage cycle.

The five bits provide 32 unique codes, one for each bank. The upper three bits select 1 of 8 chassis and the lower two bits 1 of 4 banks on the chassis.

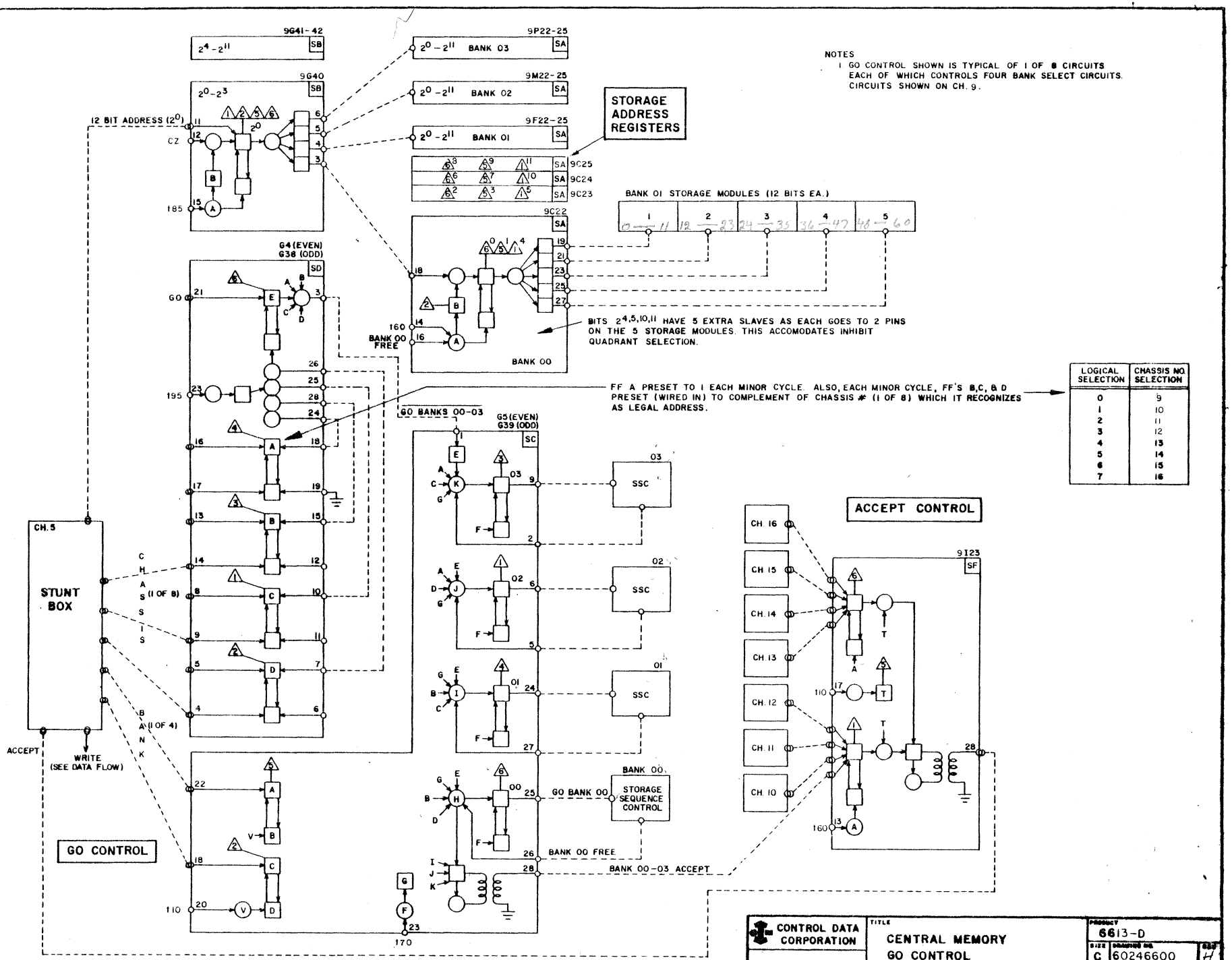
The 17-bit address and bank quantity is stored in an input FF register. Before an address is received, a clock pulse presets the upper three of the five bank bits to the complement of the quantity it should recognize. Thus, for a zero chassis selection (physical chassis 3), the upper three bits are preset to 111XX, the complement of 000XX. A 000XX bank code then is necessary to complete the go FF output gate, which in turn allows recognition of the lower two bits of the bank selection.

Four unique translations are made from the lower two bits of the bank selection bits and stored in separate FFs. A go from the 1 of 8 translator, a bank free condition from the storage sequence control circuit, and a clock pulse gates the 1 of 4 storage and turns on the accept signal. The set FF then starts an associated storage sequence control circuit.

ACCEPT CONTROL

The accept signal indicates a bank is free and has accepted the address in its chassis input register. The time interval from address issue from the stunt box to receipt of the accept in the stunt box allows the stunt box to determine if the address has been accepted. If so, the address in the stunt box hopper is destroyed, and address tags are sent from the stunt box to the data distributor and other areas to tell the address sender to send its data word (write reference) or be ready for receipt of the word read (read reference).

One accept is associated with each chassis for a maximum of eight signals. All are combined in a common OR circuit which feeds the stunt box. Since an address may be sent each 100 nsecs, an accept may be sent to the stunt box every 100 nsecs, with each accept delayed from its associated address by 200 nsecs.


NOTES
1 GO CONTROL SHOWN IS TYPICAL OF 1 OF 8 CIRCUITS EACH OF WHICH CONTROLS FOUR BANK SELECT CIRCUITS. CIRCUITS SHOWN ON CH. 9.
STORAGE ADDRESS REGISTERS
BANK 01 STORAGE MODULES (12 BITS EA.)
BITS 2^4,5,10,11 HAVE 5 EXTRA SLAVES AS EACH GOES TO 2 PINS ON THE 5 STORAGE MODULES. THIS ACCOMODATES INHIBIT QUADRANT SELECTION.
FF A PRESET TO 1 EACH MINOR CYCLE. ALSO, EACH MINOR CYCLE, FF'S B,C, & D PRESET (WIRED IN) TO COMPLEMENT OF CHASSIS # (1 OF 8) WHICH IT RECOGNIZES AS LEGAL ADDRESS.
LOGICAL SELECTION
CHASSIS NO. SELECTION
0 9
1 10
2 11
3 12
4 13
5 14
6 15
7 16
12 BIT ADDRESS (2^0)
CH. 5
STUNT BOX
CHASS (1 OF 8)
BANK (1 OF 4)
ACCEPT
WRITE (SEE DATA FLOW)
GO CONTROL
GO BANKS 00-03
BANK 00 FREE
GO BANK 00
BANK 00-03 ACCEPT
ACCEPT CONTROL
SSC
STORAGE SEQUENCE CONTROL
CH. 16
CH. 15
CH. 14
CH. 13
CH. 12
CH. 11
CH. 10
CONTROL DATA CORPORATION
COMPUTER DIVISION
CENTRAL MEMORY
GO CONTROL
ACCEPT CONTROL
6613-D
C
60246600

STORAGE SEQUENCE CONTROL

Storage sequence control responds to a bank go condition from go control and generates a series of timing signals which direct the basic cycle of the storage module. In general, the circuit establishes the bank free condition, makes the address available to the storage module, and then issues read, sense, start and end inhibit, bank merge, and write drive signals to sequence reading and writing. The sense signal samples the differential amplifier which receives the data word read out on the double-ended sense lines from storage. The signals time the basic pulse sequence of the 1000 nsec storage cycle. The storage module discussion details the circuits which respond to the address and read and write drive signals, and thereby make the read word available on the sense lines, or store the word to be written or restored in memory.

TIMING CHAIN

The timing chain is a series chain of FFs whose outputs drive slave inverters, which in turn supply the various signals to sequence reading and writing in CM. A pulse enters the chain and is transferred to successive FFs at 50 nsec intervals. A bank go signal sets the read FF to start the sequence. Each FF is set for 400 nsecs; slave inverters from set and cleared FFs in the chain are combined to establish timed gating signals for the various drive signals.

BANK FREE

The bank free condition is established when all FFs in the chain are cleared, i.e., no pulse is travelling down the chain. The read FF, and intermediate FF, and write FFs (last FF in chain), contribute timing signals to the bank free circuit and indicate whether a pulse is in the chain. All three FFs must be cleared to signal bank free, but their set states overlap to signal bank busy when a pulse is in the chain.

The bank free signal allows go control to respond to its back translation circuits and issue a bank go signal which sets the read FF to turn off the bank free signal.

STORAGE CYCLE TIMING

The following are the recommended times or timing durations for Central Memory in all 6000 series computers:

Strobe (time 75 ± 5 nsec)

This is measured on TP5 of the SE module, (see page 7). This time should be adjusted by varying the length of wire to pin 16 of the SG module.

Read-On(255 nsec ± 5 nsec) before Strobe.

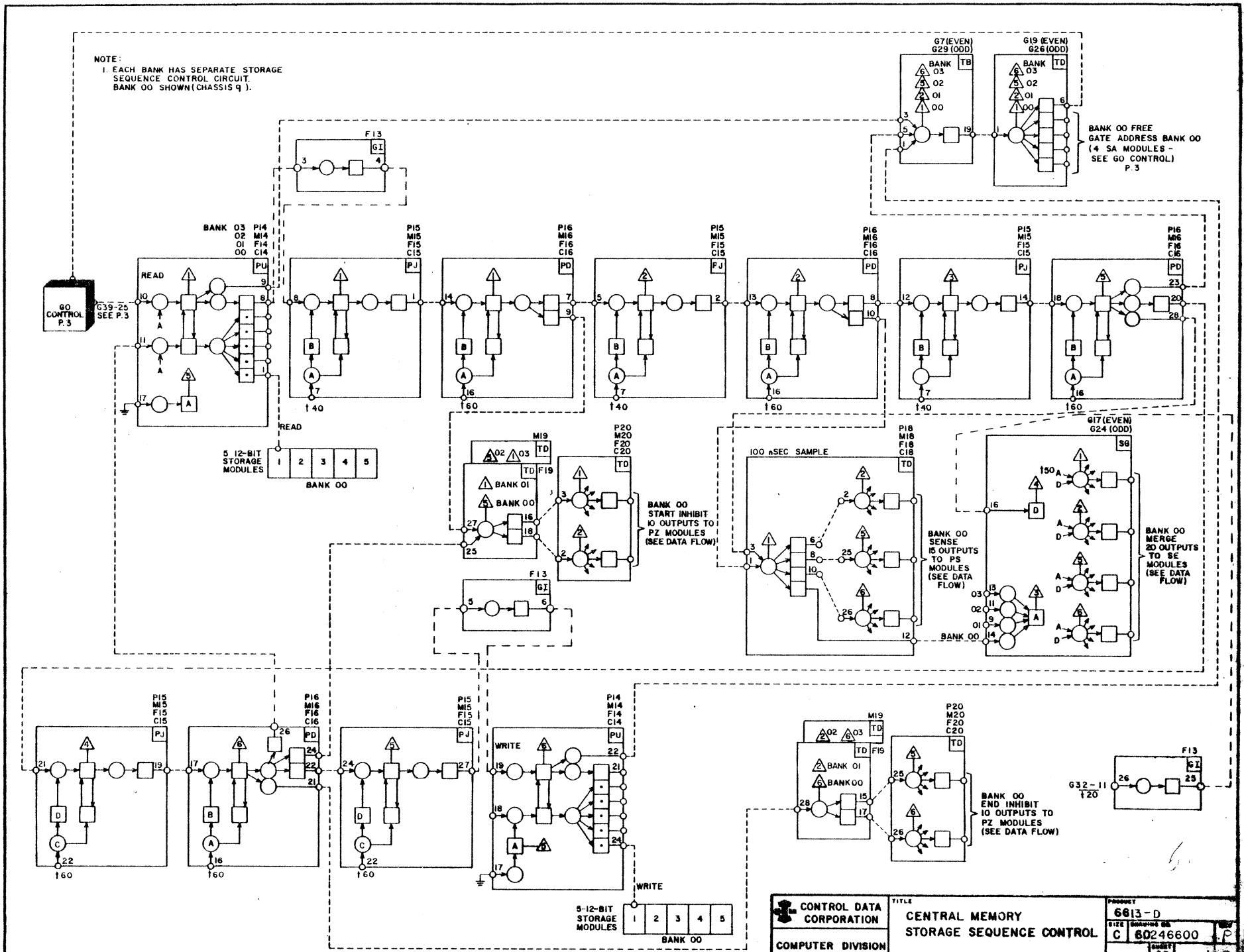
This is measured on pin 1 of the PU module. This time should be adjusted by varying the length of wire to pin 10 of the PU module and/or pin 2 of the GI module.

Read-Off (395 nsec ± 5 nsec) after the start of Read

This is measured on pin 1 of the PU module. This time should be adjusted by varying the length of wire to pin 11 of the PU module.

Write (355 nsec ± 5 nsec) 340

This is measured on pin 24 of the PU module. This time should be adjusted by varying the length of wire to pin 19 of the PU module and/or pin 5 of the GI module. See also page 7. 350


NOTE:
1. EACH BANK HAS SEPARATE STORAGE SEQUENCE CONTROL CIRCUIT. BANK 00 SHOWN (CHASSIS 9).
GO CONTROL P.3
G39-25 SEE P.3
READ
BANK 03 02 01 00
P14 M14 F14 C14
PU
P15 M15 F15 C15
PJ
P16 M16 F16 C16
PD
F13
GI
G7 (EVEN) G29 (ODD)
G19 (EVEN) G26 (ODD)
BANK TB
BANK TD
BANK 00 FREE GATE ADDRESS BANK 00 (4 SA MODULES - SEE GO CONTROL) P.3
5 12-BIT STORAGE MODULES
BANK 00
M19
P20 M20 F20 C20
TD
F19
BANK 01
BANK 00
BANK 00 START INHIBIT 10 OUTPUTS TO PZ MODULES (SEE DATA FLOW)
100 nSEC SAMPLE
P18 M18 F18 C18
BANK 00 SENSE 15 OUTPUTS TO PS MODULES (SEE DATA FLOW)
G17 (EVEN) G24 (ODD)
SG
BANK 00 MERGE 20 OUTPUTS TO SE MODULES (SEE DATA FLOW)
WRITE
BANK 00 END INHIBIT 10 OUTPUTS TO PZ MODULES (SEE DATA FLOW)
G32-11
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
CENTRAL MEMORY STORAGE SEQUENCE CONTROL
PRODUCT
6613-D
SIZE C
60246600
SHEET 40

DATA FLOW

In a read reference, the read word from the specified address flows from the storage modules to the data distributor and also back to the storage modules for restoration. The SE modules send the read word to the distributor and start the restore portion of the cycle. The restore FFs on these modules are cleared just before receiving the read word.

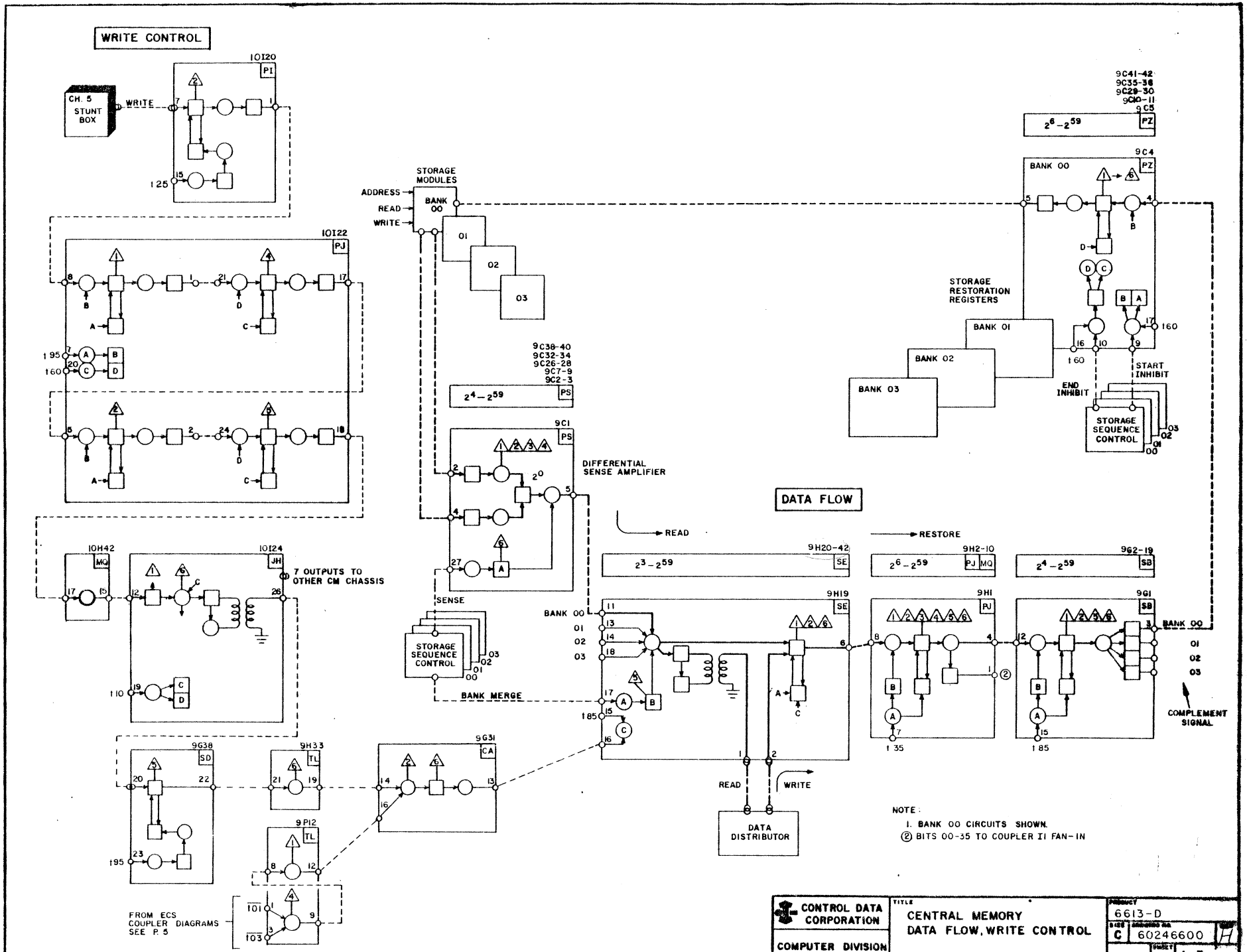
In a write reference, the read word from the specified address is sent to the data distributor and entered in the restore FFs of the SE modules. The restore FFs are cleared again to destroy the read word and reset with the write word which is stored in place of the read word during its normal restore cycle. The write control circuit and timing of stunt box tags direct the sequence.

WRITE CONTROL

Write control clears the restore FFs in the SE modules when writing in memory and thereby allows entry of the write word into the restore circuits.

A write signal from the stunt box enters the write control timing chain at the same time as the memory address is received in the input register of all memory chassis. The timing chain feeds a pulse to all chassis where they are fanned out and clear the restore FFs on the respective chassis SE modules. The delay time through the chain and format just exceeds the read access time and thereby destroys the read word immediately after it enters the SE restore FF. Effectively, the pulse in the timing chain runs in parallel with the pulse in the storage sequence control associated with the selected bank, but the write pulse from the timing chain fanout is emitted just after the bank merge pulse (which enters the read word in the SE restore FFs) from storage sequence control. Write pulses may enter the chain at minor cycle intervals and each is associated with a parallel operating storage sequence control.

The timing within the data distributor is such that a write word is sent to the SE modules slightly later than the SE modules sent the read word to the data distributor.


WRITE CONTROL
CH. 5 STUNT BOX
WRITE
1O120
PI
1O122
PJ
STORAGE MODULES
ADDRESS
READ
WRITE
BANK 00
01
02
03
9C38-40
9C32-34
9C26-28
9C7-9
9C2-3
2^4-2^{59}
PS
9C1
DIFFERENTIAL SENSE AMPLIFIER
SENSE
STORAGE SEQUENCE CONTROL
BANK MERGE
10H42
MQ
1O124
JH
7 OUTPUTS TO OTHER CM CHASSIS
9G38
SD
9H33
TL
9P12
9G31
CA
FROM ECS COUPLER DIAGRAMS SEE P. 5
DATA FLOW
READ
RESTORE
2^3-2^{59}
9H20-42
SE
2^6-2^{59}
PJ MQ
9H2-10
2^4-2^{59}
SB
9G2-19
9H19
SE
9H1
PJ
9G1
SB
BANK 00
01
02
03
COMPLEMENT SIGNAL
DATA DISTRIBUTOR
READ
WRITE
9C41-42
9C35-36
9C29-30
9C10-11
9C5
2^6-2^{59}
PZ
9C4
PZ
BANK 00
STORAGE RESTORATION REGISTERS
BANK 01
BANK 02
BANK 03
START INHIBIT
END INHIBIT
STORAGE SEQUENCE CONTROL
NOTE:
1. BANK 00 CIRCUITS SHOWN.
(2) BITS 00-35 TO COUPLER II FAN-IN
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
CENTRAL MEMORY
DATA FLOW, WRITE CONTROL
PROJECT
6613-D
SIZE
C
DRAWING NO.
60246600
REV
H
SHEET
271
1-7

DATA DISTRIBUTOR

The data distributor distributes read and write words to and from CM. Read words are sent to CP control on chassis 5, CP registers on chassis 7 and 8, and to the PP on chassis 1.

Write words are accepted from CP control on chassis 5 (exchange jump or return jump instructions), CP register chassis 7 and 8 (X^{0-7} registers), or from the PP on chassis 1.

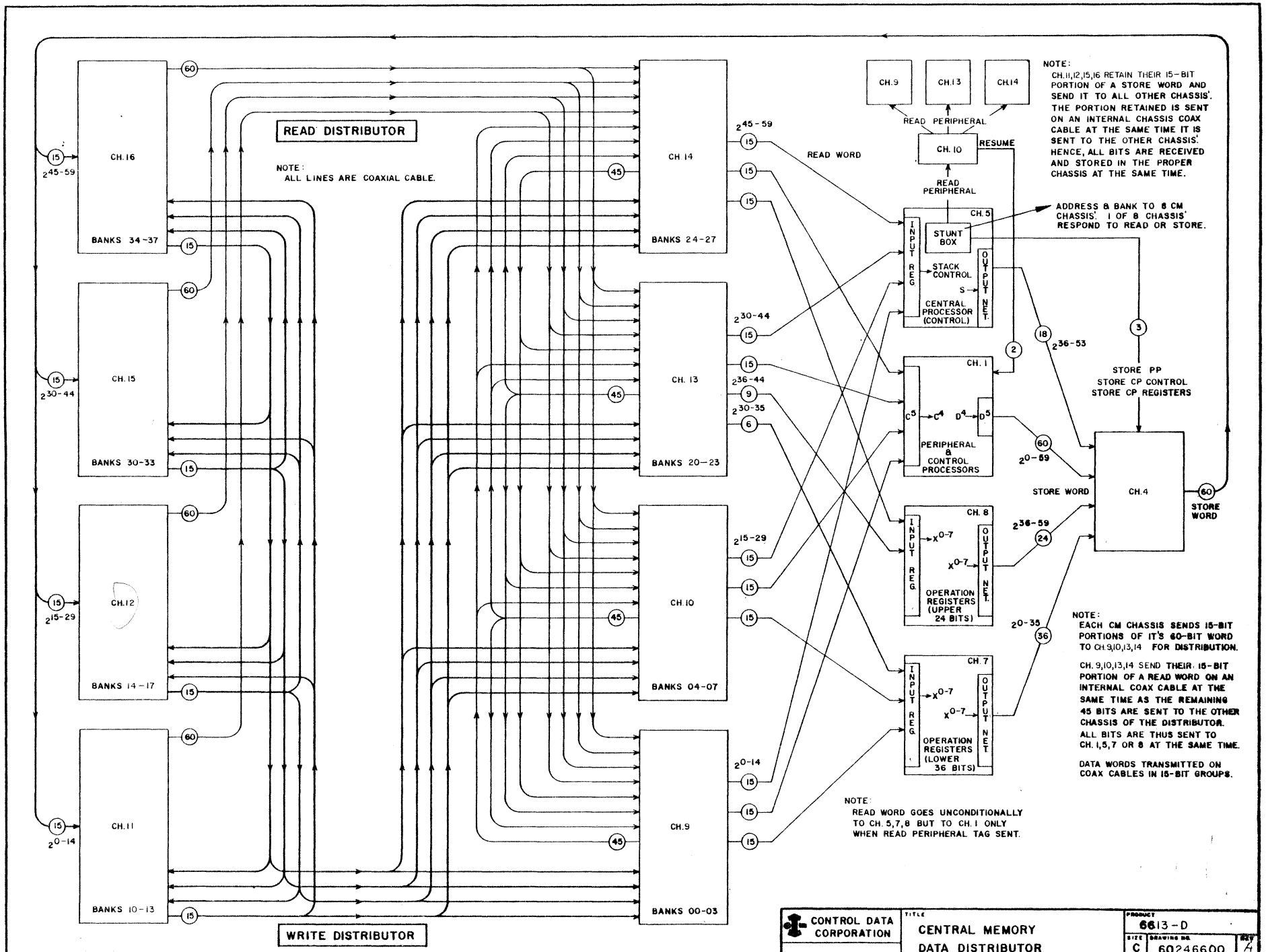
Address tags from the CP stunt box define the read or write cases and the origin or destination of the data.

STORAGE CYCLE TIMING

Inhibit On and Off

The inhibit should turn on at least 20 nsec before the start of the Write, and stay on at least 15 nsec after the end of the Write. The inhibit time is measured on pin 5 of the PZ module and is compared to the Write on pin 24 of the PU module. It should not be necessary to adjust the on time for the inhibit 30-50 nsec is the usual delay between inhibit-on and write-on. The off time is adjusted by varying the length of wire to pin 14 of C21, F21, M21, or P21 (clock working ranks).

The read pulse should be adjusted to obtain 395 nsec ± 5 nsec.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE
CENTRAL MEMORY
DATA DISTRIBUTOR

PRODUCT 6613-D
SIZE C DRAWING NO. 60246600 REV A
SHEET 42

READ DISTRIBUTOR

The read distributor accepts read words from the 8 CM chassis and routes them to the several destinations.

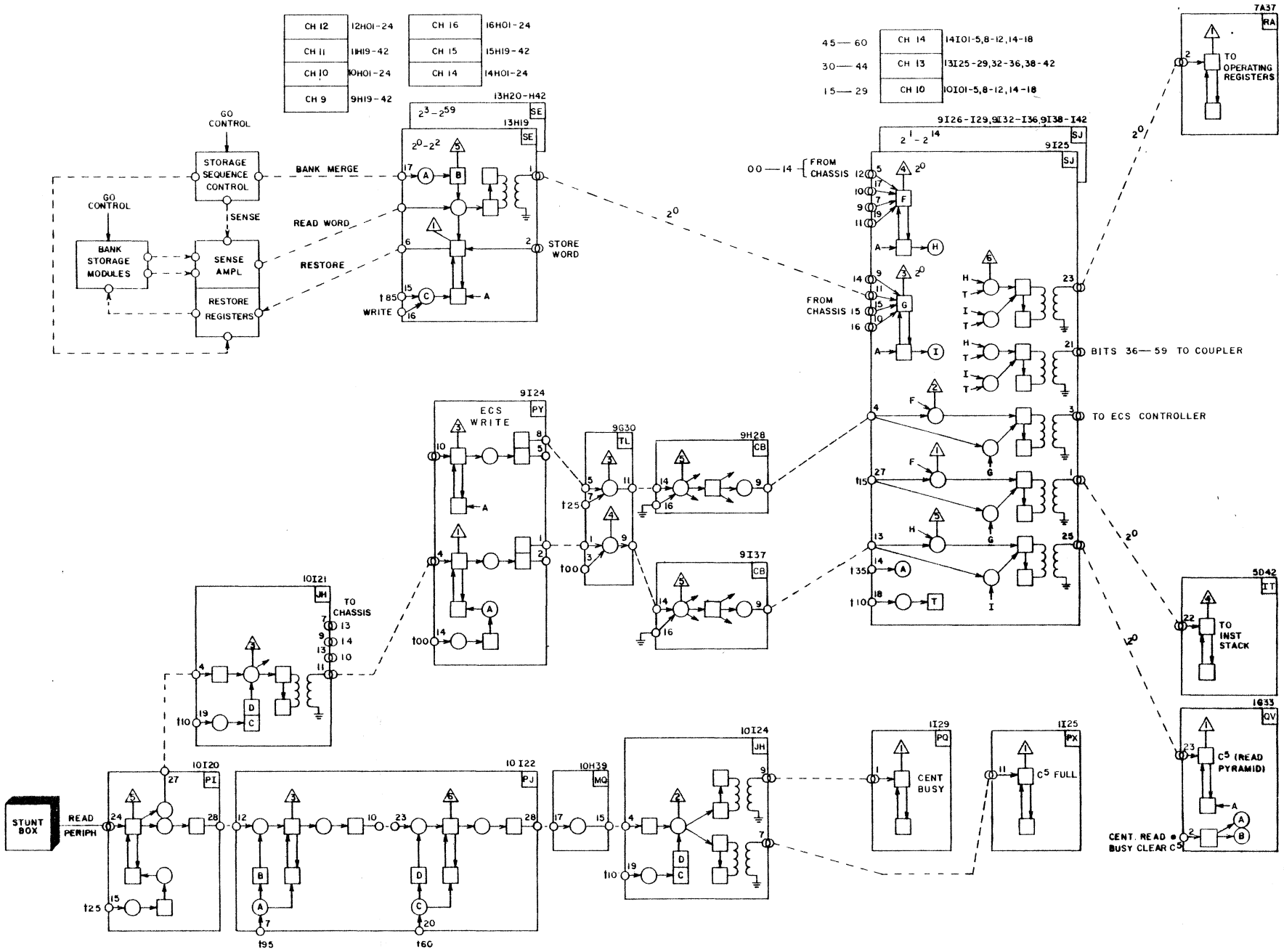
The distributor is organized on chassis 9, 10, 11 and 12 each of which handles 15 bits of the 60-bit word. Chassis cable limitations dictate the organization. The listing below shows the bits handled by each chassis.

CHASSIS	BITS
9	0-14
10	15-29
13	30-44
14	45-59

Chassis 13-16 each send the same 15-bit group to chassis 9-10-11 and 12. A read word from chassis 9 retains bits 0-14 but sends remaining bits in three groups to chassis 10, 13 and 14. Read words from chassis 10, 13 and 14 are handled similarly. Intra-chassis coaxial cables are used on chassis 9, 10, 13 and 14 for their 15-bit portions so that timing is consistent with the chassis receiving the data.

Each read word is sent unconditionally from chassis 9, 10, 13 and 14 to chassis 5 (CP control) and chassis 7 and 8 (CP registers). A read peripheral tag from the stunt box is sent to chassis 10 and then on to chassis 9, 13 and 14. The tag gates the read word to the C^5 register in the read pyramid on PP chassis 1.

The read peripheral tag also enters a time delay chain and is returned to the PP as a resume signal. The resume sets the C^5 full FF in the PP (after data word is in C^5) to signal the presence of the read word. The same resume also clears the central busy FF to indicate to PP control that the address has been accepted by the stunt box and CM has delivered the word. This allows the PPs to proceed and send another address to the stunt box.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL MEMORY READ DISTRIBUTOR	PRODUCT 6613-D SIZE C · DRAWING NO. 60246600 · REV. P SHEET 269 · PAGE 1-11

Bit	Module	Pin	TP	Module	Pin	TP
59	9H42	28	6	14I18	5	4
58		8	2	17	5	
57		1	1	16	5	
56	9H41	28	6	15	5	
55		8	2	14	5	
54		1	1	12	5	
53	9H40	28	6	11	5	
52		8	2	10	5	
51		1	1	09	5	
50	9H39	28	6	08	5	
49		8	2	05	5	
48		1	1	04	5	
47	9H37	28	6	03	5	
46		8	2	02	5	
45		1	1	01	5	
44	9H36	28	6	13I42	5	
43		8	2	41	5	
42		1	1	40	5	
41	9H35	28	6	39	5	
40		8	2	38	5	
39		1	1	36	5	
38	9H34	28	6	35	5	
37		8	2	34	5	
36		1	1	33	5	
35	9H32	28	6	32	5	
34		8	2	29	5	
33		1	1	28	5	
32	9H31	28	6	27	5	
31		8	2	26	5	
30		1	1	25	5	
29	9H30	29	6	10I18	17	
28		8	2	17		
27		1	1	16		
26	9H29	28	6	15		
25		8	2	14		
24		1	1	12		
23	9H27	28	6	11		
22		8	2	10		
21		1	1	09		
20	9H26	28	6	08		
19		8	2	05		
18		1	1	04		
17	9H25	28	6	03		
16		8	2	02		
15		1	1	01	17	
14	9H24	28	6	9I42	7	
13		8	2	41		
12		1	1	40		
11	9H22	28	6	39		
10		8	2	38		
9		1	1	36		
8	9H21	28	6	35		
7		8	2	34		
6		1	1	33		
5	9H20	28	6	32		
4		8	2	29		
3		1	1	28		
2	9H19	28	6	27		
1		8	3	26		
0		1	1	25	7	4

Read/Dist. Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	10H24	28	6	14I18	17	4
58		8	2	17		
57		1	1	16		
56	10H23	28	6	15		
55		8	2	14		
54		1	1	12		
53	10H22	28	6	11		
52		8	2	10		
51		1	1	09		
50	10H21	28	6	08		
49		8	2	05		
48		1	1	04		
47	10H19	28	6	03		
46		8	2	02		
45		1	1	01	17	
44	10H18	28	6	13I42	7	
43		8	2	41		
42		1	1	40		
41	10H17	28	6	39		
40		8	2	38		
39		1	1	36		
38	10H16	28	6	35		
37		8	2	34		
36		1	1	33		
35	10H14	28	6	32		
34		8	2	29		
33		1	1	28		
32	10H13	28	6	27		
31		8	2	26		
30		1	1	25		
29	10H12	28	6	10I18		
28		8	2	17		
27		1	1	16		
26	10H11	28	6	15		
25		8	2	14		
24		1	1	12		
23	10H09	28	6	11		
22		8	2	10		
21		1	1	09		
20	10H08	28	6	08		
19		8	2	05		
18		1	1	04		
17	10H07	28	6	03		
16		8	2	02		
15		1	1	01	7	
14	10H06	28	6	9I42	17	
13		8	2	41		
12		1	1	40		
11	10H04	28	6	39		
10		8	2	38		
9		1	1	36		
8	10H03	28	6	35		
7		8	2	34		
6		1	1	33		
5	10H02	28	6	32		
4		8	2	29		
3		1	1	28		
2	10H01	28	6	27		
1		8	2	26		
0		1	1	25	17	4

Read/Dist. Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	11H42	28	6	14I18	10	3
58		8	2	17		
57		1	1	16		
56	11H41	28	6	15		
55		8	2	14		
54		1	1	12		
53	11H40	28	6	11		
52		8	2	10		
51		1	1	09		
50	11H39	28	6	08		
49		8	2	05		
48		1	1	04		
47	11H37	28	6	03		
46		8	2	02		
45		1	1	01		
44	11H36	28	6	13I42		
43		8	2	41		
42		1	1	40		
41	11H35	28	6	39		
40		8	2	38		
39		1	1	36		
38	11H34	28	6	35		
37		8	2	34		
36		1	1	33		
35	11H32	28	6	32		
34		8	2	29		
33		1	1	28		
32	11H31	28	6	27		
31		8	2	26		
30		1	1	25	10	3
29	11H30	28	6	10I18	19	4
28		8	2	17		
27		1	1	16		
26	11H29	28	6	15		
25		8	2	14		
24		1	1	12		
23	11H27	28	6	11		
22		8	2	10		
21		1	1	09		
20	11H26	28	6	08		
19		8	2	05		
18		1	1	04		
17	11H25	28	6	03		
16		8	2	02		
15		1	1	01		
14	11H24	28	6	9I42		
13		8	2	41		
12		1	1	40		
11	11H22	28	6	39		
10		8	2	38		
9		1	1	36		
8	11H21	28	6	35		
7		8	2	34		
6		1	1	33		
5	11H20	28	6	32		
4		8	2	29		
3		1	1	28		
2	11H19	28	6	27		
1		8	2	26		
0		1	1	25	19	4

Read/Dist. Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	12H24	28	6	14I18	11	3
58		8	2	17		
57		1	1	16		
56	12H23	28	6	15		
55		8	2	14		
54		1	1	12		
53	12H22	28	6	11		
52		8	2	10		
51		1	1	09		
50	12H21	28	6	08		
49		8	2	05		
48		1	1	04		
47	12H19	28	6	03		
46		8	2	02		
45		1	1	01		
44	12H18	28	6	13I42		
43		8	2	41		
42		1	1	40		
41	12H17	28	6	39		
40		8	2	38		
39		1	1	36		
38	12H16	28	6	35		
37		8	2	34		
36		1	1	33		
35	12H14	28	6	32		
34		8	2	29		
33		1	1	28		
32	12H13	28	6	27		
31		8	2	26		
30		1	1	25	11	3
29	12H12	28	6	10I18	5	4
28		8	2	17		
27		1	1	16		
26	12H11	28	6	15		
25		8	2	14		
24		1	1	12		
23	12H09	28	6	11		
22		8	2	10		
21		1	1	09		
20	12H08	28	6	08		
19		8	2	05		
18		1	1	04		
17	12H07	28	6	03		
16		8	2	02		
15		1	1	01		
14	12H06	28	6	9I42		
13		8	2	41		
12		1	1	40		
11	12H04	28	6	39		
10		8	2	38		
9		1	1	36		
8	12H03	28	6	35		
7		8	2	34		
6		1	1	33		
5	12H02	28	6	32		
4		8	2	29		
3		1	1	28		
2	12H01	28	6	27		
1		8	2	26		
0		1	1	25	5	4

Read/Dist. Restore → Read Distributor

Data Trunks
6613-D Central Memory
Read/Distribute/Restore (CH 9,10,11,12)
to Read Distribute (CH 9,10,13,14)
Sheet 1

REV. A 1-12

Bit	Module	Pin	TP	Module	Pin	TP
59	13H42	28	6	14I18	17	4
58		8	2	17		
57		1	1	16		
56	13H41	28	6	15		
55		8	2	14		
54		1	1	12		
53	13H40	28	6	11		
52		8	2	10		
51		1	1	09		
50	13H39	28	6	08		
49		8	2	05		
48		1	1	04		
47	13H37	28	6	03		
46		8	2	02		
45		1	1	01		
44	13H36	28	6	13I42		
43		8	2	41		
42		1	1	40		
41	13H35	28	6	39		
40		8	2	38		
39		1	1	36		
38	14H34	28	6	35		
37		8	2	34		
36		1	1	33		
35	13H32	28	6	32		
34		8	2	29		
33		1	1	28		
32	13H31	28	6	27		
31		8	2	26		
30		1	1	25	17	4
29	13H30	28	6	10I18	11	3
28		8	2	17	11	
27		1	1	16	11	
26	13H29	28	6	15	11	
25		8	2	14	11	
24		1	1	12	11	
23	13H27	28	6	11	11	
22		8	2	10	11	
21		1	1	09	11	
20	13H26	28	6	08	11	
19		8	2	05	11	
18		1	1	04	11	
17	13H25	28	6	03	11	
16		8	2	02	11	
15		1	1	01	11	
14	13H24	28	6	9I42	11	
13		8	2	41	11	
12		1	1	40	11	
11	13H22	28	6	39	11	
10		8	2	38	11	
9		1	1	36	11	
8	13H21	28	6	35	11	
7		8	2	34	11	
6		1	1	33	11	
5	13H20	28	6	32	11	
4		8	2	29	11	
3		1	1	28	11	
2	13H19	28	6	27	11	
1		8	2	26	11	
0		1	1	25	11	3

Read/Dist/Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	14H24	28	6	14I18	9	3
58		8	2	17	9	
57		1	1	16	9	
56	14H23	28	6	15	9	
55		8	2	14	9	
54		1	1	12	9	
53	14H22	28	6	11	9	
52		8	2	10	9	
51		1	1	09	9	
50	14H21	28	6	08	9	
49		8	2	05	9	
48		1	1	04	9	
47	14H19	28	6	03	9	
46		8	2	02	9	
45		1	1	01	9	
44	14H18	28	6	13H42	9	
43		8	2	41	9	
42		1	1	40	9	
41	14H17	28	6	39	9	
40		8	2	38	9	
39		1	1	36	9	
38	14H16	28	6	35	9	
37		8	2	34	9	
36		1	1	33	9	
35	14H14	28	6	32	9	
34		8	2	29	9	
33		1	1	28	9	
32	14H13	28	6	27	9	
31		8	2	26	9	
30		1	1	25	9	
29	14H12	28	6	10I18	9	
28		8	2	17	9	
27		1	1	16	9	
26	14H11	28	6	15	9	
25		8	2	14	9	
24		1	1	12	9	
23	14H09	28	6	11	9	
22		8	2	10	9	
21		1	1	09	9	
20	14H08	28	6	08	9	
19		8	2	05	9	
18		1	1	04	9	
17	14H07	28	6	03	9	
16		8	2	02	9	
15		1	1	01	9	
14	14H06	28	6	9I42	9	
13		8	2	41	9	
12		1	1	40	9	
11	14H04	28	6	39	9	
10		8	2	38	9	
9		1	1	36	9	
8	14H03	28	6	35	9	
7		8	2	34	9	
6		1	1	33	9	
5	14H02	28	6	32	9	
4		8	2	29	9	
3		1	1	28	9	
2	14H01	28	6	27	9	
1		8	2	26	9	
0		1	1	25	9	3

Read/Dist/Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	15H42	28	6	14I18	15	3
58		8	2	17		
57		1	1	16		
56	15H41	28	6	15		
55		8	2	14		
54		1	1	12		
53	15H40	28	6	11		
52		8	2	10		
51		1	1	09		
50	15H39	28	6	08		
49		8	2	05		
48		1	1	04		
47	15H37	28	6	03		
46		8	2	02		
45		1	1	01		
44	15H36	28	6	13I42		
43		8	2	41		
42		1	1	40		
41	15H35	28	6	39		
40		8	2	38		
39		1	1	36		
38	15H34	28	6	35		
37		8	2	34		
36		1	1	33		
35	15H32	28	6	32		
34		8	2	29		
33		1	1	28		
32	15H31	28	6	27		
31		8	2	26		
30		1	1	25		
29	15H30	28	6	10I18		
28		8	2	17		
27		1	1	16		
26	15H29	28	6	15		
25		8	2	14		
24		1	1	12		
23	15H27	28	6	11		
22		8	2	10		
21		1	1	09		
20	15H26	28	6	08		
19		8	2	05		
18		1	1	04		
17	15H25	28	6	03		
16		8	2	02		
15		1	1	01		
14	15H24	28	6	9I42		
13		8	2	41		
12		1	1	40		
11	15H22	28	6	39		
10		8	2	38		
9		1	1	36		
8	15H21	28	6	35		
7		8	2	34		
6		1	1	33		
5	15H20	28	6	32		
4		8	2	29		
3		1	1	28		
2	15H19	28	6	27		
1		8	2	26		
0		1	1	25	15	3

Read/Dist/Restore → Read Distributor

Bit	Module	Pin	TP	Module	Pin	TP
59	16H24	28	6	14I18	19	4
58		8	2	17		
57		1	1	16		
56	16H23	28	6	15		
55		8	2	14		
54		1	1	12		
53	16H22	28	6	11		
52		8	2	10		
51		1	1	09		
50	16H21	28	6	08		
49		8	2	05		
48		1	1	04		
47	16H19	28	6	03		
46		8	2	02		
45		1	1	01		
44	16H18	28	6	13I42		
43		8	2	41		
42		1	1	40		
41	16H17	28	6	39		
40		8	2	38		
39		1	1	36		
38	16H16	28	6	35		
37		8	2	34		
36		1	1	33		
35	16H14	28	6	32		
34		8	2	29		
33		1	1	28		
32	16H13	28	6	27		
31		8	2	26		
30		1	1	25	19	4
29	16H12	28	6	10I18	10	3
28		8	2	17		
27		1	1	16		
26	16H11	28	6	15		
25		8	2	14		
24		1	1	12		
23	16H09	28	6	11		
22		8	2	10		
21		1	1	09		
20	16H08	28	6	08		
19		8	2	05		
18		1	1	04		
17	16H07	28	6	03		
16		8	2	02		
15		1	1	01		
14	16H06	28	6	9I42		
13		8	2	41		
12		1	1	40		
11	16H04	28	6	39		
10		8	2	38		
9		1	1	36		
8	16H03	28	6	35		
7		8	2	34		
6		1	1	33		
5	16H02	28	6	32		
4		8	2	29		
3		1	1	28		
2	16H01	28	6	27		
1		8	2	26		
0		1	1	25	10	3

Read/Dist. Restore → Read Distributor

Data Trunks
6613-D Central Memory
Read/Distribute/Restore (CH 13, 14, 15, 16)
to Read Distributor (CH 9,10,13,14)
Sheet 2

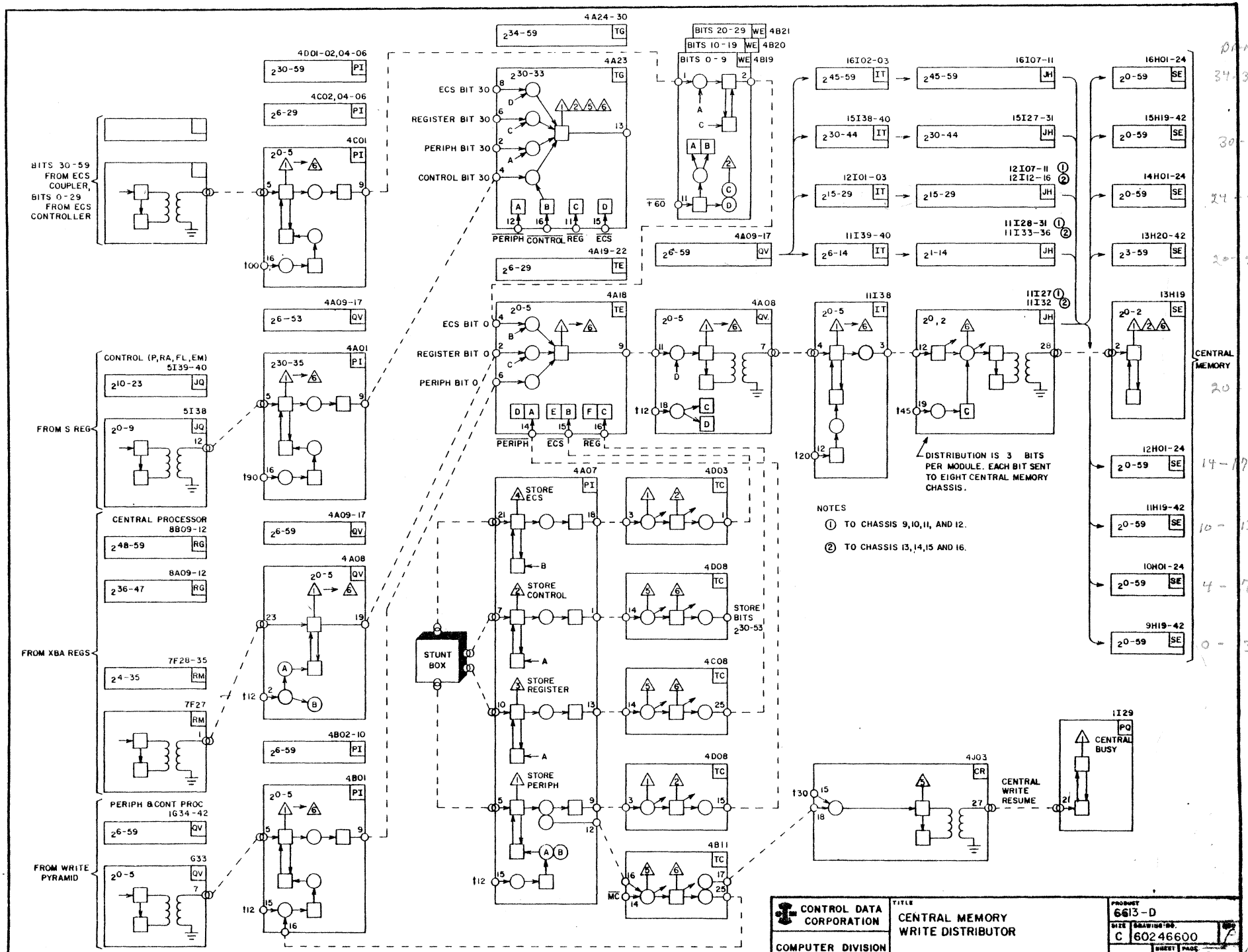
REV. A 1-13

WRITE DISTRIBUTOR

The write distributor accepts words from the several sources and stores them in 1 of 8 memory chassis. The distributor is on chassis 4. The 60-bit word on chassis 4 is split into four 15-bit groups which are sent to chassis 13-16 respectively. Each of these chassis in turn sends (or stores) its 15-bit group to the other 7 chassis unconditionally.

A 3-to-1 fan-in on chassis 4 selects the proper word under control of the store tag from the stunt box which is established ahead of the data. The word is then split and transmitted to chassis 13-16. The chassis 4 data registers and the tag FFs are cleared simultaneously.

One minor cycle after the register clear, a central write resume is sent to the PP to clear the central busy FF and allow the PPs to send another address to the stunt box.


BITS 30-59 FROM ECS COUPLER, BITS 0-29 FROM ECS CONTROLLER
4D01-02,04-06
4C02,04-06
4C01
4A09-17
4A01
CONTROL (P,RA,FL,EM) 5I39-40
FROM S REG
5I38
CENTRAL PROCESSOR 8B09-12
8A09-12
FROM XBA REGS
7F28-35
7F27
PERIPH &CONT PROC 1G34-42
FROM WRITE PYRAMID
G33
4A24-30
4A23
ECS BIT 30
REGISTER BIT 30
PERIPH BIT 30
CONTROL BIT 30
PERIPH
CONTROL
REG
ECS
+60
BITS 20-29 WE 4B21
BITS 10-19 WE 4B20
BITS 0-9 WE 4B19
4A09-17
4A19-22
4A18
ECS BIT 0
REGISTER BIT 0
PERIPH BIT 0
4A08
4A07
4D03
4D08
4C08
4B11
STORE ECS
STORE CONTROL
STORE REGISTER
STORE PERIPH
STORE BITS 2^30-53
STUNT BOX
16I02-03
16I07-11
15I38-40
15I27-31
12I01-03
12I07-11
12I12-16
11I39-40
11I28-31
11I33-36
11I38
11I27
11I32
DISTRIBUTION IS 3 BITS PER MODULE. EACH BIT SENT TO EIGHT CENTRAL MEMORY CHASSIS.
NOTES
① TO CHASSIS 9,10,11, AND 12.
② TO CHASSIS 13,14,15 AND 16.
16H01-24
15H19-42
14H01-24
13H20-42
13H19
12H01-24
11H19-42
10H01-24
9H19-42
CENTRAL MEMORY
4J03
CENTRAL WRITE RESUME
1I29
CENTRAL BUSY
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
CENTRAL MEMORY WRITE DISTRIBUTOR
PRODUCT 6613-D
SIZE C
DRAWING NO. 60246600
SHEET 250
PAGE 1-15

Bit	Module	Pin	TP	Module	Pin	TP
59	4A17	24	6	16I03	7	3
58		26	5		6	2
57		28	4		4	1
56		1	3	16I02	27	6
55		5	2		25	5
54		7	1		22	4
53	4A16	24	5		7	3
52		26	5		6	2
51		28	4		4	1
50		1	3	16I01	27	6
49		5	2		25	5
48		7	1		22	4
47	4A15	24	6		7	3
46		26	5		6	2
45		28	4		4	1
44		1	3	15I40	7	3
43		5	2		6	2
42		7	1		4	1
41	4A14	24	6	15I39	27	6
40		26	5		25	5
39		28	4		22	4
38		1	3		7	3
37		5	2		6	2
36		7	1		4	1
35	4A13	24	6	15I38	27	6
34		26	5		26	5
33		28	4		22	4
32		1	3		7	3
31		5	2		6	2
30		7	1		4	1
29	4A12	24	6	12I03	7	3
28		26	5		6	2
27		28	4		4	1
26		1	3	12I02	27	6
25		5	2		25	5
24		7	1		22	4
23	4A11	24	6		7	3
22		26	5		6	2
21		28	4		4	1
20		1	3	12I01	27	6
19		5	2		23	5
18		7	1		22	4
17	4A10	24	6		7	3
16		26	5		6	2
15		28	4		4	1
14		1	3	11I40	7	3
13		5	2		6	2
12		7	1		4	1
11	4A09	24	6	11I39	27	6
10		26	5		25	5
9		28	4		22	4
8		1	3		7	3
7		5	2		6	2
6		7	1		4	1
5	4A08	24	6	11I38	27	6
4		26	5		25	5
3		28	4		22	4
2		1	3		7	3
1		5	2		6	2
0		7	1		4	1

Write Dist

Bit	Module	Pin	TP	Module	Pin	TP
59	16I16	18	4	9H42	24	6
58		9	2		19	2
57		3	1		2	1
56	16I15	18	4	9H41	24	6
55		9	2		19	2
54		3	1		2	1
53	16I14	18	4	9H40	24	6
52		9	2		19	2
51		3	1		2	1
50	16I13	18	4	9H39	24	6
49		9	2		19	2
48		3	1		2	1
47	16I12	18	4	9H37	24	6
46		9	2		19	2
45		3	1		2	1
44	15I36	20	4	9H36	24	6
43		7	2		19	2
42		5	1		2	1
41	15I35	20	4	9H35	24	6
40		7	2		19	2
39		5	1		2	1
38	15I34	20	4	9H34	24	6
37		7	2		19	2
36		5	1		2	1
35	15I33	20	4	9H32	24	6
34		7	2		19	2
33		5	1		2	1
32	15I32	20	4	9H31	24	6
31		7	2		19	2
30		5	1		2	1
29	12I11	18	4	9H30	24	6
28		9	2		19	2
27		3	1		2	1
26	12I10	18	4	9H29	24	6
25		9	2		19	2
24		3	1		2	1
23	12I09	18	4	9H27	24	6
22		9	2		19	2
21		3	1		2	1
20	12I08	18	4	9H26	24	6
19		9	2		19	2
18		3	1		2	1
17	12I07	18	4	9H25	24	6
16		9	2		19	2
15		3	1		2	1
14	11I31	24	5	9H24	24	6
13		11	3		19	2
12		28	6		2	1
11	11I30	24	5	9H22	24	6
10		11	3		19	2
9		28	6		2	1
8	11I29	24	5	9H21	24	6
7		11	3		19	2
6		28	6		2	1
5	11I28	24	5	9H20	24	6
4		11	3		19	2
3		28	6		2	1
2	11I27	24	5	9H19	24	6
1		11	3		19	2
0		28	6		2	1

Store Dist

Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I16	20	4	10H24	24	6
58		7	2		19	2
57		5	1		2	1
56	16I15	20	4	10H23	24	6
55		7	2		19	2
54		5	1		2	1
53	16I14	20	4	10H22	24	6
52		7	2		19	2
51		5	1		2	1
50	16I13	20	4	10H21	24	6
49		7	2		19	2
48		5	1		2	1
47	16I12	20	4	10H19	24	6
46		7	2		19	2
45		5	1		2	1
44	15I36	18	4	10H18	24	6
43		9	2		19	2
42		3	1		2	1
41	15I35	18	4	10H17	24	6
40		9	2		19	2
39		3	1		2	1
38	15I34	18	4	10H16	24	6
37		9	2		19	2
36		3	1		2	1
35	15I33	18	4	10H14	24	6
34		9	2		19	2
33		3	1		2	1
32	15I32	18	4	10H13	24	6
31		9	2		19	2
30		3	1		2	1
29	12I11	20	4	10H12	24	6
28		7	2		19	2
27		5	1		2	1
26	12I10	20	4	10H11	24	6
25		7	2		19	2
24		5	1		2	1
23	12I09	20	4	10H09	24	6
22		7	2		19	2
21		5	1		2	1
20	12I08	20	4	10H08	24	6
19		7	2		19	2
18		5	1		2	1
17	12I07	20	4	10H07	24	6
16		7	2		19	2
15		5	1		2	1
14	11I31	20	4	10H06	24	6
13		7	2		19	2
12		5	1		2	1
11	11I30	20	4	10H04	24	6
10		7	2		19	2
9		5	1		2	1
8	11I29	20	4	10H03	24	6
7		7	2		19	2
6		5	1		2	1
5	11I28	20	4	10H02	24	6
4		7	2		19	2
3		5	1		2	1
2	11I27	20	4	10H01	24	6
1		7	2		19	2
0		5	1		2	1

Store Dist

Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I16	22	5	11H42	24	6
58		13	3		19	2
57		26	6		2	1
56	16I15	22	5	11H41	24	6
55		13	3		19	2
54		26	6		2	1
53	16I14	22	5	11H40	24	6
52		13	3		19	2
51		26	6		2	1
50	16I13	22	5	11H39	24	6
49		13	3		19	2
48		26	6		2	1
47	16I12	22	5	11H37	24	6
46		13	3		19	2
45		26	6		2	1
44	15I36	24	5	11H36	24	6
43		11	3		19	2
42		28	6		2	1
41	15I35	24	5	11H35	24	6
40		11	3		19	2
39		28	6		2	1
38	15I34	24	5	11H34	24	6
37		11	3		19	2
36		28	6		2	1
35	15I33	24	5	11H32	24	6
34		11	3		19	2
33		28	6		2	1
32	15I32	24	5	11H31	24	6
31		11	3		19	2
30		28	6		2	1
29	12I11	24	5	11H30	24	6
28		**11**	3		19	2
27		**28**	6		2	1
26	12I10	24	5	**11H29**	24	6
25		**11**	3		19	2
24		**28**	6		2	1
23	12I09	24	5	11H27	24	6
22		**11**	3		19	2
21		**28**	6		2	1
20	12I08	24	5	11H26	24	6
19		**11**	3		19	2
18		**28**	6		2	1
17	12I07	24	5	11H25	24	6
16		**11**	3		19	2
15		**28**	6		2	1
14	11I31	22	5	11H24	24	6
13		13	3		19	2
12		26	6		2	1
11	11I30	22	5	11H22	24	6
10		13	3		19	2
9		26	6		2	1
8	11I29	22	5	11H21	24	6
7		13	3		19	2
6		26	6		2	1
5	11I28	22	5	11H20	24	8
4		13	3		19	2
3		26	6		2	1
2	11I27	22	5	11H19	24	6
1		13	3		19	2
0		26	6		2	1

Store Dist

Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16I16	24	5	12I124	24	6
58		11	3		19	2
57		28	6		2	1
56	16I15	24	5	12I123	24	6
55		11	3		19	2
54		28	6		2	1
53	16I14	24	5	12I122	24	6
52		11	3		19	2
51		28	6		2	1
50	16I13	24	5	12I121	24	6
49		11	3		19	2
48		28	6		2	1
47	16I12	24	5	12I119	24	6
46		11	3		19	2
45		28	6		2	1
44	15I36	22	5	12I118	24	6
43		13	3		19	2
42		26	6		2	1
41	15I35	22	5	12I117	24	6
40		13	3		19	2
39		26	6		2	1
38	15I34	22	5	12I116	24	6
37		13	3		19	2
36		26	6		2	1
35	15I33	22	5	12I114	24	6
34		13	3		19	2
33		26	6		2	1
32	15I32	22	5	12I113	24	6
31		13	3		19	2
30		26	6		2	1
29	12I11	22	5	12I112	24	6
28		13	3		19	2
27		26	6		2	1
26	12I10	22	5	12H11	24	6
25		13	3		19	2
24		26	6		2	1
23	12I09	22	5	12H09	24	6
22		13	3		19	2
21		26	6		2	1
20	12I08	22	5	12I108	24	6
19		13	3		19	2
18		26	6		2	1
17	12I07	22	5	12I107	24	6
16		13	3		19	2
15		26	6		2	1
14	11I31	18	4	12H06	24	6
13		9	2		19	2
12		3	1		2	1
11	11I30	18	4	12H04	24	6
10		9	2		19	2
9		3	1		2	1
8	11I29	18	4	12I103	24	6
7		9	2		19	2
6		3	1		2	1
5	11I28	18	4	12I102	24	6
4		9	2		19	2
3		3	1		2	1
2	11I27	18	4	12I101	24	6
1		9	2		19	2
0		3	1		2	1

Store Dist

Read/ Dist/ Restore

Data Trunks
6613-D Central Memory

Store Distributor (CH 4)
to Write Distributor (CH 11, 12, 15, 16)

Read Distributor
to Store-Distribute
(CH 9, 10, 11, 12)

Sheet 1

Bit	Module	Pin	TP	Module	Pin	TP
59	4A17	24	6	16103	7	3
58		26	5		6	2
57		28	4		4	1
56		1	3	16102	27	6
55		5	2		25	5
54		7	1		22	4
53	4A16	24	6		7	3
52		26	5		6	2
51		28	4		4	1
50		1	3	16101	27	6
49		5	2		25	5
48		7	1		22	4
47	4A15	24	6		7	3
46		26	5		6	2
45		28	4		4	1
44		1	3	15140	7	3
43		5	2		6	2
42		7	1		4	1
41	4A14	24	6	15139	27	6
40		26	5		25	5
39		28	4		22	4
38		1	3		7	3
37		5	2		6	2
36		7	1		4	1
35	4A13	24	6	15138	27	6
34		26	5		25	5
33		28	4		22	4
32		1	3		7	3
31		5	2		6	2
30		7	1		4	1
29	4A12	24	6	12103	7	3
28		26	5		6	2
27		28	4		4	1
26		1	3	12102	27	6
25		5	2		25	5
24		7	1		22	4
23	4A11	24	6		7	3
22		26	5		6	2
21		28	4		4	1
20		1	3	12101	27	6
19		5	2		25	5
18		7	1		22	4
17	4A10	24	6		7	3
16		26	5		6	2
15		28	4		4	1
14		1	3	11140	7	3
13		5	2		6	2
12		7	1		4	1
11	4A09	24	6	11139	27	6
10		26	5		25	5
9		28	4		22	4
8		1	3		7	3
7		5	2		6	2
6		7	1		4	1
5	4A08	24	6	11138	27	6
4		26	5		25	5
3		28	4		22	4
2		1	3		7	3
1		5	2		6	2
0		7	1		4	1

Write Dist

Bit	Module	Pin	TP	Module	Pin	TP
59	16111	18	4	13H42	24	6
58		9	2		19	2
57		3	1		2	1
56	16110	18	4	13H41	24	6
55		9	2		19	2
54		3	1		2	1
53	16109	18	4	13H40	24	6
52		9	2		19	2
51		3	1		2	1
50	16108	18	4	13H39	24	6
49		9	2		19	2
48		3	1		2	1
47	16107	18	4	13H37	24	6
46		9	2		19	2
45		3	1		2	1
44	15131	18	4	13H36	24	6
43		9	2		19	2
42		3	1		2	1
41	15130	18	4	13H35	24	6
40		9	2		19	2
39		3	1		2	1
38	15129	18	4	13H34	24	6
37		9	2		19	2
36		3	1		2	1
35	15128	18	4	13H32	24	6
34		9	2		19	2
33		3	1		2	1
32	15127	18	4	13H31	24	6
31		9	2		19	2
30		3	1		2	1
29	12116	24	5	13H30	24	6
28		11	3		19	2
27		28	6		2	1
26	12115	24	5	13H29	24	6
25		11	3		19	2
24		28	6		2	1
23	12114	24	5	13H27	24	6
22		11	3		19	2
21		26	6		2	1
20	12113	24	5	13H26	24	6
19		11	3		19	2
18		28	6		2	1
17	12112	24	5	13H25	24	6
16		11	3		19	2
15		28	6		2	1
14	11136	24	5	13H24	24	6
13		11	3		19	2
12		28	6		2	1
11	11135	24	5	13H22	24	6
10		11	3		19	2
9		28	6		2	1
8	11134	24	5	13H21	24	6
7		11	3		19	2
6		28	6		2	1
5	11133	24	5	13H20	24	6
4		11	3		20	2
3		28	6		2	1
2	11132	24	5	13H19	24	6
1		11	3		19	2
0		28	6		2	1

Store Dist | Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16111	20	4	14H24	24	6
58		7	2		19	2
57		5	1		2	1
56	16110	20	4	14H23	24	6
55		7	2		19	2
54		5	1		2	1
53	16109	20	4	14H22	24	6
52		7	2		19	2
51		5	1		2	1
50	16108	20	4	14H21	24	6
49		7	2		19	2
48		5	1		2	1
47	16107	20	4	14H19	24	6
46		7	2		19	2
45		5	1		2	1
44	15131	20	4	14H18	24	6
43		7	2		19	2
42		5	1		2	1
41	15130	20	4	14H17	24	6
40		7	2		19	2
39		5	1		2	1
38	15129	20	4	14H16	24	6
37		7	2		19	2
36		5	1		2	1
35	15128	20	4	14H14	24	6
34		7	2		19	2
33		5	1		2	1
32	15127	20	4	14H13	24	6
31		7	2		19	2
30		5	1		2	1
29	12116	22	5	14H12	24	6
28		13	3		19	2
27		26	6		2	1
26	12115	22	5	14H11	24	6
25		13	3		19	2
24		26	6		2	1
23	12114	22	5	14H09	24	6
22		13	3		19	2
21		26	6		2	1
20	12113	22	5	14H08	24	6
19		13	3		19	2
18		26	6		2	1
17	12112	22	5	14H07	24	6
16		13	3		19	2
15		26	6		2	1
14	11136	22	5	14H06	24	6
13		13	3		19	2
12		26	6		2	1
11	11135	22	5	14H04	24	6
10		13	3		19	2
9		26	6		2	1
8	11134	22	5	14H03	24	6
7		13	3		19	2
6		26	6		2	1
5	11133	22	5	14H02	24	6
4		13	3		19	2
3		26	6		2	1
2	11132	22	5	14H01	24	6
1		13	3		19	2
0		26	6		2	1

Store Dist | Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16111	22	5	15H42	24	6
58		13	3		19	2
57		26	6		2	1
56	16110	22	5	15H41	24	6
55		13	3		19	2
54		26	6		2	1
53	16109	22	5	15H40	24	6
52		13	3		19	2
51		26	6		2	1
50	16108	22	5	15H39	24	6
49		13	3		19	2
48		26	6		2	1
47	16107	22	5	15H37	24	6
46		13	3		19	2
45		26	6		2	1
44	15131	22	5	15H36	24	6
43		13	3		19	2
42		26	6		2	1
41	15130	22	5	15H35	24	6
40		13	3		19	2
39		26	6		2	1
38	15129	22	5	15H34	24	6
37		13	3		19	2
36		26	6		2	1
35	15128	22	5	15H32	24	6
34		13	3		19	2
33		26	6		2	1
32	15127	22	5	15H31	24	6
31		13	3		19	2
30		26	6		2	1
29	12116	18	4	15H30	24	6
28		9	2		19	2
27		3	1		2	1
26	12115	18	4	15H29	24	6
25		9	2		19	2
24		3	1		2	1
23	12114	18	4	15H27	24	6
22		9	2		19	2
21		3	1		2	1
20	12113	18	4	15H26	24	6
19		9	2		19	2
18		3	1		2	1
17	12112	18	4	15H25	24	6
16		9	2		19	2
15		3	1		2	1
14	11136	18	4	15H24	24	6
13		9	2		19	2
12		3	1		2	1
11	11135	18	4	15H22	24	6
10		9	2		19	2
9		3	1		2	1
8	11134	18	4	15H21	24	6
7		9	2		19	2
6		3	1		2	1
5	11133	18	4	15H20	24	6
4		9	2		19	2
3		3	1		2	1
2	11132	18	4	15H19	24	6
1		9	2		19	2
0		3	1		2	1

Store Dist | Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	16111	24	5	16H24	24	6
58		11	3		19	2
57		28	6		2	1
56	16110	24	5	16H23	24	6
55		11	3		19	2
54		28	6		2	1
53	16109	24	5	16H22	24	6
52		11	3		19	2
51		28	6		2	1
50	16108	24	5	16H21	24	6
49		11	3		19	2
48		28	6		2	1
47	16107	24	5	16H19	24	6
46		11	3		19	2
45		28	6		2	1
44	15131	24	5	16H18	24	6
43		11	3		19	2
42		28	6		2	1
41	15130	24	5	16H17	24	6
40		11	3		19	2
39		28	6		2	1
38	15129	24	5	16H16	24	6
37		11	3		19	2
36		28	6		2	1
35	15128	24	5	16H14	24	6
34		11	3		19	2
33		28	6		2	1
32	15127	24	5	16H13	24	6
31		11	3		19	2
30		28	6		2	1
29	12116	20	4	16H12	24	6
28		7	2		19	2
27		5	1		2	1
26	12115	20	4	16H11	24	6
25		7	2		19	2
24		5	1		2	1
23	12114	20	4	16H09	24	6
22		7	2		19	2
21		5	1		2	1
20	12113	20	4	16H08	24	6
19		7	2		19	2
18		5	1		2	1
17	12112	20	4	16H07	24	6
16		7	2		19	2
15		5	1		2	1
14	11136	20	4	16H06	24	6
13		7	2		19	2
12		5	1		2	1
11	11135	20	4	16H04	24	6
10		7	2		19	2
9		5	1		2	1
8	11134	20	4	16H03	24	6
7		7	2		19	2
6		5	1		2	1
5	11133	20	4	16H02	24	6
4		7	2		19	2
3		5	1		2	1
2	11132	20	4	16H01	24	6
1		7	2		19	2
0		5	1		2	1

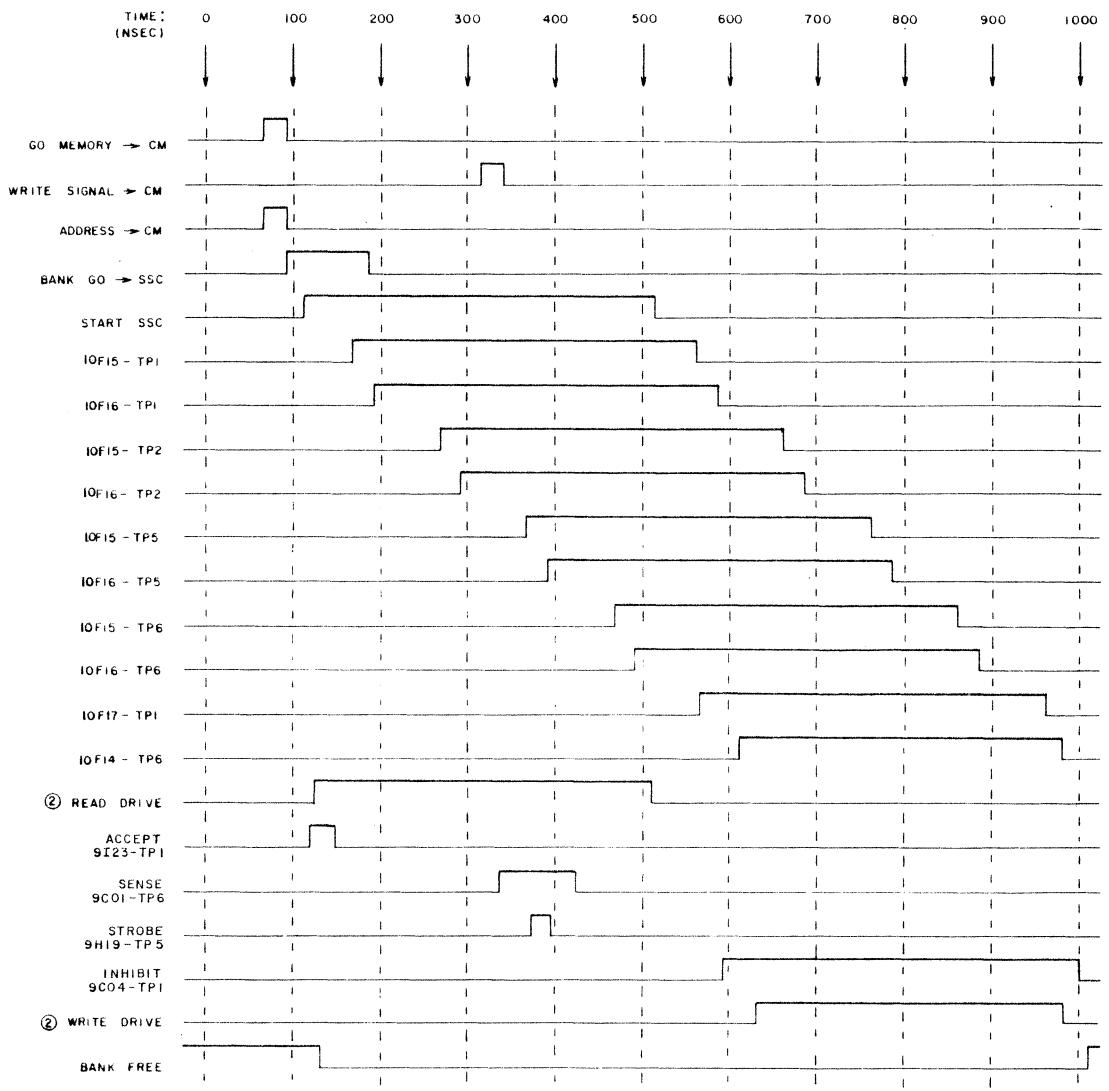
Store Dist | Read/ Dist/ Restore

Data Trunks
6613-D Central Memory

Store Distributor (CH 4)
to Write Distributor (CH 11, 12, 15, 16)

Store Distributor
to Read-Distribute-Restore
(CH 13, 14, 15, 16)

Sheet 2



NOTES:

1. STORAGE CYCLE TIMING IS TYPICAL FOR ALL MEMORY CHASSIS (CHASSIS 10, BANK 00 LOCATIONS AND TP'S SHOWN).
② READ/WRITE DRIVE TIMES SHOWN ARE THAT OF OUTPUT PINS ON 10F14

THIS SHEET IS IDENTICAL TO CENTRAL MEMORY (65K) PAGE 15

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL MEMORY STORAGE CYCLE TIMING	PRODUCT 6613-D SIZE C | DRAWING NO. 60246600 | REV. A SHEET 45 | PAGE 1-19

PART 2

CENTRAL MEMORY (65 K)

PART 2

CENTRAL MEMORY (65K)

CONTENTS

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2-2	Go Control
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2-7	Data Flow/Write Control
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2-13	Write Distributor
2-14	Write Distributor Test Points
2-15	Storage Cycle Timing

ADDRESSING

The CP programs are stored in CM, and all PPs may use CM for supplementary storage or inter-communication control. Thus CM addresses are generated by the CP and all PPs.

Each processor sends a CM address to a common address clearing house, or stunt box, from where they are sent on to CM. The stunt box can accept addresses from the several sources at 100-nsec intervals (maximum rate) on a priority basis and in turn issue one address every 100 nsec to CM.

An address goes to all banks of CM for decoding, and the referenced bank returns an accept signal to the stunt box if the bank is not busy (free) with a previous reference. The stunt box saves each address that it sends to CM in a hopper mechanism, and, if the address is not accepted, it is recovered from the hopper and re-issued to CM and again saved. The issue-save cycle repeats until an accept is received to void the hopper address. Up to three addresses can be saved in the hopper. However, an address is always accepted within 2000 nsec (worst case because of bank conflict) of the first time it is issued.

DATA DISTRIBUTION

Data to and from CM is distributed from a data distributor. The word from a read reference goes from CM to the data distributor and then to the requesting processor. A word to be stored during a write reference goes from the processor to the data distributor to CM. The distributor can transfer a word to or from CM every 100 nsec. A store word goes to all banks of CM, but separate storage control mechanisms for each bank ensure that the word is stored in the proper bank.

The distributor routes data to and from proper origins and destinations as directed by control information or tags received from the stunt box. The tags are entered in the stunt box along with each address and serve to identify the address sender, origin or destination of data, and nature of the address, e.g., read, write, or PP exchange jump. The stunt box sends the tags to the data distributor (and to destinations in the processors for read references) when an address is accepted, and the distributor accomplishes the data transmission. For write references, the data source sends the word to the distributor, where it is held temporarily before it is stored.

STORAGE

The many banks of storage in CM are evenly distributed on 4 chassis in the computer. There are four banks per chassis.

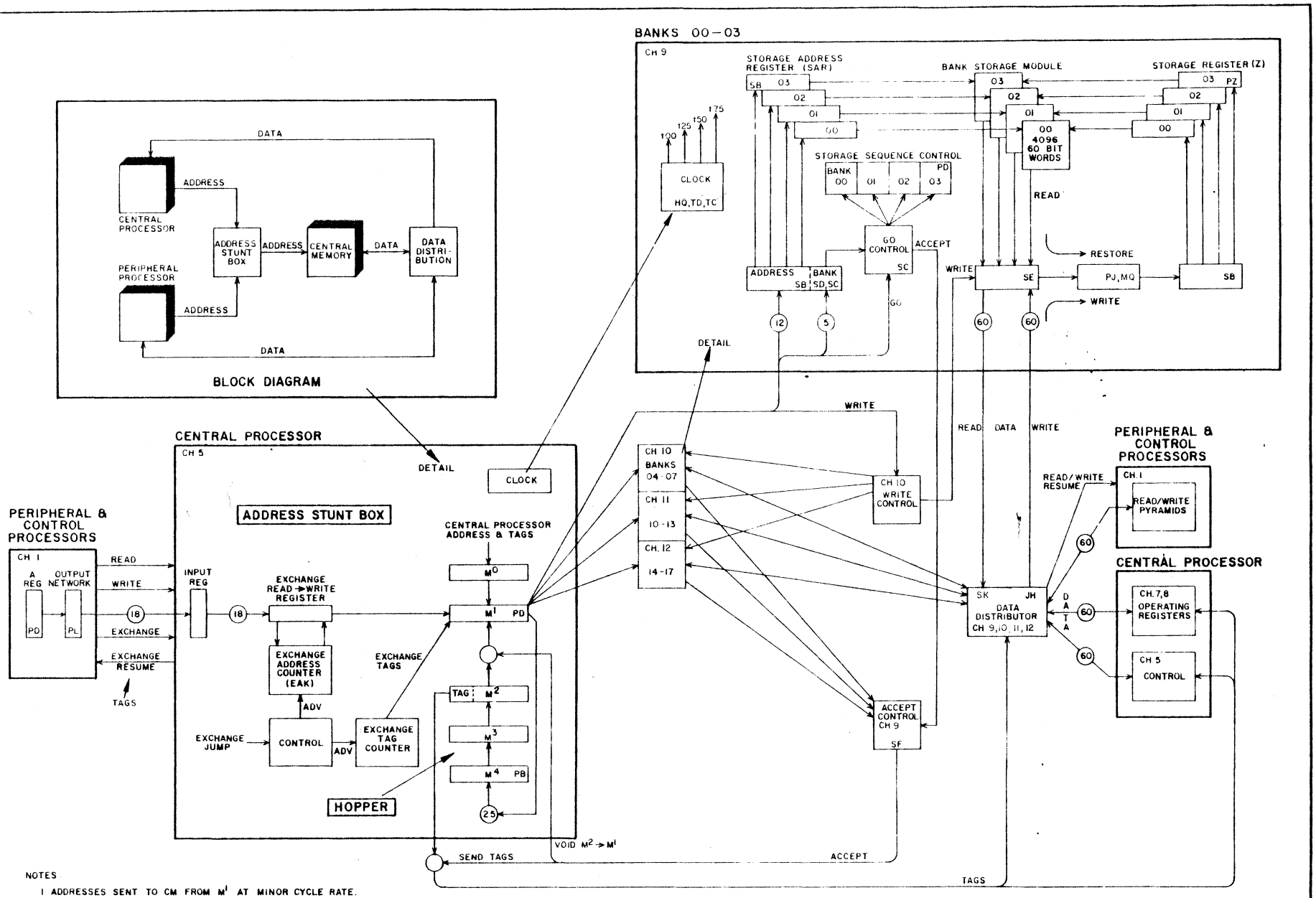
The circuit organization allows the four banks to operate independently and be phased into operation at 100-nsec intervals, which corresponds to the maximum rate at which the stunt box issues addresses. A chassis input register receives the 17-bit address from the stunt box and distributes the 12-bit address to 1 of 4 storage address registers associated with the four banks. Hence 16 consecutive addresses referencing 16 separate banks may be accepted at 16 consecutive minor cycle intervals and result in a data word flowing to or from CM in 16 consecutive minor cycle intervals. The independent controls for each bank and treatment of the address and data word ensure that only one bank is in a given time segment of its 1000 nsec storage cycle at any one time. At least one minor cycle separates the storage cycle of all banks.

A word read from any bank is sent to a common temporary storage register and to the data distributor by a common path. A word to be restored is then sent to a write register by way of a buffer register. The write register sends the word to 1 or 4 restoration registers for restoring in the proper bank.

A word from the data distributor during a write reference goes to the temporary storage register on all chassis and then follows the restore path for writing in memory. Only one of the many banks is in the proper time spot in its storage cycle to store the word received, and this bank is the one associated with the write address.

A go signal with each address from the stunt box allows a group of four banks (one chassis) to recognize and translate the bank bits. The referenced bank, if not busy, sends an accept to the stunt box and starts 1 of 4 storage sequence control circuits, which in turn direct the 1000 nsec storage cycle for the selected address.

A write signal may also accompany each address from the stunt box. It distinguishes read and write references and controls the path to the restoration registers. The CM uses the same 12-bit storage module as used in the PPs, but five are driven in parallel to hold the 60-bit word.



NOTES

1. ADDRESSES SENT TO CM FROM M^1 AT MINOR CYCLE RATE.
2. DATA MOVES TO/FROM CM AT MINOR CYCLE RATE
3. ADDRESS TAGS DEFINE ORIGIN / DESTINATION OF DATA.
4. TIME FROM M^1 → CM TO RESPONSE TO CM ACCEPT IS 200 NSEC
   a. M^1 STORED IN M^4 AT ISSUE TIME AND MOVES TO M^2 IN TIME SEQUENCE
   b. ACCEPT VOIDS RE-ISSUE OF ADDRESS FROM HOPPER.

CONTROL DATA CORPORATION	TITLE: CENTRAL MEMORY (65K) ADDRESS - DATA FLOW	PRODUCT: 6614-D	
COMPUTER DIVISION		SIZE: C	DRAWING NO: 60246600
		SHEET: 242	2-1

GO CONTROL (65K)

A go control circuit is associated with each chassis (four banks) of CM. The circuit has several functions.

1. Recognize an address from the stunt box and determine if it is located in an associated bank.
2. Sends an accept to the stunt box if the address is valid and the bank if free.
3. Starts the 1000 nsec storage cycle to read or store the word at the selected address.

No accept is sent to the stunt box if the selected bank is executing a storage cycle from a previously issued address (bank busy case). The address is ignored in this case. The time of address issue from the stunt box and the time the accept should be received back at the stunt box is 200 nsec, and this time is used by the stunt box to determine if the address has been accepted. An accept at the proper time voids reissue of the address; otherwise address reissue continues until the accept is received.

BANK SELECTION

The go signal accompanying each address signals all CM go control circuits to search the bank selection bits and determine if the 12-bit address is located in one of its associated banks. A translator circuit in each go control translates the lower five bits of the address, stores the selection in a FF (one FF for each bank), sends the accept, and starts the storage sequence control circuit to start the storage cycle.

The five bits provide 16 unique codes, one for each bank. The upper three bits select 1 of 4 chassis and the lower two bits 1 of 4 banks on the chassis.

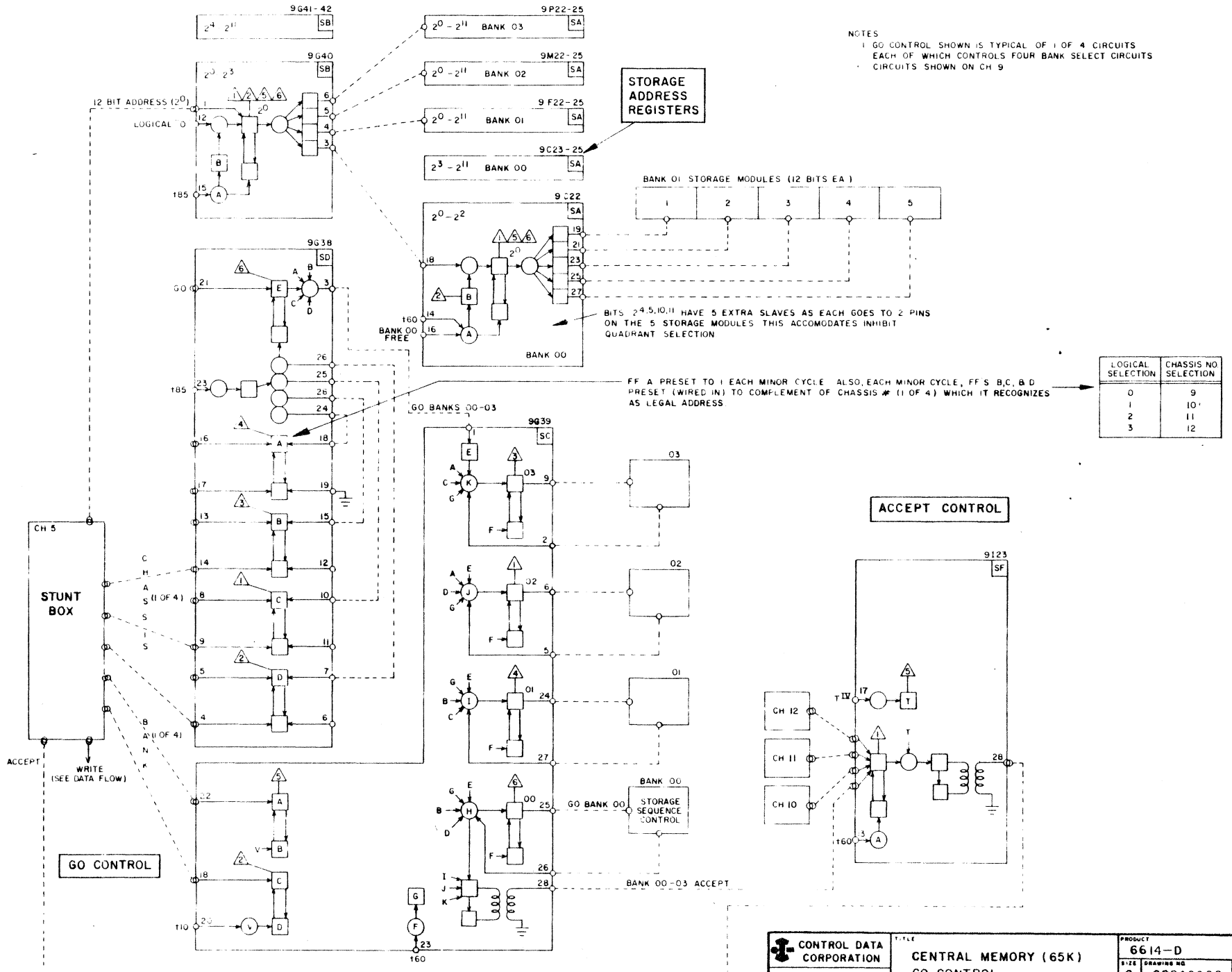
The 17-bit address and bank quantity is stored in an input FF register. Before an address is received, a clock pulse presets the upper three of the five bank bits to the complement of the quantity it should recognize. Thus, for a zero chassis selection (physical chassis 3), the upper three bits are preset to 111XX, the complement of 000XX. A 000XX bank code then is necessary to complete the go FF output gate, which in turn allows recognition of the lower two bits of the bank selection.

Four unique translations are made from the lower two bits of the bank selection bits and stored in separate FFs. A go from the 1 of 8 translator, a bank free condition from the storage sequence control circuit, and a clock pulse gates the 1 of 4 storage and turns on the accept signal. The set FF then starts an associated storage sequence control circuit.

ACCEPT CONTROL

The accept signal indicates a bank is free and has accepted the address in its chassis input register. The time interval from address issue from the stunt box to receipt of the accept in the stunt box allows the stunt box to determine if the address has been accepted. If so, the address in the stunt box hopper is destroyed, and address tags are sent from the stunt box to the data distributor and other areas to tell the address sender to send its data word (write reference) or be ready for receipt of the word read (read reference).

One accept is associated with each chassis for a maximum of eight signals. All are combined in a common OR circuit which feeds the stunt box. Since an address may be sent each 100 nsecs, an accept may be sent to the stunt box every 100 nsecs, with each accept delayed from its associated address by 200 nsecs.



CONTROL DATA CORPORATION	TITLE	CENTRAL MEMORY (65K)	PRODUCT 6614-D
COMPUTER DIVISION		GO CONTROL	SIZE C DRAWING NO. 60246600 REV A
		ACCEPT CONTROL	SHEET 243 2-3

STORAGE SEQUENCE CONTROL

Storage sequence control responds to a bank go condition from go control and generates a series of timing signals which direct the basic cycle of the storage module. In general, the circuit establishes the bank free condition, makes the address available to the storage module, and then issues read, sense, start and end inhibit, bank merge, and write drive signals to sequence reading and writing. The sense signal samples the differential amplifier which receives the data word read out on the double-ended sense lines from storage. The signals time the basic pulse sequence of the 1000 nsec storage cycle. The storage module discussion details the circuits which respond to the address and read and write drive signals, and thereby make the read word available on the sense lines, or store the word to be written or restored in memory.

TIMING CHAIN

The timing chain is a series chain of FFs whose outputs drive slave inverters, which in turn supply the various signals to sequence reading and writing in CM. A pulse enters the chain and is transferred to successive FFs at 50 nsec intervals. A bank go signal sets the read FF to start the sequence. Each FF is set for 400 nsecs; slave inverters from set and cleared FFs in the chain are combined to establish timed gating signals for the various drive signals.

BANK FREE

The bank free condition is established when all FFs in the chain are cleared, i.e., no pulse is travelling down the chain. The read FF, an intermediate FF, and write FFs (last FF in chain), contribute timing signals to the bank free circuit and indicate whether a pulse is in the chain. All three FFs must be cleared to signal bank free, but their set states overlap to signal bank busy when a pulse is in the chain.

The bank free signal allows go control to respond to its back translation circuits and issue a bank go signal which sets the read FF to turn off the bank free signal.

STORAGE CYCLE TIMING

The following are the recommended times or timing durations for Central Memory in all 6000 series computers:

Strobe (time 75 ± 5 nsec)

This is measured on TP5 of the SE module, (see page 7). This time should be adjusted by varying the length of wire to pin 16 of the SG module.

Read-On (255 nsec ± 5 nsec) before Strobe.

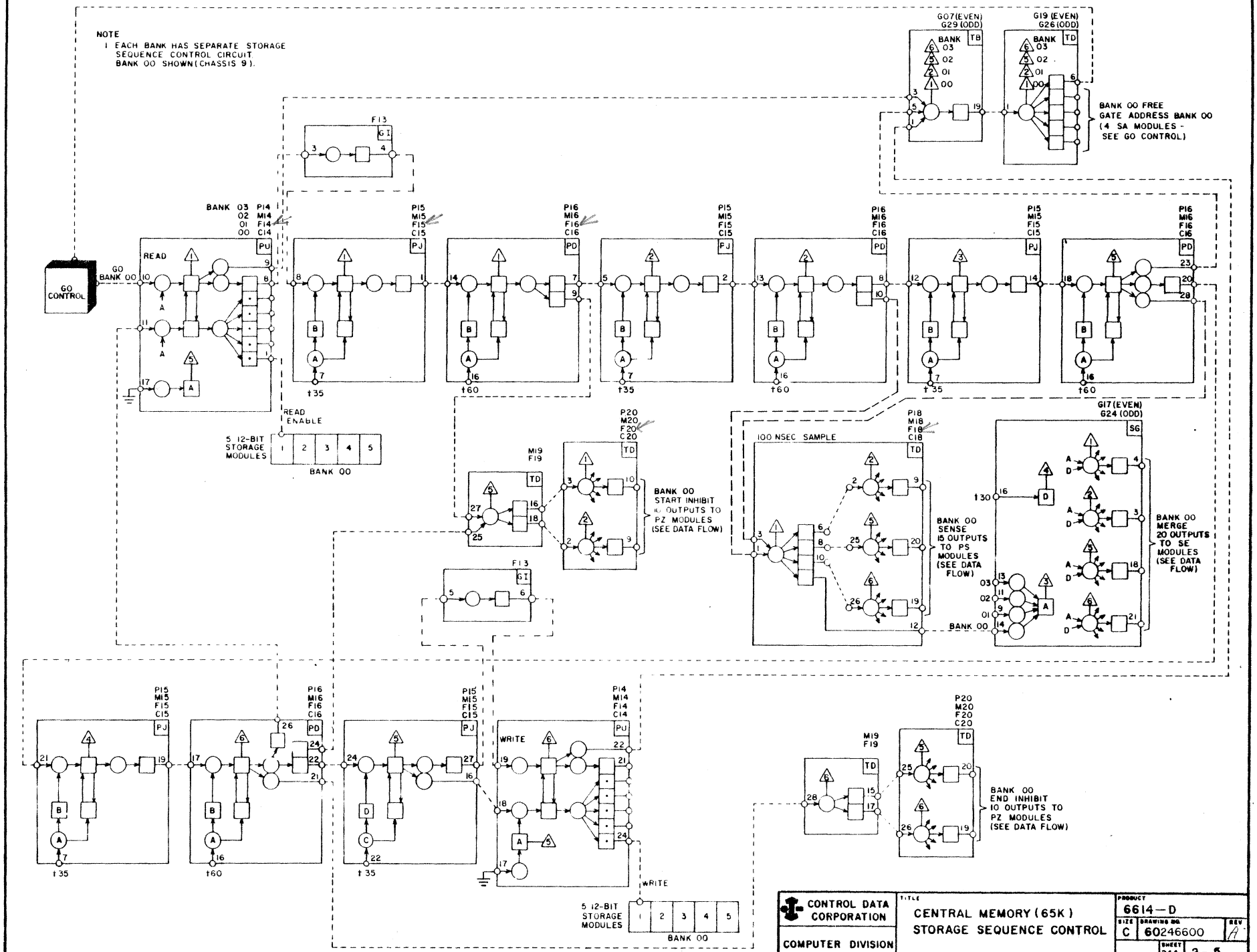
This is measured on pin 1 of the PU module. This time should be adjusted by varying the length of wire to pin 10 of the PU module and/or pin 2 of the GI module.

Read-Off (395 nsec ± 5 nsec) after the start of Read.

This is measured on pin 1 of the PU module. This time should be adjusted by varying the length of wire to pin 11 of the PU module.

Write (355 nsec ± 5 nsec)

This is measured on pin 24 of the PU module. This time should be adjusted by varying the length of wire to pin 19 of the PU module and/or pin 5 of the GI module. (See also page 7).



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE
CENTRAL MEMORY (65K)
STORAGE SEQUENCE CONTROL

PRODUCT 6614-D
SIZE C | DRAWING NO. 60246600 | REV A
SHEET 244 | 2-5

In a read reference, the read word from the specified address flows from the storage modules to the data distributor and also back to the storage modules for restoration. The SE modules send the read word to the distributor and start the restore portion of the cycle. The restore FFs on these modules are cleared just before receiving the read word.

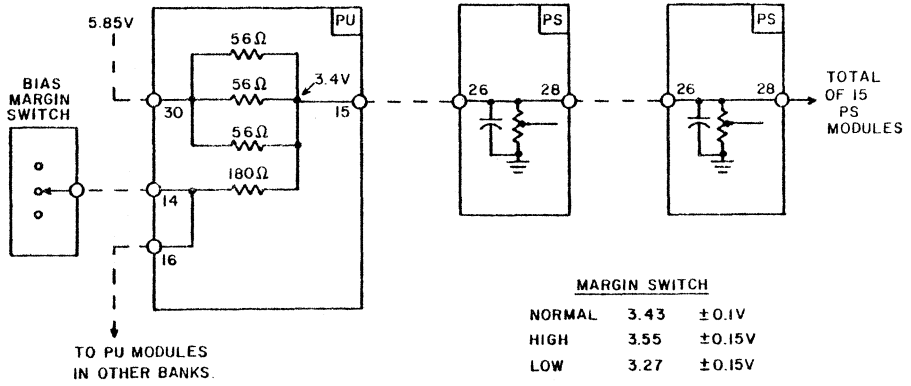
In a write reference, the read word from the specified address is sent to the data distributor and entered in the restore FFs of the SE modules. The restore FFs are cleared again to destroy the read word and reset with the write word which is stored in place of the read word during its normal restore cycle. The write control circuit and timing of stunt box tags direct the sequence.

WRITE CONTROL

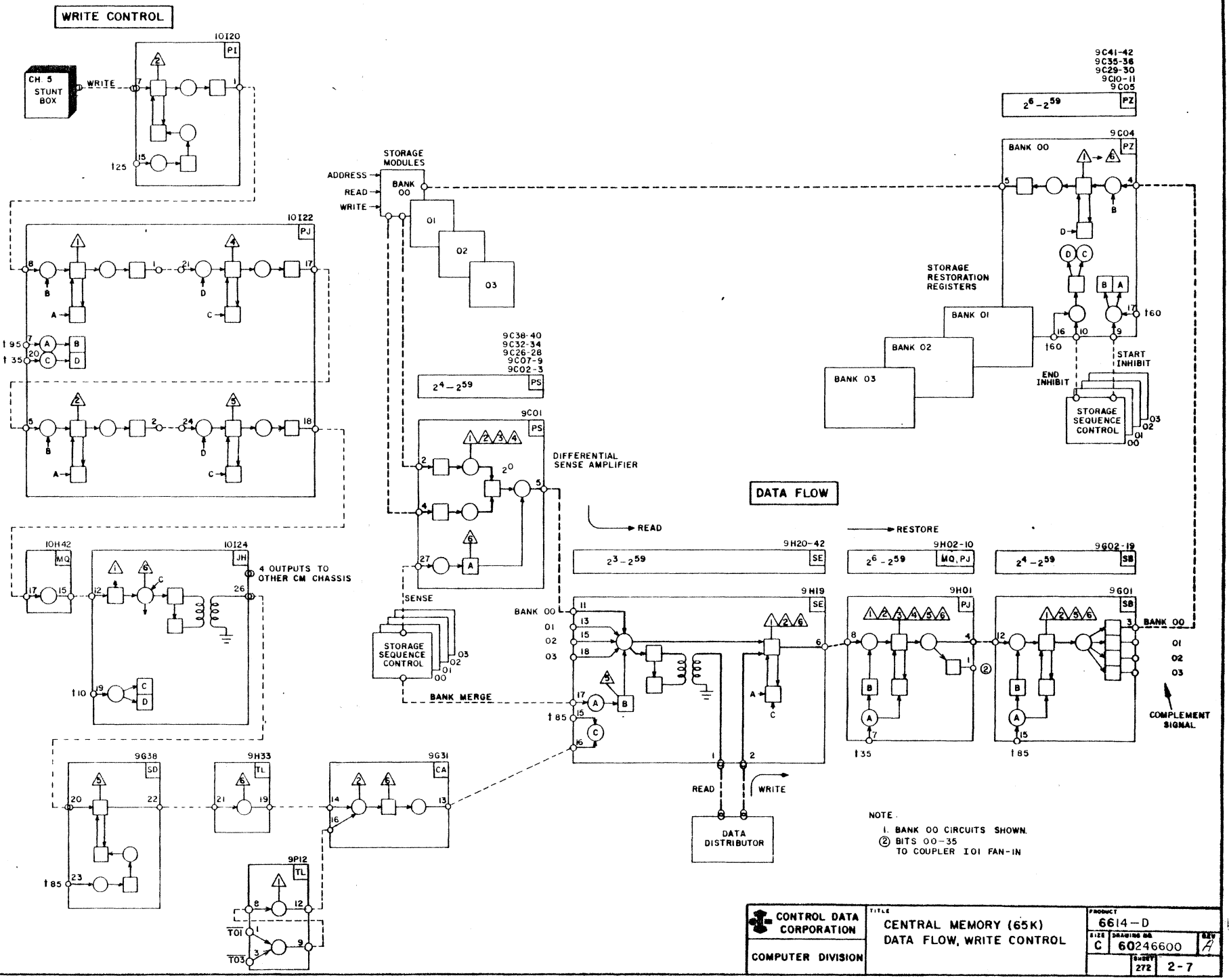
Write control clears the restore FFs in the SE modules when writing in memory and thereby allows entry of the write word into the restore circuits.

A write signal from the stunt box enters the write control timing chain the same time as the memory address is received in the input register of all memory chassis. The timing chain feeds a pulse to all chassis where they are fanned out and clear the restore FFs on the respective chassis SE modules. The delay time through the chain and format just exceeds the read access time and thereby destroys the read word immediately after it enters the SE restore FF. Effectively, the pulse in the timing chain runs in parallel with the pulse in the storage sequence control associated with the selected bank, but the write pulse from the timing chain fanout is emitted just after the bank merge pulse (which enters the read word in the SE restore FFs) from storage sequence control. Write pulses may enter the chain at minor cycle intervals and each is associated with a parallel operating storage sequence control.

The timing within the data distributor is such that a write word is sent to the SE modules slightly later than the SE modules send the read word to the data distributor.



CENTRAL MEMORY SENSE BIAS CIRCUIT


WRITE CONTROL
CH 5 STUNT BOX
WRITE
10I20
PI
10I22
PJ
STORAGE MODULES
ADDRESS
READ
WRITE
BANK 00
01
02
03
9C38-40
9C32-34
9C26-28
9C07-9
9C02-3
2^4-2^{59}
PS
9C01
DIFFERENTIAL SENSE AMPLIFIER
9C41-42
9C35-36
9C29-30
9C10-11
9C05
2^6-2^{59}
PZ
9C04
STORAGE RESTORATION REGISTERS
BANK 01
BANK 02
BANK 03
START INHIBIT
END INHIBIT
STORAGE SEQUENCE CONTROL
DATA FLOW
READ
RESTORE
2^3-2^{59}
9H20-42
SE
2^6-2^{59}
9H02-10
MQ, PJ
2^4-2^{59}
9G02-19
SB
9H19
9H01
9G01
10H42
MQ
10I24
JH
4 OUTPUTS TO OTHER CM CHASSIS
SENSE
STORAGE SEQUENCE CONTROL
BANK MERGE
BANK 00
COMPLEMENT SIGNAL
9G38
SD
9H33
TL
9G31
CA
9P12
TL
DATA DISTRIBUTOR
NOTE
1. BANK 00 CIRCUITS SHOWN.
(2) BITS 00-35 TO COUPLER 101 FAN-IN
CONTROL DATA CORPORATION
COMPUTER DIVISION
TITLE
CENTRAL MEMORY (65K)
DATA FLOW, WRITE CONTROL
PRODUCT
6614-D
SIZE C
DRAWING NO. 60246600
REV A
SHEET 272
2-7

DATA DISTRIBUTOR

The data distributor distributes read and write words to and from CM. Read words are sent to CP control on chassis 5, CP registers on chassis 7 and 8, and to the PP on chassis 1.

Write words are accepted from CP control on chassis 5 (exchange or return jump instructions), CP register chassis 7 and 8 (X^{0-7} registers), or from the PP on chassis 1.

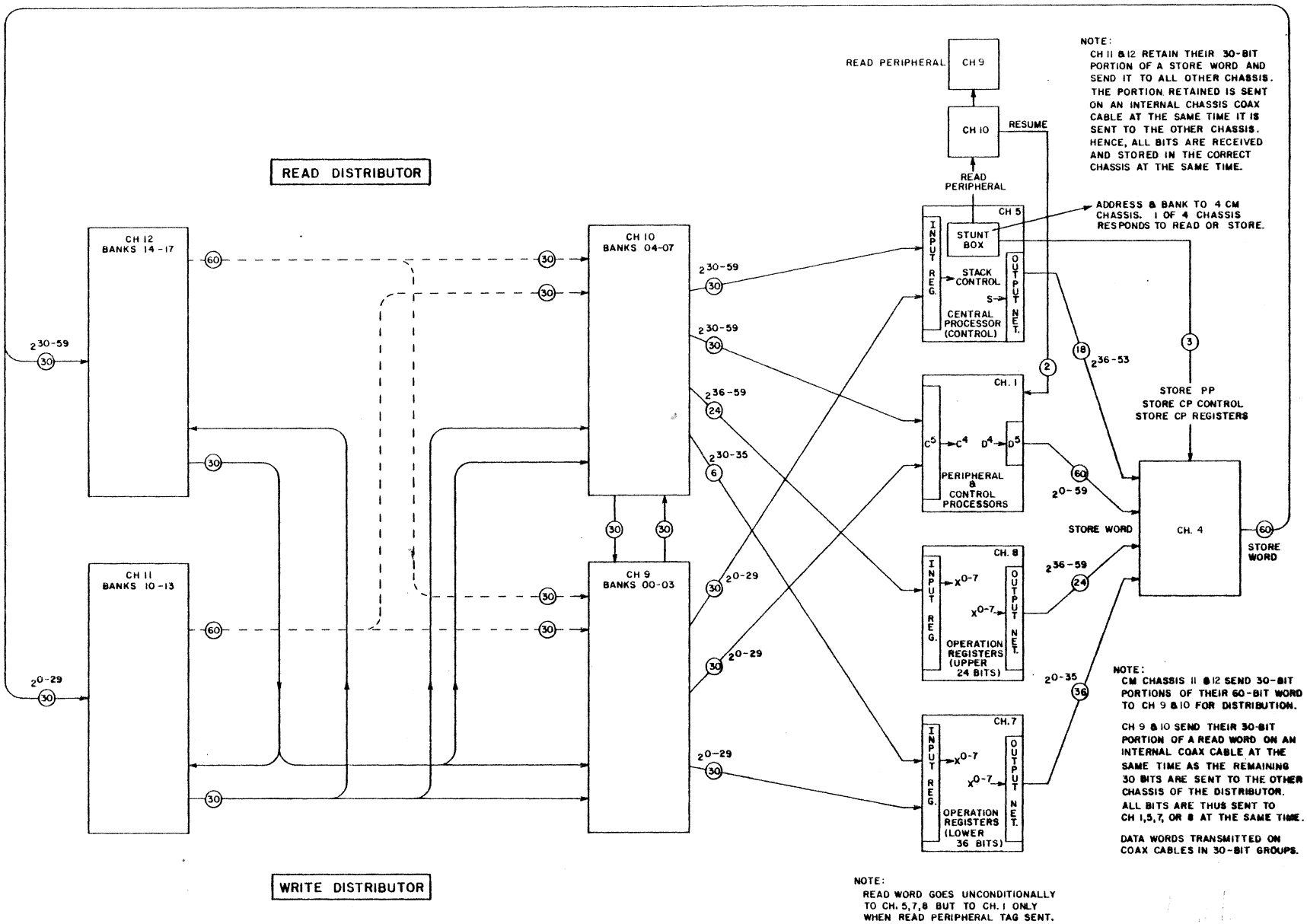
Address tags from the CP stunt box define the read or write cases and the origin or destination of the data.

STORAGE CYCLE TIMING

Inhibit On and Off

The inhibit should turn on at least 20 nsec before the start of the Write, and stay on at least 15 nsec after the end of the Write. The inhibit time is measured on pin 5 of the PZ module and is compared to the Write on pin 24 of the PU module. It should not be necessary to adjust the on time for the inhibit 30-50 nsec is the usual delay between inhibit-on and write-on. The off time is adjusted by varying the length of wire to pin 14 of C21, F21, M21, or P21 (clock working ranks).

The read pulse should be adjusted to obtain 395 nsec ± 5 nsec.



CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL MEMORY (65K) DATA DISTRIBUTOR	PROJECT 6614-D SIZE C · DRAWING NO. 60246600 · REV A SHEET 2 · PAGE 2-9

READ DISTRIBUTOR

The read distributor accepts read words from the 4 CM chassis and routes them to the several destinations.

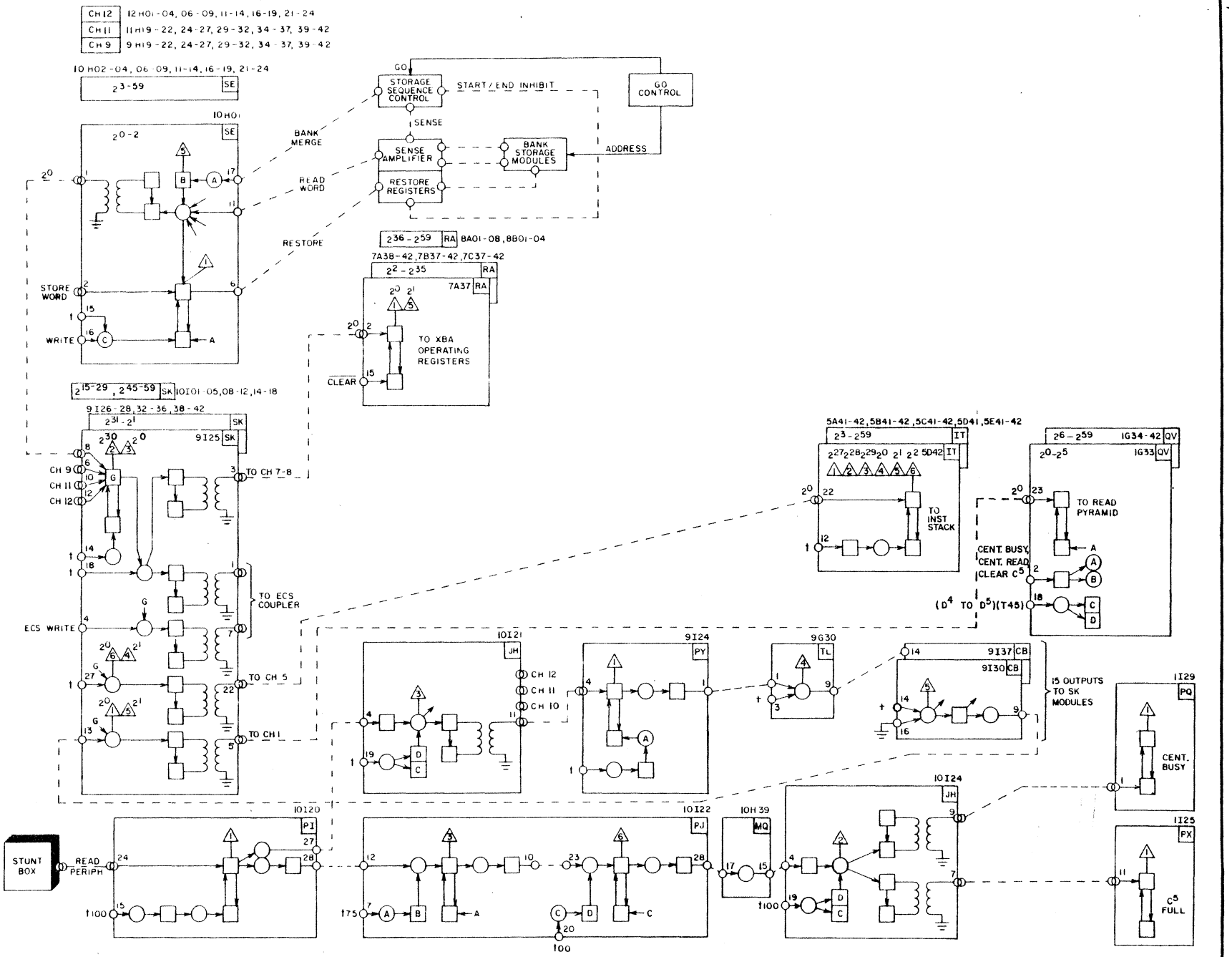
The distributor is organized on chassis 9 and 10 each of which handles 30 bits of the 60-bit word. Chassis cable limitations dictate the organization. The listing below shows the bits handled by each chassis.

CHASSIS	BITS
9	0-14, 30-44
10	15-29, 45-59

Chassis 11-12 each send the same 30-bit group to chassis 9 and 10. A read word from chassis 9 retains bits 0-29 but sends remaining bits to chassis 10. Read words from chassis 10 are handled similarly. Intra-chassis coaxial cables are used on chassis 9 and 10 or their 30-bit portions so that timing is consistent with the chassis receiving the data.

Each read word is sent unconditionally from chassis 9 and 10 to chassis 5 (CP control) and chassis 7 and 8 (CP registers). A read peripheral tag from the stunt box is sent to chassis 4 and then on to chassis 8. The tag gates the read word to the C^5 register in the read pyramid on PP chassis 1.

The read peripheral tag also enters a time delay chain and is returned to the PP as a resume signal. The resume sets the C^5 full FF in the PP (after data word is in C^5) to signal the presence of the read word. The same resume also clears the central busy FF to indicate to PP control that the address has been accepted by the stunt box and CM has delivered the word. This allows the PPs to proceed and send another address to the stunt box.



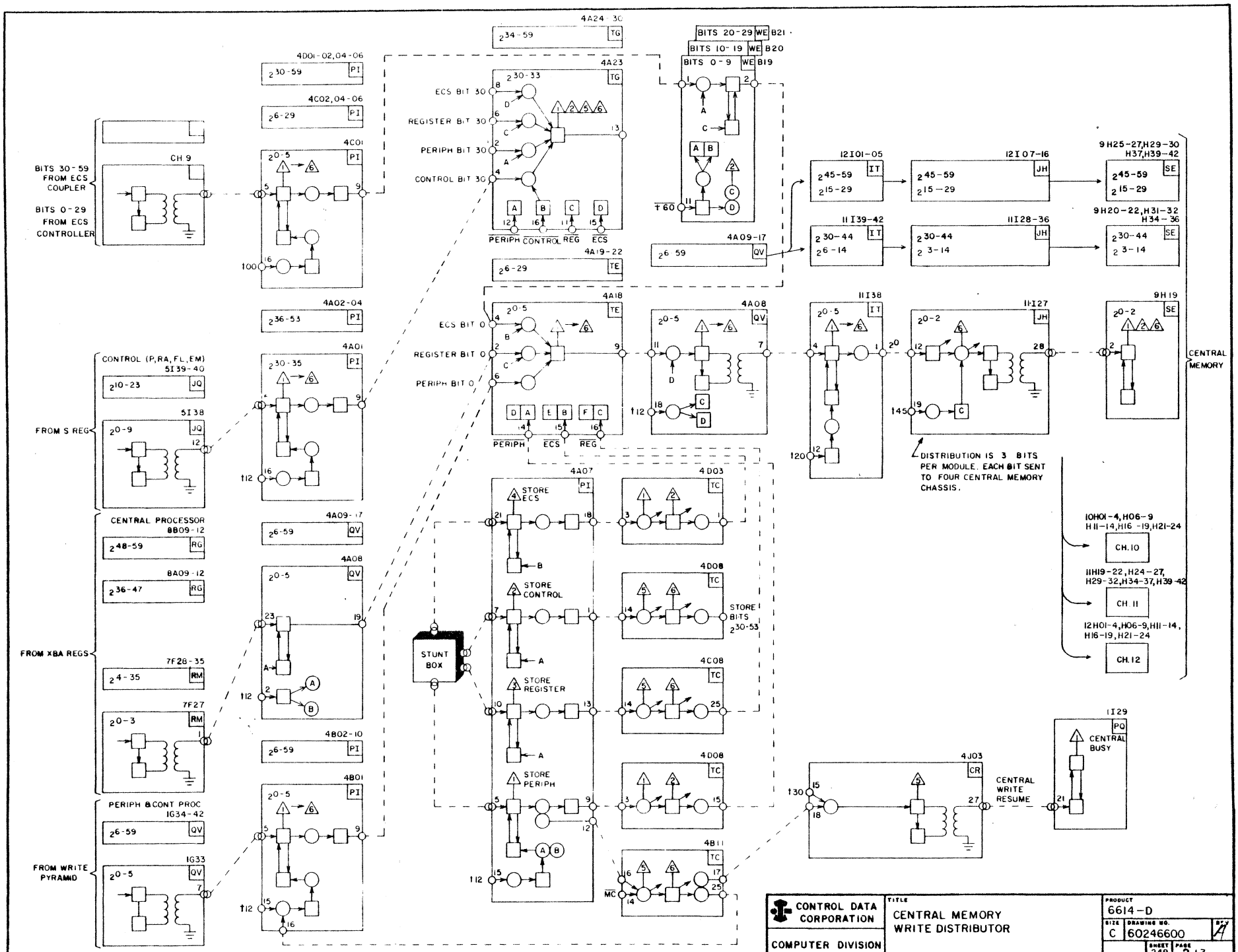
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL MEMORY (65K) READ DISTRIBUTOR	PRODUCT 6614-D	
		SIZE C	DRAWING NO. 60246600 REV P
		SHEET 265	PAGE 2-11

WRITE DISTRIBUTOR

The write distributor accepts words from the several sources and stores them in 1 of 4 memory chassis. The distributor is on chassis 4. The 60-bit word on chassis 4 is split into two 30-bit groups which are sent to chassis 11-12 respectively. Each of these chassis in turn sends (or stores) its 30-bit group to the other 2 chassis unconditionally.

A 3-to-1 fan-in on chassis 4 selects the proper word under control of the store tag from the stunt box which is established ahead of the data. The word is then split and transmitted to chassis 9-10. The chassis 4 data registers and the tag FFs are cleared simultaneously.

One minor cycle after the register clear, a central write resume is sent to the PP to clear the central busy FF and allow the PPs to send another address to the stunt box.



CONTROL DATA CORPORATION
COMPUTER DIVISION

TITLE
CENTRAL MEMORY WRITE DISTRIBUTOR

PRODUCT 6614-D
SIZE C
DRAWING NO. 60246600
REV H
SHEET 249
PAGE 2-13

Bit	Module	Pin	TP	Module	Pin	TP
59	4A17	24	6	12I05	27	6
58		26	5		25	5
57		28	4		22	4
56		1	3		7	3
55		5	2		6	2
54		7	1		4	1
53	4A16	24	6	12I04	27	6
52		26	5		25	5
51		28	4		22	4
50		1	3		7	3
49		5	2		6	2
48		7	1		4	1
47	4A15	24	6	12I03	27	6
46		26	5		25	5
45		28	4		22	4
44		1	3	11I42	27	6
43		5	2		25	5
42		7	1		22	4
41	4A14	24	6		7	3
40		26	5		6	2
39		28	4		4	1
38		1	3	11I41	27	6
37		5	2		25	5
36		7	1		22	4
35	4A13	24	6		7	3
34		26	5		6	2
33		28	4		4	1
32		1	3	11I40	27	6
31		5	2		25	5
30		7	1		22	4
29	4A12	24	6	12I03	7	3
28		26	5		6	2
27		28	4		4	1
26		1	3	12I02	27	6
25		5	2		25	5
24		7	1		22	4
23	4A11	24	6		7	3
22		26	5		6	2
21		28	4		4	1
20		1	3	12I01	27	6
19		5	2		25	5
18		7	1		22	4
17	4A10	24	6		7	3
16		26	5		6	2
15		28	4		4	1
14		1	3	11I40	7	3
13		5	2		6	2
12		7	1		4	1
11	4A09	24	6	11I39	27	6
10		26	5		25	5
9		28	4		22	4
8		1	3		7	3
7		5	2		6	2
6		7	1		4	1
5	4A08	24	6	11I38	27	6
4		26	5		25	5
3		28	4		22	4
2		1	3		7	3
1		5	2		6	2
0		7	1		4	1

Store Dist

Bit	Module	Pin	TP	Module	Pin	TP
59	12I16	18	4	9H42	24	6
58		9	2		19	2
57		3	1		2	1
56	12I15	18	4	9H41	24	6
55		9	2		19	2
54		3	1		2	1
53	12I14	18	4	9H40	24	6
52		9	2		19	2
51		3	1		2	1
50	12I13	18	4	9H39	24	6
49		9	2		19	2
48		3	1		2	1
47	12I12	18	4	9H37	24	6
46		9	2		19	2
45		3	1		2	1
44	11I36	20	4	9H36	24	6
43		7	2		19	2
42		5	1		2	1
41	11I35	20	4	9H35	24	6
40		7	2		19	2
39		5	1		2	1
38	11I34	20	4	9H34	24	6
37		7	2		19	2
36		5	1		2	1
35	11I33	20	4	9H32	24	6
34		7	2		19	2
33		5	1		2	1
32	11I32	20	4	9H31	24	6
31		7	2		19	2
30		5	1		2	1
29	12I11	18	4	9H30	24	6
28		9	2		19	2
27		3	1		2	1
26	12I10	18	4	9H29	24	6
25		9	2		19	2
24		3	1		2	1
23	12I09	18	4	9H27	24	6
22		9	2		19	2
21		3	1		2	1
20	12I08	18	4	9H26	24	6
19		9	2		19	2
18		3	1		2	1
17	12I07	18	4	9H25	24	6
16		9	2		19	2
15		3	1		2	1
14	11I31	24	5	9H24	24	6
13		11	3		19	2
12		28	6		2	1
11	11I30	24	5	9H22	24	6
10		11	3		19	2
9		28	6		2	1
8	11I29	24	5	9H21	24	6
7		11	3		19	2
6		28	6		2	1
5	11I28	24	5	9H20	24	6
4		11	3		19	2
3		28	6		2	1
2	11I27	24	5	9H19	24	6
1		11	3		19	2
0		28	6		2	1

Store Dist

Bit	Module	Pin	TP	Module	Pin	TP
59	12I16	20	4	10H24	24	6
58		7	2		19	2
57		5	1		2	1
56	12I15	20	4	10H23	24	6
55		7	2		19	2
54		5	1		2	1
53	12I14	20	4	10H22	24	6
52		7	2		19	2
51		5	1		2	1
50	12I13	20	4	10H21	24	6
49		7	2		19	2
48		5	1		2	1
47	12I12	20	4	10H19	24	6
46		7	2		19	2
45		5	1		2	1
44	11I36	18	4	10H18	24	6
43		9	2		19	2
42		3	1		3	1
41	11I35	18	4	10H17	24	6
40		9	2		19	2
39		3	1		3	1
38	11I34	18	4	10H16	24	6
37		9	2		19	2
36		3	1		2	1
35	11I33	18	4	10H14	24	6
34		9	2		19	2
33		3	1		2	1
32	11I32	18	4	10H13	24	6
31		9	2		19	2
30		3	1		2	1
29	12I11	20	4	10H12	24	6
28		7	2		19	2
27		5	1		2	1
26	12I10	20	4	10H11	24	6
25		7	2		19	2
24		5	1		2	1
23	12I09	20	4	10H09	24	6
22		7	2		19	2
21		5	1		2	1
20	12I08	20	4	10H08	24	6
19		7	2		19	2
18		5	1		2	1
17	12I07	20	4	10H07	24	6
16		7	2		19	2
15		5	1		2	1
14	11I31	20	4	10H06	24	6
13		7	2		19	2
12		5	1		2	1
11	11I30	20	4	10H04	24	6
10		7	2		19	2
9		5	1		2	1
8	11I29	20	4	10H03	24	6
7		7	2		19	2
6		5	1		2	1
5	11I28	20	4	10H02	24	6
4		7	2		19	2
3		5	1		2	1
2	11I27	20	4	10H01	24	6
1		7	2		19	2
0		5	1		2	1

Store Dist / Read/ Dist/ Restore

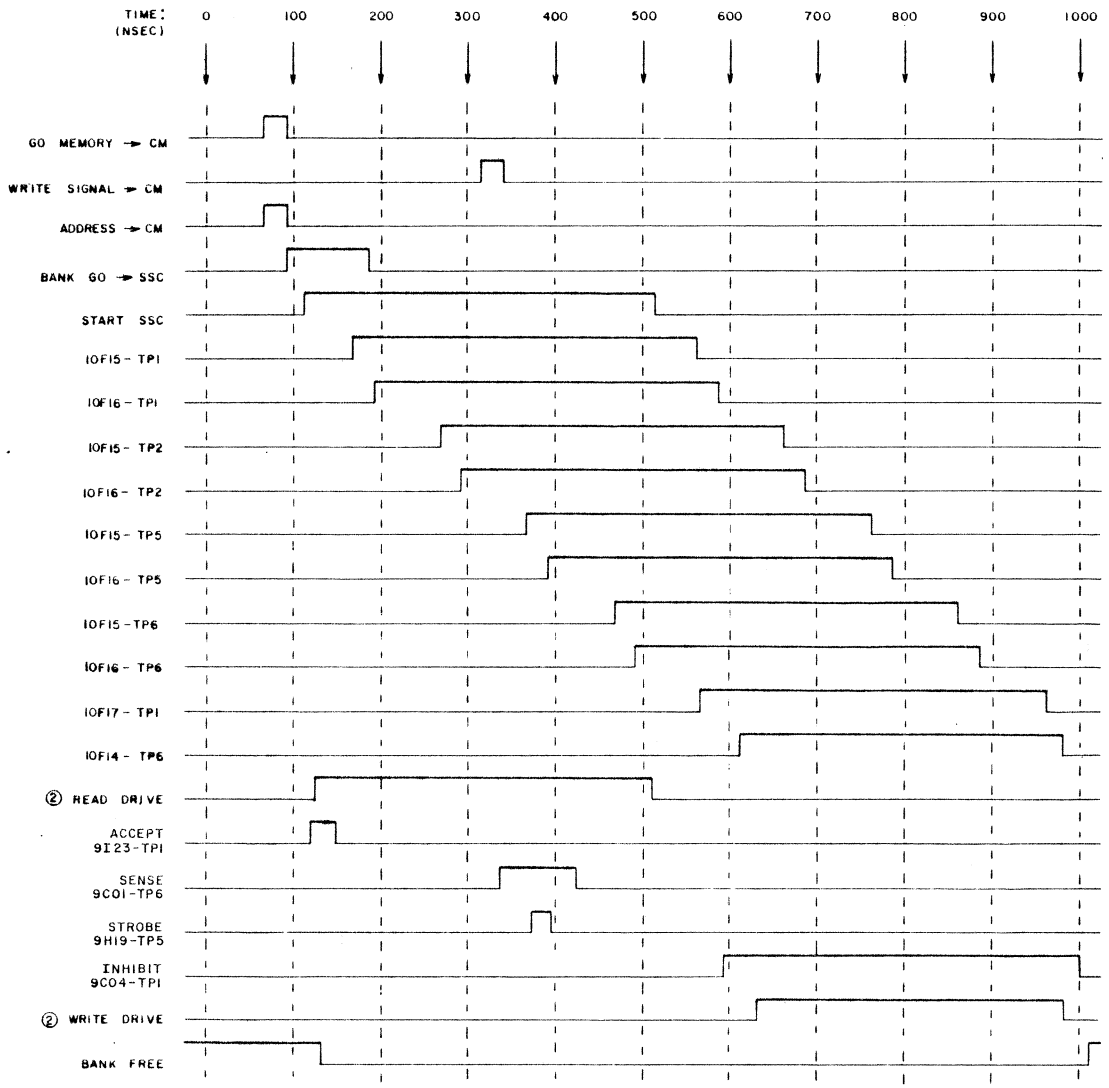
Bit	Module	Pin	TP	Module	Pin	TP
59	12I16	22	5	11I42	24	6
58		13	3		19	2
57		26	6		2	1
56	12I15	22	5	11I41	24	6
55		13	3		19	2
54		26	6		2	1
53	12I14	22	5	11I40	24	6
52		13	3		19	2
51		26	6		2	1
50	12I13	22	5	11H39	24	6
49		13	3		19	2
48		26	6		2	1
47	12I12	22	5	11H37	24	6
46		13	3		19	2
45		26	6		2	1
44	11I36	24	5	11H36	24	6
43		11	3		19	2
42		28	6		2	1
41	11I35	24	5	11H35	24	6
40		11	3		19	2
39		28	6		2	1
38	11I34	24	5	11H34	24	6
37		11	3		19	2
36		28	6		2	1
35	11I33	24	5	11H32	24	6
34		11	3		19	2
33		28	6		2	1
32	11I32	24	5	11H31	24	6
31		11	3		19	2
30		28	6		2	1
29	12I11	24	5	11H30	24	6
28		11	3		19	2
27		28	6		2	1
26	12I10	24	5	11H29	24	6
25		11	3		19	2
24		28	6		2	1
23	12I09	24	5	11H27	24	6
22		11	3		19	2
21		28	6		2	1
20	12I08	24	5	11H26	24	6
19		11	3		19	2
18		28	6		2	1
17	12I07	24	5	11H25	24	6
16		11	3		19	2
15		28	6		2	1
14	11I31	22	5	11H24	24	6
13		13	3		19	2
12		26	6		2	1
11	11I30	22	5	11H22	24	6
10		13	3		19	2
9		26	6		2	1
8	11I29	22	5	11H21	24	6
7		13	3		19	2
6		26	6		2	1
5	11I28	22	5	11H20	24	6
4		13	3		19	2
3		26	6		2	1
2	11I27	22	5	11H19	24	6
1		13	3		19	2
0		26	6		2	1

Store Dist / Read/ Dist/ Restore

Bit	Module	Pin	TP	Module	Pin	TP
59	12I16	24	5	12H24	24	6
58		11	3		19	2
57		28	6		2	1
56	12I15	24	5	12H23	24	6
55		11	3		19	2
54		28	6		2	1
53	12I14	24	5	12H22	24	6
52		11	3		19	2
51		28	6		2	1
50	12I13	24	5	12H21	24	6
49		11	3		19	2
48		28	6		2	1
47	12I12	24	5	12H19	24	6
46		11	3		19	2
45		28	6		2	1
44	11I36	22	5	12H18	24	6
43		13	3		19	2
42		26	6		2	1
41	11I35	22	5	12H17	24	6
40		13	3		19	2
39		26	6		2	1
38	11I34	22	5	12H16	24	6
37		13	3		19	2
36		26	6		2	1
35	11I33	22	5	12H14	24	6
34		13	3		19	2
33		26	6		2	1
32	11I32	22	5	12H13	24	6
31		13	3		19	2
30		26	6		2	1
29	12I11	22	5	12H12	24	6
28		13	3		19	2
27		26	6		2	1
26	12I10	22	5	12H11	24	6
25		13	3		19	2
24		26	6		2	1
23	12I09	22	5	12H09	24	6
22		13	3		19	2
21		26	6		2	1
20	12I08	22	5	12H08	24	6
19		13	3		19	2
18		26	6		2	1
17	12I07	22	5	12H07	24	6
16		13	3		19	2
15		26	6		2	1
14	11I31	18	4	12H06	24	6
13		9	2		19	2
12		3	1		2	1
11	11I30	18	4	12H04	24	6
10		9	2		19	2
9		3	1		2	1
8	11I29	18	4	12H03	24	6
7		9	2		19	2
6		3	1		2	1
5	11I28	18	4	12H02	24	6
4		9	2		19	2
3		3	1		2	1
2	11I27	18	4	12H01	24	6
1		9	2		19	2
0		3	1		2	1

Store Dist / Read/ Dist/ Restore

Data trunks 6f14-D Memory
Read/Distribute/Restore
Ch. 9, 10, 11, 12



NOTES:

1. STORAGE CYCLE TIMING IS TYPICAL FOR ALL MEMORY CHASSIS (CHASSIS 10, BANK 00 LOCATIONS AND TP'S SHOWN).
2. READ/WRITE DRIVE TIMES SHOWN ARE THAT OF OUTPUT PINS ON 10F14.

THIS SHEET IS IDENTICAL TO CENTRAL MEMORY (131K) PAGE 19

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL MEMORY STORAGE CYCLE TIMING	PRODUCT 6614-D SIZE C | DRAWING NO 60246600 | REV A SHEET 45 | PAGE 2-15

PART 3

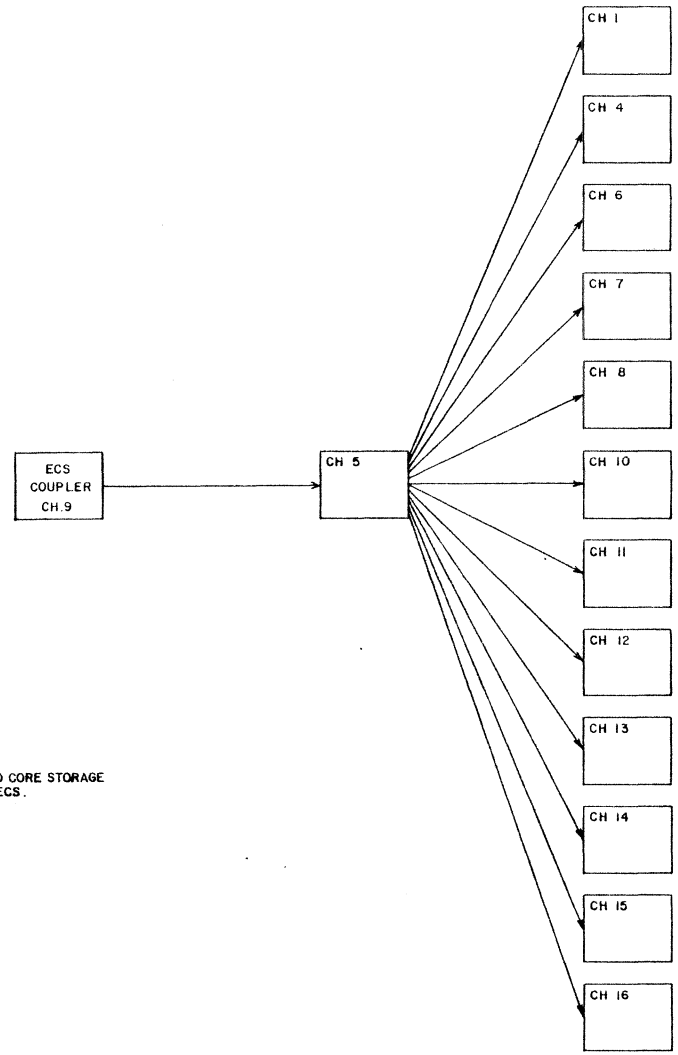
CLOCK

PART 3

CLOCK

CONTENTS

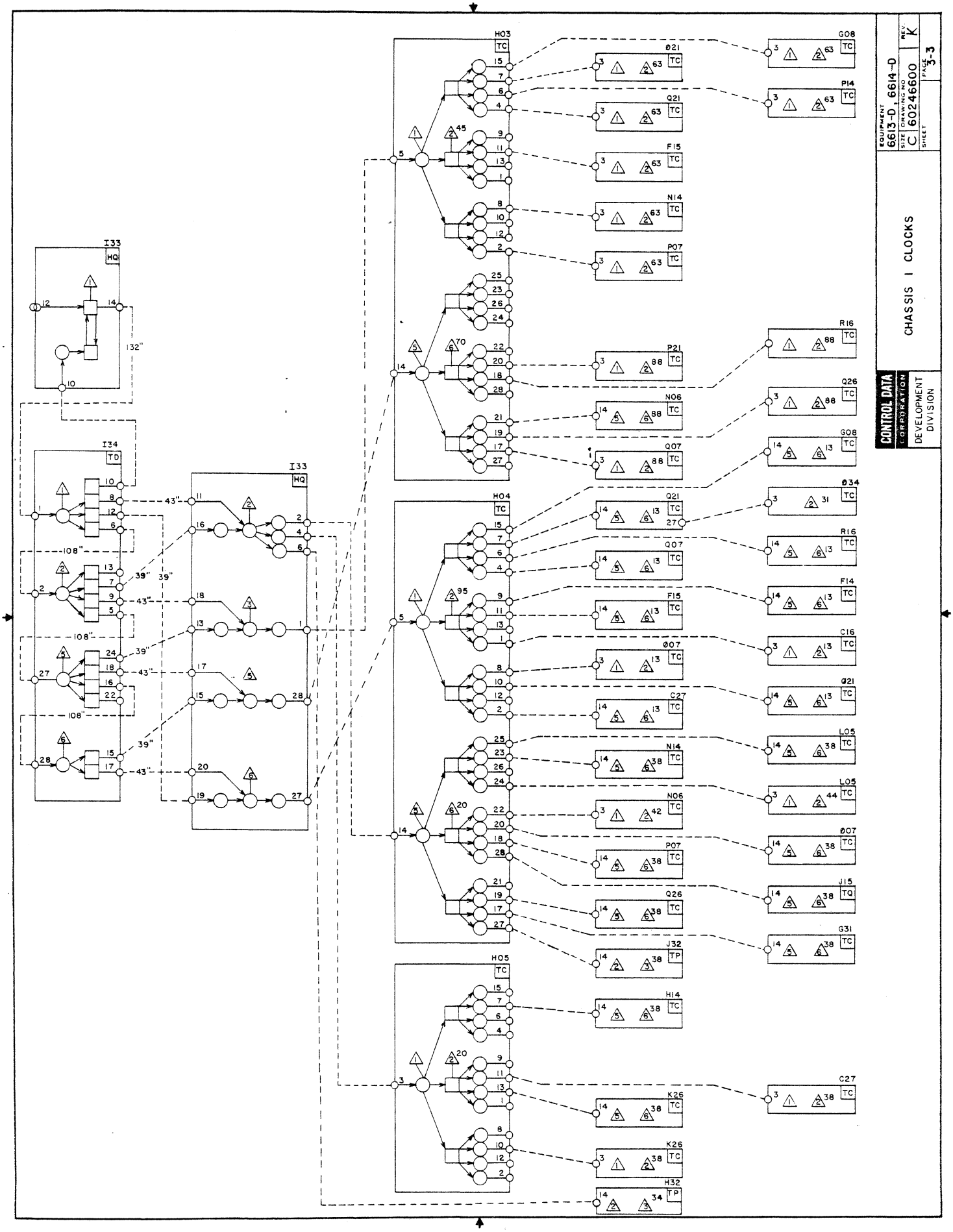
Page	
3-1	Central Computer Clock System
3-3	Central Processor Clock, Chassis 1
3-5	Central Processor Clock, Chassis 4
3-7	Central Processor Clock, Chassis 5
3-9	Central Processor Clock, Chassis 6
3-11	Central Processor Clock, Chassis 7
3-13	Central Processor Clock, Chassis 8
3-13.1	10 MHz Clock, ECS Coupler
3-15	Central Memory Clock, Chassis 9
3-17	Central Memory Clock, Chassis 10
3-19	Central Memory Clock, Chassis 11 and 15
3-21	Central Memory Clock, Chassis 12 and 16
3-23	Central Memory Clock, Chassis 13
3-25	Central Memory Clock, Chassis 14

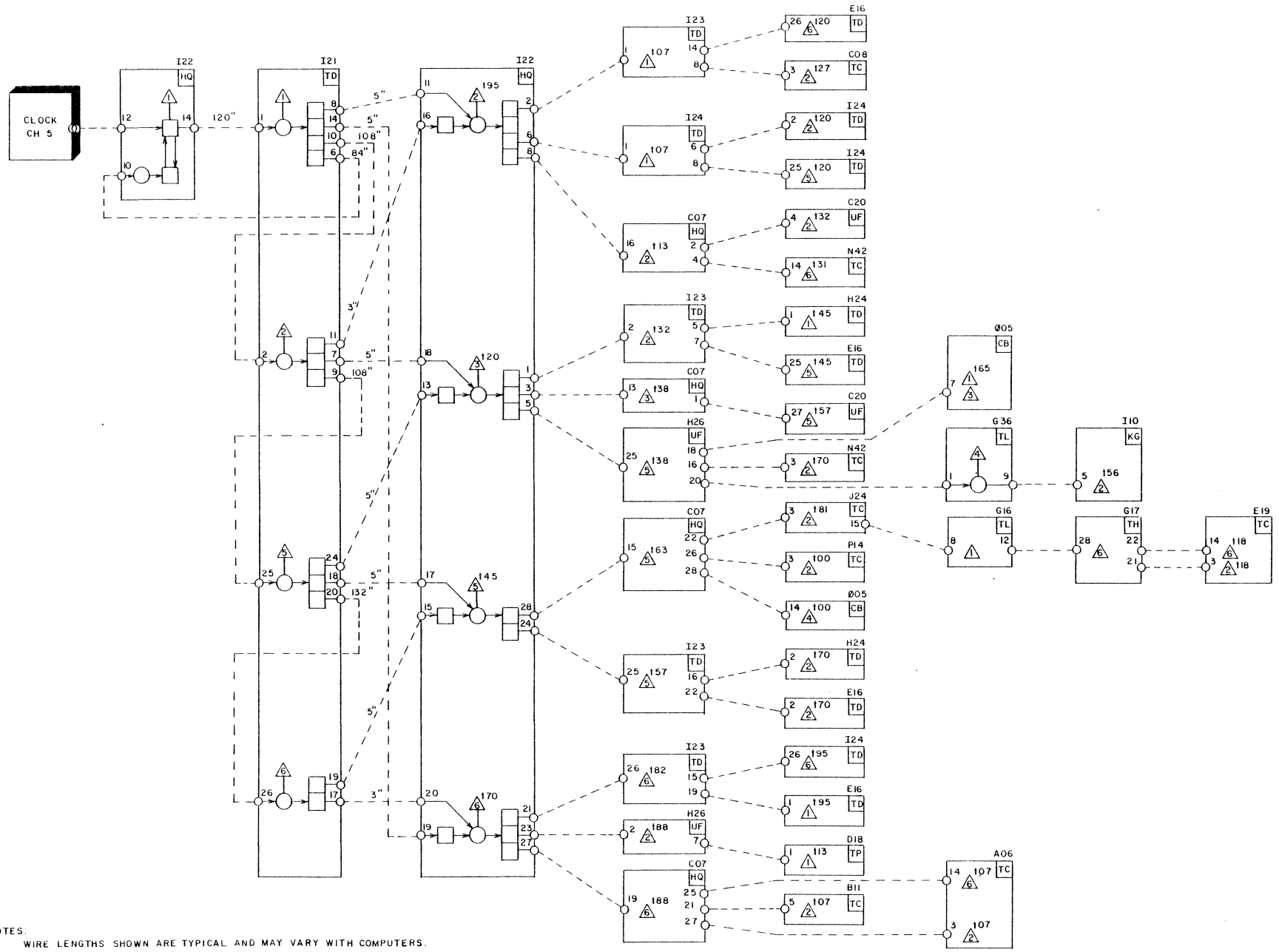


NOTE :

THE 6600 CLOCK SYSTEM IS DRIVEN BY THE EXTENDED CORE STORAGE (ECS) COUPLER ONLY ON THOSE SYSTEMS CONTAINING ECS.

CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL COMPUTER CLOCK SYSTEM	PRODUCT 6613-D, 6614-D SIZE C · DRAWING NO. 60246600 · REV SHEET 115 · PAGE 3-1


I33
HQ
I34
TD
I33
HQ
H03
TC
H04
TC
H05
TC
Ø21
Q21
F15
N14
P07
P21
N06
Q07
Q21
F15
Ø07
C27
N14
N06
P07
Q26
J32
H14
K26
K26
H32
TP
G08
P14
R16
Q26
G08
Ø34
R16
F14
C16
Ø21
L05
L05
Ø07
J15
G31
C27
43"
39"
108"
132"
CHASSIS I CLOCKS
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
EQUIPMENT 6613-D, 6614-D
SIZE C
DRAWING NO 60246600
SHEET
REV K
PAGE 3-3



NOTES:
WIRE LENGTHS SHOWN ARE TYPICAL AND MAY VARY WITH COMPUTERS.

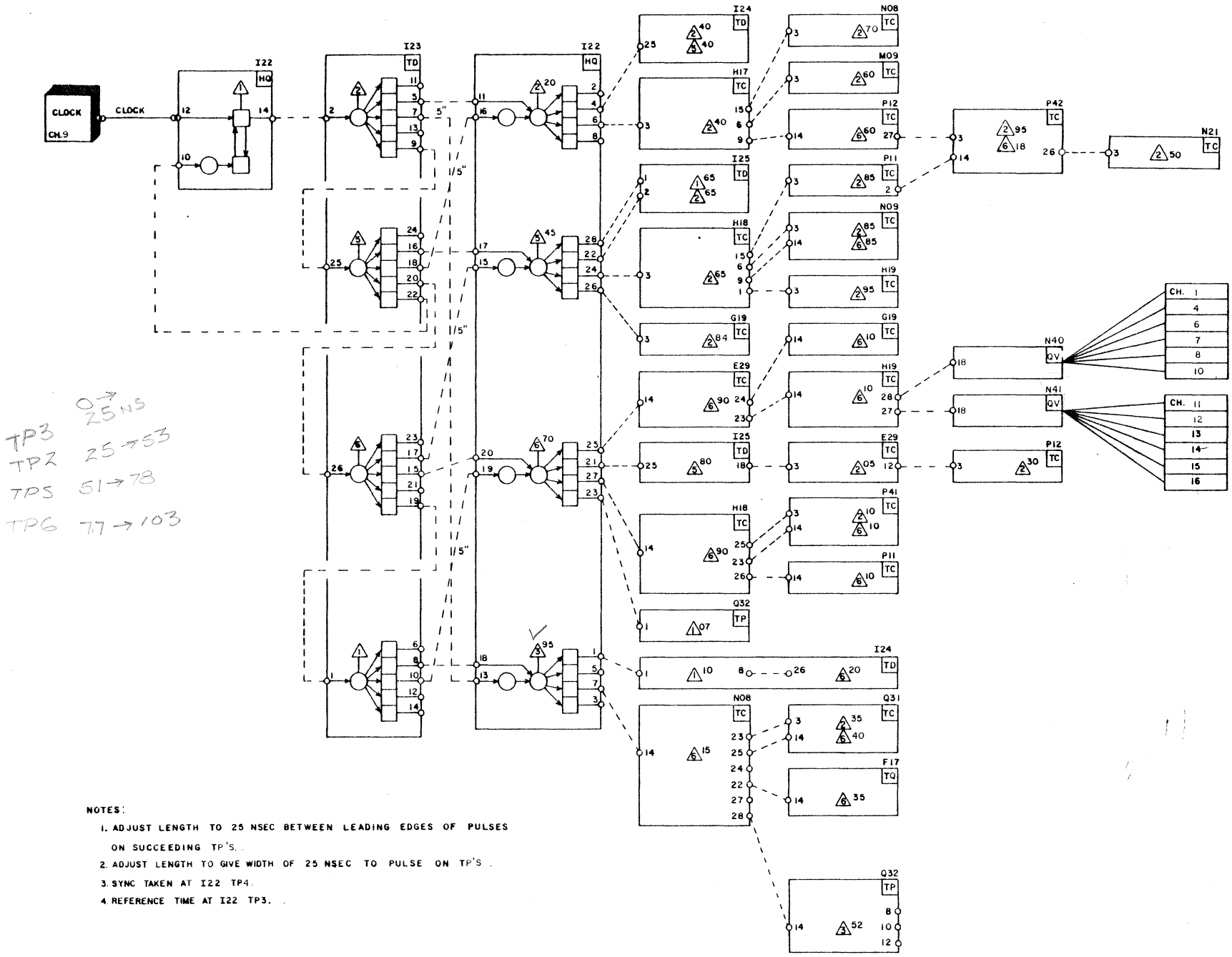
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE
CENTRAL PROCESSOR
CLOCK
CH 4

PRODUCT
6613-D, 6614-D

SIZE C | DRAWING NO. 60246600 | REV. e

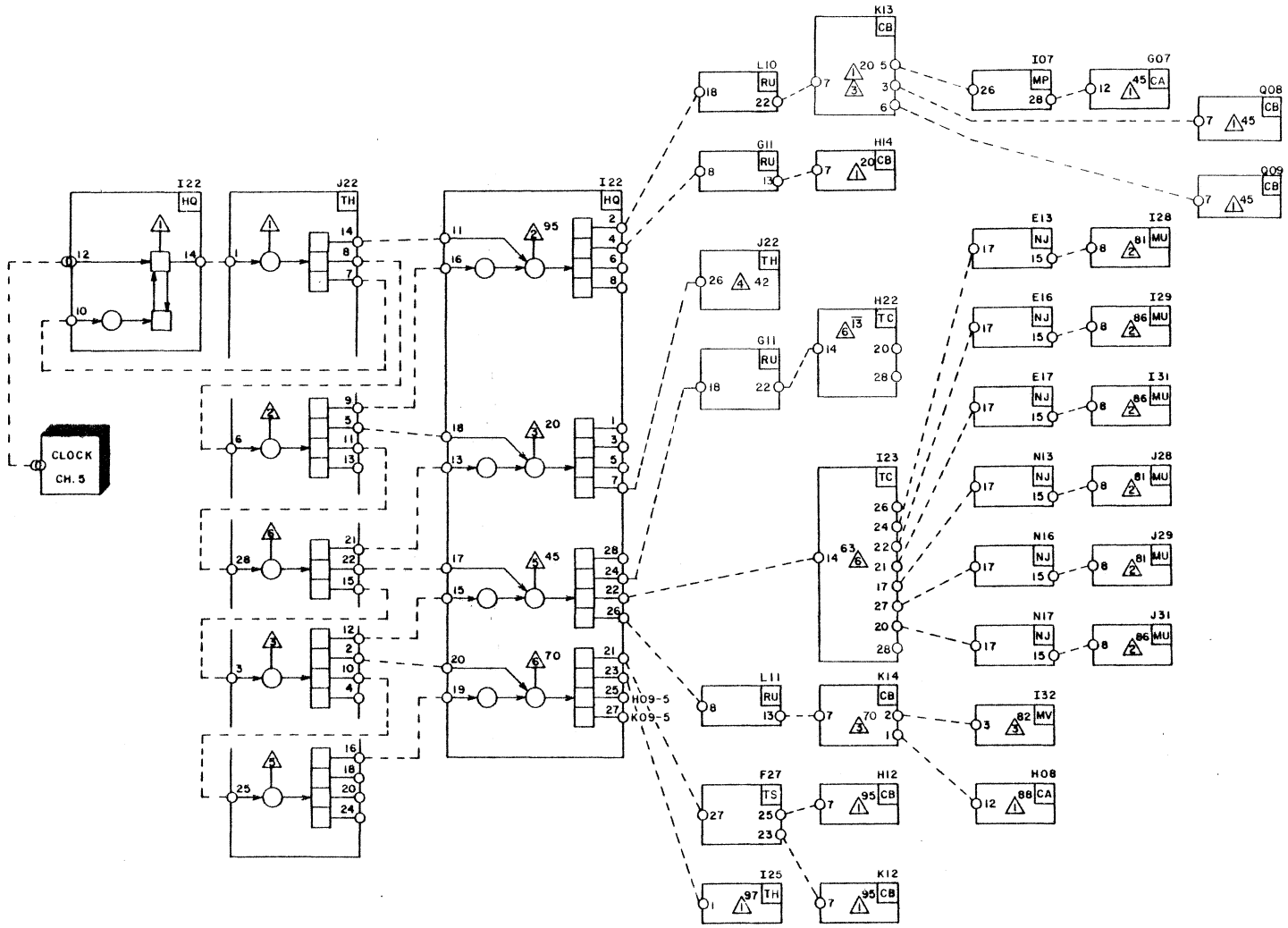
SHEET 117 | PAGE 3-5



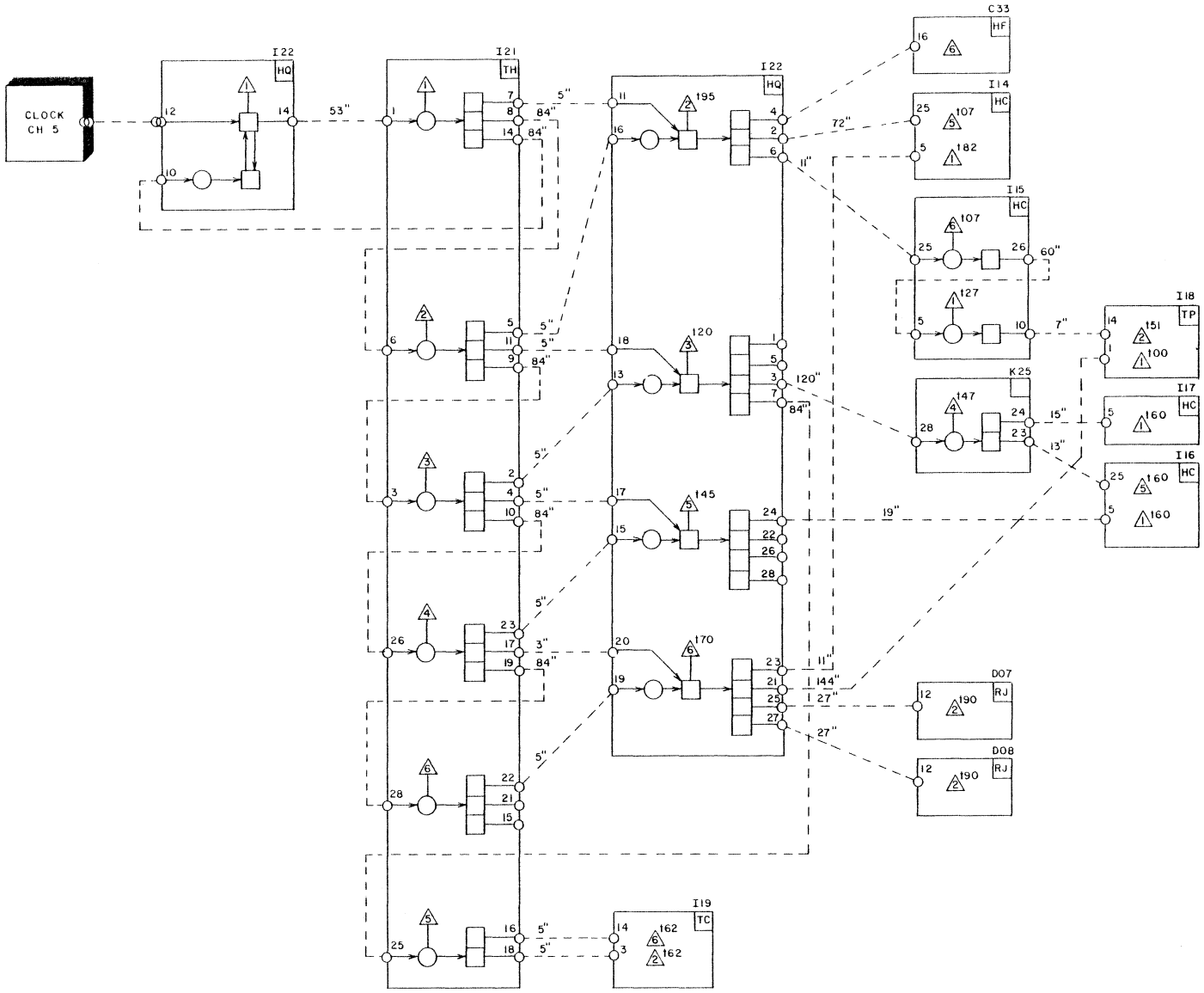
NOTES:

1. ADJUST LENGTH TO 25 NSEC BETWEEN LEADING EDGES OF PULSES ON SUCCEEDING TP'S.
2. ADJUST LENGTH TO GIVE WIDTH OF 25 NSEC TO PULSE ON TP'S.
3. SYNC TAKEN AT I22 TP4.
4. REFERENCE TIME AT I22 TP3.

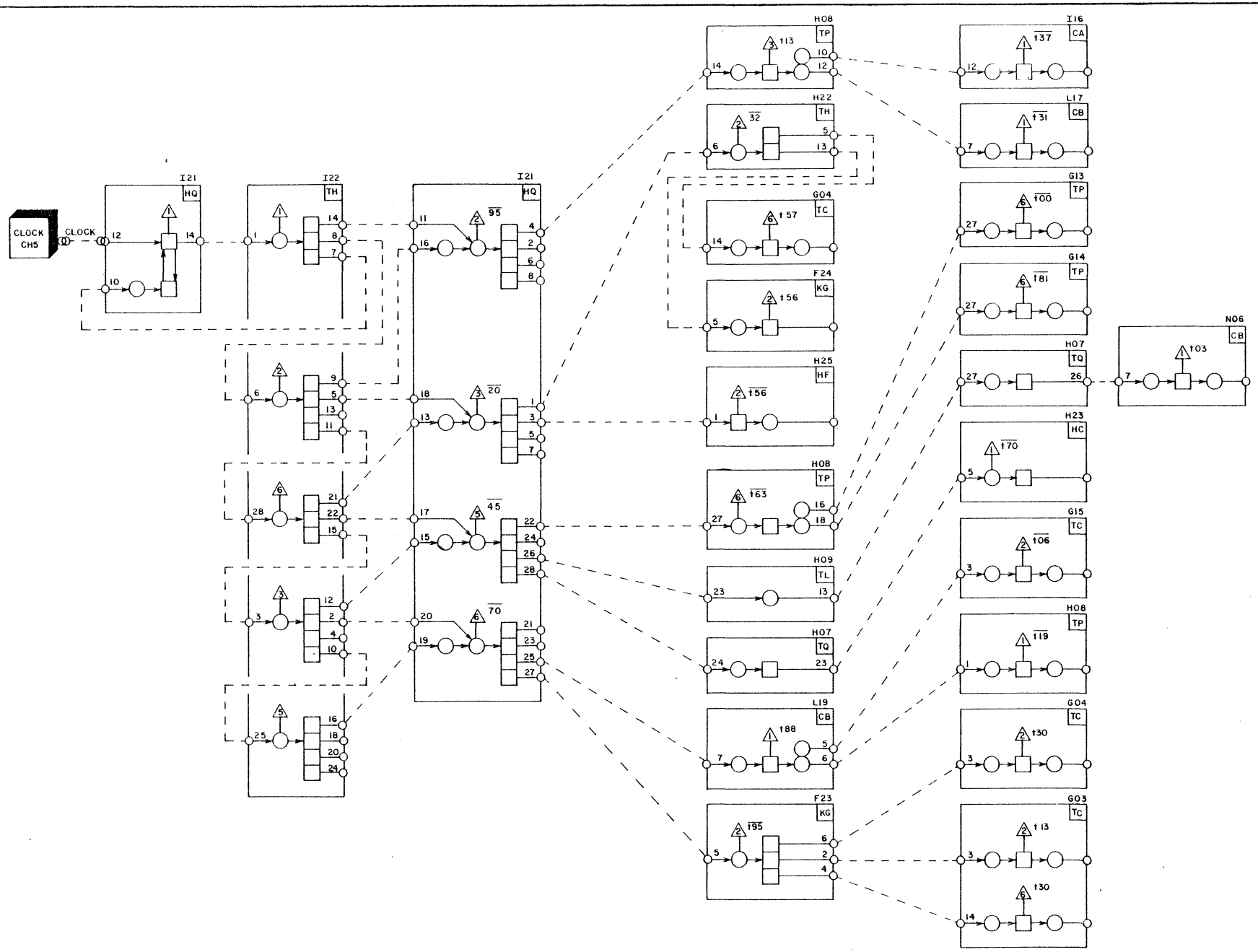
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL PROCESSOR CLOCK CH. 5	PRODUCT 6613-D, 6614-D	
		SIZE C	DRAWING NO 60246600 REV N
		SHEET 273	3-7



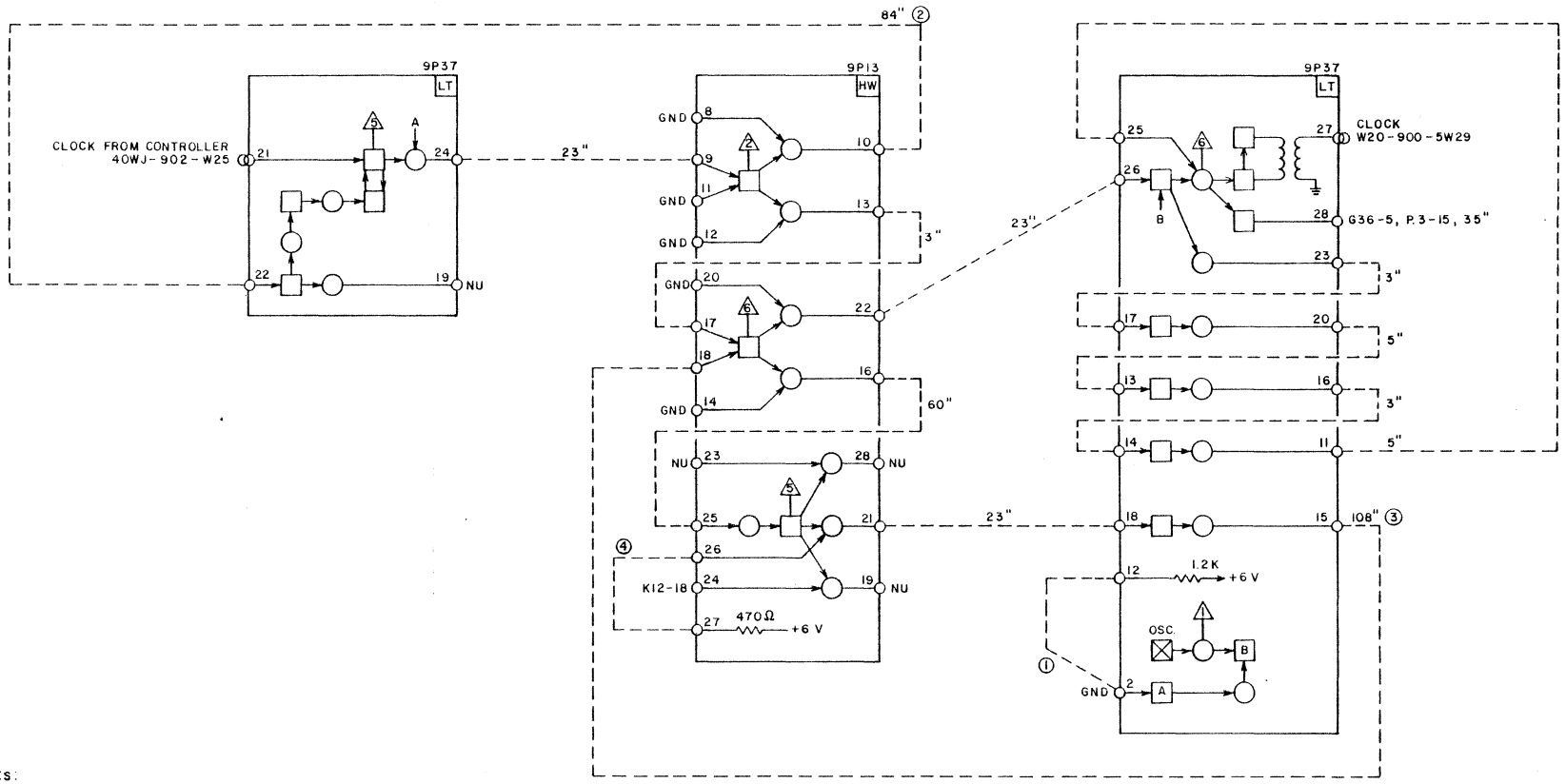
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE CENTRAL PROCESSOR CLOCK CH. 6	PRODUCT 6613-D, 6614-D	
		SIZE C	DRAWING NO. 60246600 REV N
		SHEET 121	PAGE 3-9



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL PROCESSOR CLOCK CH 7	PRODUCT 6613-D, 6614-D	
		SIZE C	DRAWING NO. 60246600 REV A
		SHEET	PAGE 3-11



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL PROCESSOR CLOCK CH 8	EQUIPMENT 6613-D, 6614-D	
		SIZE C	DRAWING NO. 60246600 REV. A
		SHEET 123	PAGE 3-13



NOTES:

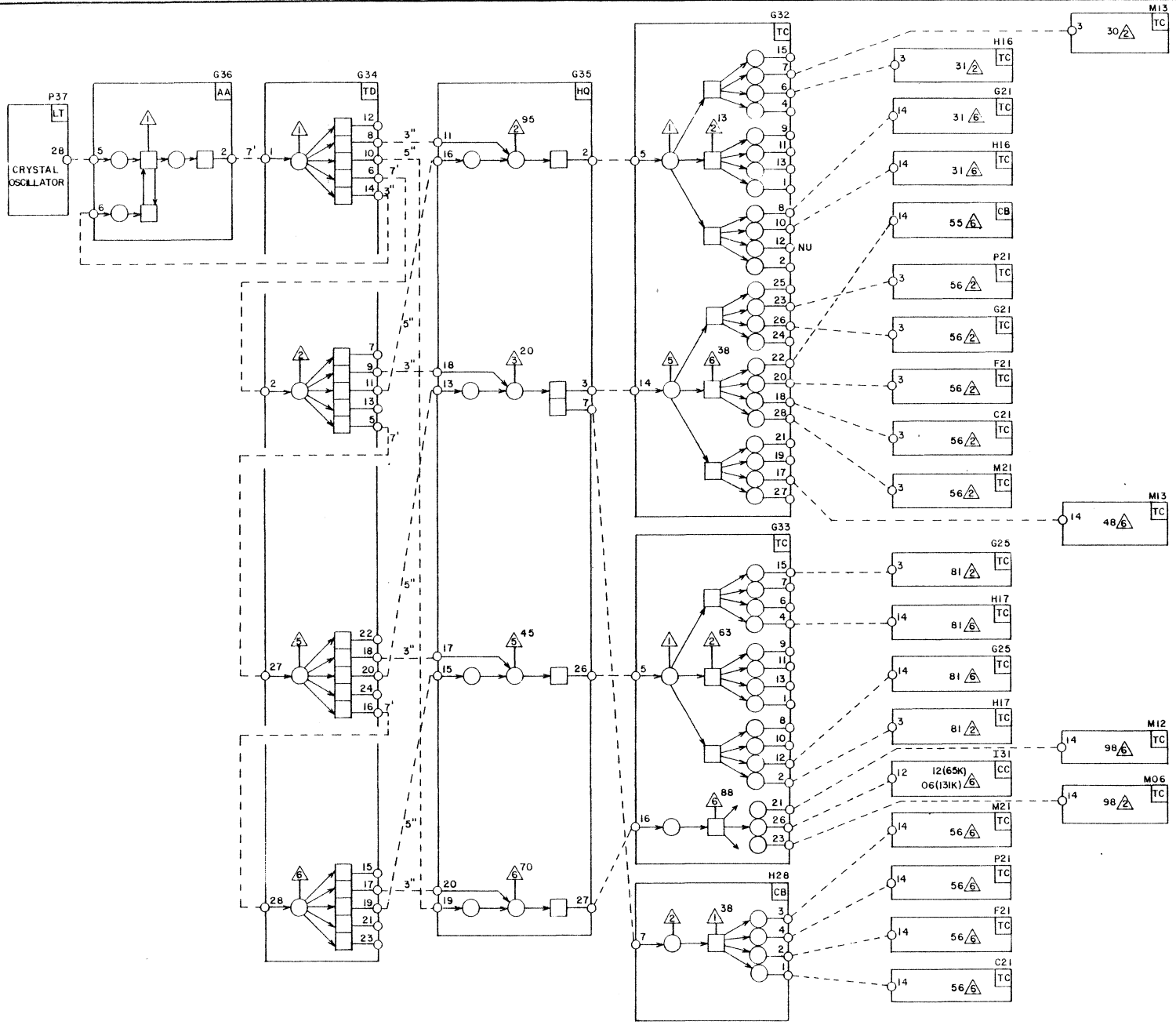
① P37-2 CONNECTED TO GROUND UNTIL ECS COUPLER ENABLE SUBASSEMBLY IS INSTALLED, THEN P37-2 IS CONNECTED TO P37-12.

② ADJUST FOR 55 NS AT P37 TP5

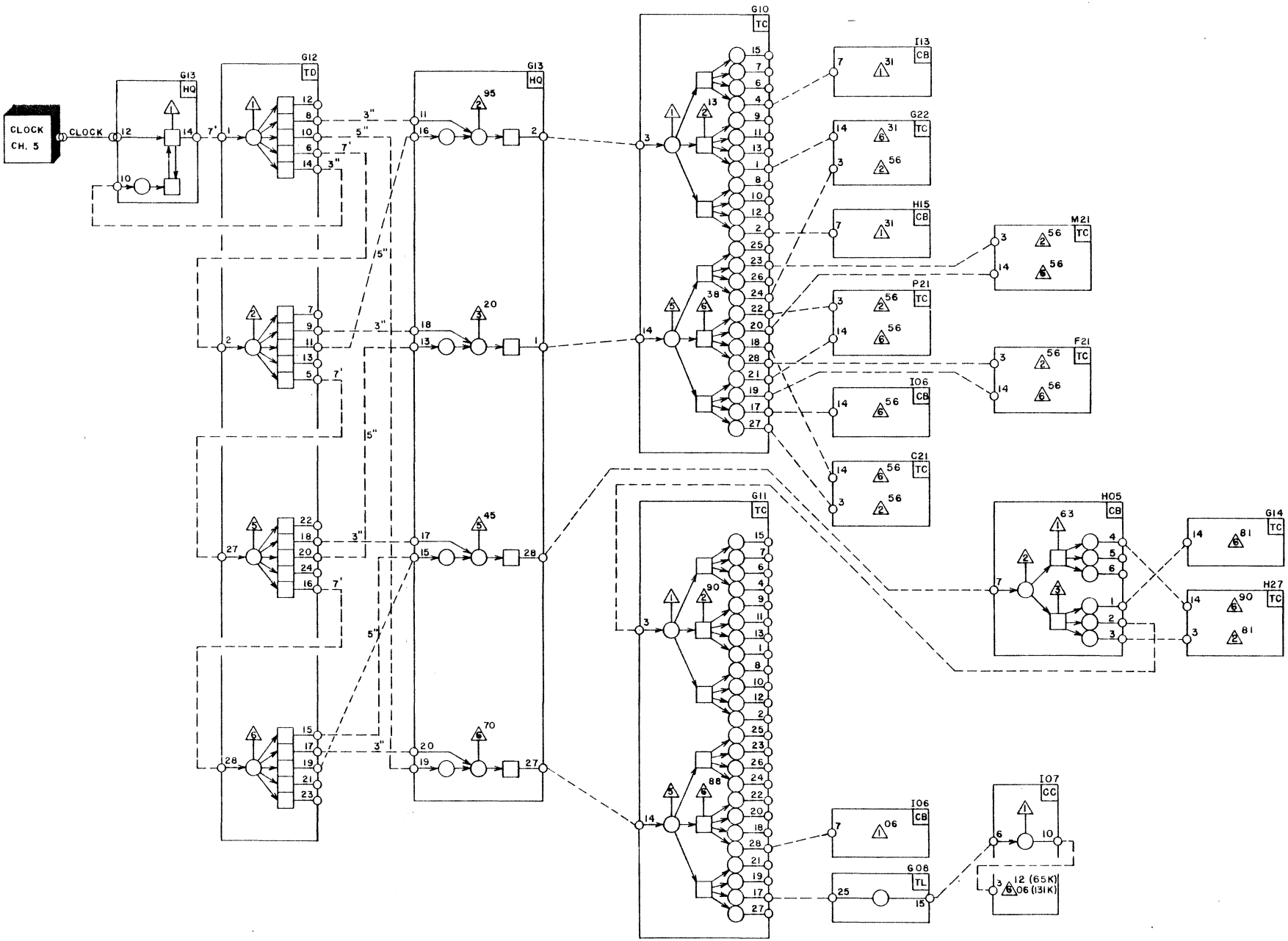
③ ADJUST FOR BACKUP CLOCK PERIOD SAME AS ECS CLOCK.

④ THIS WIRE ENABLES BACKUP CLOCK AND SHOULD BE REMOVED WHEN RUNNING WITH ECS.

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	10 MHZ CLOCK ECS COUPLER	CODE IDENT 34010	DWG NO 60246600	REV U
		SIZE C	SHEET	PAGE 3-13.1



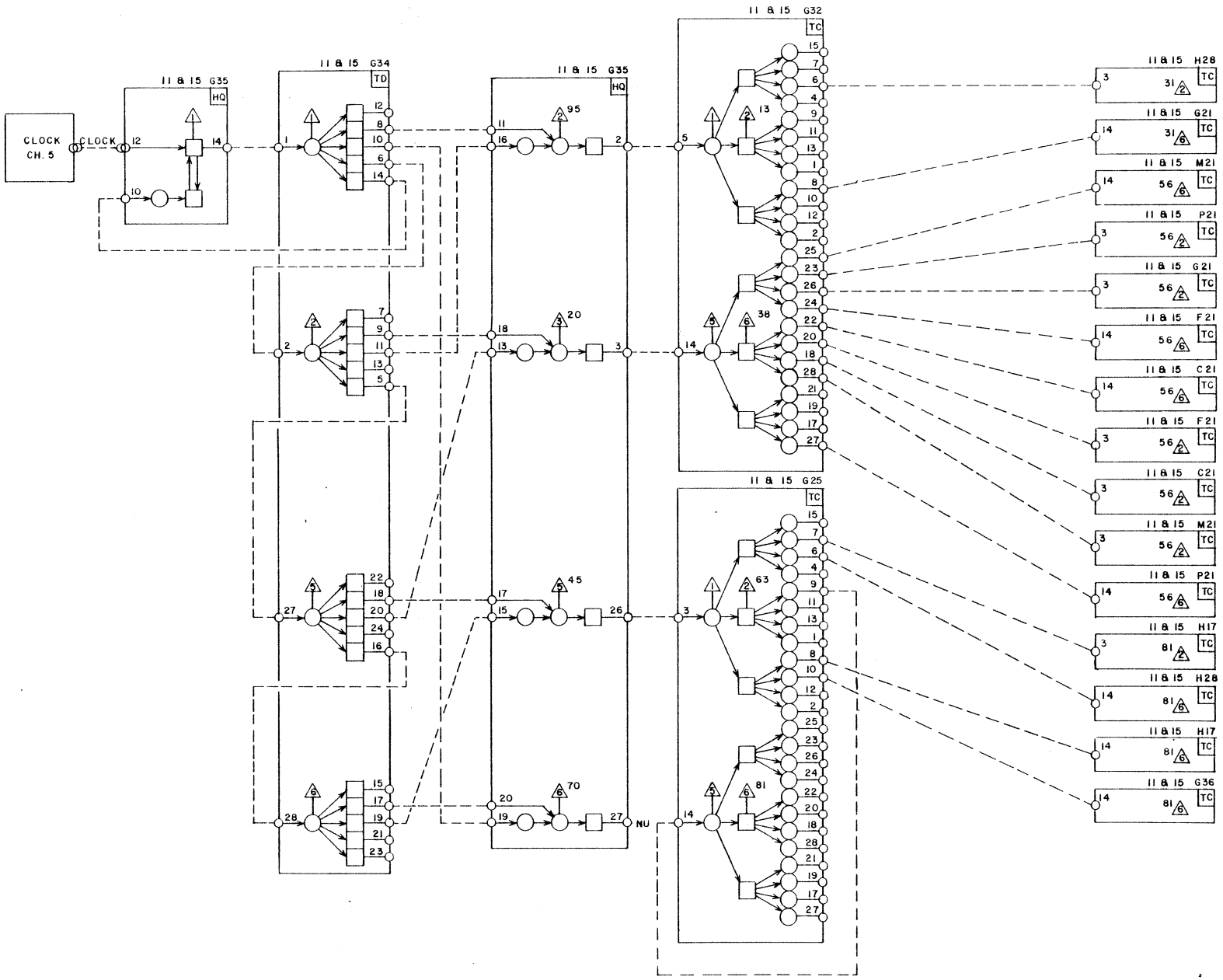
CONTROL DATA CORPORATION DEVELOPMENT DIVISION	CENTRAL MEMORY CLOCK CHASSIS 9	EQUIPMENT 6613-D, 6614-D	
		SIZE C	DRAWING NO 60246600
		REV M	
		SHEET 118	PAGE 3-15



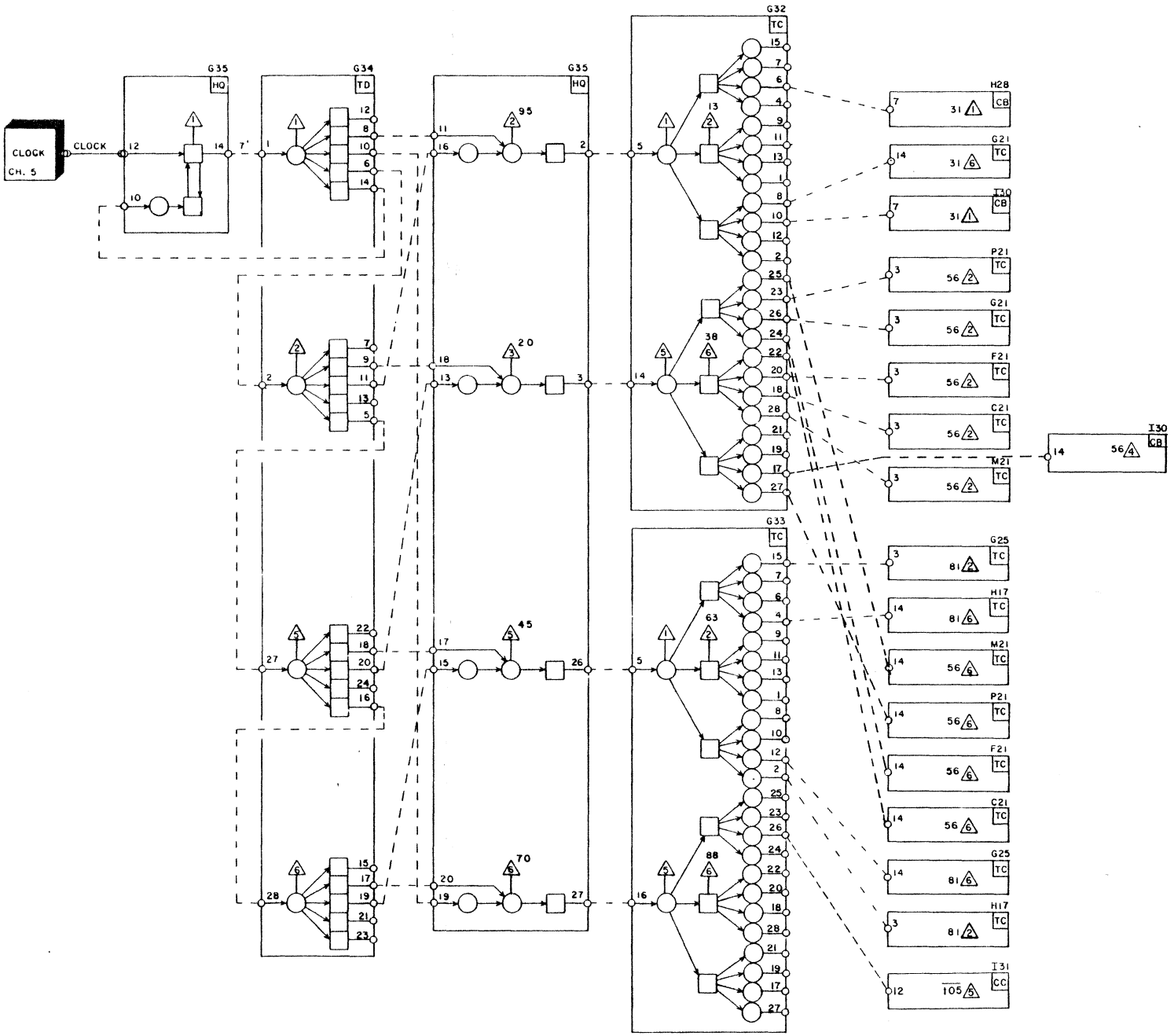
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

CENTRAL MEMORY CLOCK
CH. 10

EQUIPMENT 6613-D/6614-D
SIZE C | DRAWING NO 60246600 | REV K
SHEET | PAGE 3-17



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	CENTRAL MEMORY CLOCK CHASSIS 11 & 15	EQUIPMENT 6613-D, 6614-D SIZE C · DRAWING NO 60246600 · REV H SHEET · PAGE 3-19



CONTROL DATA CORPORATION

COMPUTER DIVISION

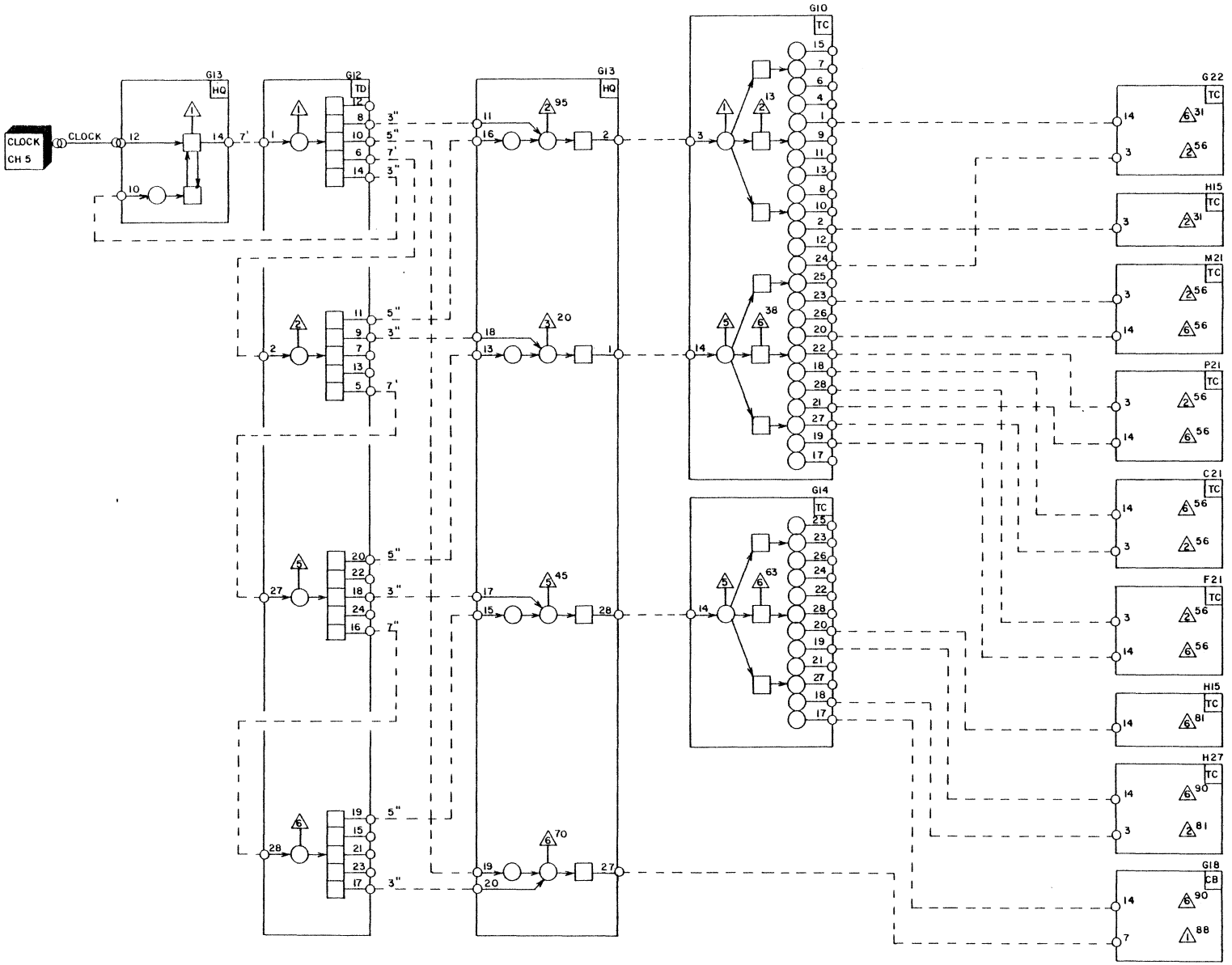
TITLE

CENTRAL MEMORY CLOCK
CH. 13

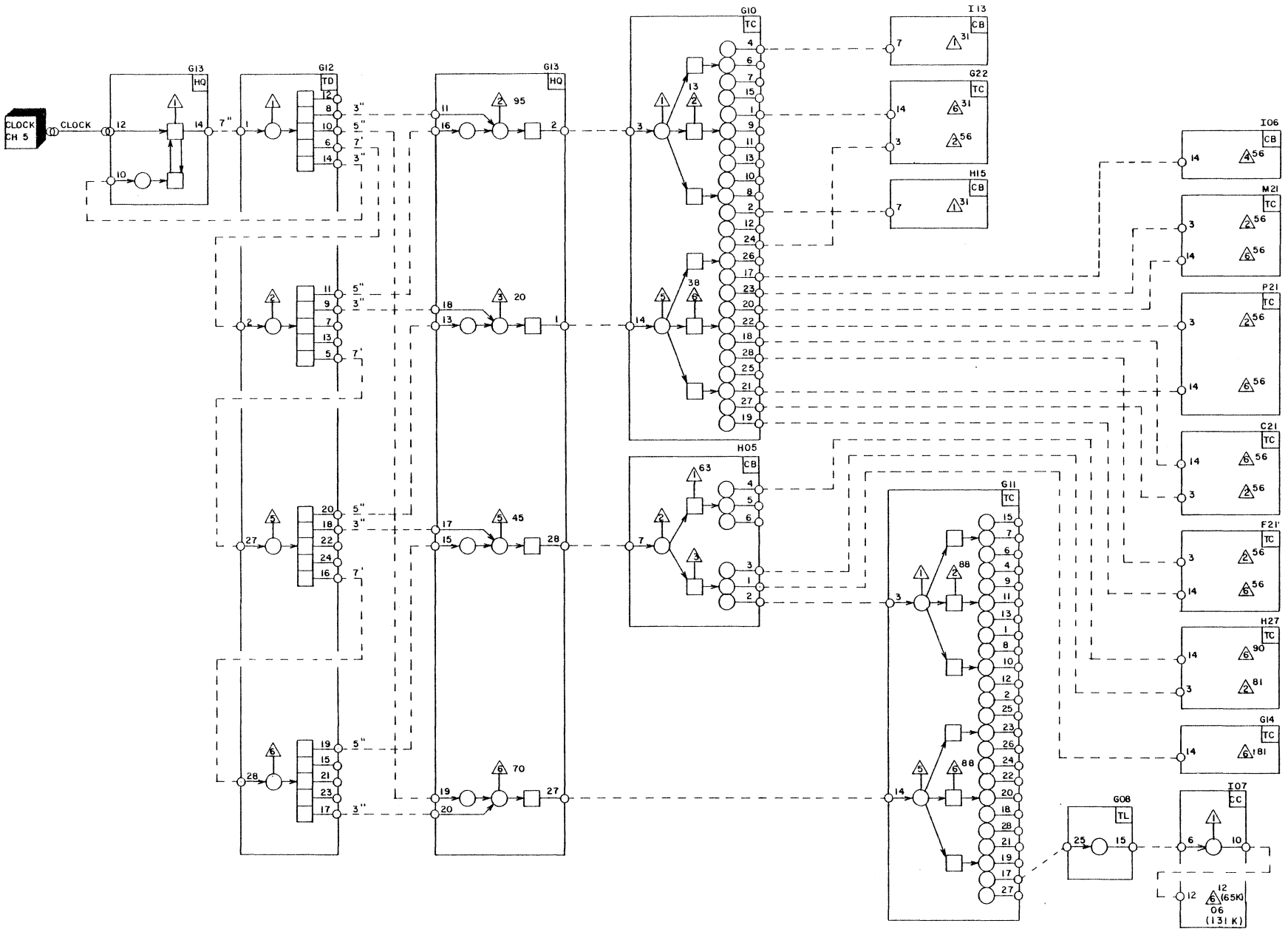
PRODUCT 6613-D

SIZE C | DRAWING NO. 60246600 | REV P

SHEET NO. 123



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL MEMORY CLOCK CH 12 AND 16	PRODUCT 6613-D	
		SIZE C	DRAWING NO. 60246600
		REV. A	
		SHEET	PAGE 3-21



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL MEMORY CLOCK CH 14	PRODUCT 6613-D	
		SIZE C	DRAWING NO. 60246600
		REV. P	
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PART 4

EXTENDED CORE STORAGE COUPLER

PART 4

ECS COUPLER

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18	WE	17, 19
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24	FA	23
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GENERAL DESCRIPTION

The ECS Coupler allows the CPU to communicate with ECS via the Controller. The coupler has two major functions. First, it computes the actual starting addresses in CM and ECS and checks to see if these addresses are out of range. This is the only error check made by the coupler. Second, it keeps count of the number of words transferred and terminates the transfer accordingly.

Most of the coupler's complexity arises from the fact that the programmer specifies initial addresses in CM and ECS and the number of 60-bit words to be transferred. However, ECS uses 8-word records and the coupler must automatically keep requesting new locations in ECS every eight words.

Coupler action can be interrupted by a PPU requesting CM. Action is started once the PPU read/write request is completed. Coupler action can also be interrupted if another computer is using ECS and the controller.

Coupler action is stopped if an Exchange Jump occurs. The transfer must be restarted at its beginning as intermediate values of word counts and addresses are not stored.

The coupler acts on an Abort or a Parity Error signal and relays them to CPU.

LOGICAL ELEMENTS

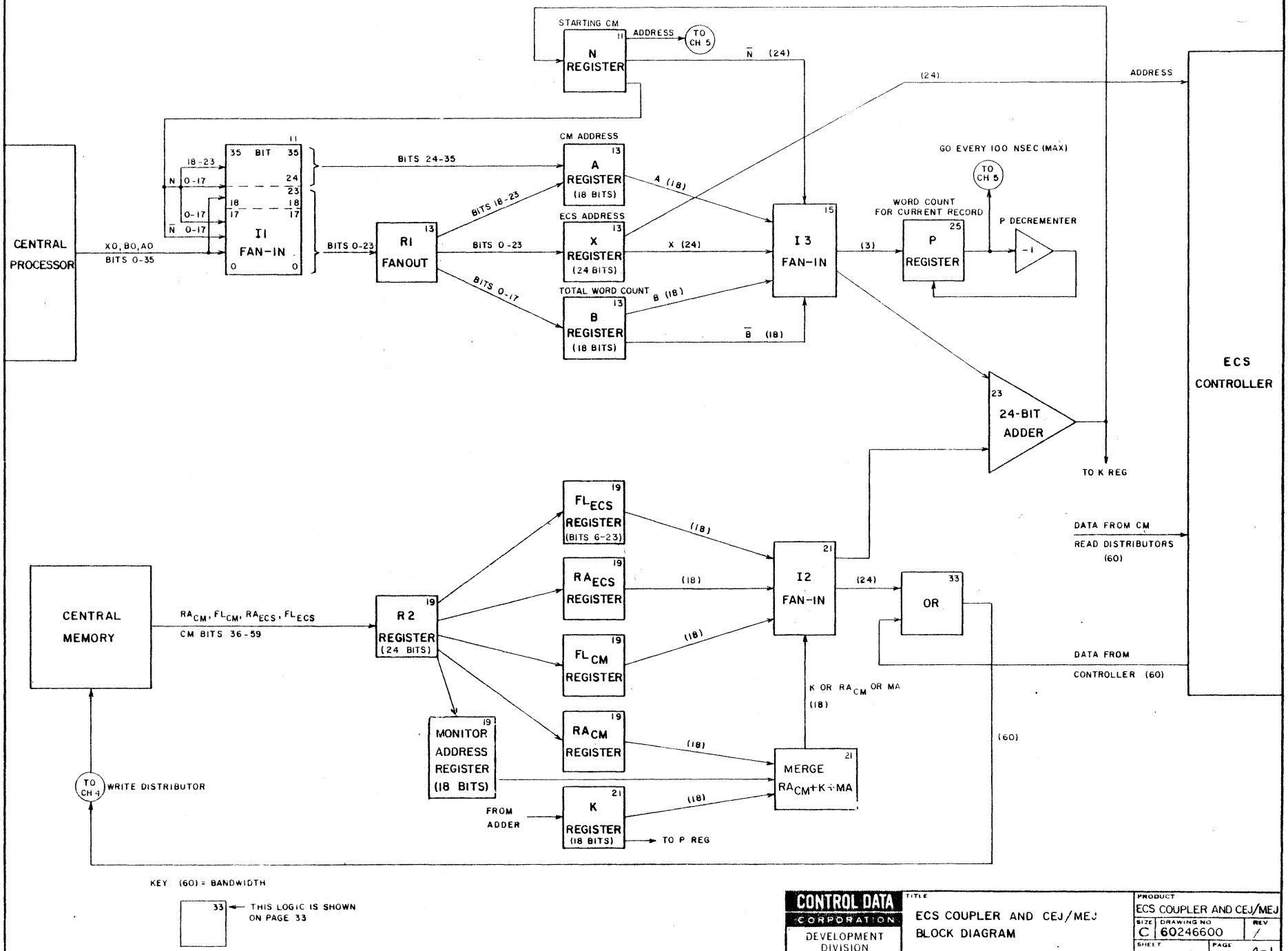
Four registers hold the values of Field Length for CM and ECS and the values of the Reference Address for CM and ECS. These values are not changed during a data transfer, and are restored, via the data paths, on an Exchange Jump.

The N and K registers are used for holding intermediate values generated during a transfer.

The adder is a 24-bit adder resembling 2 stages of the CPU Long Add unit.

P Register holds the 3-bit word count of the record in transfer. Its contents are decremented during a transfer.

The X, A and B Registers initially hold the same values as X_0, A_0 and B_0 respectively. X holds the ECS address and is incremented during a transfer; A holds the CM address and B the number of words left to transfer.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: ECS COUPLER AND CEJ/MEJ BLOCK DIAGRAM

PRODUCT: ECS COUPLER AND CEJ/MEJ
SIZE C | DRAWING NO 60246600 | REV /
SHEET | PAGE 4-1

SEQUENCE OF OPERATIONS

INTRODUCTION

Coupler operation is divided into three parts:

1. Transfer Setup.
   This portion is performed only at the beginning of a transfer and is not repeated.
2. Record Setup.
   This part of the operation is performed before each record transferred.
3. Data Transfers.
   If 524K of ECS are used, the data can be transferred at the rate of one word every 100 nsec. The coupler handles 8-word records and to sustain this rate, it must request a new record while the data transfer is in progress. That is, the Record Set-Up for the next record is performed at the same time as the data transfer. (See block transfers below.)

The coupler has a path for an address to CM (chassis 5). This path (and the coupler timing chain) is used by the CEJ/MEJ instructions (St. Opt. 10104).

TRANSFER SETUP

On any Exchange Jump, FL(ECS), FL(CM), RA(ECS), RA(CM) are sent from the package to the coupler.

When an ECS instruction is translated,

1. The timing chain is started.
2. The contents of X0 and A0 are sent to the coupler X and A registers. (These address relocation quantities must be stored prior to instruction execution.)
3. The Clear signal on B0 is dropped and the word count (Bj + K) is formed in the increment unit and sent to B0 which is sent in turn to coupler B register.

All required values are not stored in the coupler. Note that the values of FL(ECS), FL(CM), RA(ECS) and RA(CM) are not changed during an ECS transfer. They are restored to CM if an Exchange jump occurs.

4. The coupler then checks to see if the initial addresses are in bounds. If either CM or ECS Field Length errors occur, the transfer is terminated.
5. The first ECS address is computed, (X+RA(ECS), and stored in X. This absolute address will be updated after each record.

RECORD SETUP

FIRST RECORD

ECS reads/writes eight 60-bit words at once. This single record is disassembled/assembled in ECS under control the lowest 3 bits of the ECS address (see Definition Of Word Count Bits on diagram). These bits specify where in the record the operation should start. ECS always continues from the starting point to the end of record. If only word three is required, then the record at that address sends five words starting at word three. However, the word count is one, and this is entered in the P register. The single word is accepted and the transfer concluded even though ECS sends the remaining four words.

First record proceeds as follows:

1. The first record may be a partial record. Therefore, the lower 3 bits of X (60-bit word count bits) are subtracted from 10_8 to give the number of words to be transferred in this record. This result is sent to K.
2. K is checked against B. If K-B is negative, more than one record is to be transferred. K is sent to P as this number of words is the first record. (If K-B is positive, then this becomes the last record and B is sent to P (see Last Record).
3. B is reduced by K words.
4. The ECS address, Store bit and Request bit are sent to the controller.
5. The ECS address is incremented by K. This means that the lower 3 bits of X are clear and that the following records must be complete ones.
6. The Accept is received from the controller. The coupler waits until this occurs.
7. The Central Memory address, (A+RA(CM), is computed and stored in the A register. It is also sent to the Exchange Address Counter (EAK), where it is incremented by the P decrementer Go pulses.
8. The P decrementer is enabled and the data transfer is started.

SECOND RECORD

While the data is being transferred for the first record, the second Record Setup is starting the next ECS bank into its Read/Write cycle. The differences between the second record (or any intermediate record) and the first are:

1. Since they cannot be partial records, step 1 simply transfers 10_8 to K. Also the ECS address is incremented by 10_8.
2. Since the Exchange Address counter holds the CM address, a new address is not sent to CPU as in 7.

LAST RECORD

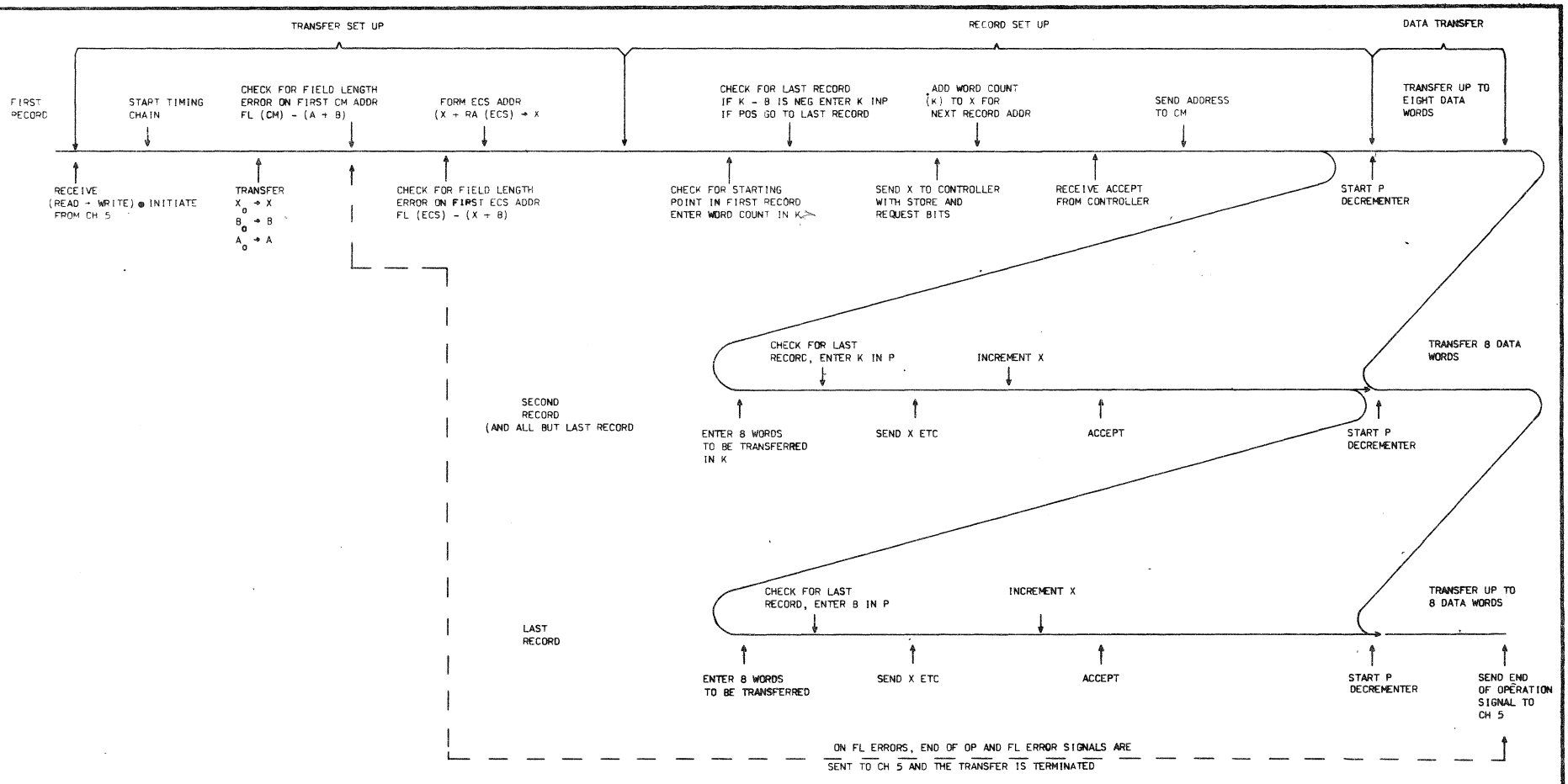
Any record may become a last record if the K-B test is positive. If so, B is sent to P register. Since B may be 0-7, the record can be a partial record but only in that it is terminated early (when B is less than 7). Note that a Last Record is different only in that the parameters for the record following are not generated and that an End of Operation signal is sent to CPU.

DATA TRANSFERS

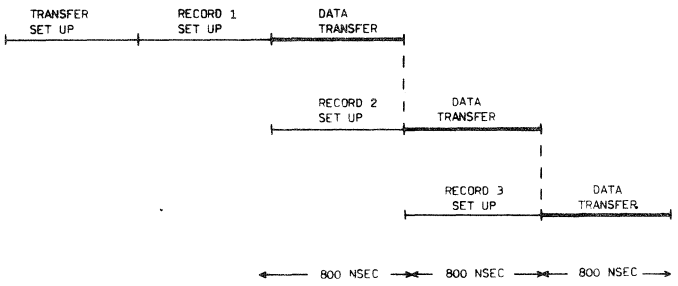
Note that data transfers must be continuous; that is, non-consecutive address are not possible in a block transfer. However, it is possible to reference a single word in ECS.

PPU INTERRUPT

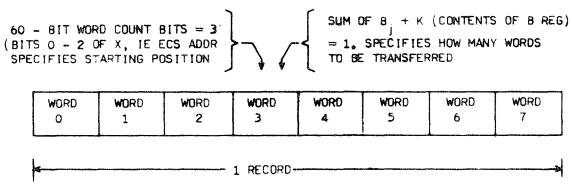
Provision is made for a PPU to perform a read or write or an exchange jump during an ECS transfer. The PPU interrupt can occur only between ECS records and only one interrupt per record is allowed.



SEQUENCE OF OPERATIONS



BLOCK TRANSFERS



DEFINITION OF WORD COUNT BITS

CONTROL DATA DEVELOPMENT DIVISION	TITLE: SEQUENCE OF OPERATION ECS COUPLER	PRODUCT: ECS COUPLER AND CEJ/MEJ			
		SIZE: C	DRAWING NO.: 6024660C	REV.: A	
		SHEET	PAGE: 43		

TIMING CHAIN DESCRIPTION

Each FF in the timing chain is set for 100 nsec, but there is only a 50 nsec delay between the setting of consecutive FF's. The timing chain runs for 2.4 μsec minimum and controls most of the Coupler's operations. T01 to T26 of the timing chain are used for Normal Transfer Setup, Flag Function and CEJ sequences. T27 to T42 of the timing chain are used for Normal Transfer completion, Next Record Setup sequence and PPU Break-in operations. Note that all adder results go unconditionally to N, which is cleared every 100 nsec.

TRANSFER SETUP

The Initiate, Read (or Write) FF's are set. Read/Write FF is set. Timing chain is started at T00.

T01 (NORMAL TRANSFER) Enable Pass on; Enable X0, B0, A0 to X, B and A registers.

T02 (NORMAL TRANSFER) Clear K register; force "0" into B.

T03 (NORMAL TRANSFER) Enter X0 in X via I1.

T05/T06 (NORMAL TRANSFER) Enter A0 and B0 into A and B via I1.

T07 (NORMAL TRANSFER) Continue timing chain.
(CEJ/MEJ) Enable END of operation.
(FLAG FUNCTION) Clear Flag Function FF.

T08 (NORMAL TRANSFER) Enable B (word count) to I3 and to the adder.
(CEJ/MEJ) Enable Monitor address to the adder.

T09 (NORMAL TRANSFER) Continue timing chain.
(FLAG FUNCTION) Enable Flag Function FF.

T10 (NORMAL TRANSFER) Enter adder results in K. This is the transmission of B to K in preparation for FL checks.
(CEJ/MEJ) Enable Monitor Flag; Exchange Go to CH 5 if CEJ.

T11 (NORMAL TRANSFER) Clear Word Count $\leq$ 8 FF.

T12 (NORMAL TRANSFER) Send A via I3 and K to the adder.
(FLAG FUNCTION) Enable address to ECS Controller for Flag Function.

T13 (NORMAL TRANSFER) Enable B to the adder.
(CEJ/MEJ) Clear Block Flag Function FF.

T14 (NORMAL TRANSFER) Extend Sign.

T16 (NORMAL TRANSFER) Perform FL check, (FL (cm) (A + B), by sending N, (A + K) and FL (cm) to the adder; results to N. If FL error send error signal (T20).

T18 (NORMAL TRANSFER) Send X and K to the adder, result to N.
(FLAG FUNCTION) Send End of operation.

T20 (NORMAL TRANSFER) Send FL error signal if N register is negative (Bit 23 set).

T21 (NORMAL TRANSFER) Clear K register.

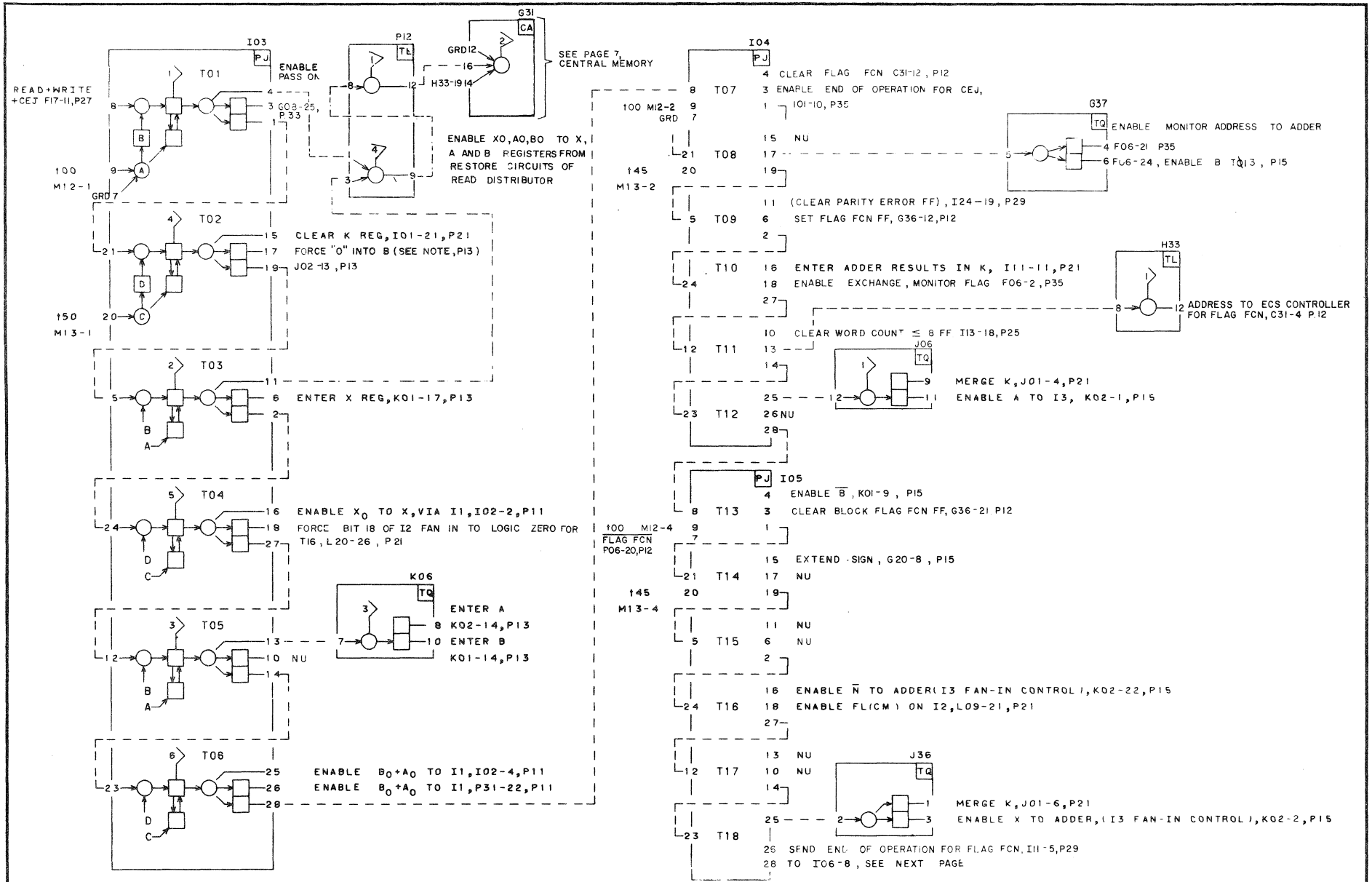
T22 (NORMAL TRANSFER) Perform FL check (FL (ECS) - (X + B) by sending X + B, and + FL (ECS) to adder; results to N register. If error send error signal at T25.

T23 (NORMAL TRANSFER) Set First FF.

T24 (NORMAL TRANSFER) Perform X + RA (ECS); result to N register.

T25 (NORMAL TRANSFER) Send FL error signal, if N register is negative.

T26 (NORMAL TRANSFER) For first record only, send X and RA (cm) to the adder. Enable E term.



CONTROL DATA	TITLE	PRODUCT	
DEVELOPMENT DIVISION	TIMING CHAIN T01-T18	ECS COUPLER AND CEJ/MEJ	
		SIZE C	DRAWING NO. 60246600
		REV. Y	
		SHEET	PAGE 4-5

END OF TRANSFER SETUP

START RECORD SETUP

If this were and intermediate record, the Record Setup would begin for the next record, the Read 2 or Write 2 FF's would be cleared and the timing chain would not be restarted.

PPU BREAK IN

If a PPU interrupts between records the timing chain continues from T27 to T40. At T30 the address to controller X register is blocked and no Accept will be received at T41 to continue the timing chain.

T27 (NORMAL TRANSFER) Set Clear K FF.

T28 (NORMAL TRANSFER) Set K = 10_8; mask all bits of I3 Fan-in (extend sign) except bits 0-2. Send K and N to the adder. X and N both contain the actual ECS address, from N we have: 7← 7x (note that the 7's are masks and the X is the complement of the 60 Bit Word Count); from K we have: 0 ← 010 Results from the adder; 0 ← 0X + 1 (end around carry) extend in K. Since the lower 3 bits of X may possibly be zero (partial record) the Coupler must determine what to enter in P. (First record only)

(PPU BREAK IN) PPU Break-in is the same as a Normal Operation except that set K = 10_8 is blocked by a cleared condition being held on the K Reg, K is held clear to avoid the loss of the word count for the interrupt record.

T29 (NORMAL TRANSFER) Clear K. Enter A (if this record is not the first) with A + 10_8 (see T42). If this is the first record, send N (cm address) to A (see T26) Send Addr. to controller (x Register)

(PPU BREAK-IN) Clear K. Enter A with A + 0. A is added to 0 on a PPU Break-in because set K = 10_8 was disabled at T28. A in this case holds the CM address for the interrupted record and must not be incremented by 10_8. Addr. to controller (x Reg) is blocked, but Timing Chain continues

T30 (NORMAL TRANSFER) Enter adder results (T28) in K. This is the number of words to be transferred for this record.

(PPU BREAK IN) Enter adder results in K. This is the result of the A + 0 addition (T28).

T31 (NORMAL TRANSFER) Enable B to the adder. This will initiate the check to determine if this is last record and if so, how many words will be transferred. This is done by subtracting the Word Count (B_j + K), now in B, from K (T32).

T32 (NORMAL TRANSFER) B and K to adder; force "1" into bits 18-23 of adder input to make B negative.

T34 (NORMAL TRANSFER) K and X to the adder. This is updating the ECS address by the number of 60 bit words for this record. Note that for the first pass this made any address have its lower 3 bits all zeros. There after, any record will to started at word 0. If this is any record but the first, 10_8 is added to X and the ECS record address is incremented by 1. Also, if this is any record other than the first, 10_8 is added to X, and the ECS record address is incremented by 1.

T35 (Enter N into B register via I1. This is the result of K - B, complemented. If N is negative, B was larger than K and this is not last record, K is entered in P at T38. If N is positive, the Word Count $\leq$ 8 FF is set and B is entered in P at T37.

T36 (NORMAL TRANSFER) Send A to the adder. N will send A to CM (T38)

T37 (NORMAL TRANSFER) Send B to P if last record. Enable N to the VIA I1.

T38 (NORMAL TRANSFER) Enter N in X. From I this is the result of the K and X addition at T34 and is the ECS address fro the next record. Enable N to CM. Enable K to P.

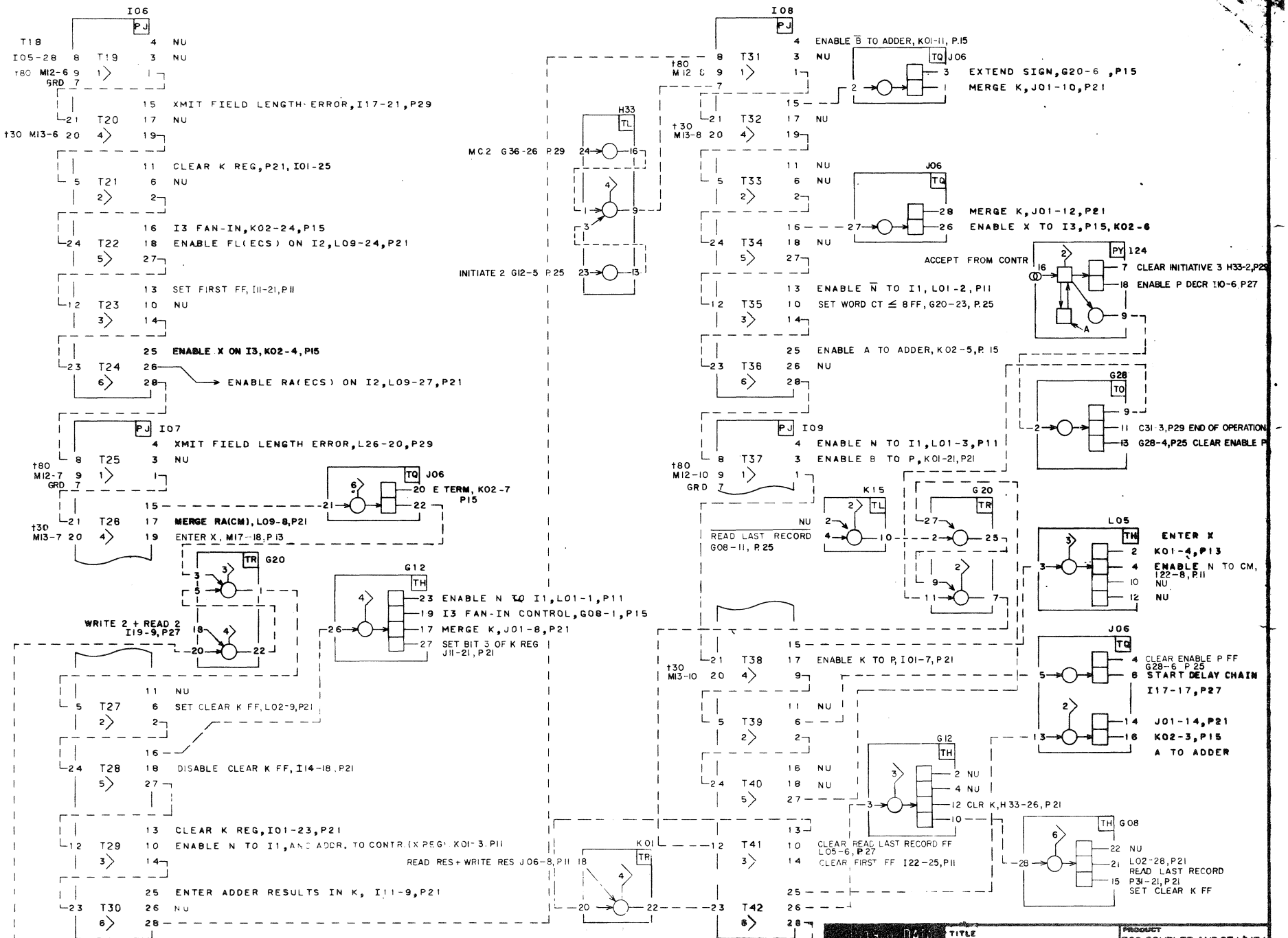
T39 (NORMAL TRANSFER) Start the delay chain if this is a read operation; this is to delay the start of the decrementer long enough to get the data back from ECS. Clear ENABLE P FF.

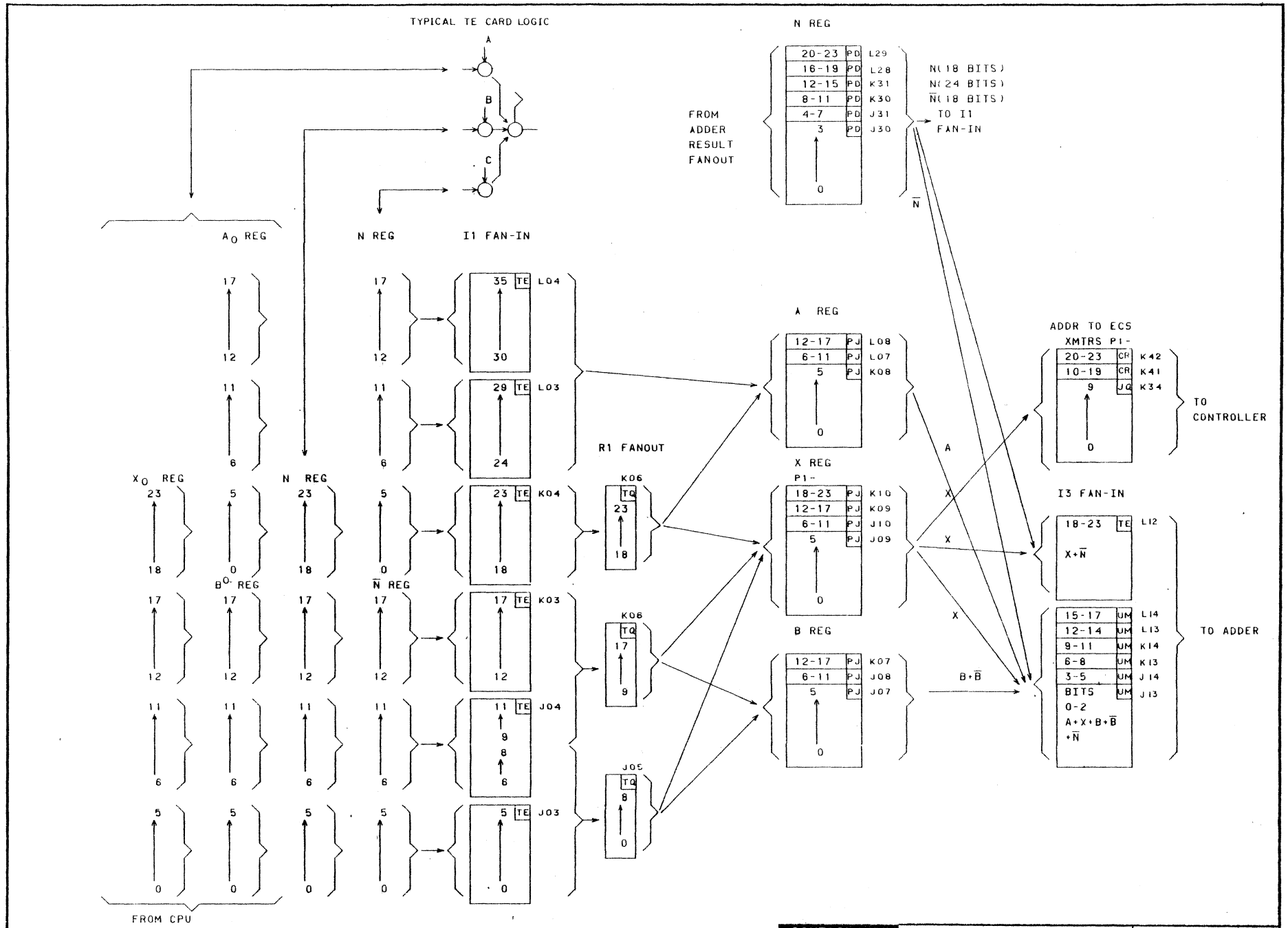
T41 (NORMAL TRANSFER) An Accept from the Controller sets T41 FF and enables the P decrementer. T41 clears Read Last Record FF and clears FIRST FF. If last record (Read Last Record FF is set) this FF blocks the timing chain and prevents the requesting of any further records.

(PPU BREAK-IN) The Accept from the controller to T41 is blocked at T30 when Address to Controller (X Reg) was disabled by the PPU Break-In. The timing chain hangs at T40 until a Read or Write Resume signal sets T42 FF.

T42 (NORMAL TRANSFER) Set FF. Send A and K to the adder. This up dates the CM address by 10_8. This new address is entered in at T29. It is not sent to CM each record but is available if needed; that is, after a PPU interrupts the transfer. Enable No Interrupt FF to clear K. Enable Read Last Record FF. Set T27 FF which starts a new Record Setup sequence. Note that T27 FF is set 25 nsec after T42 and T28 FF is set 75 nsec after T42. Therefore, T42 at 75 is the same as T28 at T00. This overlap ensure that K = 10_8 and A are sent to the adder at the same time.

(PPU BREAK-IN) Set by Read or Write Resume signal. Send A and K to the adder. A is holding the CM address for the interrupted record and K is clear. Therefore we are adding A to 0 to re-establish the interrupt record. T27 FF is set and a new record sequence is set up.


I06
PJ
T18
I05-28 8 T19 3 NU
t80 MI2-6 9 1
GRD 7
15 XMIT FIELD LENGTH ERROR, I17-21, P29
21 T20 17 NU
t30 MI3-6 20 4 19
11 CLEAR K REG, P21, I01-25
5 T21 6 NU
2 2
16 I3 FAN-IN, K02-24, P15
24 T22 18 ENABLE FL(ECS) ON I2, L09-24, P21
5 27
13 SET FIRST FF, I11-21, P11
12 T23 10 NU
3 14
25 ENABLE X ON I3, K02-4, P15
23 T24 26 ENABLE RA(ECS) ON I2, L09-27, P21
6 28
PJ I07
4 XMIT FIELD LENGTH ERROR, L26-20, P29
8 T25 3 NU
t80 MI2-7 9 1
GRD 7
TQ J06
20 E TERM, K02-7 P15
15
21 T26 17 MERGE RA(CM), L09-8, P21
t30 MI3-7 20 4 19 ENTER X, MI7-18, P13
TR G20
WRITE 2 + READ 2 I19-9, P27
G12
TH
23 ENABLE N TO I1, L01-1, P11
19 I3 FAN-IN CONTROL, G08-1, P15
17 MERGE K, J01-8, P21
27 SET BIT 3 OF K REG J11-21, P21
11 NU
5 T27 6 SET CLEAR K FF, L02-9, P21
2 2
16
24 T28 18 DISABLE CLEAR K FF, I14-18, P21
5 27
13 CLEAR K REG, I01-23, P21
12 T29 10 ENABLE N TO I1, AND ADDR. TO CONTR. (X REG) K01-3, P11
3 14
READ RES + WRITE RES J06-8, P11
25 ENTER ADDER RESULTS IN K, I11-9, P21
23 T30 26 NU
6 28
K01
TR
I08
PJ
4 ENABLE B̄ TO ADDER, K01-11, P15
t80 M12 8 9 1 8 T31 3 NU
TQ J06
3 EXTEND SIGN, G20-6, P15
2 1 MERGE K, J01-10, P21
15
21 T32 17 NU
t30 M13-8 20 4 19
H33
TL
MC2 G36-26 P29
INITIATE 2 G12-5 P25
11 NU
5 T33 6 NU
2 2
J06
TQ
28 MERGE K, J01-12, P21
16 27 26 ENABLE X TO I3, P15, K02-6
24 T34 18 NU
5 27
13 ENABLE N̄ TO I1, L01-2, P11
12 T35 10 SET WORD CT ≤ 8 FF, G20-23, P25
3 14
25 ENABLE A TO ADDER, K02-5, P15
23 T36 26 NU
6 28
PJ I09
4 ENABLE N TO I1, L01-3, P11
8 T37 3 ENABLE B TO P, K01-21, P21
t80 MI2-10 9 1
GRD 7
NU
READ LAST RECORD G08-11, P25
K15
TL
G20
TR
PY 124
ACCEPT FROM CONTR
7 CLEAR INITIATIVE 3 H33-2, P29
18 ENABLE P DECR I10-6, P27
G28
TO
11 C3I-3, P29 END OF OPERATION
13 G28-4, P25 CLEAR ENABLE P
L05
TH
ENTER X
2 K01-4, P13
4 ENABLE N TO CM, I22-8, P11
10 NU
12 NU
J06
TQ
4 CLEAR ENABLE P FF G28-6, P25
6 START DELAY CHAIN I17-17, P27
14 J01-14, P21
16 K02-3, P15
A TO ADDER
15
21 T38 17 ENABLE K TO P, I01-7, P21
t30 MI3-10 20 4 9
11 NU
5 T39 6
2 2
G12
TH
16 NU
24 T40 18 NU
5 27
2 NU
4 NU
12 CLR K, H33-26, P21
10
13
12 T41 10 CLEAR READ LAST RECORD FF L05-6, P27
3 14 CLEAR FIRST FF I22-25, P11
25
23 T42 26
6 28
TH G08
22 NU
21 L02-28, P21 READ LAST RECORD
15 P31-21, P21 SET CLEAR K FF
DEVELOPMENT DIVISION
TITLE
TIMING CHAIN
T19 - T42
PRODUCT
ECS COUPLER AND CEJ/MEJ
SIZE C
DRAWING NO. 60246600
REV. Y
SHEET
PAGE 4-7



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

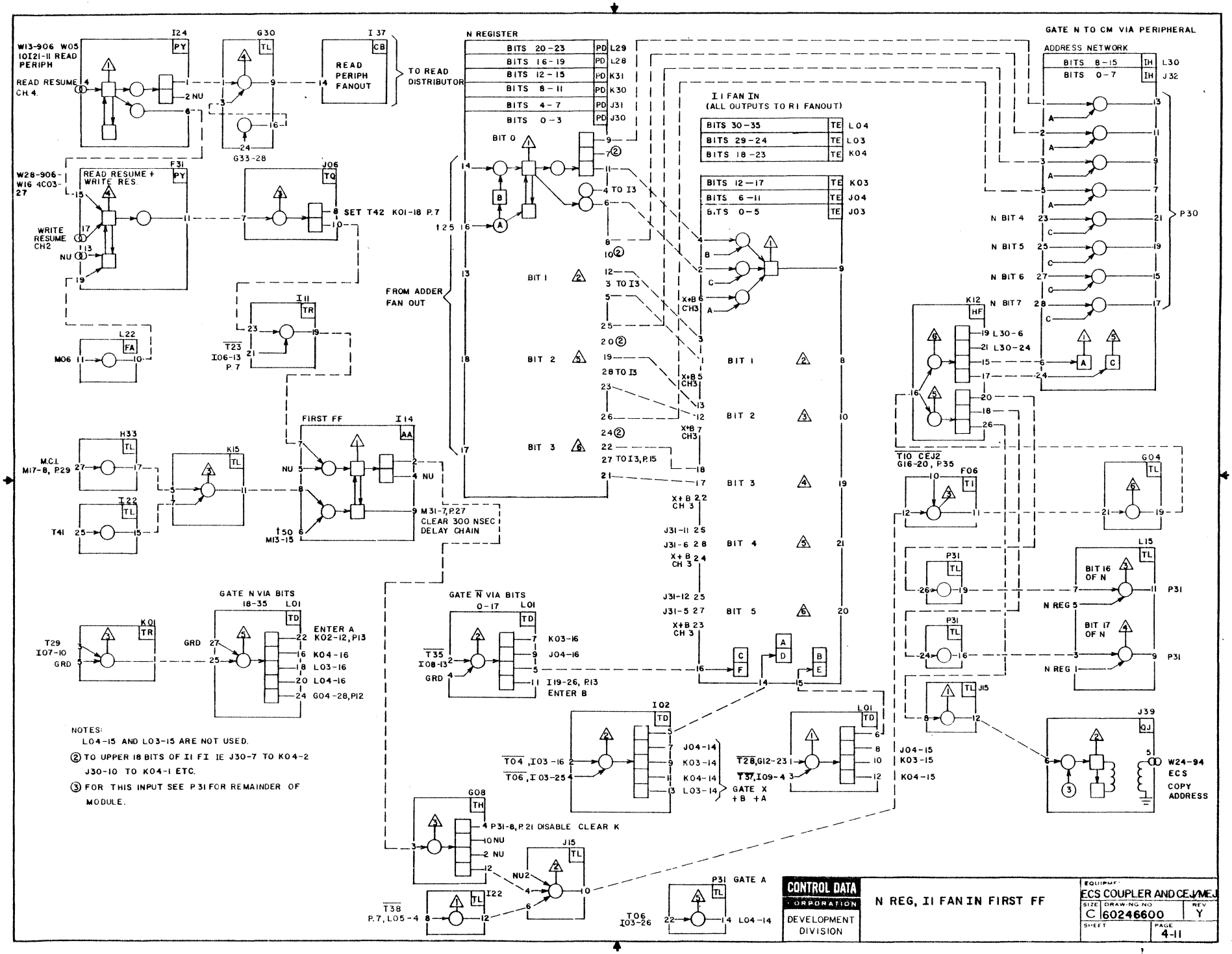
TITLE
DATA FLOW I
II AND I3 FAN-INS
RI FANOUTS
X,A,B, AND N REGS

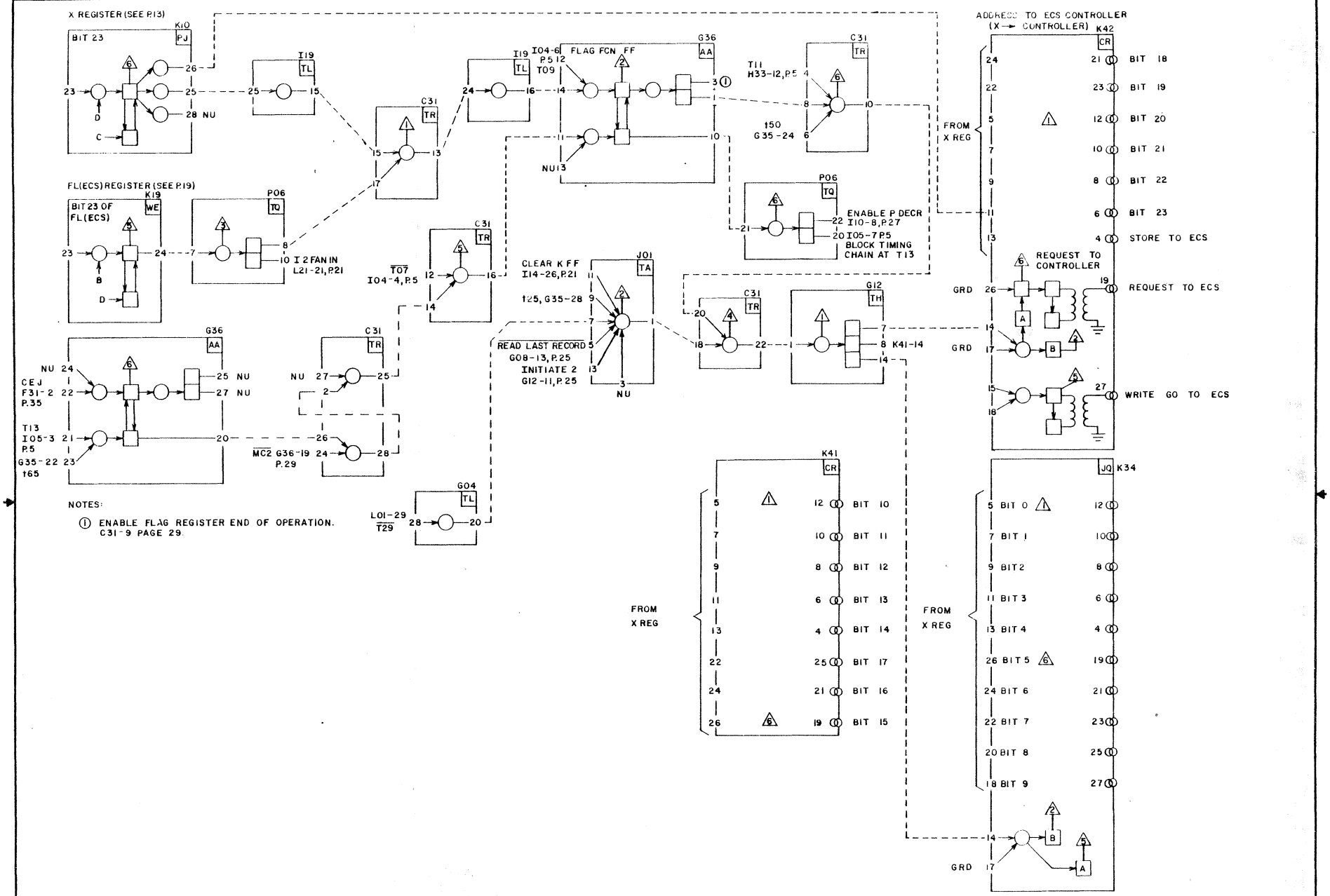
PRODUCT
ECS COUPLER AND CEJ/MEJ

SIZE	DRAWING NO.	REV.
C	60246600	

SHEET

PAGE 49


N REGISTER
BITS 20-23 PD L29
BITS 16-19 PD L28
BITS 12-15 PD K31
BITS 8-11 PD K30
BITS 4-7 PD J31
BITS 0-3 PD J30
TO READ DISTRIBUTOR
I 37 CB
READ PERIPH FANOUT
I24 PY
G30 TL
G33-28
W13-906 W05 I0I21-11 READ PERIPH
READ RESUME CH 4.
2 NU
W28-906-W16 4C03-27
F31 PY
READ RESUME + WRITE RES.
WRITE RESUME CH2
NU
J06 TQ
SET T42 K0I-18 P.7
I11 TR
T23 I06-13 P.7
L22 FA
M06
FIRST FF I14 AA
NU
4 NU
M31-7, P.27 CLEAR 300 NSEC DELAY CHAIN
H33 TL
M.C.L. MI7-8, P.29
K15 TL
I22 TL
T41
I50 MI3-15
FROM ADDER FAN OUT
BIT 0
BIT 1
BIT 2
BIT 3
4 TO I3
3 TO I3
28 TO I3
27 TO I3, P15
I1 FAN IN
(ALL OUTPUTS TO R1 FANOUT)
BITS 30-35 TE L04
BITS 29-24 TE L03
BITS 18-23 TE K04
BITS 12-17 TE K03
BITS 6-11 TE J04
BITS 0-5 TE J03
X+B 6 CH3
X+B 5 CH3
X+B 7 CH3
X+B 22 CH 3
X+B 24 CH 3
X+B 23 CH 3
J31-11 25
J31-6 28
J31-12 25
J31-5 27
GATE N TO CM VIA PERIPHERAL
ADDRESS NETWORK
BITS 8-15 IH L30
BITS 0-7 IH J32
N BIT 4
N BIT 5
N BIT 6
N BIT 7
P30
K12 HF
L30-6
L30-24
T10 CEJ2 G16-20, P35
F06 TI
G04 TL
P31 TL
BIT 16 OF N
BIT 17 OF N
N REG 5
N REG 1
L15 TL
J15 TL
J39 QJ
W24-94 ECS COPY ADDRESS
K01 TR
T29 I07-10
GRD
GATE N VIA BITS 18-35 L01 TD
ENTER A K02-12, P13
K04-16
L03-16
L04-16
G04-28, P12
GATE N VIA BITS 0-17 L01 TD
T35 I08-13
K03-16
J04-16
I19-26, P13 ENTER B
I02 TD
T04, I03-16
T06, I03-25
J04-14
K03-14
K04-14
L03-14
GATE X +B +A
L01 TD
T28, G12-23
T37, I09-4
J04-15
K03-15
K04-15
G08 TH
P31-8, P.21 DISABLE CLEAR K
NU
2 NU
J15 TL
NU2
T38 P.7, L05-4
I22 TL
P31 GATE A
T06 I03-26
L04-14
NOTES:
L04-15 AND L03-15 ARE NOT USED.
② TO UPPER 18 BITS OF I1 FI IE J30-7 TO K04-2 J30-10 TO K04-1 ETC.
③ FOR THIS INPUT SEE P 31 FOR REMAINDER OF MODULE.
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
N REG, I1 FAN IN FIRST FF
EQUIPMENT ECS COUPLER AND CEJ/MEJ
SIZE C
DRAWING NO 60246600
REV Y
SHEET
PAGE 4-11



NOTES:

① ENABLE FLAG REGISTER END OF OPERATION. C31-9 PAGE 29.

CONTROL DATA CORPORATION DEVELOPMENT DIVIS	FLAG FUNCTION FLIP-FLOP	EQUIPMENT ECS COUPLER CEJ/MEJ	
		SIZE C	DRAWING NO 60246600 REV V
		SHEET	PAGE 4-1

A, B, X AND FLAG REGISTERS DESCRIPTION

A REGISTER

This is an 18-bit register which initially holds the contents of A_0 (relocation quantity for CM addresses). During Transfer Setup, RA(CM) is added to A and the result is entered in A and sent to the EAK. The initial CM address (page 11) A is updated every eighth word (once every record) by a count of 10; however, this updated address is entered in N and sent to CM T38 (P. 11) for each record.

B REGISTER

This 18-bit register holds the total number of words to be transferred. Initially, it has the contents of B_0 (Bj + K), but it is decremented by the number of words to be transferred in the next record. This is done during Record Setup. If it is the last record, the lower 3 bits of B are sent to the decrementer. This condition is determined by N being positive; that is, K was greater or equal to B. B is not changed if this condition is met.

X REGISTER

This 24-bit register holds the ECS address. It is updated by 10_8 for each record request made to the ECS Controller. The initial contents of X is the relocation quantity X_0. During transfer set up time RA(ECS) is added to X and the result entered in X. The address is sent to the controller at T34, but the updating for the address took place during the previous Record Setup time. This is done to ensure sufficient time for the Request to be processed by the Controller. Note that the Store Bit transmitter is on module K42 and is sent at the same time, (see page 27).

FLAG REGISTER

The Flag register is selected by executing an ECS Read or Write instruction with bit 23 set in both the ECS address (X0) and FLECS. No FL(ECS) checking is performed and RA(ECS) is not added to the ECS address (X0). The operation is the same for either ECS instruction and is not affected by the Fifty Percent Capacity Reduction.

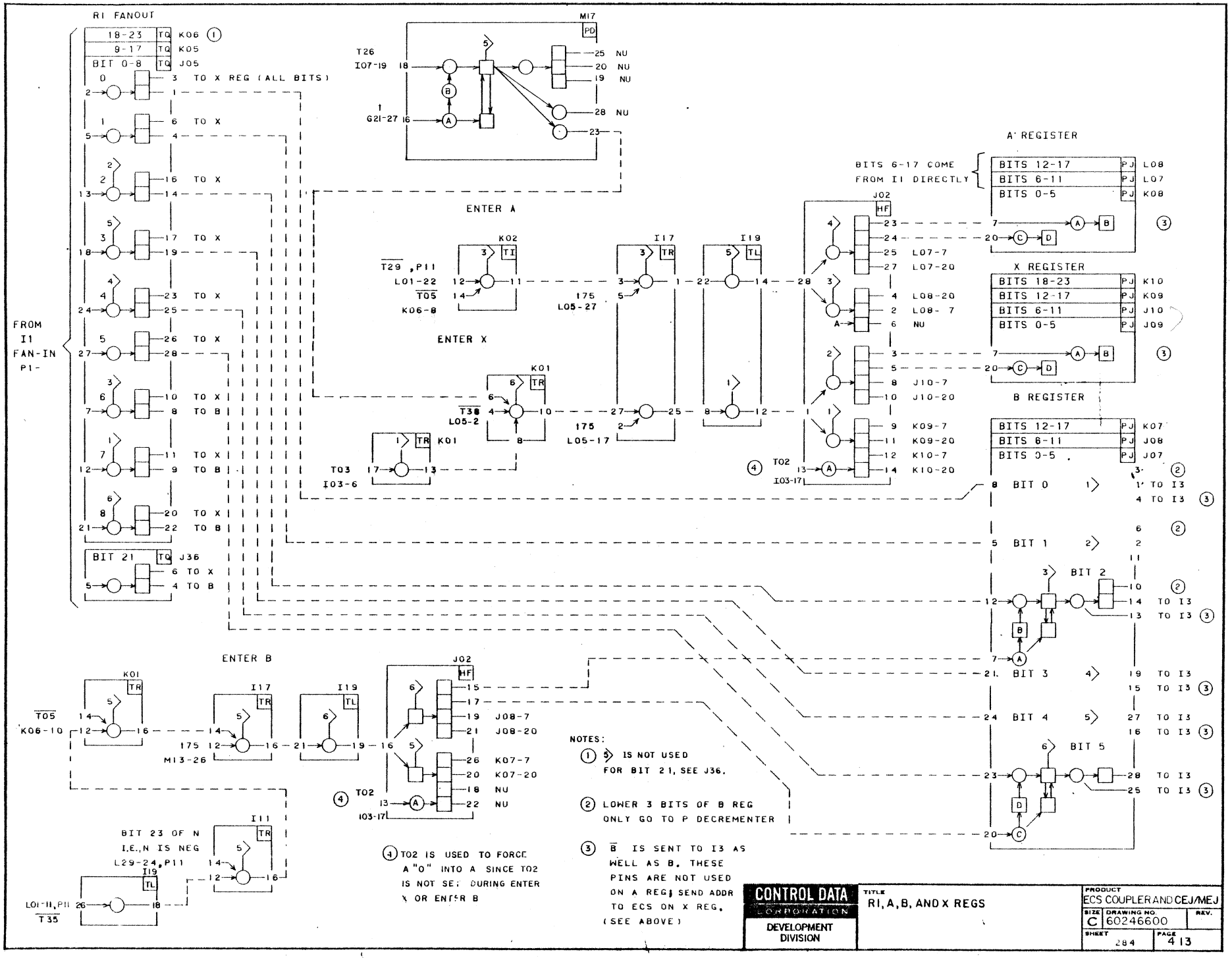
The contents of X0 are sent to the controller as is any other ECS address. Since bit 23 is set, the controller recognizes this as a Flag register operation. It then translates bits 22 and 21 to see what function is to be performed.

The response to a Flag register Function is either an error exit or a normal exit from the ECS instruction. Receipt of either an Accept or an abort from the controller enables an End of Operation for a Flag Function (see P29).

For a Flag register operation the ECS address is considered to have three parts (Figure 3-2).

Function Code			Flag Word	
23	21	20 18	17	0

1. Function Code (N) is bits 21-23. Bit 23 is always set for a Flag register operation.
2. Bits 18-20 are not used.
3. The flag word is bits 0-17. These bits are compared with or entered into the Flag register depending on the function specified by N.

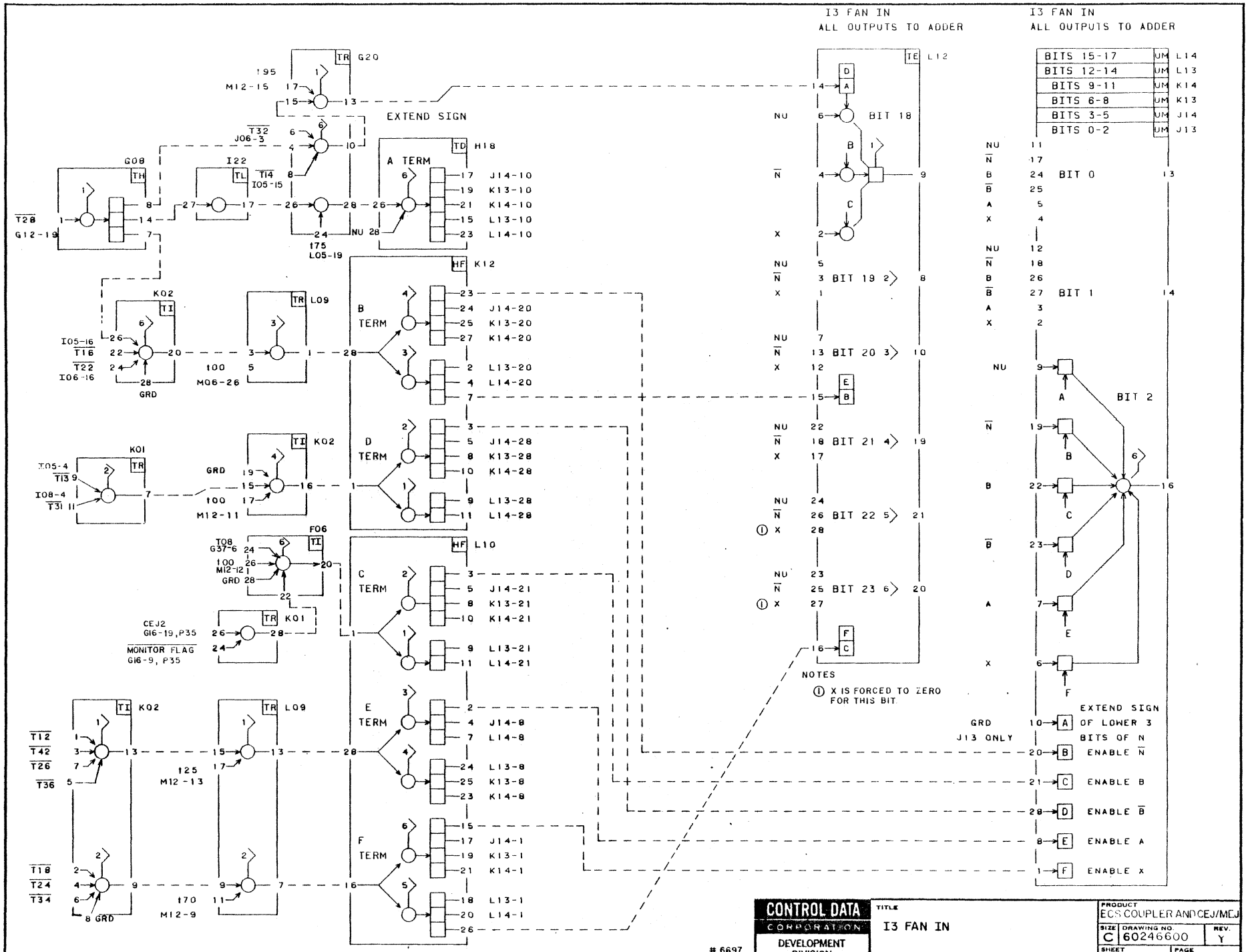

R1 FANOUT
18-23 TQ K06
9-17 TQ K05
BIT 0-8 TQ J05
TO X REG (ALL BITS)
TO X
TO B
BIT 21 TQ J36
FROM I1 FAN-IN P1-
M17
T26 I07-19
G21-27 16
ENTER A
ENTER X
ENTER B
K01
K02
I17
I19
J02
T29 ,P11 L01-22
T05 K06-8
T36 L05-2
T03 I03-6
175 L05-27
175 L05-17
T02 I03-17
BITS 6-17 COME FROM I1 DIRECTLY
A REGISTER
X REGISTER
B REGISTER
BITS 12-17 PJ L08
BITS 6-11 PJ L07
BITS 0-5 PJ K08
BITS 18-23 PJ K10
BITS 12-17 PJ K09
BITS 6-11 PJ J10
BITS 0-5 PJ J09
BITS 12-17 PJ K07
BITS 6-11 PJ J08
BITS 0-5 PJ J07
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
I11
BIT 23 OF N I.E.,N IS NEG L29-24,P11
L01-11,P11 T35
NOTES:
(1) 5 IS NOT USED FOR BIT 21, SEE J36.
(2) LOWER 3 BITS OF B REG ONLY GO TO P DECREMENTER
(3) B IS SENT TO I3 AS WELL AS B. THESE PINS ARE NOT USED ON A REG; SEND ADDR TO ECS ON X REG. (SEE ABOVE)
(4) T02 IS USED TO FORCE A "0" INTO A SINCE T02 IS NOT SET DURING ENTER A OR ENTER B
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE R1, A, B, AND X REGS
PRODUCT ECS COUPLER AND CEJ/MEJ
SIZE C DRAWING NO. 60246600 REV.
SHEET 284 PAGE 413

I3 FAN IN DESCRIPTION

The I3 Fan In allows the X, B, A or N registers to enter the adder.

Note:

1. The lowest 3 bits of the fan in are gated by the timing chain only.
2. Bits 3 through 23 can be forced to ones by the extend sign (A term). This is done at T28 to extend the negative sign of the complement of the lower 3 bits of X register. This is done when N (holding the newly updated ECS address) and K are sent to the coupler is determining the number of words to be transferred on all records except last.
3. Bits 18 through 23 can be forced to ones by the extend sign (A term). This extends an 18-bit negative number to 23 bits. The sign is extended at T16 when (A+K) is in N and is to be subtracted from FL(CM) for Field Length checks. At the K-B test is performed with B being sent to the adder, and its sign is therefore extended.


I3 FAN IN
ALL OUTPUTS TO ADDER
I3 FAN IN
ALL OUTPUTS TO ADDER
EXTEND SIGN
A TERM
B TERM
D TERM
C TERM
E TERM
F TERM
BIT 18
BIT 0
BIT 1
BIT 2
BIT 19 2
BIT 20 3
BIT 21 4
BIT 22 5
BIT 23 6
BITS 15-17
BITS 12-14
BITS 9-11
BITS 6-8
BITS 3-5
BITS 0-2
EXTEND SIGN OF LOWER 3 BITS OF N
ENABLE N
ENABLE B
ENABLE B
ENABLE A
ENABLE X
NOTES
① X IS FORCED TO ZERO FOR THIS BIT
MONITOR FLAG
CEJ2
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
6697
TITLE
I3 FAN IN
PRODUCT
ECS COUPLER AND CEJ/MEJ
SIZE C
DRAWING NO. 60246600
REV. Y
SHEET
PAGE 4-15

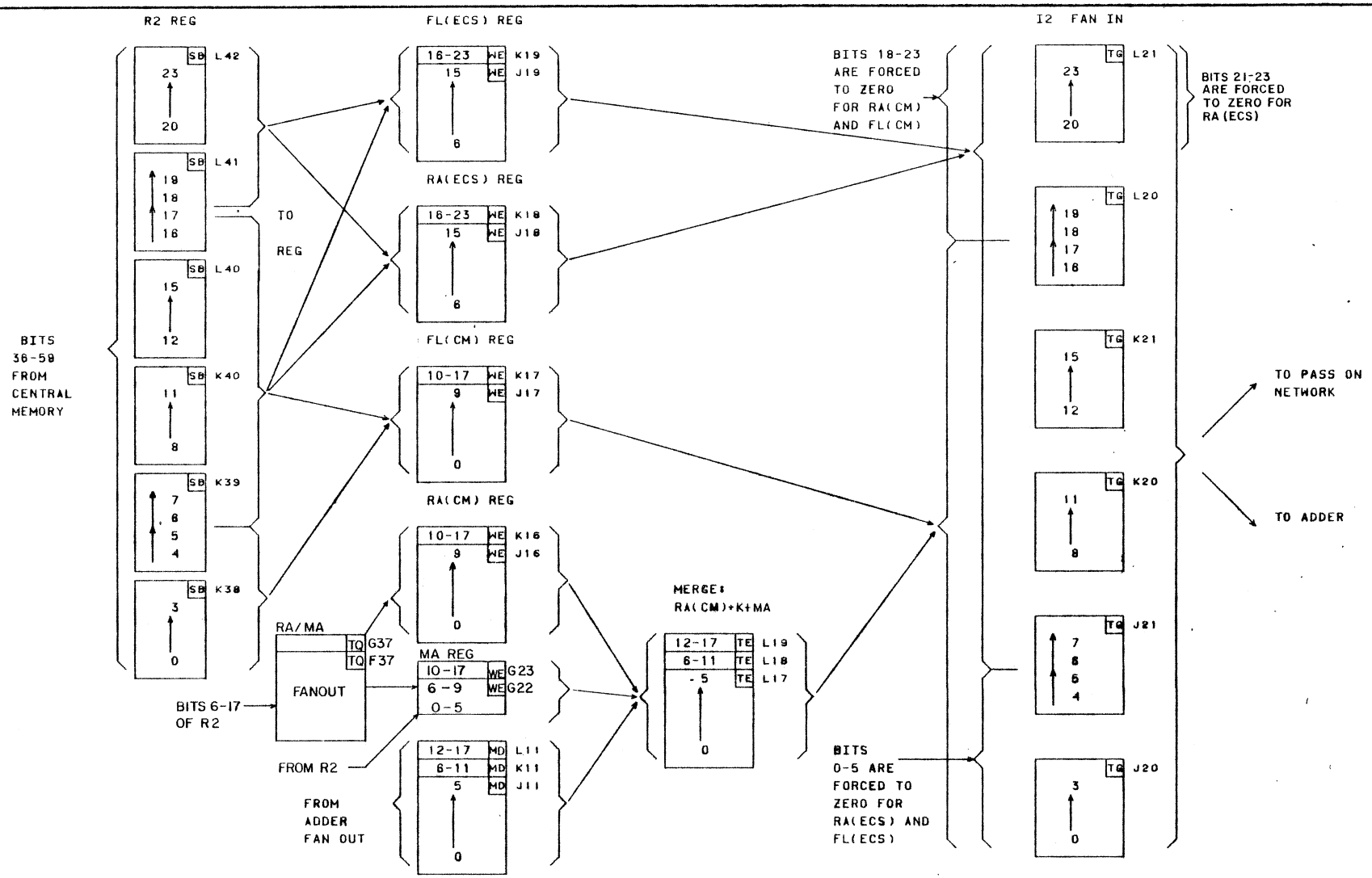
R2, RA AND FL REGISTERS

R2 REGISTER

This is a 24-bit catching register. Its contents are directed to the RA or FL registers by the address tags. These tag bits are the Increment Unit to A bits which are not used during ECS instructions and are therefore assigned to directing the ECS and CM parameters.

MA, RA AND FL REGISTER

These hold MA, RA and FL quantities from the Exchange Jump package. Note that the lower 6 bits of the ECS registers do not exist.



#6698

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

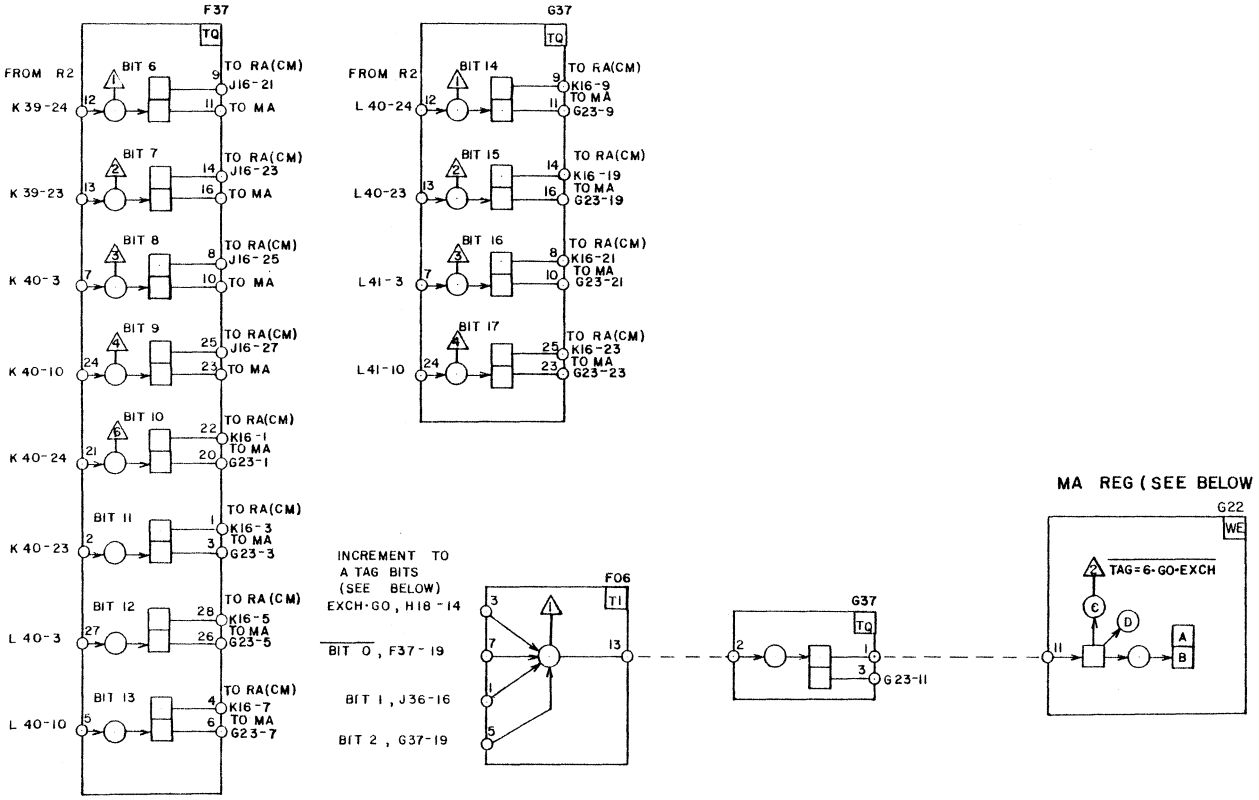
TITLE
DATA FLOW 2
R2, FL AND RA REGS
I2 FAN-IN

PRODUCT
ECS COUPLER AND CEJ/MEJ

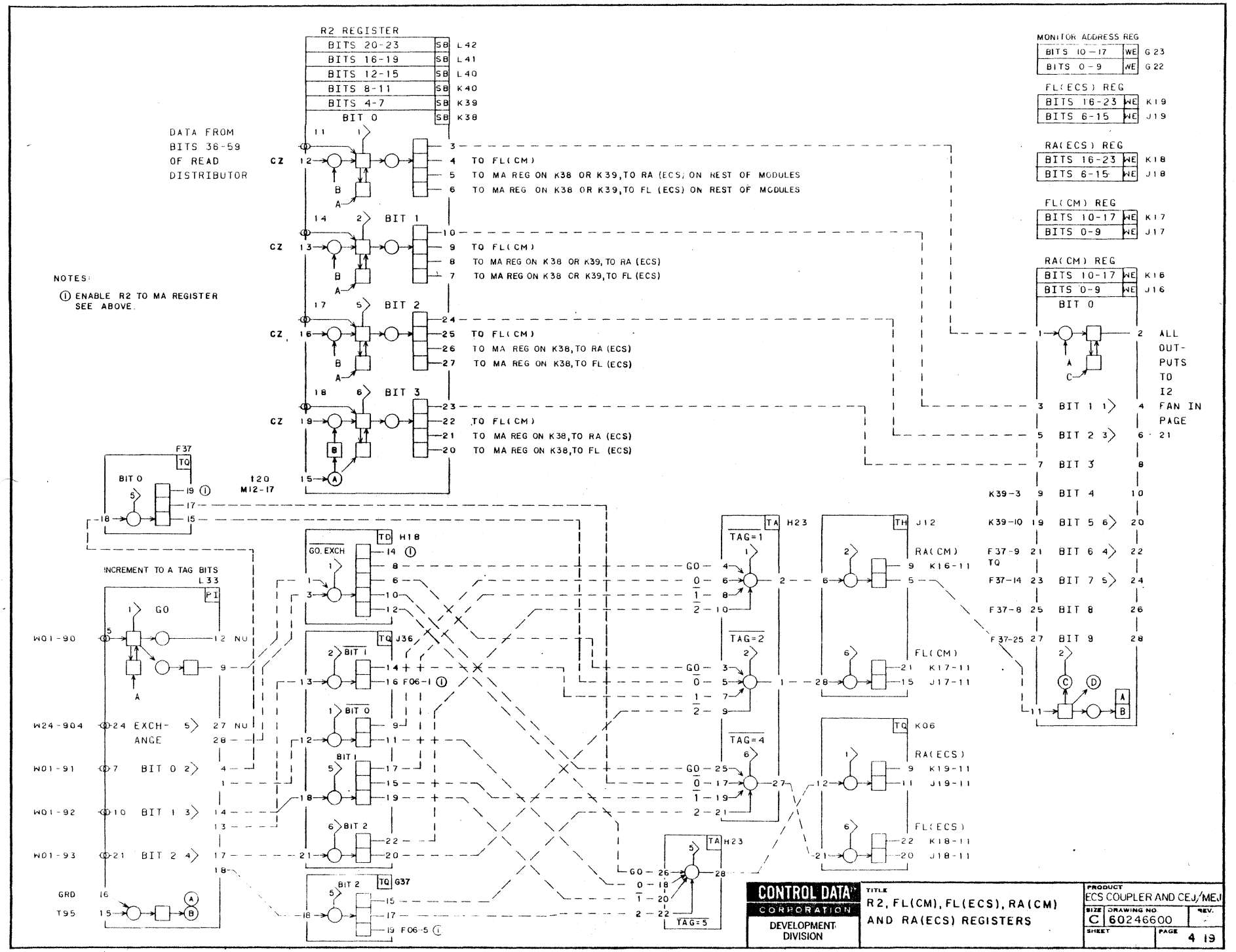
SIZE C | DRAWING NO. 60246600 | REV.

SHEET | PAGE 4 17

R2→ MA FANOUTS
(LOWER 6 BITS GO DIRECTLY TO MA)



PUB. NO. 60246600
REV. G 4-18


R2 REGISTER
BITS 20-23 SB L42
BITS 16-19 SB L41
BITS 12-15 SB L40
BITS 8-11 SB K40
BITS 4-7 SB K39
BIT 0 SB K38
DATA FROM BITS 36-59 OF READ DISTRIBUTOR
CZ
BIT 1
BIT 2
BIT 3
TO FL(CM)
TO MA REG ON K38 OR K39,TO RA (ECS) ON REST OF MODULES
TO MA REG ON K38 OR K39,TO FL (ECS) ON REST OF MODULES
TO MA REG ON K38 OR K39,TO RA (ECS)
TO MA REG ON K38,TO FL (ECS)
TO MA REG ON K38,TO RA (ECS)
NOTES:
① ENABLE R2 TO MA REGISTER SEE ABOVE.
MONITOR ADDRESS REG
BITS 10-17 WE G23
BITS 0-9 WE G22
FL(ECS) REG
BITS 16-23 WE K19
BITS 6-15 WE J19
RA(ECS) REG
BITS 16-23 WE K18
BITS 6-15 WE J18
FL(CM) REG
BITS 10-17 WE K17
BITS 0-9 WE J17
RA(CM) REG
BITS 10-17 WE K16
BITS 0-9 WE J16
ALL OUTPUTS TO I2 FAN IN PAGE 21
INCREMENT TO A TAG BITS L33
GO. EXCH
TAG=1
TAG=2
TAG=4
TAG=5
RA(CM) K16-11
FL(CM) K17-11
RA(ECS) K19-11
FL(ECS) K18-11
F37-9 TQ
F37-14
F37-8
F37-25
K39-3
K39-10
W01-90
W24-904
W01-91
W01-92
W01-93
GRD
T95
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE
R2, FL(CM), FL(ECS), RA(CM) AND RA(ECS) REGISTERS
PRODUCT
ECS COUPLER AND CEJ/MEJ
SIZE C
DRAWING NO 60246600
REV.
SHEET
PAGE 4 19

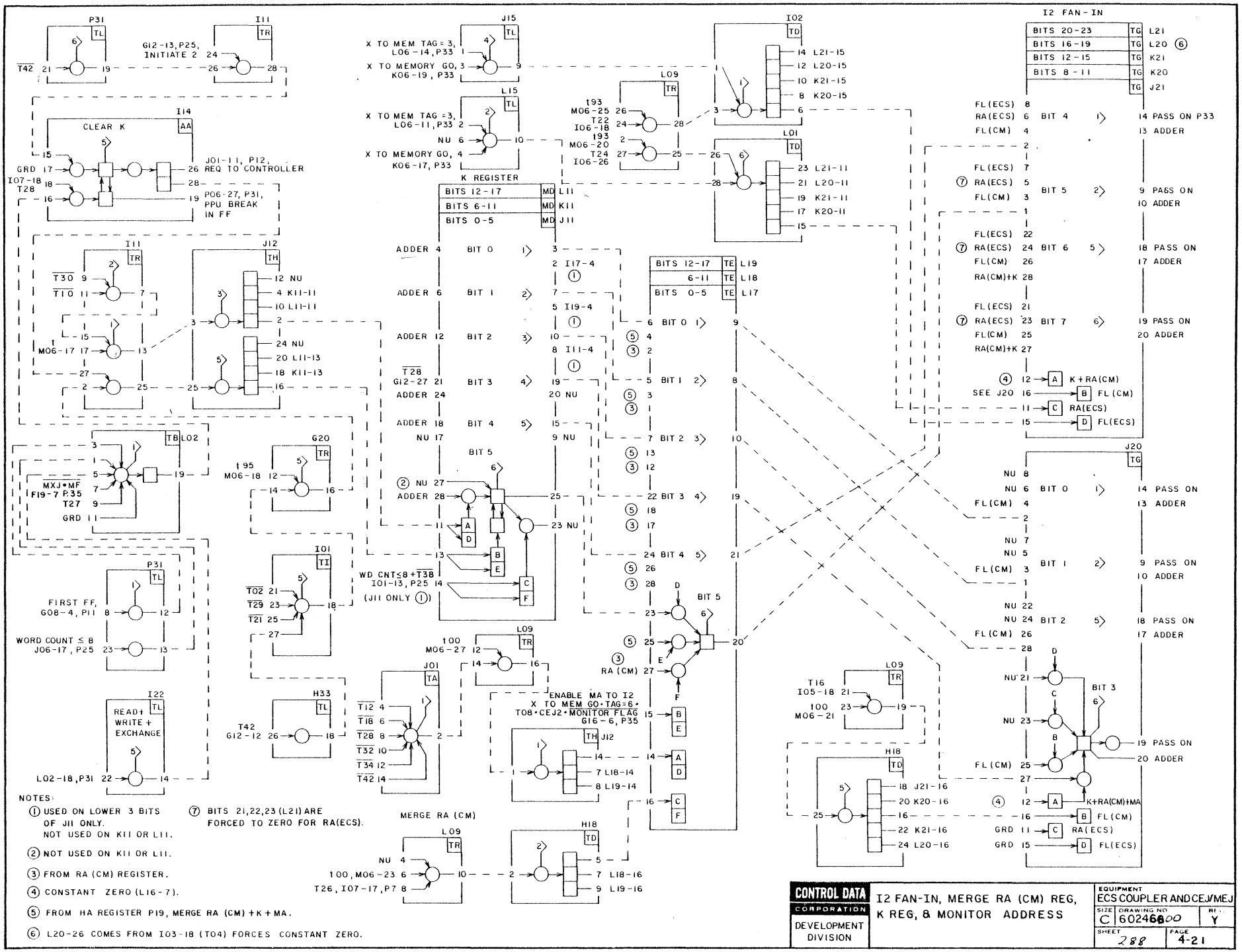
I2 FAN IN AND K REGISTER DESCRIPTION

K REGISTER

This 18-bit register holds the word count for one record. It also can have bit 3 forced to a one, which is used to increment quantities by 10_8. An exception occurs during PPU Break-in when K is held clear disabling the $K + 10_8$ addition. Its inputs on I2 are shared with RA(CM) register and they are controlled by the merge RA(CM) or K gates which allow one or the other to I2. The lower 3 bits of K are sent to the P register except on the last record, when B is sent to P.

I2 FAN IN

This fan in allows RA, FL and K to send operands to the adder or to the pass on network. The letter would be done only if an Exchange Jump occurred. Since the lower 6 bits of the ECS registers do not exist, their inputs on I2 are not used. Also, since RA(CM) and K are controlled by the merge gates, their gating term (A) on I2 is always a logical one output.



NOTES:

(1) USED ON LOWER 3 BITS OF J11 ONLY. NOT USED ON K11 OR L11.

(2) NOT USED ON K11 OR L11.

(3) FROM RA (CM) REGISTER.

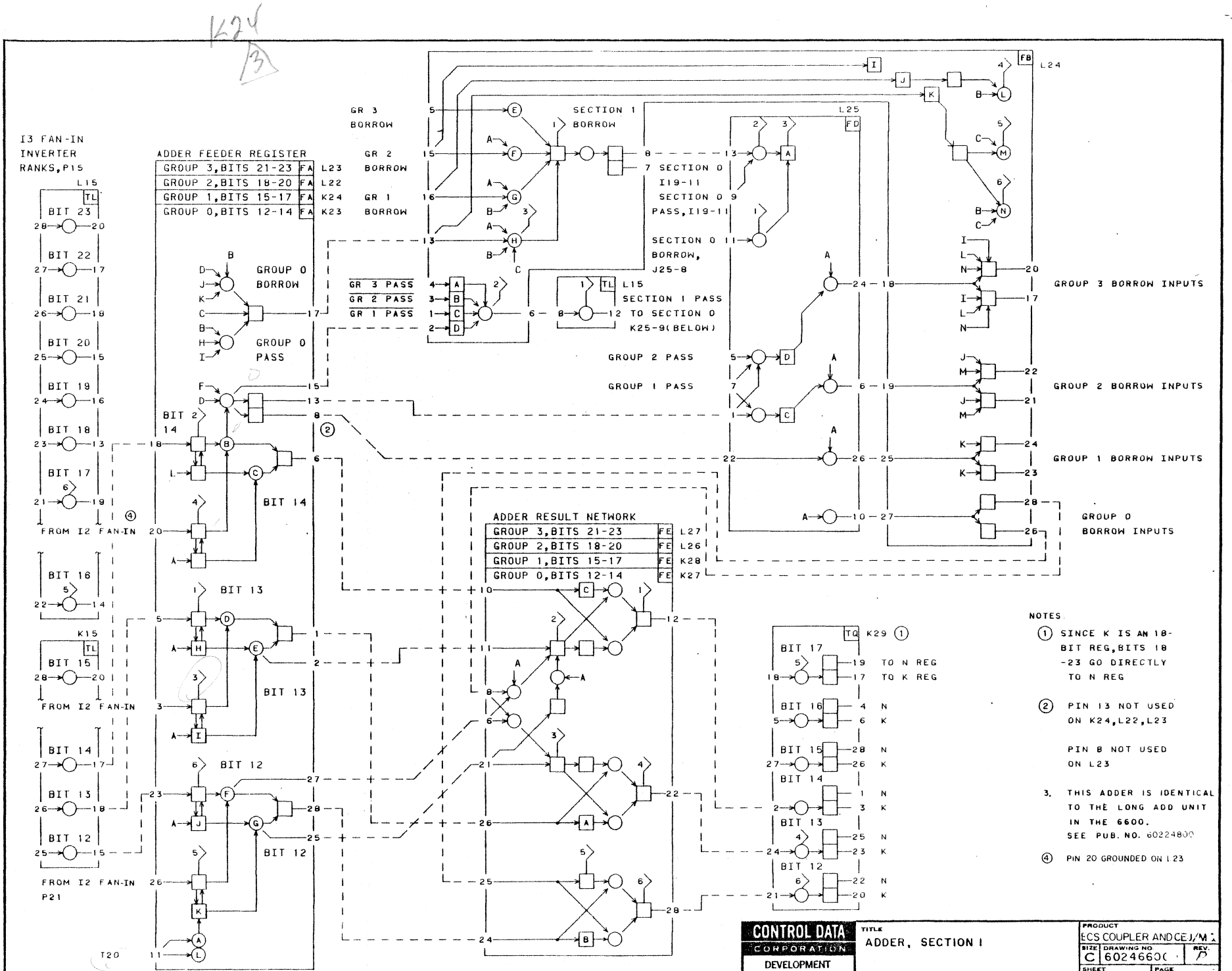
(4) CONSTANT ZERO (L16-7).

(5) FROM HA REGISTER P19, MERGE RA (CM) +K+MA.

(6) L20-26 COMES FROM I03-18 (T04) FORCES CONSTANT ZERO.

(7) BITS 21,22,23 (L21) ARE FORCED TO ZERO FOR RA(ECS).

CONTROL DATA CORPORATION DEVELOPMENT DIVISION	I2 FAN-IN, MERGE RA (CM) REG, K REG, & MONITOR ADDRESS	EQUIPMENT: ECS COUPLER AND CEJ/MEJ SIZE C · DRAWING NO 60246800 · REV Y SHEET 288 · PAGE 4-21	



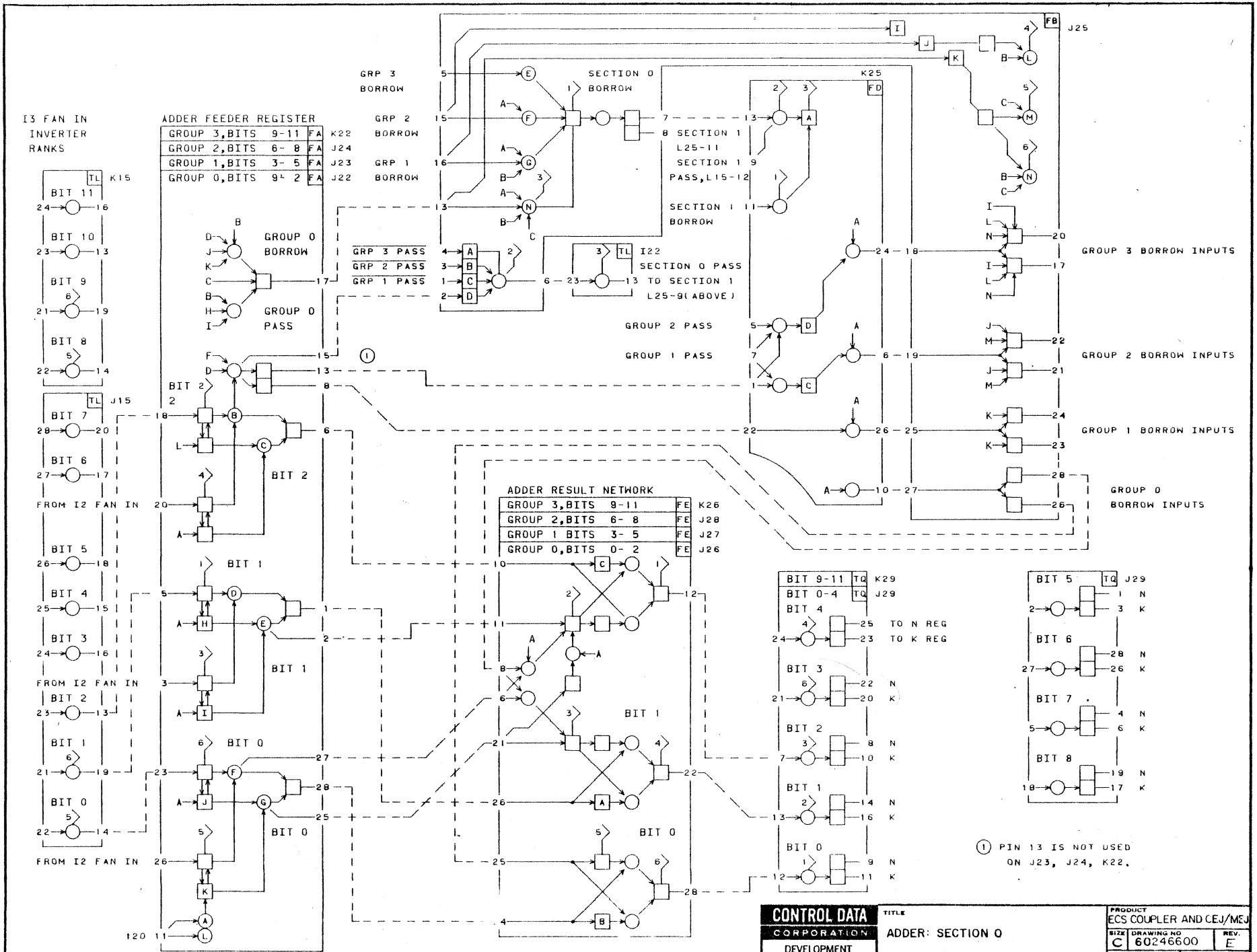
NOTES

1. SINCE K IS AN 18-BIT REG, BITS 18-23 GO DIRECTLY TO N REG
2. PIN 13 NOT USED ON K24, L22, L23
   PIN 8 NOT USED ON L23
3. THIS ADDER IS IDENTICAL TO THE LONG ADD UNIT IN THE 6600. SEE PUB. NO. 60224800
4. PIN 20 GROUNDED ON L23

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: ADDER, SECTION 1

PRODUCT: ECS COUPLER AND CE J/M
SIZE C | DRAWING NO. 6024660(| REV. P
SHEET | PAGE 4.2



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: ADDER: SECTION 0

PRODUCT: ECS COUPLER AND CEJ/MEJ
SIZE C | DRAWING NO 60246600 | REV. E
SHEET | PAGE 4-23

6702

P DECREMENTER AND REGISTER

The output of the decrementer is one count less than the 3-bit quantity in the P register. When the clear/set input to P is strobed at T00, this reduced quantity is entered in P.

The lower 3 bits of K are entered in P unless it is the last record; then the lower 3 bits of B are entered in P.

The decrementer runs only when the Enable P FF is set. On a write operation this is at T41 but on a Read operation there is a considerable delay before the data arrives, so the Read 2 FF is sent through a 300 nsec delay chain before setting the Enable P FF. Once this FF is set, the remainder of the coupler's logic can start the next Record Setup and the clock pulses decrement P and send the GO signal to the Exchange Address Counter. When P = 0 the Enable FF will be clear unless a new request has been sent; that is, it was not the last record. Note that the decrementer logic is cyclic; it will decrement an all zero P register to all ones.

LAST RECORD CONTROL

WORD COUNT $\leq$ FLIP FLOP

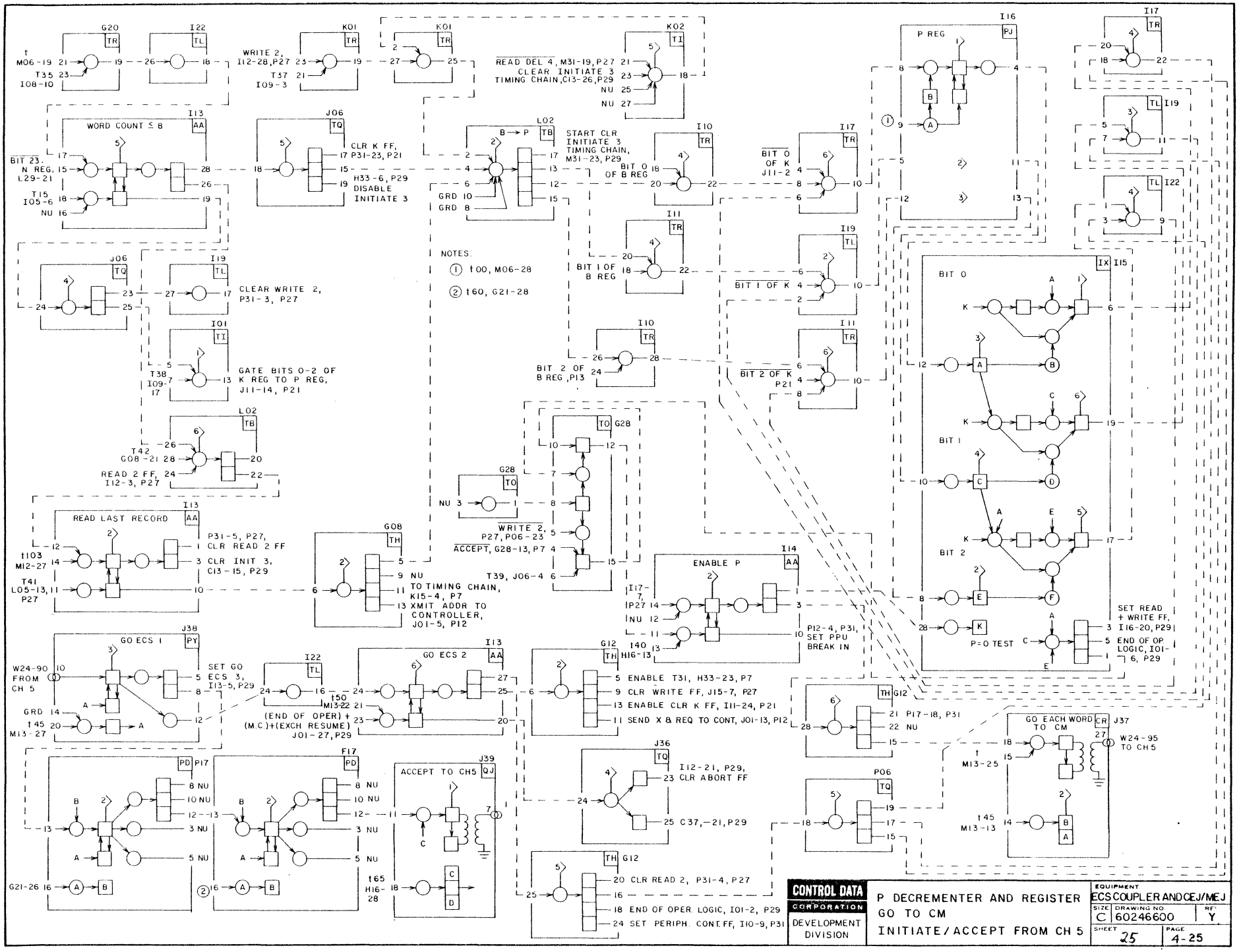
This is set if the N register is positive after the K-B check on the last record only. If set, B is sent to P; if clear, K is sent to P.

READ LAST RECORD FLIP FLOP

This set by the Word Count $\leq$ 8 FF, Read 2 FF and T42 and blocks the reset Record Setup sequence from occurring.

INITIATE 1 FLIP FLOP

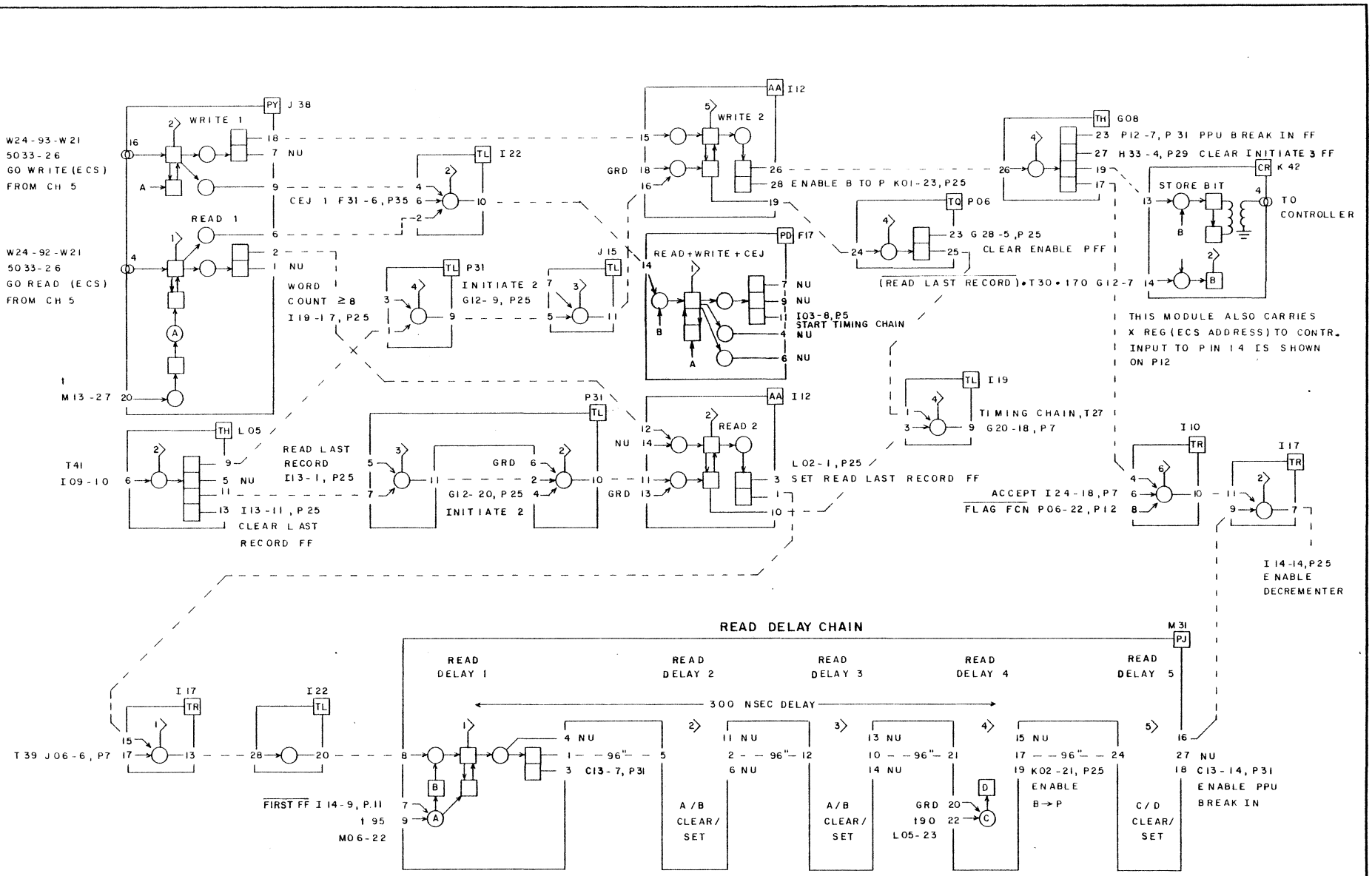
This is set from CPU when the instruction is translated. The Accept signal is returned immediately to CPU.


NOTES:
(1) t00, M06-28
(2) t60, G21-28
P REG
BIT 0
BIT 1
BIT 2
P=0 TEST
ENABLE P
READ LAST RECORD
WORD COUNT ≤ 8
GO ECS 1
GO ECS 2
ACCEPT TO CH5
GO EACH WORD TO CM
CLEAR WRITE 2, P31-3, P27
GATE BITS 0-2 OF K REG TO P REG, J11-14, P21
START CLR INITIATE 3 TIMING CHAIN, M31-23, P29
CLR K FF, H33-6, P29 DISABLE INITIATE 3
READ DEL 4, M31-19, P27 CLEAR INITIATE 3 TIMING CHAIN, C13-26, P29
TO TIMING CHAIN, K15-4, P7 XMIT ADDR TO CONTROLLER, J01-5, P12
SET READ + WRITE FF, I16-20, P29
END OF OP LOGIC, I01-6, P29
P12-4, P31, SET PPU BREAK IN
SET GO ECS 3, I13-5, P29
I12-21, P29, CLR ABORT FF
ENABLE T31, H33-23, P7
CLR WRITE FF, J15-7, P27
ENABLE CLR K FF, I11-24, P21
SEND X & REQ TO CONT, J01-13, P12
P17-18, P31
SET PERIPH. CONT. FF, I10-9, P31
END OF OPER. LOGIC, I01-2, P29
CLR READ 2, P31-4, P27
W24-95 TO CH5
W24-90 FROM CH 5
P DECREMENTER AND REGISTER GO TO CM
INITIATE/ACCEPT FROM CH 5
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
EQUIPMENT ECS COUPLER AND CEJ/MEJ
SIZE C
DRAWING NO 60246600
REV Y
SHEET 25
PAGE 4-25

READ AND WRITE FF DESCRIPTIONS

Along with the Initiate 1 signal, CPU sets either the Write 1 or Read 1 FFs. The Read/Write FF is set by either one and the timing chain started. On a Read operation the decrementer is not enabled until T39 + 400 nsec to give the data time to reach the coupler. On a Write operation, the delay is not necessary.

When the last record reaches T42 and tries to restart at T27, the timing chain will be blocked. Either Write 2 or Read 2 must be set for it to continue.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE READ AND WRITE FFS	PRODUCT ECS COUPLER AND CEJ/MEJ	
		SIZE C	DRAWING NO. 60246600
		REV Y	
		SHEET 2 OF 3	PAGE 4-27

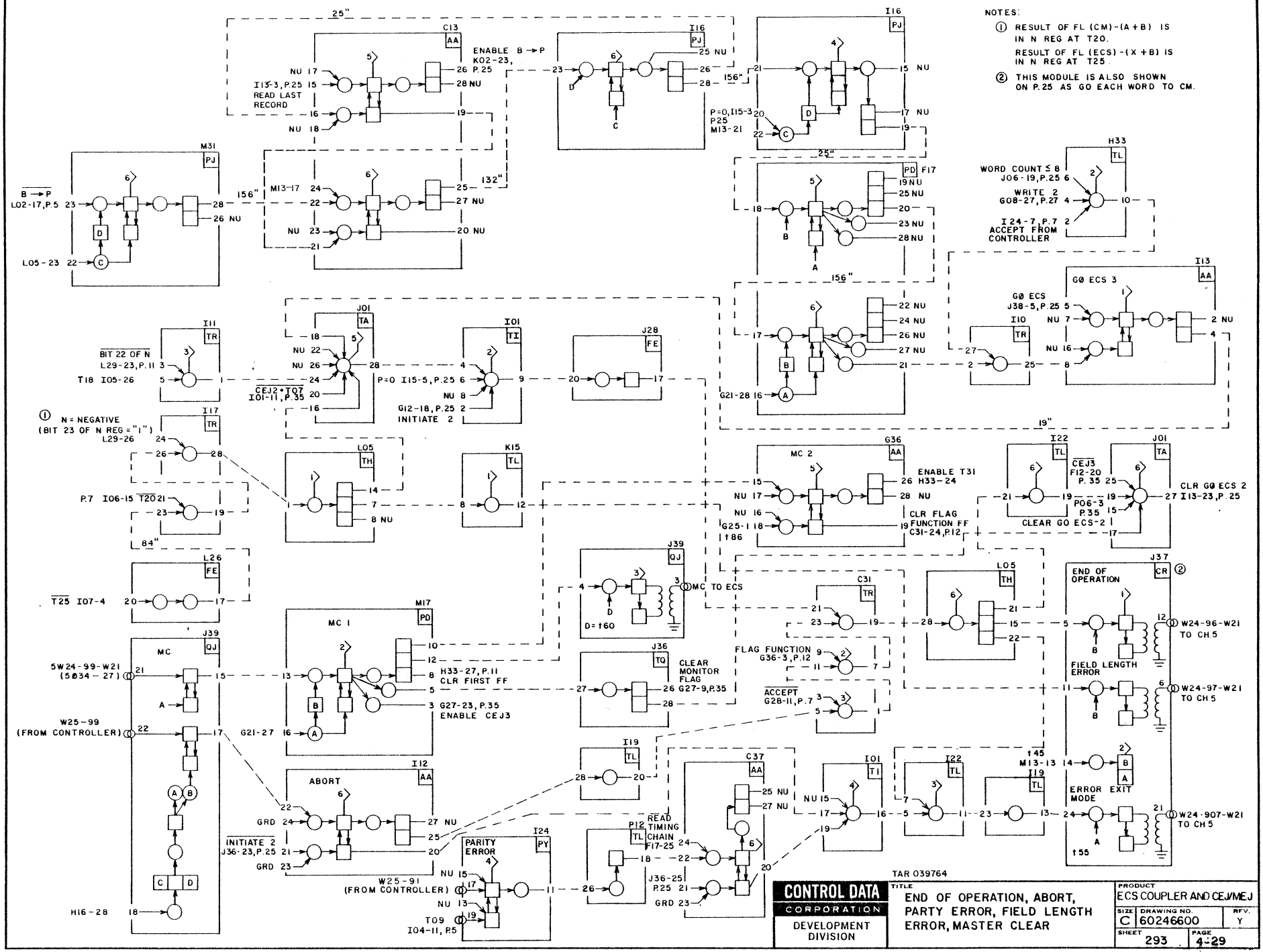
ERROR AND TERMINATION CONDITIONS

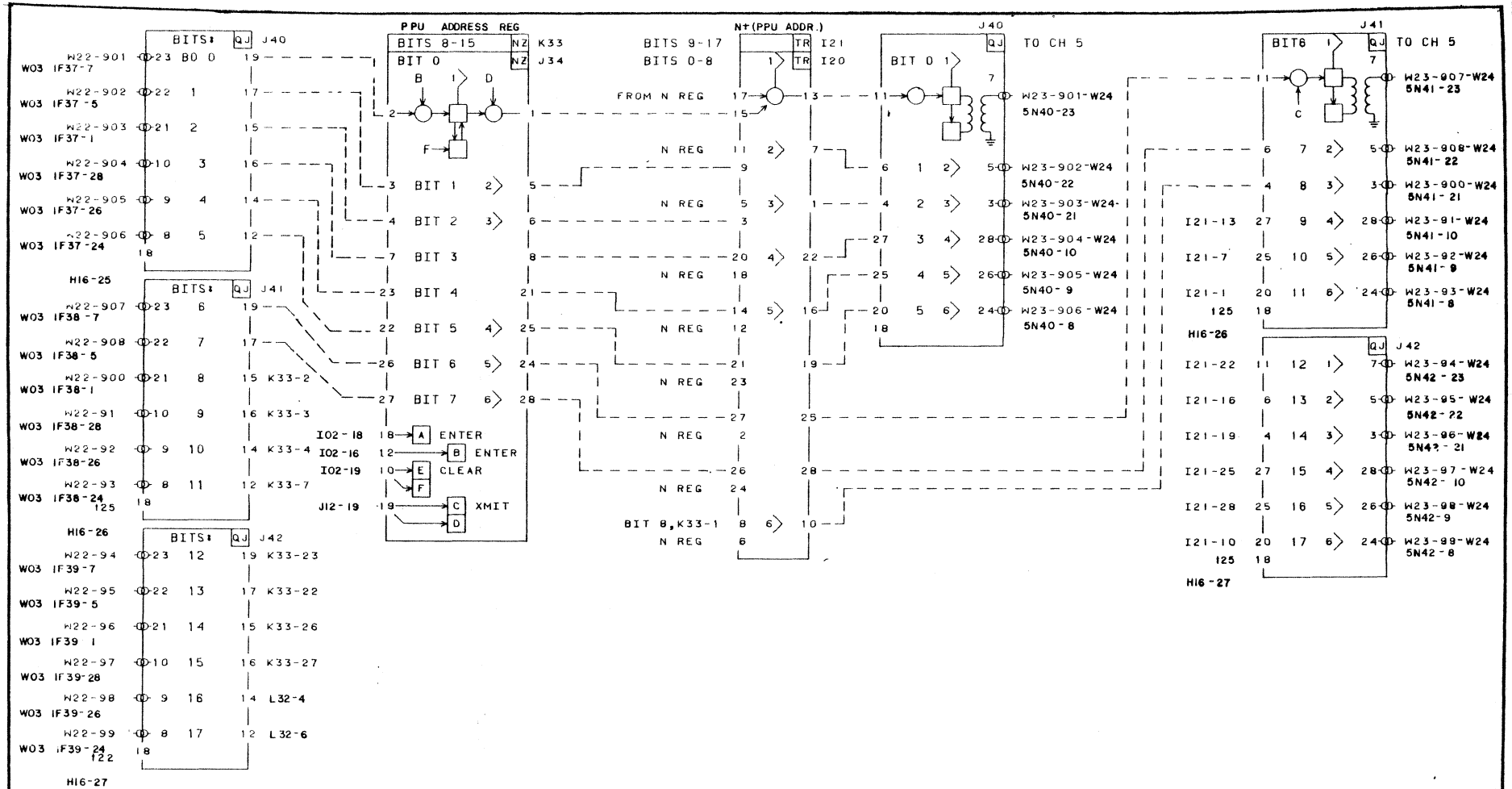
End of Operation signal is sent if the decrementer reaches 0 and this is the last record, or if a Field Length error occurs.

A Field Length error signal is sent after checking FL(CM)-(A+B) and FL(ECS)-(X+B) and getting a negative result. This is the only error condition that the coupler checks or acts upon.

Error Exit Mode signal is sent on any Field Length error, Abort or Parity error. Note that CPU cannot distinguish between a Parity Error and an Abort.

On a Read operation, an Abort is used in place of the Accept to keep the timing chain running. This allows the programmer to transfer all zeroes to CM if he wishes. On a Write operation CPU discontinues the transfer. On a Parity Error, the coupler relays the signal as an Error Exit Mode. Neither Abort nor Parity Error cause an End of Operation signal.


NOTES:
① RESULT OF FL (CM)-(A+B) IS IN N REG AT T20.
RESULT OF FL (ECS)-(X+B) IS IN N REG AT T25.
② THIS MODULE IS ALSO SHOWN ON P.25 AS GO EACH WORD TO CM.
ENABLE B → P K02-23,
I13-3,P.25 READ LAST RECORD
P=0,I15-3 P25 M13-21
B → P L02-17,P.5
L05-23
M13-17
WORD COUNT ≤ 8 J06-19,P.25
WRITE 2 G08-27,P.27
I24-7,P.7 ACCEPT FROM CONTROLLER
GØ ECS J38-5,P.25
GØ ECS 3
BIT 22 OF N L29-23,P.11
T18 I05-26
CEJ2*T07 I01-11,P.35
P=0 I15-5,P.25
G12-18,P.25 INITIATE 2
① N = NEGATIVE (BIT 23 OF N REG = "1") L29-26
P.7 I06-15 T20
T25 I07-4
G21-28
ENABLE T31 H33-24
CLR FLAG FUNCTION FF C31-24,P.12
G25-1 †86
CEJ3 F12-20 P.35
P06-3 P.35
CLEAR GO ECS-2
CLR GØ ECS 2 I13-23,P.25
MC TO ECS
D=†60
MC 1
MC
5W24-99-W21 (5034-27)
W25-99 (FROM CONTROLLER)
H33-27,P.11 CLR FIRST FF
G27-23,P.35 ENABLE CEJ3
CLEAR MONITOR FLAG G27-9,P.35
FLAG FUNCTION G36-3,P.12
ACCEPT G28-11,P.7
END OF OPERATION
W24-96-W21 TO CH 5
FIELD LENGTH ERROR
W24-97-W21 TO CH 5
ERROR MODE EXIT
W24-907-W21 TO CH 5
ABORT
INITIATE 2 J36-23,P.25
PARITY ERROR
W25-91 (FROM CONTROLLER)
T09 I04-11,P.5
H16-28
READ TIMING CHAIN F17-25
J36-25 P.25
M13-13 †45
†55
TAR 039764
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
TITLE
END OF OPERATION, ABORT, PARTY ERROR, FIELD LENGTH ERROR, MASTER CLEAR
PRODUCT ECS COUPLER AND CEJ/MEJ
SIZE C
DRAWING NO. 60246600
REV. Y
SHEET 293
PAGE 4-29



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE PERIPHERAL ADDRESS NETWORK (TO CM)	PRODUCT ECS COUPLER AND CEJ/MEJ	
		SIZE C	DRAWING NO. 6024660
		REV. C	
		SHEET	PAGE 4-30

PPU BREAK IN

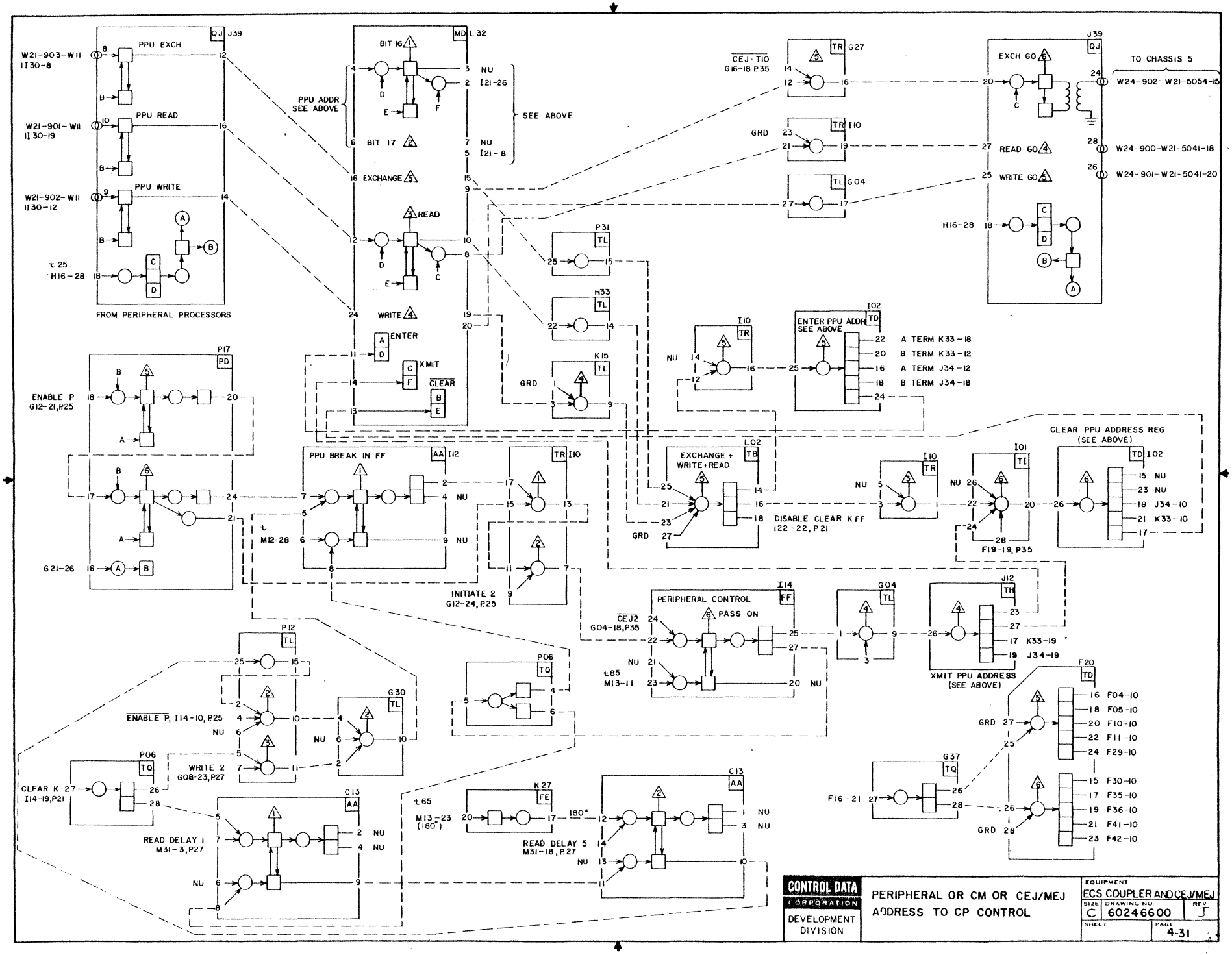
A PPU may interrupt any record except the first and last record. To enable a PPU Break in these conditions must exist:

First FF is clear.

Enable P FF is set.

Clear K FF is clear.

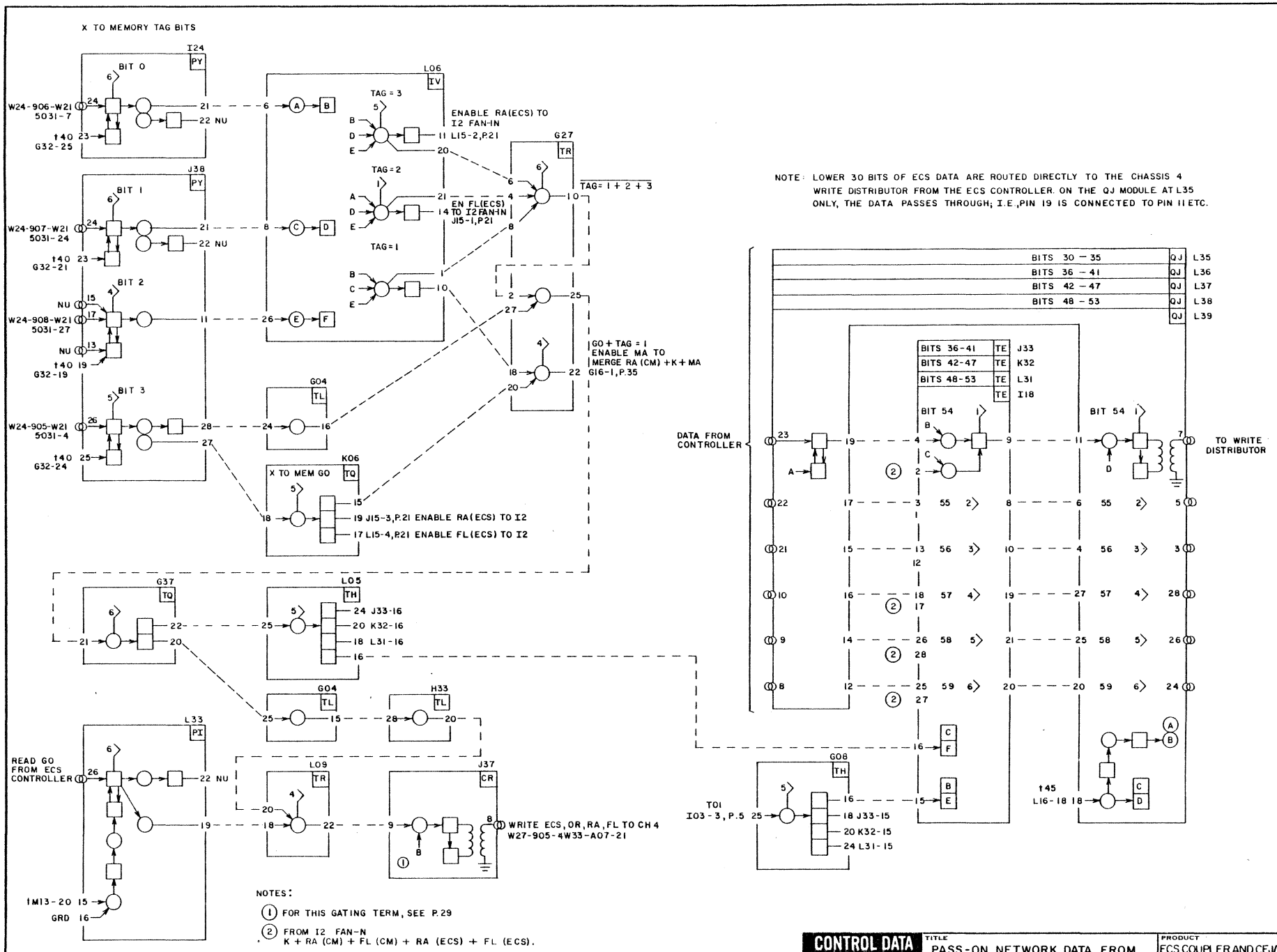
At T30 a PPU Break in disables the Address to Controller for the interrupted record, but allows the timing chain for that record to continue to T40. At T40 the timing chain stops because an Accept from the Controller was not received. During a PPU Break in K is held clear to disable the $K + 10_8$ addition which increments the word count of the interrupted record. The incremented word count would be used for the next record on a Normal Transfer; however, during a PPU Breakin, with K being held clear, 0 is added to K to maintain the word count of the interrupted record. At the end of a PPU Break in a Read or Write Resume signal sets T42 FF, repeating the Record Setup for the interrupted record and resets the First FF.


PPU EXCH
PPU READ
PPU WRITE
W21-903-W11 I130-8
W21-901-W11 I130-19
W21-902-W11 I130-12
FROM PERIPHERAL PROCESSORS
PPU ADDR SEE ABOVE
BIT 16
BIT 17
EXCHANGE
READ
WRITE
ENTER
XMIT
CLEAR
SEE ABOVE
I21-26
I21-8
EXCH GO
READ GO
WRITE GO
TO CHASSIS 5
W24-902-W21-5054-15
W24-900-W21-5041-18
W24-901-W21-5041-20
ENTER PPU ADDR SEE ABOVE
A TERM K33-18
B TERM K33-12
A TERM J34-12
B TERM J34-18
ENABLE P G12-21,P25
PPU BREAK IN FF
DISABLE CLEAR K FF I22-22, P21
CLEAR PPU ADDRESS REG (SEE ABOVE)
F19-19, P35
INITIATE 2 G12-24, P25
PERIPHERAL CONTROL
PASS ON
XMIT PPU ADDRESS (SEE ABOVE)
ENABLE P, I14-10, P25
WRITE 2 G08-23, P27
CLEAR K 27 I14-19, P21
READ DELAY 1 M31-3, P27
READ DELAY 5 M31-18, P27
180"
F16-21
CONTROL DATA CORPORATION
DEVELOPMENT DIVISION
PERIPHERAL OR CM OR CEJ/MEJ ADDRESS TO CP CONTROL
EQUIPMENT ECS COUPLER AND CEJ/MEJ
SIZE C
DRAWING NO 60246600
REV J
SHEET
PAGE 4-31

PASS-ON NETWORK DESCRIPTION

The data path from the Controller to CM has provision for the contents of the Coupler's registers to be restored into memory. This logic is the OR gate marked on the block diagram and provides a restore path for RA(ECS) and FL(ECS) if an Exchange Jump is executed. RA(CM) and FL(CM) are restored from the CPU. As long as the coupler is involved in a data transfer, the data path from the Controller to the Write Distributor (Chassis 2) is enabled. This is done by the Initiate 2 FF, which is cleared only on an End of Operation condition.

The address tags from the stunt box are translated for an Exchange Jump and enable RA(ECS) and FL(ECS) to be stored in Exchange Jump packet. (Note that bit 1 of these tags is also used; see 12 fan in, page 21.) It is not necessary to restore the CM parameters, as these are also held on the CPU and restored from there.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TITLE: PASS-ON NETWORK DATA FROM CONTROLLER TO CM AND RESTORE PATHS FOR EXCHANGE JUMP

PRODUCT: ECS COUPLER AND CEJ/MEJ
SIZE C | DRAWING NO. 60246600 | REV. Y
SHEET | PAGE 4-33

Standard Option 10104 (CEJ/MEJ) makes PPU exchange jumps (MDJ) conditional and allows one of two starting addresses for Central Processor exchange jumps (CEJ). The condition determining the execution of a CEJ or MEJ instruction is the status of the Monitor Flag (See Table 1).

TABLE 1. EXCHANGE INSTRUCTION DIFFERENCES

INSTRUCTION	CONDITIONAL/ UNCONDITIONAL	OPERATIONAL DIFFERENCES Effect on Monitor Flag Bit	Location of Starting Address for Exchange
261 (Peripheral Processor Monitor Exchange Jump)	Conditional (occurs only if monitor flag is clear; passes is flag is set)	Sets Flag	Peripheral Processor A register.
013 (Central Exchange Jump) with monitor flag bit set.	Unconditional	Sets Flag	Central Processor Monitor Address Register
013 (Central Exchange Jump) with monitor flag bit set.	Unconditional	Clears Flag	Address formed by K + (Bj)

CONDITIONS AFFECTING MONITOR FLAG

Monitor Flag set by: Monitor Control FF set - T85
cleared by: Monitor Control FF clear - T85

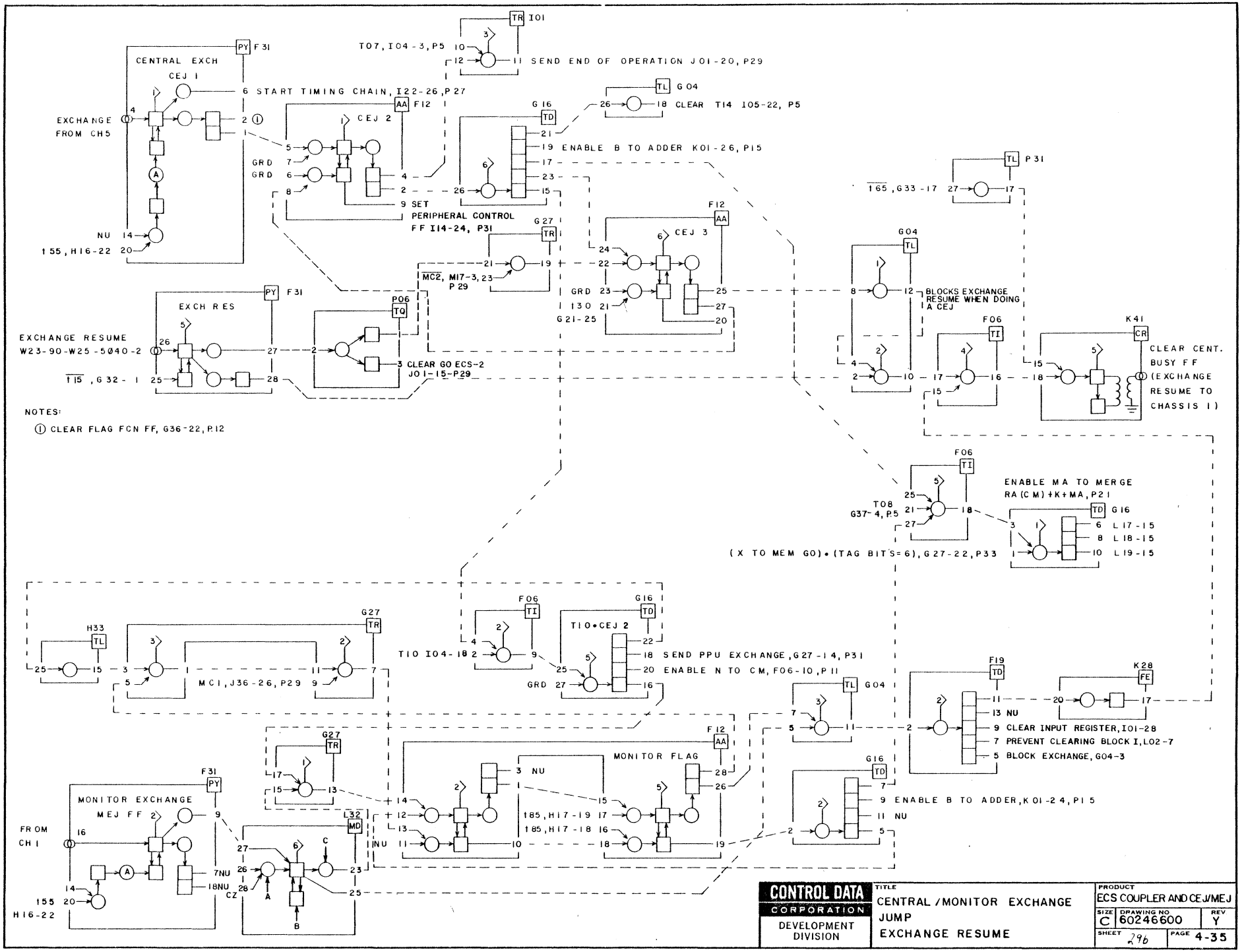
Monitor Control FF set by: Monitor Flag Clear - (T10 - CEJ 2) + (MEJ)
cleared by: Monitor Flag set - (MC) + (T10 - CEJ2)
(Note that MEJ cannot clear Monitor Flag)

CEJ INSTRUCTION SEQUENCE

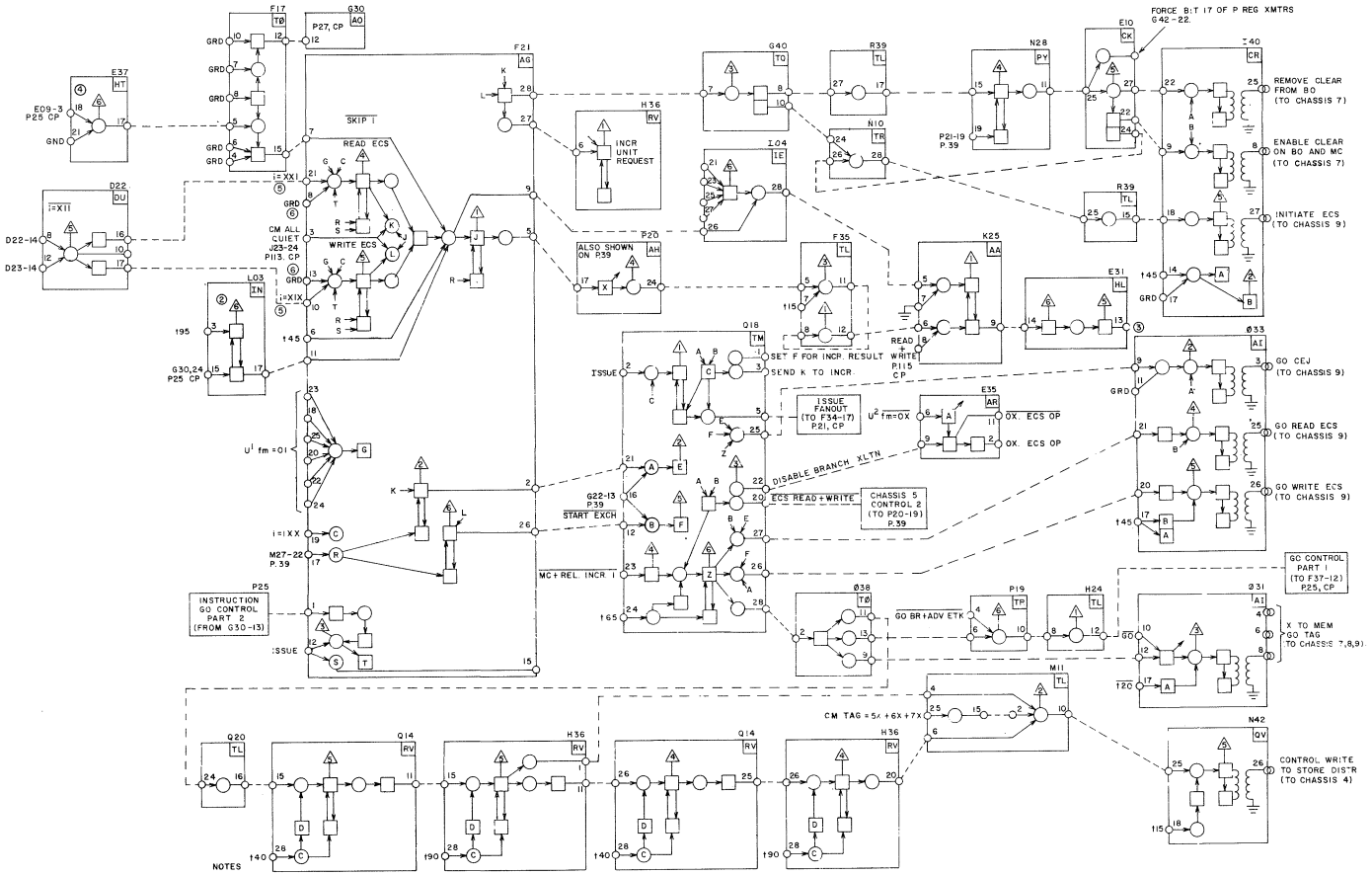
1) A CEJ instruction is issued from Chassis 5.
2) Bj + K computed by Incremented 1, results are sent to Coupler's B register (enter B, T05, P. 5)
3) Select starting address, (MA) or (B) depending on the status of tne Monitor Flag. (See Table 1).
4) Send starting address at T08 (P. 5) via adder to N and then to chassis 5.

MEJ INSTRUCTION SEQUENCE

1) If the Monitor Flag is clear enable (MA) at T08 (P. 5) via adder to N and than to chassis 5.
2) If the Monitor Flag is set, MEJ passes.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL / MONITOR EXCHANGE JUMP EXCHANGE RESUME	PRODUCT ECS COUPLER AND CEJ/MEJ	
		SIZE C	DRAWING NO. 60246600
		REV Y	
		SHEET 296	PAGE 4-35



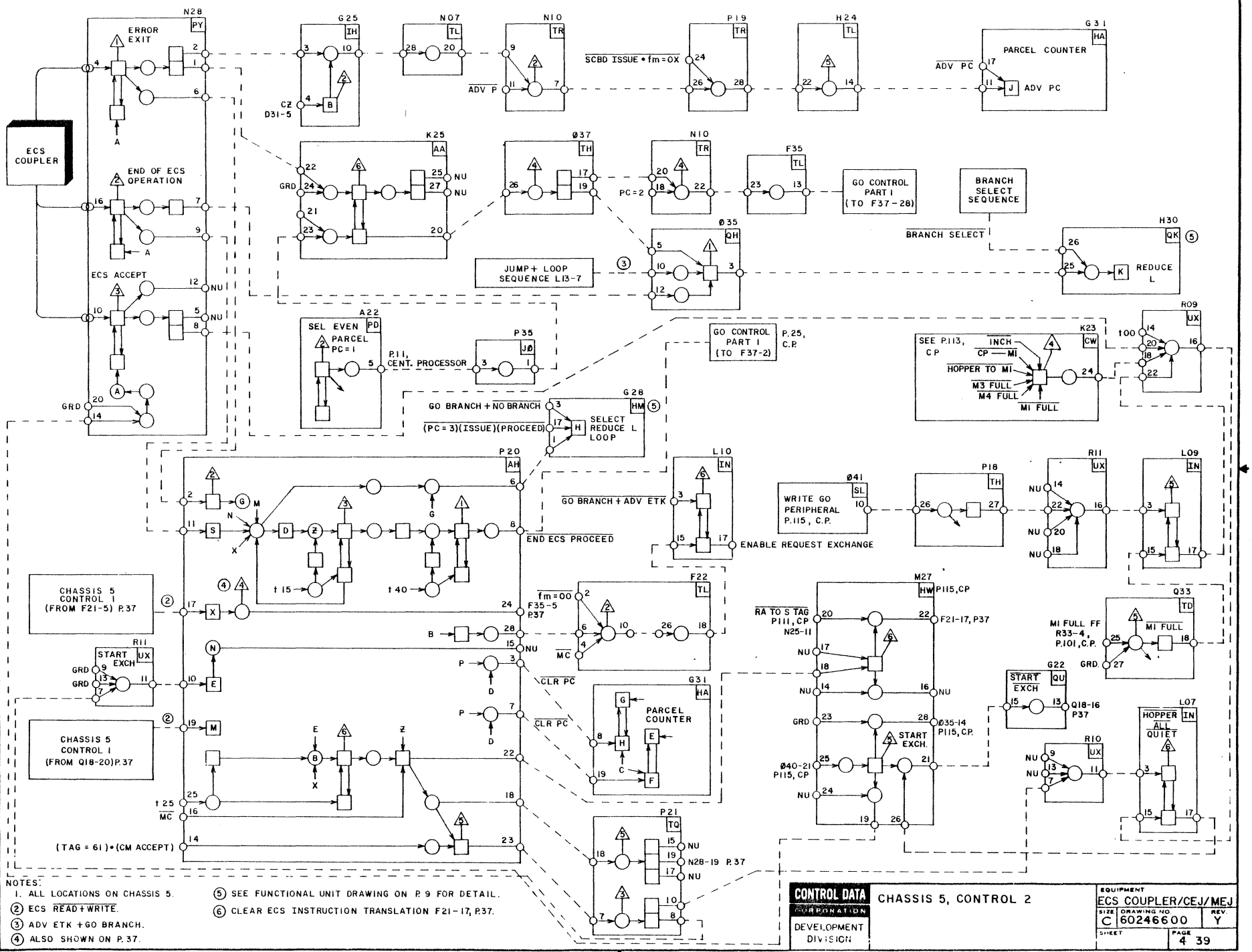
REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP

CONTROL DATA CORPORATION
ARDEN HILLS OPERATIONS

CHASSIS 5, CONTROL I

CODE IDENT		DWG NO	REV
34010	D	60246600	W
		SHEET	137



NOTES:

1. ALL LOCATIONS ON CHASSIS 5.
2. ECS READ+WRITE.
3. ADV ETK +GO BRANCH.
4. ALSO SHOWN ON P. 37.
5. SEE FUNCTIONAL UNIT DRAWING ON P. 9 FOR DETAIL.
6. CLEAR ECS INSTRUCTION TRANSLATION F21-17, P.37.

CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

CHASSIS 5, CONTROL 2

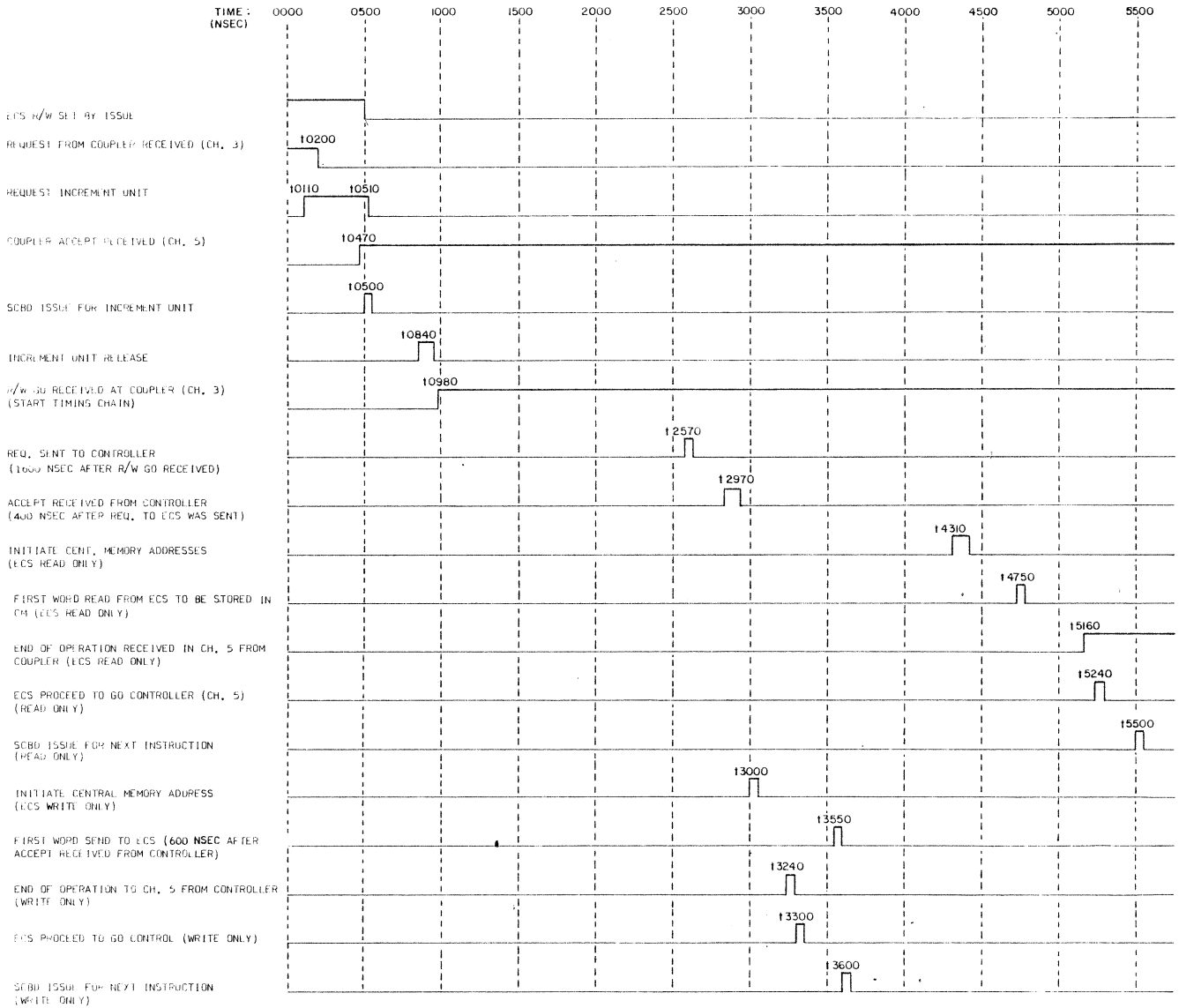
EQUIPMENT: ECS COUPLER/CEJ/MEJ
SIZE C | DRAWING NO. 60246600 | REV. Y
SHEET | PAGE 4 39

6600 ECS TIMING

Duration (NSEC)	Assuming no PPU Conflicts:
400	(Read/Write) From Issue setting ECS Read until accept is received at Chassis 5.
500	(Read/Write) From Accept received at Chassis 5 until Go Read is received at the Coupler.
1600	(Read/Write) From Go Read received at Coupler until Request is sent to ECS.

Duration (NSEC)	Assuming no Controller Channel or Bank Conflicts:
400	(Read/Write) From Sending Request to ECS until an ECS Accept is received at the Coupler.
2100	(Read only) From ECS Accept received at the Coupler until an End of Operation is received at Chassis 5 (+100 nsec for each word).
180	(Write only) From ECS Accept received at Coupler until End of Operation is received at Chassis 5 (+100 nsec for each word)

100	(Read/Write) From End of Operation received at Chassis 5 until ECS Proceed.
300	(Read/Write) From ECS Proceed until SCBD issue for next instruction.



CONTROL DATA CORPORATION
DEVELOPMENT DIVISION

TIMING DIAGRAM

EQUIPMENT 6600-D ECS
SIZE C | DRAWING NO 60246600 | REV C
SHEET | PAGE 4-41

PART 5

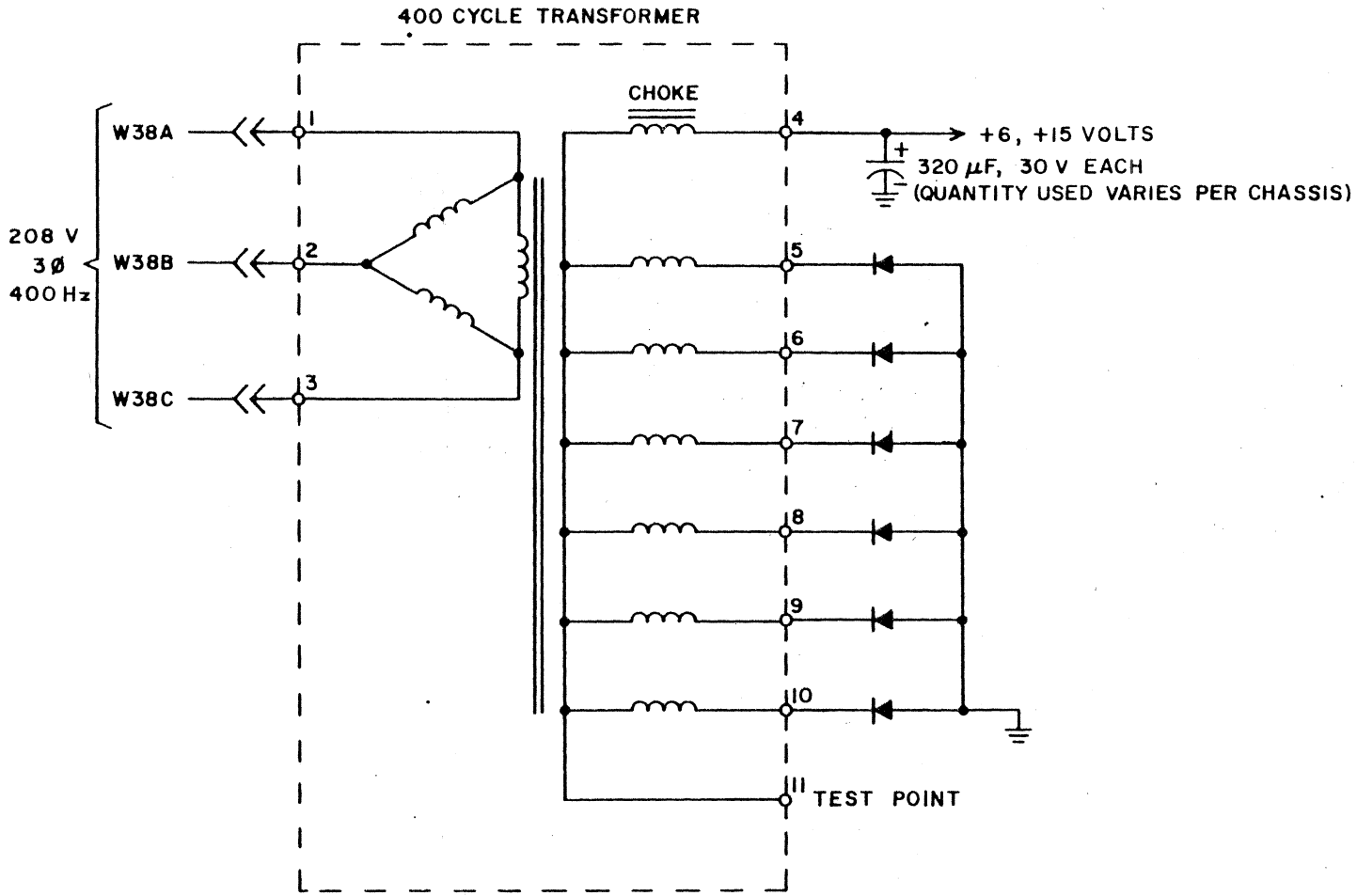
POWER WIRING

PART 5

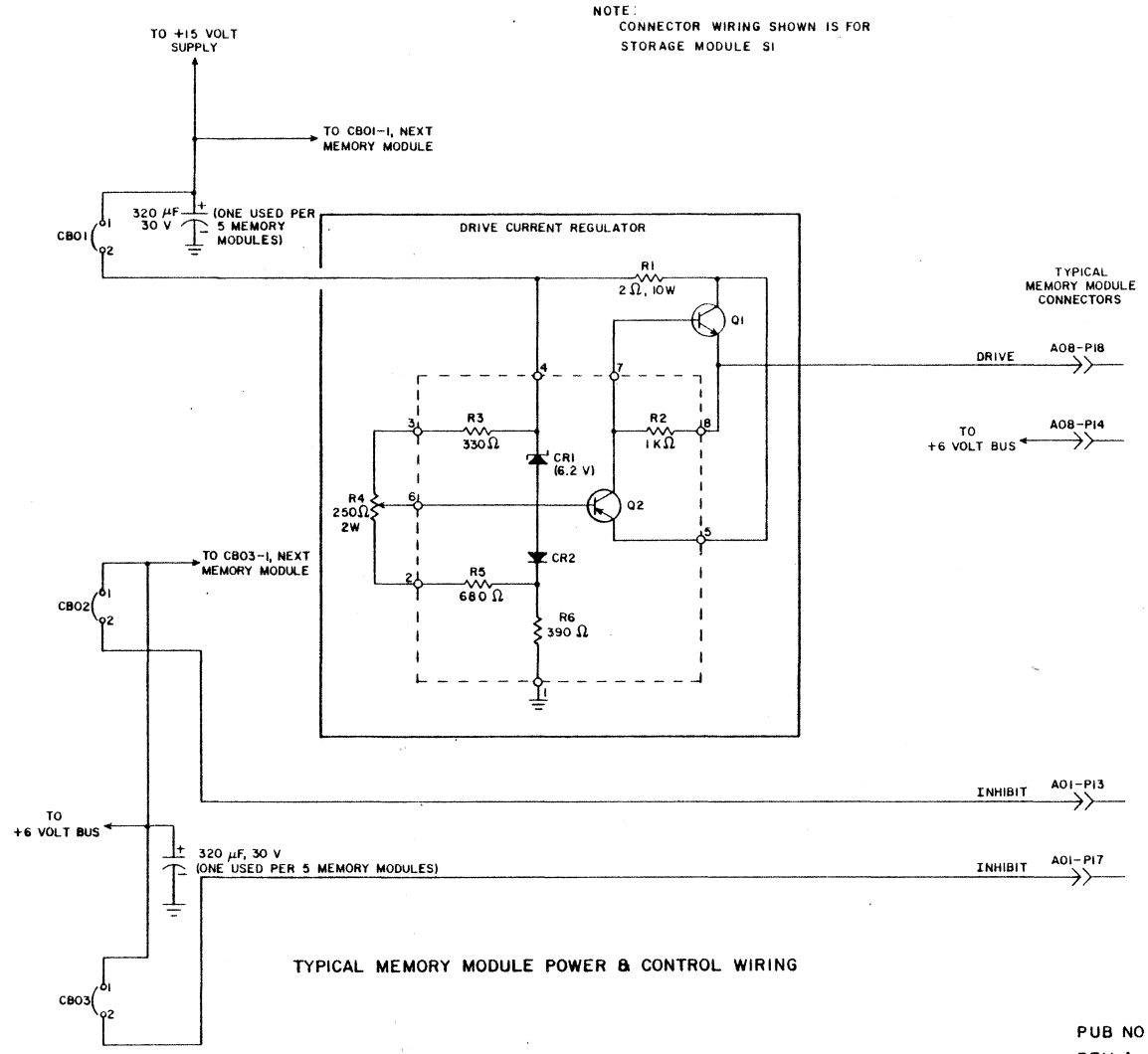
POWER WIRING

CONTENTS

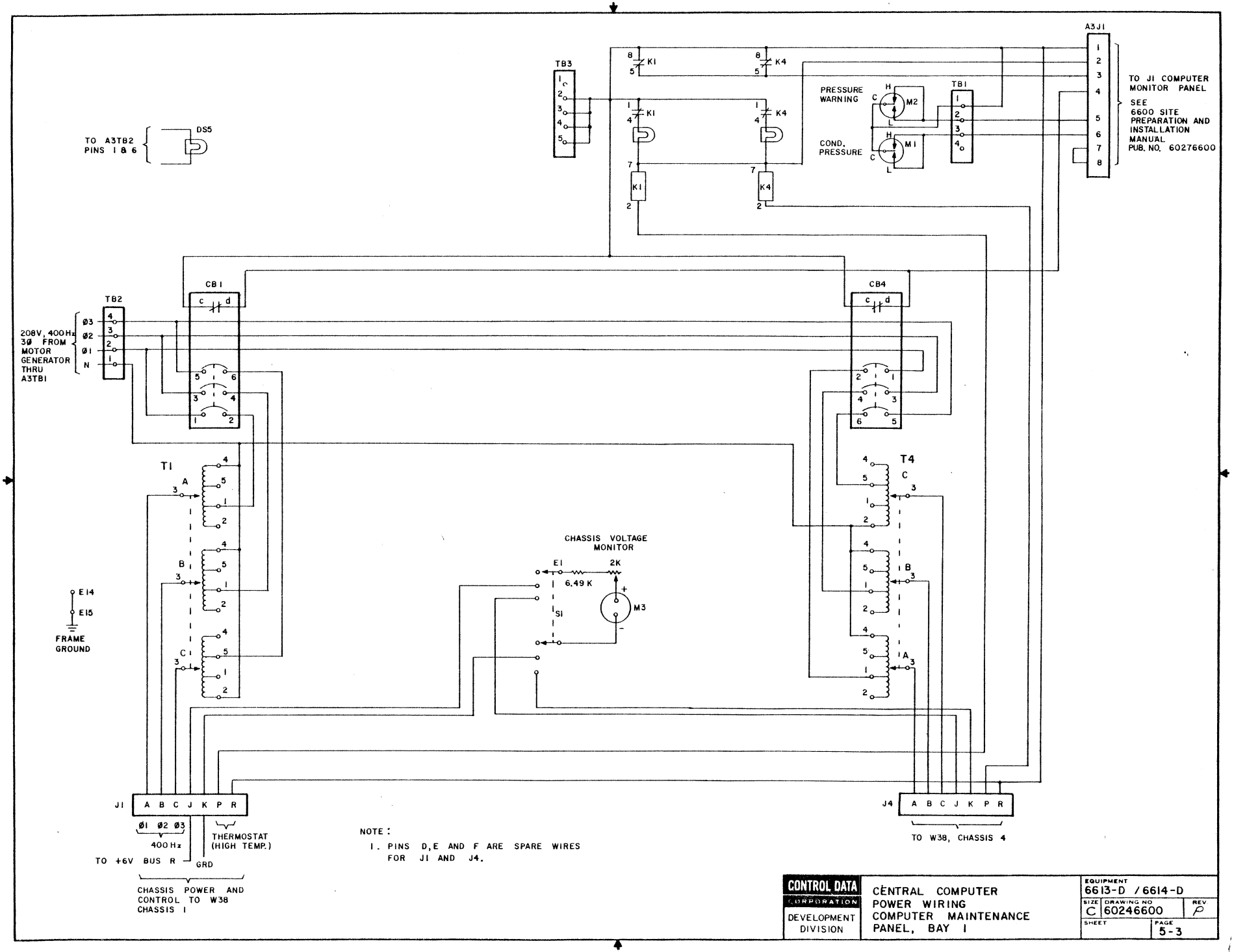
Page	
5-1	Typical Power Supply Configurations
5-2	Typical Memory Module Power and Control Wiring
5-3	Power Wiring, Maintenance Panel, Bay 1
5-5	Power Wiring, Maintenance Panel, Bays 2, 3, 4
5-7	Power Wiring, Condenser Unit and Cabinet
5-9	Power Wiring, Chassis 1
5-13	Power Wiring, Even Logic Chassis
5-13	Power Wiring, Odd Logic Chassis
5-15	Power Wiring, Even Memory Chassis
5-17	Power Wiring, Odd Memory Chassis
5-19	Electrical Interference Grounding



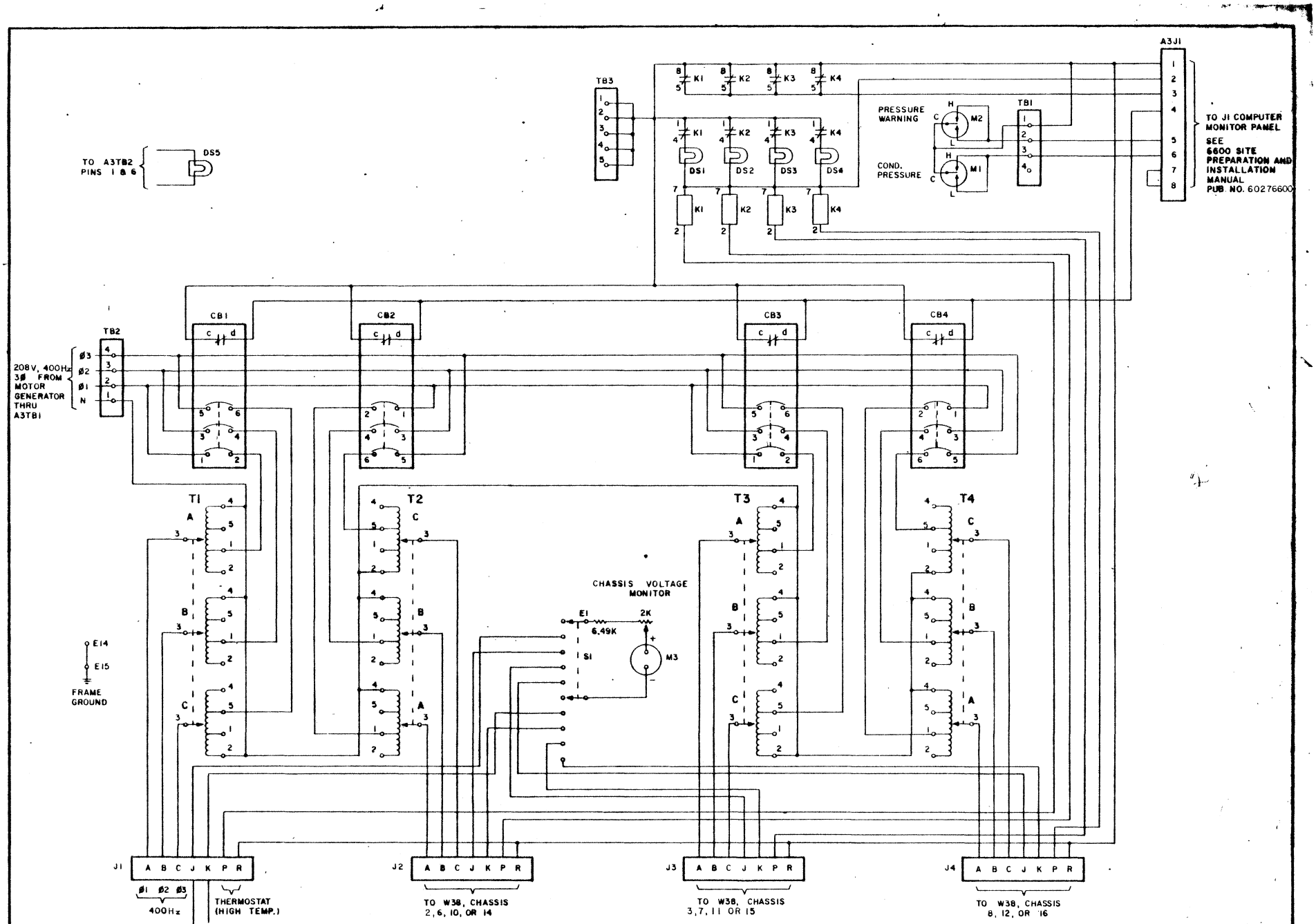
TYPICAL 6 OR 15 VOLT
POWER SUPPLY



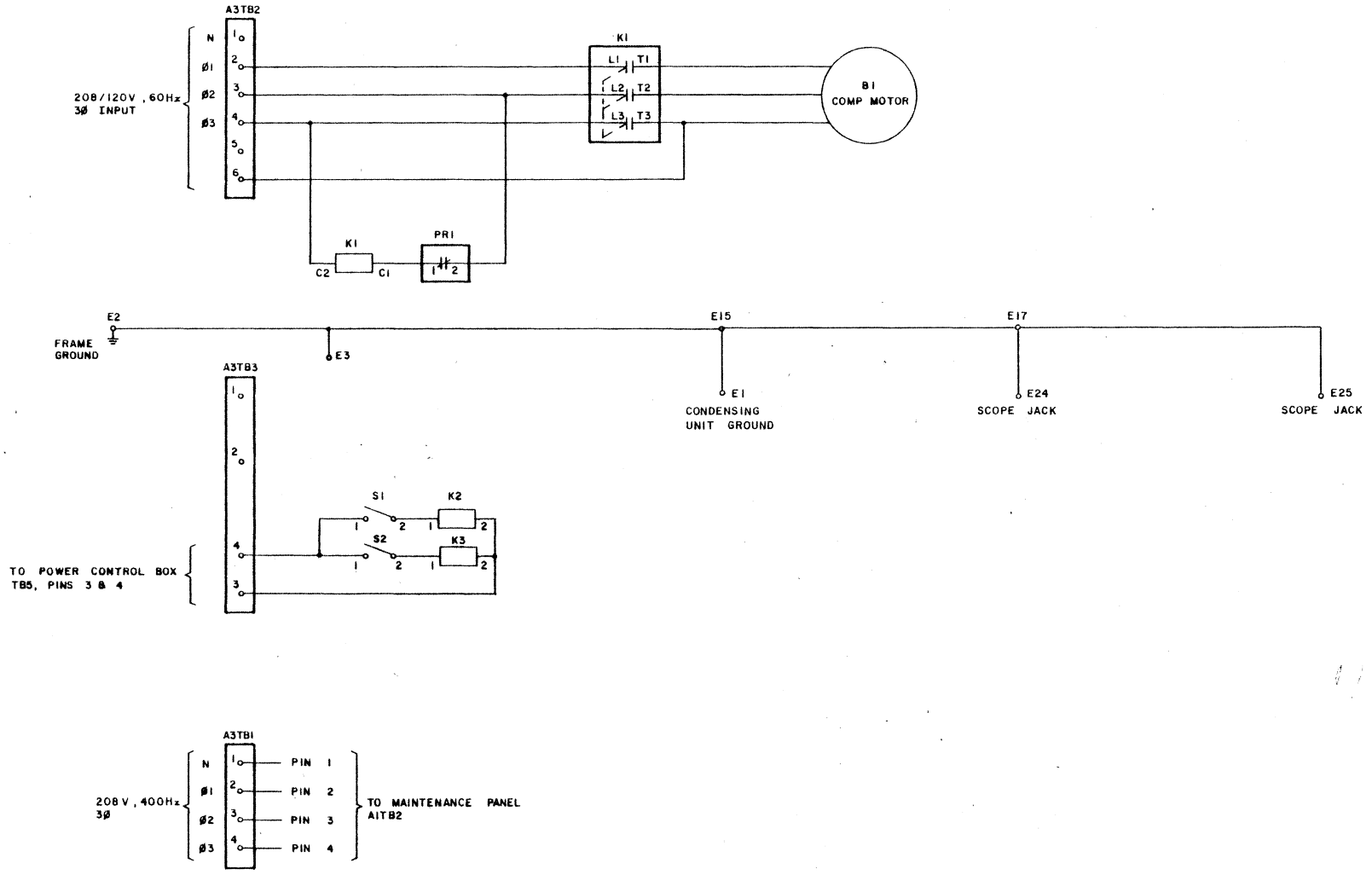
TYPICAL MEMORY MODULE POWER & CONTROL WIRING



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	CENTRAL COMPUTER POWER WIRING COMPUTER MAINTENANCE PANEL, BAY 1	EQUIPMENT 6613-D / 6614-D SIZE C · DRAWING NO 60246600 · REV P SHEET · PAGE 5-3

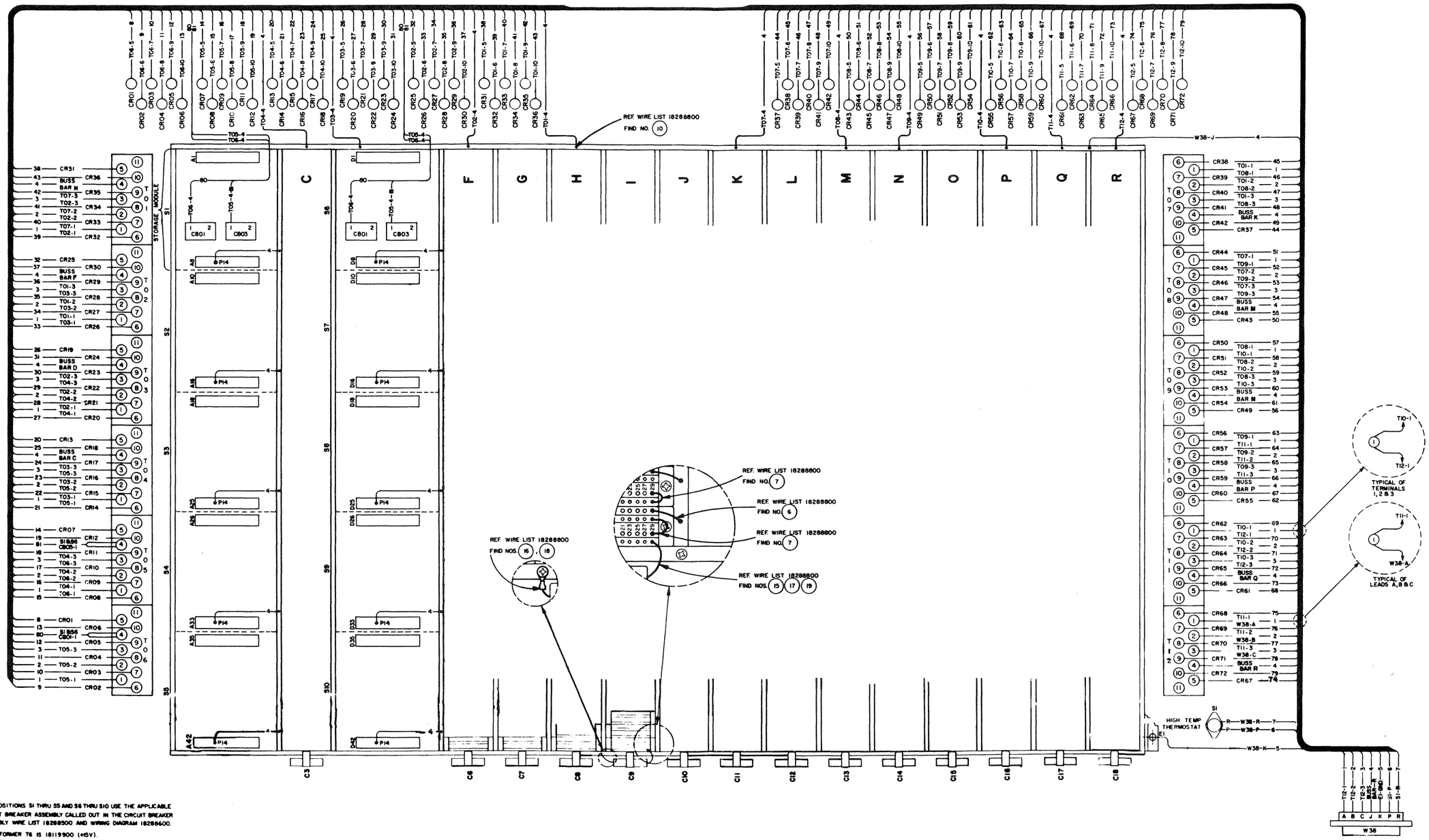


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CENTRAL COMPUTER POWER WIRING COMPUTER MAINTENANCE PANEL, BAYS 2,3 AND 4	PRODUCT 6613-D, 6614-D	
		SIZE C	DRAWING NO. 60246600
		REV. P	
		SHEET 276	PAGE 5-5



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE CONDENSER UNIT & CABINET POWER WIRING	PRODUCT 6613-D, 6614D	
		SIZE C	DRAWING NO. 60246600
		REV. A	
		SHEET 277	PAGE 5-7

ENG. DWG. NO.
18289300 REV. A

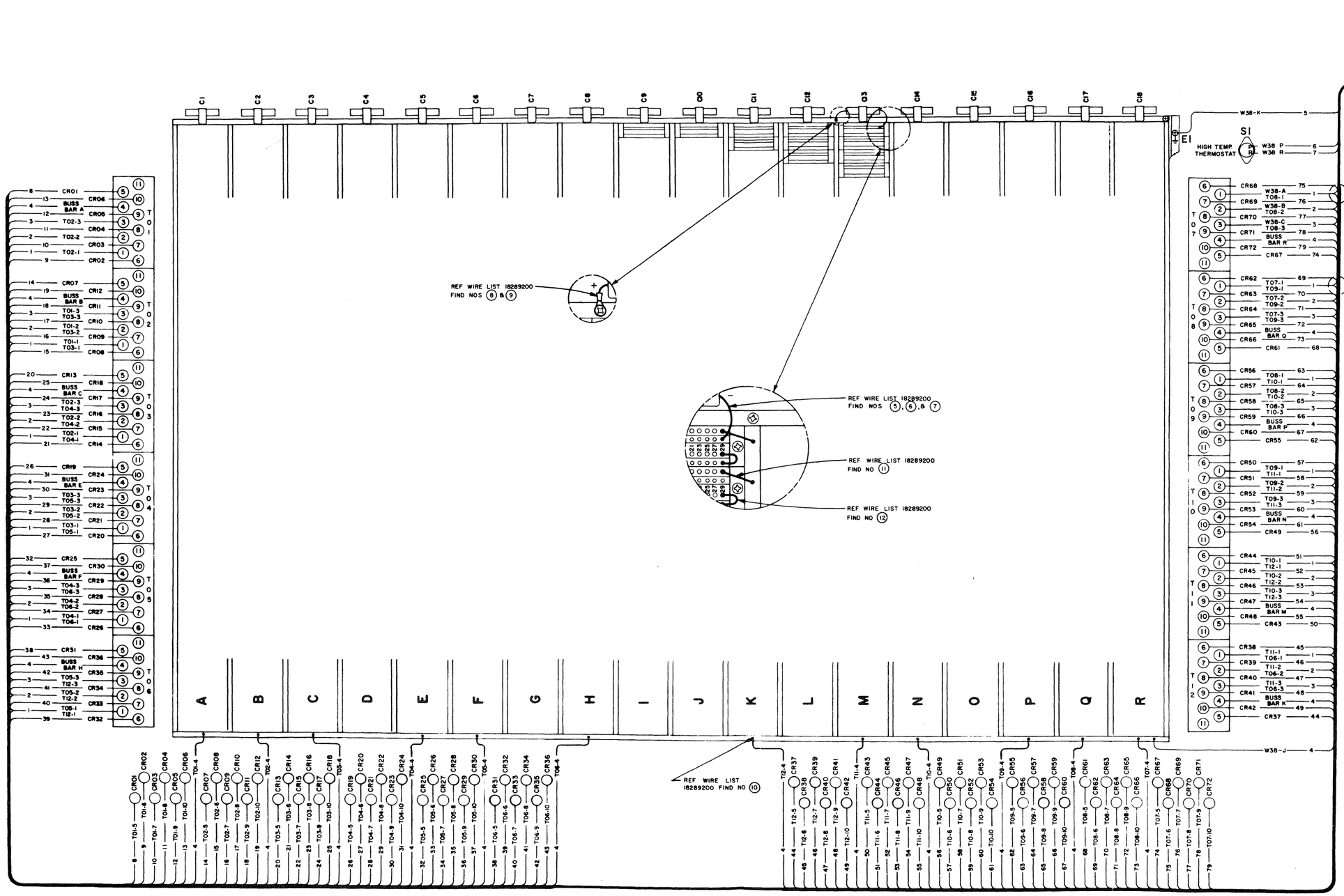


NOTES:

1. FOR POSITIONS S1 THRU S5 AND S6 THRU S10 USE THE APPLICABLE CIRCUIT BREAKER ASSEMBLY CALLED OUT IN THE CIRCUIT BREAKER ASSEMBLY WIRE LIST 18288500 AND WIRING DIAGRAM 18286600.
2. TRANSFORMER T6 IS 18119900 (415V).
   TRANSFORMER T01 THRU T05 AND T07 THRU T12 ARE 97010100 (46V).
3. REFERENCE DOCUMENTS
   A. 18288800 — WIRE LIST
   B. 60246600, 60119300 — ELECTRICAL SCHEMATIC
   C. MECHANICAL ASSEMBLIES:

SYSTEM	CHASSIS NO.	DRAWING NO.
6414 / 6415 /6416	1	18312400
6613 / 6614	1	18346200

PERIPH & CONTROL PROCESSOR 6613-D, 6614-D
POWER WIRING DIAGRAM 60246600 A
CHASSIS 1 5-9



NOTE

1. REFERENCE DOCUMENTS:
   A. WIRE LIST — 18289200
   B. ELECTRICAL SCHEMATIC — 60146100, 60119300
2. AS SHOWN THIS DIAGRAM INDICATES A FULL CHASSIS. FOR CERTAIN APPLICATIONS THE BUGGIE CONNECTORS IN ROWS G, H, I, J, K, L, M, N, O, P, Q, & R, IN DIFFERENT COMBINATIONS, ARE NOT USED. THE RED AND BLACK POWER JUMPERS AND THE CAPACITORS ATTACHED TO THESE ROWS ARE NOT NEEDED UNDER THESE APPLICATIONS.

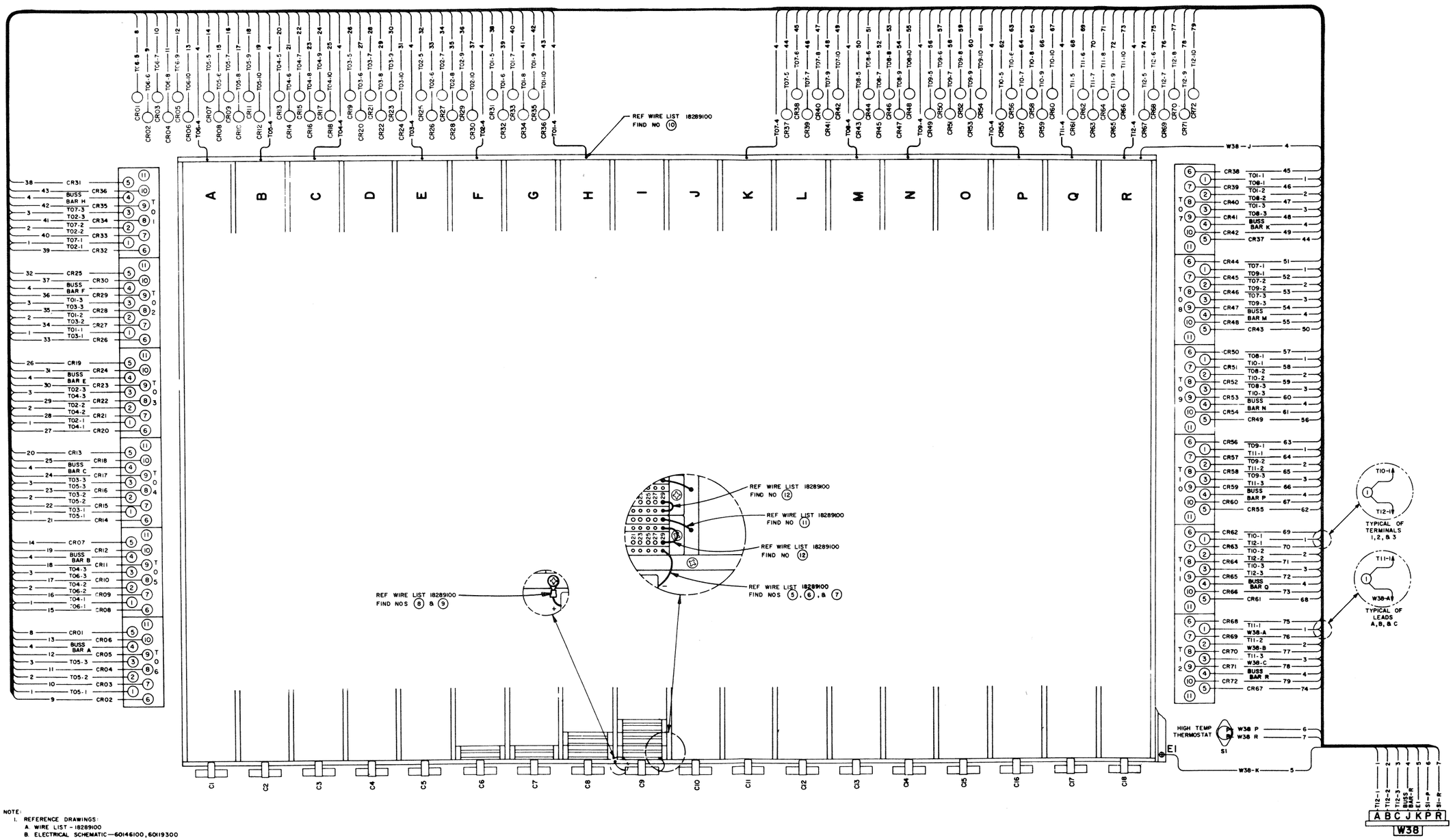
C. MECHANICAL ASSEMBLIES:

SYSTEM	CHASSIS NO.	DRAWING NO.
6414/6415	2	18312300
6414/6415	8	18320700
6416	4	18320800
6613/6614	2	18346400
6613/6614	6	18347200
6613/6614	8	18347600
6613/6614	12	18348200

POWER WIRING DIAGRAM
EVEN LOGIC CHASSIS

6613-D, 6614-D
60246600 A

ENG. DWG. NO.
18289600 REV. A



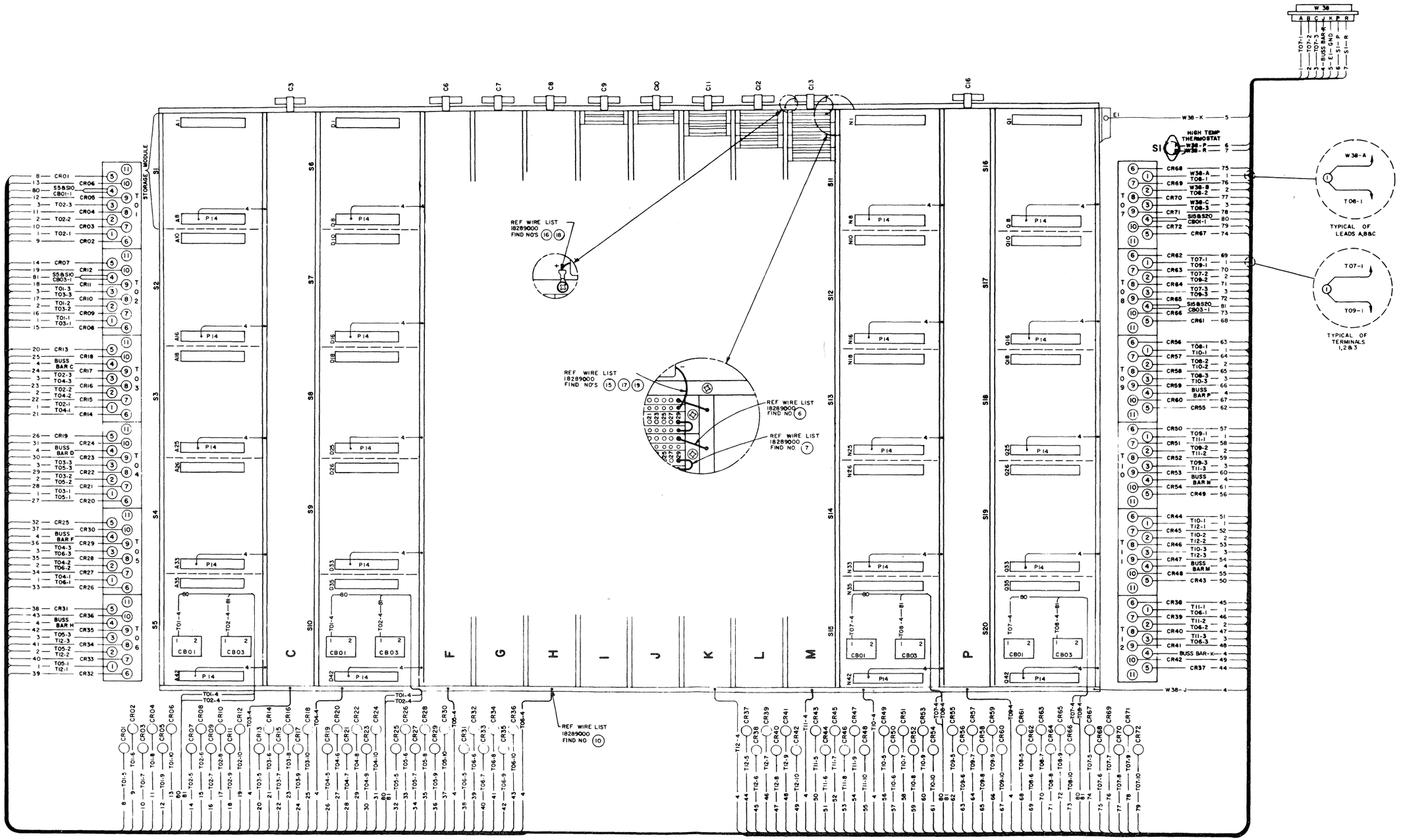
NOTE:
1. REFERENCE DRAWINGS:
   A. WIRE LIST - 18289100
   B. ELECTRICAL SCHEMATIC — 60146100, 60119300
   C. MECHANICAL ASSEMBLIES:

SYSTEM	CHASSIS NO.	DRAWING NO.
6613	5	18347000
6613/6614	7	18347400
6614	5	18350000

POWER WIRING DIAGRAM
ODD LOGIC CHASSIS

6613-D, 6614-D
60246600 **A**

ENG. DWG. NO.
18289500 REV. B



NOTES:

1. FOR POSITION S1 THRU S5, S6 THRU S10, S11 THRU S15, AND S16 THRU S20 USE THE APPLICABLE CIRCUIT BREAKER ASSEMBLY CALLED OUT IN THE CIRCUIT BREAKER ASSEMBLY WIRE LIST 18288500 AND THE WIRING DIAGRAM 18288600.
2. TRANSFORMER T01 AND T07 ARE 18119900 (+ 15V)
   TRANSFORMER T02 THRU T06 AND T08 THRU T12 ARE 97010100 (+6V)
3. REFERENCE DOCUMENTS:
   A18289000 – WIRELIST
   B60146100, 60119300 – ELECTRICAL SCHEMATIC
4. AS SHOWN THIS DIAGRAM INDICATES A FULL CHASSIS. FOR CERTAIN APPLICATIONS THE BUGGIE CONNECTORS IN ROWS J, K, & L ARE NOT USED. THE RED AND BLACK POWER JUMPERS AND THE CAPACITORS ATTACHED TO THESE ROWS ARE NOT NEEDED UNDER THESE APPLICATIONS.

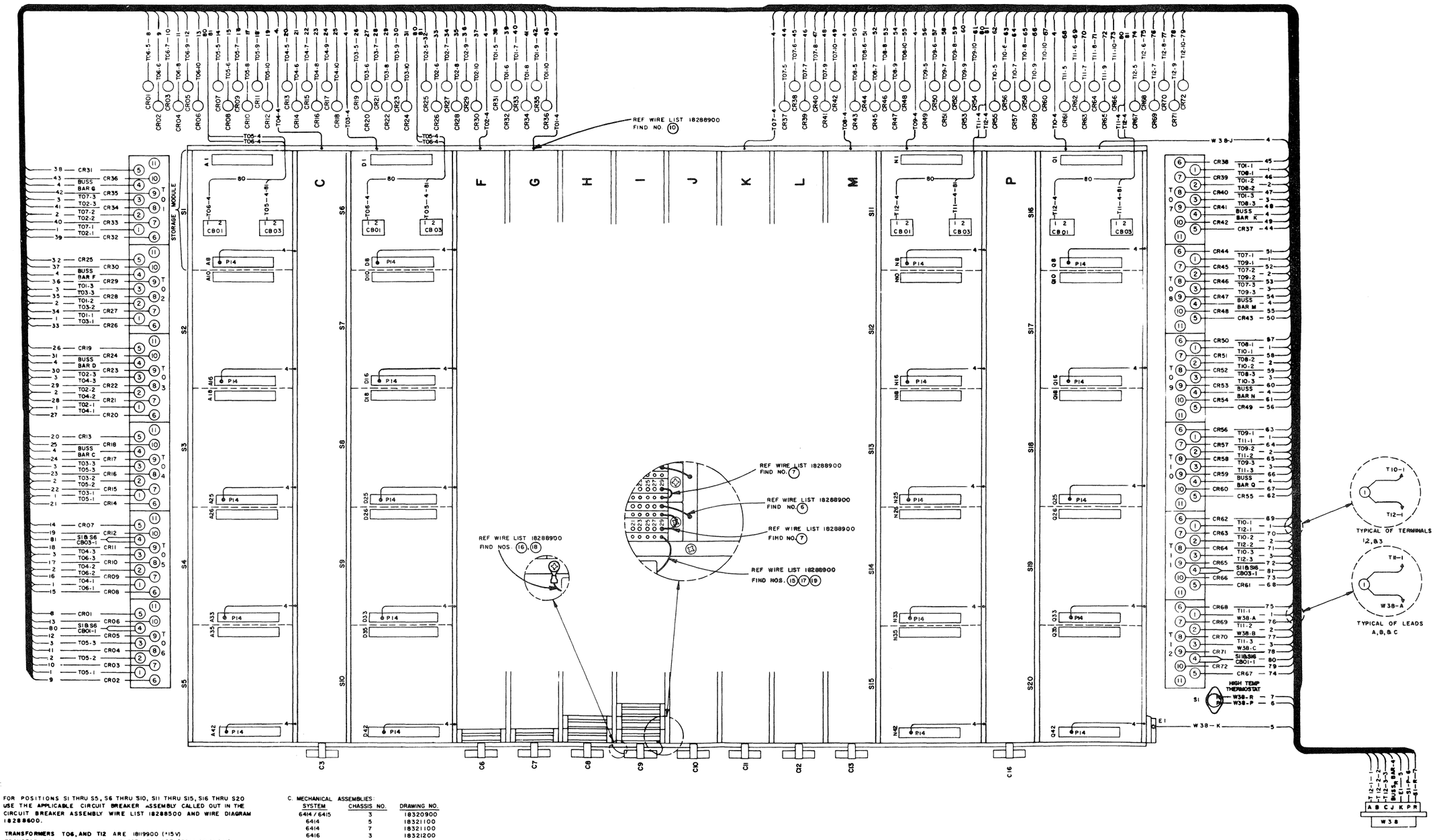
C. MECHANICAL ASSEMBLIES:

SYSTEM	CHASSIS NO.	DRAWING NO.
6414/6415	4	18321000
6613	4	18346800
6613	10	18348000
6613	14	18348600
6613	16	18349000
6614	4	18349400
6614	10	18349800

POWER WIRING DIAGRAM
EVEN MEMORY CHASSIS

6613-D, 6614-D
60246600 A
5-15

ENG. DWG. NO.
18289400 REV. B



NOTES:

1. FOR POSITIONS S1 THRU S5, S6 THRU S10, S11 THRU S15, S16 THRU S20 USE THE APPLICABLE CIRCUIT BREAKER ASSEMBLY CALLED OUT IN THE CIRCUIT BREAKER ASSEMBLY WIRE LIST 18288500 AND WIRE DIAGRAM 18288600.
2. TRANSFORMERS T06, AND T12 ARE 18119900 (+15 V)
   TRANSFORMERS T01, ——T05 AND T07—T11 ARE 97010100 (+6 V)
3. REFERENCE DOCUMENTS
   A WIRE LIST—18288900
   B ELECTRICAL SCHEMATIC—60146100, 60119300
4. AS SHOWN THIS DIAGRAM INDICATES A FULL CHASSIS. FOR CERTAIN APPLICATIONS THE BUGGIE CONNECTORS IN ROWS J, K, & L ARE NOT USED THE RED AND BLACK POWER JUMPERS AND THE CAPACITORS ATTACHED TO THESE ROWS ARE NOT NEEDED UNDER THESE APPLICATIONS.

C. MECHANICAL ASSEMBLIES:

SYSTEM	CHASSIS NO.	DRAWING NO.
6414 / 6415	3	18320900
6414	5	18321100
6414	7	18321100
6416	3	18321200
6613	3	18346600
6613	15	18348800
6614	3	18349200

POWER WIRING DIAGRAM
CDD MEMORY CHASSIS

6613-D, 6614-D
60246600 A

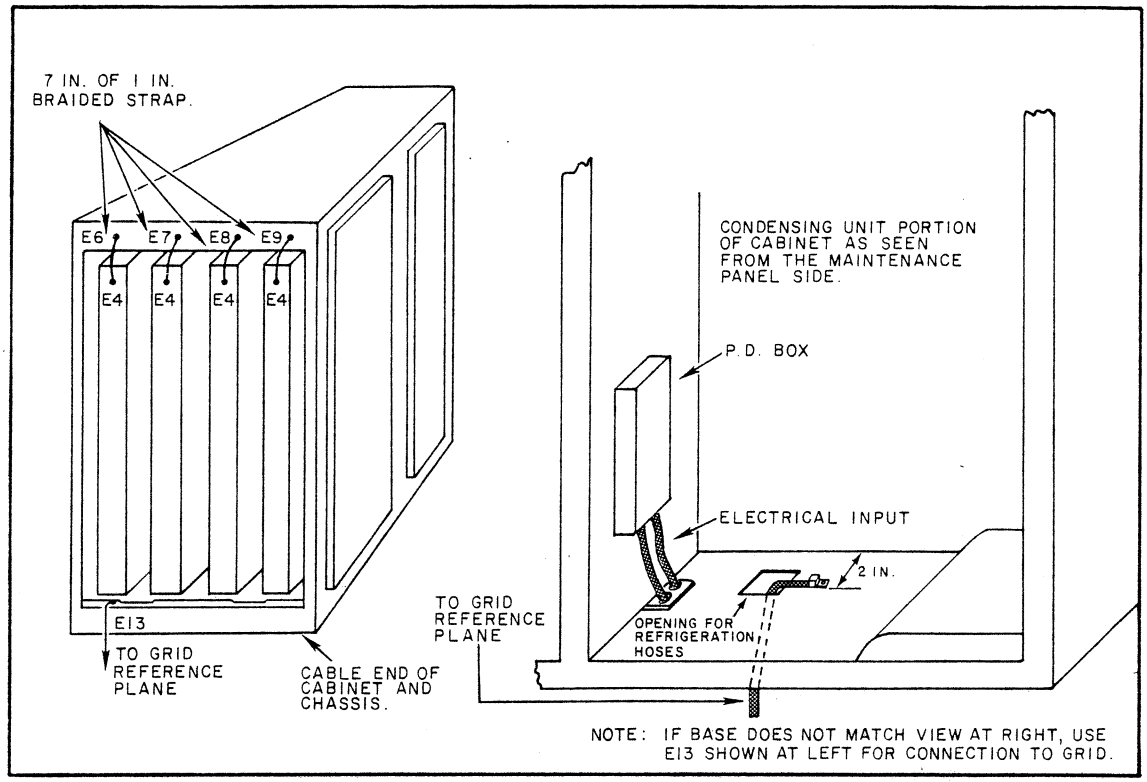


Figure 5-1. Electrical Interference Grounding; Cabinet and Chassis.

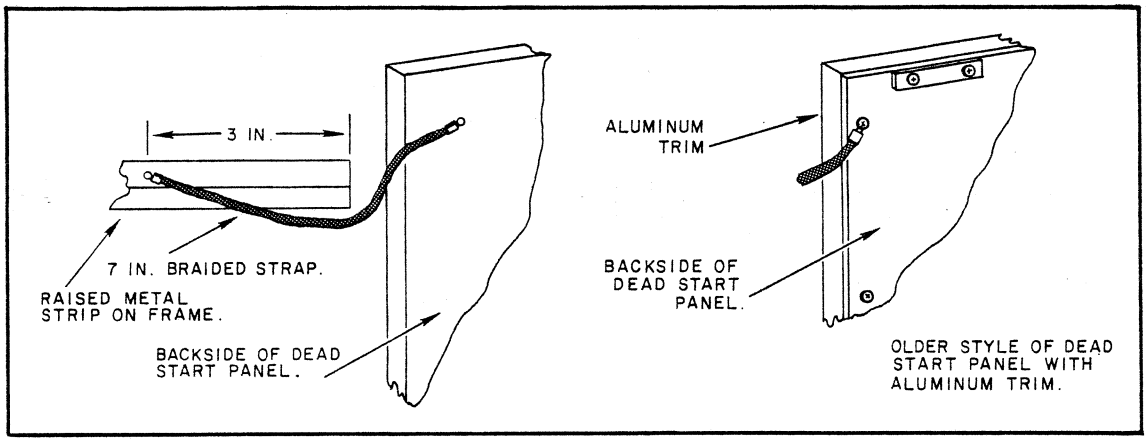


Figure 5-2. Electrical Interference Grounding; Dead Start Panel.

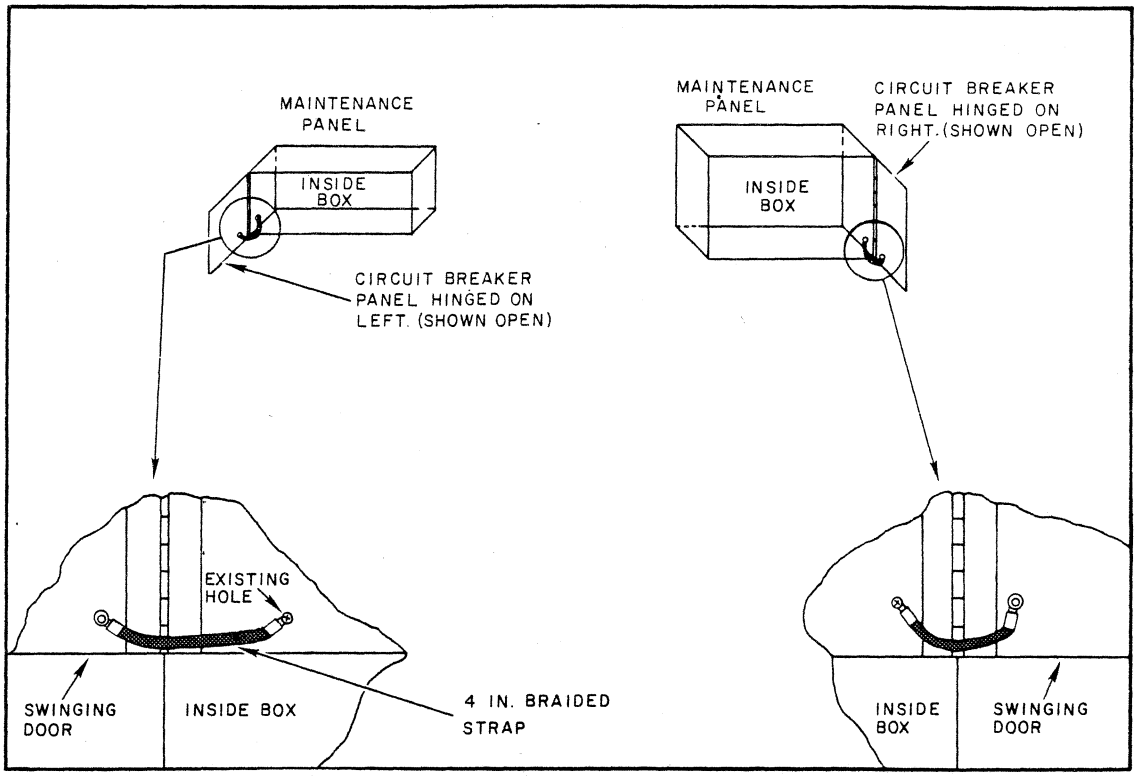


Figure 5-3. Electrical Interference Gounding, Maintenance Panel.

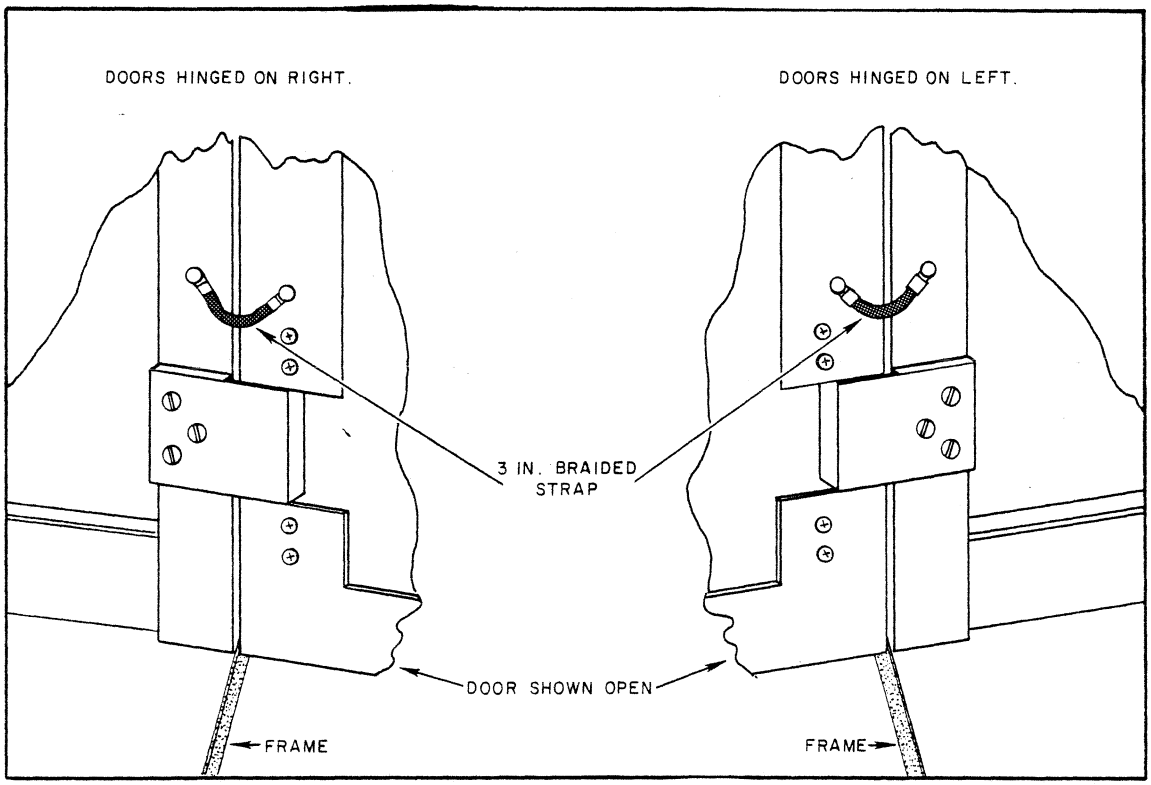


Figure 5-4. Electrical Interference Grounding; Cabinet Doors.

COMMENT SHEET

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Hardware Maintenance Manual

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