Contents

1. Introduction 2
2. Block Diagram 3
3. Functional Diagram 4
4. Description of Signals 5
5. Programming Model 8
   5.1 Register Overview 8
   5.2 Video Palette 10
   5.3 Border Colour Register 11
   5.4 Cursor Palette 11
   5.5 Stereo Image Registers 12
   5.6 Horizontal Cycle Register (HCR) 13
   5.7 Horizontal Sync Width Register (HSWR) 13
   5.8 Horizontal Border Start Register (HBSR) 14
   5.9 Horizontal Display Start Register (HDSR) 14
   5.10 Horizontal Display End Register (HDER) 15
   5.11 Horizontal Border End Register (HBER) 15
   5.12 Horizontal Cursor Start Register (HCSR) 16
   5.13 Horizontal Interface Register (HIR) 16
   5.14 Vertical Cycle Register (VCR) 17
   5.15 Vertical Sync Width Register (VSWR) 17
   5.16 Vertical Border Start Register (VBSR) 17
   5.17 Vertical Display Start Register (VDSR) 18
   5.18 Vertical Display End Register (VDER) 18
   5.19 Vertical Border End Register (VBER) 18
   5.20 Vertical Cursor Start Register (VCSR) 19
   5.21 Vertical Cursor End Register (VCER) 19
   5.22 Sound Frequency Register (SFR) 19
   5.23 Control Register (CR) 20
6. Device Operation 21
   6.1 The DMA Interface 21
      6.1.1 Sound FIFO 21
      6.1.2 Cursor FIFO 21
      6.1.3 Video FIFO 21
      6.1.4 The Video DMA Interface 22
   6.2 Restrictions on Parameters 23
      6.2.1 FIFO Request Pointer Values 23
      6.2.2 Horizontal Sync Pulse Width 25
      6.2.3 Horizontal Front Porch Width 25
      6.2.4 Horizontal Back Porch Width 25
      6.2.5 Vertical Sync Pulse and Porch Width 25
      6.2.6 Horizontal Display Width 26
      6.2.7 Border 26
      6.2.8 Cursor Position 26
   6.3 Display Formats 26
      6.3.1 Screen Modes 26
      6.3.2 Data Display 26
      6.3.3 Logical Data Fields 27
      6.3.4 Physical Data Fields 27
      6.3.5 Cursor Format 27
6.3.6 Border Field 28
6.4 Controlling the Screen 28
6.4.1 Screen On / Off 28
6.4.2 Cursor On / Off 28
6.4.3 Writing to the Palettes & Other Registers 28
6.5 Video DAC Outputs 28
6.6 High Resolution Modes 29
6.7 External Synchronisation and Mixing 30
6.8 Composite Sync. 31
6.9 Interlaced displays. 31
6.10 Sound System 32
7. DC Parameters 34
7.1 Absolute Maximum Ratings 34
7.2 DC Operating Conditions 34
7.3 DC Characteristics 35
8. AC Parameters 36
8.1 AC Operating Conditions 36
8.1.1 Input Clock 36
8.1.2 DMA Writes 36
8.1.3 Register Writes 36
8.2 AC Characteristics 38
8.2.1 Clock - Outputs 38
8.2.2 NIBSEL - Output 38
8.2.3 DMA Acknowledge - Request 40
9. Packaging 41
1. Introduction

The Video Controller (VIDC) accepts video data from memory under DMA control, serialises and parses it through a colour look-up palette, and converts it to analog signals for driving the CRT guns. The chip also controls all the display timing parameters and controls the position and pattern of the cursor sprite. In addition, the VIDC incorporates an exponential DAC and stereo image table for the generation of high quality sound from data in the memory.

The VIDC requests data from the memory when required, and buffers it in one of three FIFOs before using it. Note that the addressing of the data in memory is controlled elsewhere in the system (usually in the Memory Controller, MEMC). Data is requested in blocks of four 32-bit words, allowing efficient use of paged-mode DRAM without locking up the system data bus for long periods.

The VIDC is a highly programmable device, offering a very wide choice of display formats. The pixel rate can be selected in a range between 8 and 24MHz and the data can be serialised to either 8, 4, 2, or 1 bit per pixel. The horizontal timing parameters can be controlled to units of 2 pixels, and the vertical timing parameters can be controlled to units of a raster. The colour look-up palette which drives the three on-chip DACs is 13 bits wide, offering a choice from 4096 colours or an external video source.

Extensive use is made of pipelining throughout the device.

The cursor sprite is 32 pixels wide, and any number of rasters high. It can be positioned anywhere on the screen. Three simultaneous colours (again from a choice of 4096) are supported, and any pixel can be defined as transparent, making possible cursors of many shapes.

The sound system implemented on the device can support up to 8 channels, each with a separate stereo position.

It should be noted that there are two variants of the VIDC, designated VIDC1 and VIDC2. The two devices are identical apart from two aspects: the sense of the video DACs; and the order of the bits in the sound DAC. See sections 6.5 and 6.10.

FEATURES

* pixel rate selectable as 8, 12, 16 or 24MHz
* serialises data to 1, 2, 4, or 8 bits per pixel
* 16 word by 4096 colour look-up palette
* 4-bit DACs for each CRT gun
* highly programmable screen parameters
* border facility
* cursor sprite
* optional interlaced sync. display format
* allowance for external synchronisation
* very high resolution monochrome mode
* high quality stereo sound generation
* fabricated in CMOS for low power

2. Block Diagram
3. Functional Diagram

4. Description of Signals

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CKIN</td>
<td>19</td>
<td>IT</td>
<td>Master clock input (typically 24MHz).</td>
</tr>
<tr>
<td>VIDW</td>
<td>27</td>
<td>IT</td>
<td>Register write strobe. A LOW on this line writer data into one of the VIDC registers. The address of the register is supplied on the upper bits, and the data to be written is on the lower bits of the data bus.</td>
</tr>
<tr>
<td>D[0:31]</td>
<td>44-68,1-7</td>
<td>IT</td>
<td>Data input bus. This bus carries data for register writes, video DMA, Cursor DMA and Sound DMA, according to which type of data strobe is present.</td>
</tr>
<tr>
<td>VIDRQ</td>
<td>23</td>
<td>OC</td>
<td>Video data request. This signal is driven LOW when the VIDC requires another block of 16 bytes of video data (when HSYNC is HIGH) or cursor data (when HSYNC is LOW). It is driven HIGH again by the first valid VIDAK.</td>
</tr>
<tr>
<td>VIDAK</td>
<td>8</td>
<td>IT</td>
<td>Video data acknowledge. A LOW on this signal strobes a data word into the video or cursor FIFO depending on the state of HSYNC when the request was made. Note that a LOW on VIDRQ signifies a request for 4 words of data, and so VIDAK must go LOW 4 times to service each request.</td>
</tr>
<tr>
<td>SNDRQ</td>
<td>24</td>
<td>OC</td>
<td>Sound data request. This signal is driven LOW when the VIDC requires another block of 16 bytes of sound data. It is driven HIGH again by the first valid SNDAK.</td>
</tr>
<tr>
<td>SNDAK</td>
<td>9</td>
<td>IT</td>
<td>Sound data acknowledge. A LOW on this signal strobes a data word into the sound FIFO. Note that a LOW on SNDRQ signifies a request for 4 words of data, and so SNDAK must go LOW 4 times to service each request.</td>
</tr>
<tr>
<td>FLYBK</td>
<td>22</td>
<td>OC</td>
<td>Vertical flyback. This signal is driven HIGH when the display is in vertical flyback. Specifically, it is set HIGH at the start of the first raster which is not display data, though may be border, (at the bottom of the screen), and is cleared down at the start of the first raster which is display data (at the top of the screen).</td>
</tr>
<tr>
<td>SINK</td>
<td>20</td>
<td>IT</td>
<td>External Synchronisation pulse. A HIGH on this signal resets the vertical timing counter, and if interlaced display format is being used, the odd field is selected. The horizontal timing counter, and all other registers, are unaffected by this signal.</td>
</tr>
<tr>
<td>HI</td>
<td>21</td>
<td>OC</td>
<td>Horizontal interface marker. Test pin. When an interlaced display format is selected this signal is driven LOW half way along, and stays LOW until the end, of each raster.</td>
</tr>
<tr>
<td>SD[0:3]</td>
<td>37-34</td>
<td>OC</td>
<td>Multiplexed sound data output. Test pins. These pins are used for testing the digital data paths through the chip, and should be used in conjunction with test mode 3 and NIBSEL. For more information on test mode 3, refer to the control register, section 5.23.</td>
</tr>
</tbody>
</table>
NIBSEL 33 IT Sound data output selector. Test pin. When this signal is LOW, the sound data bus port outputs the inverse of the green DAC data, or the low nibble of the sound data. When NIBSEL is HIGH, the sound data bus port outputs the inverse of the blue DAC data, or the high nibble of the sound data.

L/R 17 OT Left / Right output. Test pin. This signal is driven LOW when the sound output is steered to the left output port, and is HIGH when the sound output is steered to the right output port. In test mode 5, the pin changes its function, and outputs the sound sampling clock instead.

RVDAC 43 IA Video DAC reference current. A current must be fed into this pin to set the output current of the video DACs. The full scale output current is 15 times this current. In most applications a resistor from VDD to this pin is sufficient to set the current.

ROUT 39 OA Red analog output. The output to the CRT guns is a current sink. On VIDC1 “black” is defined as 15 times the reference current, and on VIDC2, “black” is defined as zero current. Level shifting and buffering is normally required to drive the lines to the CRT.

GOUT 40 OA Green analog output. As for ROUT

ROUT 41 OA Blue analog output. As for ROUT

SUP 28 OC Supremacy output signal. This signal is used to control a multiplexer between the output of VIDC and an external source when video mixing is required. If bit 12 of the video or cursor palette for any logical colour is set, SUP is driven LOW when that logical colour is displayed. In this way any logical colour can be defined as being supreme or not, on a pixel-by-pixel basis.

HSYNC 25 OC Horizontal synchronisation pulse. This signal is required by some monitors. It is also used by the MEMC to discriminate between cursor and video data requests. The pulse is active LOW, and the pulse width is programmable in units of 2 pixels, though there are certain system-related restrictions. See section 6.2.

V/CSYNC 26 OC Vertical / composite synchronisation pulse. Depending on bit 7 in the control register, this pin can be either the vertical sync. pulse, or a form of composite sync. pulse. The vertical sync. pulse width is programmable in units of a raster and, if selected, is active LOW. The composite sync. pulse is the exclusive-NOR of HSYNC and VSYNC.

VED[0:3] 32-29 OC Video external data output. The inverse of the 4 bits of data which are fed to the red DAC are output on these pins. With an external serialiser, this data can be used to produce very high resolution monochrome displays.

RSDAC 12 IA Sound DAC reference current. A current must be fed into this pin to set the output current of the sound DAC. The full scale output current is approximately 32 times this current. In most applications a resistor from VDD to this pin is sufficient to set the current.

LCH+ 13 OA Left channel positive sound output. The sound output is in the form of a current sink which is switched to one of 4 pins (pins 13 - 16). The left channel signal is produced by externally integrating and subtracting the two signals LCH+ and LCH-. Similarly, the right channel signal is produced by externally integrating and subtracting the two signals RCH+ and RCH-.

RCH+ 14 OA Right channel positive sound output. See description of pin 13.

LCH- 15 OA Left channel negative sound output. See description of pin 13.

RCH- 16 OA Right channel negative sound output. See description of pin 13.

VSSd 18 PWR Digital ground. This pin is the ground supply to the digital circuits in the device.

VSSs 10 PWR Sound ground. This pin is the ground supply to the sound DAC in the device. It must be connected to the pin VSSd outside the chip.

VSSv 42 PWR Video ground. This pin is the ground supply to the video DACs in the device. It must be connected to the pin VSSd outside the chip.

VDDD 38 PWR Digital supply. This pin is the positive supply to the digital circuits in the device.

VDDS 11 PWR Sound supply. This pin is the positive supply to the sound DAC in the device. It must be at the same potential as VDDd, and should be decoupled to VSSs. Note that the sound reference current input and the sound analog output currents are all referenced to this signal.

Key to Signal Types:

<table>
<thead>
<tr>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IT</td>
<td>TTL Compatible Input</td>
</tr>
<tr>
<td>OC</td>
<td>CMOS Level Output</td>
</tr>
<tr>
<td>IA</td>
<td>Analog Input</td>
</tr>
<tr>
<td>OA</td>
<td>Analog Output</td>
</tr>
<tr>
<td>PWR</td>
<td>Supply</td>
</tr>
</tbody>
</table>
5. Programming Model

5.1 Register Overview

Apart from the three 32-bit wide FIFOs (Video, Cursor and Sound), the VIDC contains 46 write-only registers of up to 13 bits each. In all cases the address of the register is contained in the top 6 bits (26:31) of the data field. Bits 25 and 24 are not used. The actual data bits are distributed among the remaining 24 bits of the data field according to the register in question.

Treating bit 24 as the least significant address bit, the register map is shown in Table 1. Note that there are 18 reserved locations. These locations should never be written to as they may actually contain other registers (some of the registers are dual-mapped within the device).

In order to define the display format correctly, eleven registers need to be programmed as shown in the diagram below.

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Video Palette logical colour 0</td>
</tr>
<tr>
<td>04</td>
<td>Video Palette logical colour 1</td>
</tr>
<tr>
<td>08</td>
<td>Video Palette logical colour 2</td>
</tr>
<tr>
<td>0C</td>
<td>Video Palette logical colour 3</td>
</tr>
<tr>
<td>10</td>
<td>Video Palette logical colour 4</td>
</tr>
<tr>
<td>14</td>
<td>Video Palette logical colour 5</td>
</tr>
<tr>
<td>18</td>
<td>Video Palette logical colour 6</td>
</tr>
<tr>
<td>1C</td>
<td>Video Palette logical colour 7</td>
</tr>
<tr>
<td>20</td>
<td>Video Palette logical colour 8</td>
</tr>
<tr>
<td>24</td>
<td>Video Palette logical colour 9</td>
</tr>
<tr>
<td>28</td>
<td>Video Palette logical colour A</td>
</tr>
<tr>
<td>2C</td>
<td>Video Palette logical colour B</td>
</tr>
<tr>
<td>30</td>
<td>Video Palette logical colour C</td>
</tr>
<tr>
<td>34</td>
<td>Video Palette logical colour D</td>
</tr>
<tr>
<td>38</td>
<td>Video Palette logical colour E</td>
</tr>
<tr>
<td>3C</td>
<td>Video Palette logical colour F</td>
</tr>
<tr>
<td>40</td>
<td>Border Colour Register</td>
</tr>
<tr>
<td>44</td>
<td>Cursor Palette logical colour 1</td>
</tr>
<tr>
<td>48</td>
<td>Cursor Palette logical colour 2</td>
</tr>
<tr>
<td>4C</td>
<td>Cursor Palette logical colour 3</td>
</tr>
<tr>
<td>50-5C</td>
<td>reserved</td>
</tr>
<tr>
<td>60</td>
<td>Stereo Image Register 7</td>
</tr>
<tr>
<td>64</td>
<td>Stereo Image Register 0</td>
</tr>
<tr>
<td>68</td>
<td>Stereo Image Register 1</td>
</tr>
<tr>
<td>6C</td>
<td>Stereo Image Register 2</td>
</tr>
<tr>
<td>70</td>
<td>Stereo Image Register 3</td>
</tr>
<tr>
<td>74</td>
<td>Stereo Image Register 4</td>
</tr>
<tr>
<td>78</td>
<td>Stereo Image Register 5</td>
</tr>
<tr>
<td>7C</td>
<td>Stereo Image Register 6</td>
</tr>
<tr>
<td>80</td>
<td>Horizontal Cycle Register</td>
</tr>
<tr>
<td>84</td>
<td>Horizontal Sync Width Register</td>
</tr>
<tr>
<td>88</td>
<td>Horizontal Border Start Register</td>
</tr>
<tr>
<td>90</td>
<td>Horizontal Display Start Register</td>
</tr>
<tr>
<td>94</td>
<td>Horizontal Border End Register</td>
</tr>
<tr>
<td>98</td>
<td>Horizontal Cursor Start Register</td>
</tr>
<tr>
<td>9C</td>
<td>Horizontal Interface Register</td>
</tr>
<tr>
<td>A0</td>
<td>Vertical Cycle Register</td>
</tr>
<tr>
<td>A4</td>
<td>Vertical Sync Width Register</td>
</tr>
<tr>
<td>A8</td>
<td>Vertical Border Start Register</td>
</tr>
<tr>
<td>AC</td>
<td>Vertical Display Start Register</td>
</tr>
<tr>
<td>B0</td>
<td>Vertical Display End Register</td>
</tr>
<tr>
<td>B4</td>
<td>Vertical Border End Register</td>
</tr>
<tr>
<td>BB</td>
<td>Vertical Cursor Start Register</td>
</tr>
<tr>
<td>BC</td>
<td>Vertical Cursor End Register</td>
</tr>
<tr>
<td>C0</td>
<td>Sound Frequency Register</td>
</tr>
<tr>
<td>C4-DC</td>
<td>reserved</td>
</tr>
<tr>
<td>E0</td>
<td>Control Register</td>
</tr>
<tr>
<td>E4-FC</td>
<td>reserved</td>
</tr>
</tbody>
</table>

Table 1: Register Allocation
5.2 Video Palette Logical colours 0-FH : Addresses 00H-3CH

In 1, 2 & 4 bits per pixel mode, data bits D[0:12] define the physical colour corresponding to that logical colour.
D[0:3] define the Red amplitude. D[0] least significant.
D[12] defines the supremacy bit for that colour.

In 8 bits per pixel mode, only 9 bits of the palette are used.

The palette outputs define the least significant bits of each colour.

5.3 Border Colour Register : Address 40H

In all modes this register defines the physical border colour.
D[0:3] define the Red amplitude. D[0] least significant.
D[12] defines the supremacy bit for the border.

5.4 Cursor Palette Logical Colours 1-3 : Addresses 44H-4CH

In all modes these registers define the physical cursor colours corresponding to the logical colours. Note that cursor logical colour 00 is defined as being transparent (ie. no cursor display), and this location is used for the Border Colour Register.
D[0:3] define the Red amplitude. D[0] least significant.
D[12] defines the supremacy bit for that cursor colour.

Dw: These bits come from the palette field.
Lw: These bits come from the logical field.

In 4 and 8 bits per pixel mode, all 16 locations should be programmed.
In 2 bits per pixel mode only colours 0, 1, 2 and 3 need to be programmed.
In 1 bit per pixel mode only colours 0 and 1 need to be programmed.
5.5 Stereo Image Registers, Channels 0-7 : Addresses 60H-7CH

These 8 registers define the stereo image position for each of the 8 possible channels as shown in Table 2.

<table>
<thead>
<tr>
<th>Address (Hex)</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>Stereo Image Register 7</td>
</tr>
<tr>
<td>64</td>
<td>Stereo Image Register 0</td>
</tr>
<tr>
<td>68</td>
<td>Stereo Image Register 1</td>
</tr>
<tr>
<td>6C</td>
<td>Stereo Image Register 2</td>
</tr>
<tr>
<td>70</td>
<td>Stereo Image Register 3</td>
</tr>
<tr>
<td>74</td>
<td>Stereo Image Register 4</td>
</tr>
<tr>
<td>78</td>
<td>Stereo Image Register 5</td>
</tr>
<tr>
<td>7C</td>
<td>Stereo Image Register 6</td>
</tr>
</tbody>
</table>

Table 2: Stereo Image Register Allocation

When only 4 channels are used, registers 4,5,6,7 should be programmed to the same value as registers 0,1,2,3 respectively.

When only 2 channels are used, registers 0,2,4 & 6 pertain to one channel, and so should be programmed to the same value, and registers 1,3,5 & 7 pertain to the other channel.

When only one channel is used, all 8 registers should be programmed to the same value.

The 3-bit value is defined in Table 3.

<table>
<thead>
<tr>
<th>Value</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Undefined</td>
</tr>
<tr>
<td>1</td>
<td>100% left</td>
</tr>
<tr>
<td>2</td>
<td>83% left</td>
</tr>
<tr>
<td>3</td>
<td>67% left</td>
</tr>
<tr>
<td>4</td>
<td>centre</td>
</tr>
<tr>
<td>5</td>
<td>67% right</td>
</tr>
<tr>
<td>6</td>
<td>83% right</td>
</tr>
<tr>
<td>7</td>
<td>100% right</td>
</tr>
</tbody>
</table>

Table 3: Stereo Image Register Values

5.6 Horizontal Cycle Register (HCR) : Address 80H

This register defines the period, in units of 2 pixels, of the horizontal scan, i.e. display time + horizontal retrace time.

If N pixels are required in the horizontal scan period, then value (N-2)/2 should be programmed into the HCR (N must be even).

If interlaced display is selected, N/2 must also be even.

This is a 10 bit register, with bit 14 the least significant.

5.7 Horizontal Sync Width Register (HSWR) : Address 84H

This register defines the width, in units of 2 pixel periods, of the HSYNC pulse.

If N pixels are required in the HSYNC pulse, then value (N-2)/2 should be programmed into the HSWR. (N must be even).

The minimum value programmable may be 0, but system constraints impose a larger minimum value. See section 6.2.

This is a 10 bit register, with bit 14 the least significant.
5.8 Horizontal Border Start Register (HBSR) : Address 88H

![Binary Representation]

This register defines the time, in units of 2 pixel periods, from the start of the HSYNC pulse to the start of the border display.

If M pixels are required in this time, then value (M-1)/2 should be programmed into the HBSR. [M must be odd].

Note that this register must always be programmed, even when a border is not required. If a border is not required, then the value in the HBSR must be such as to start the border in the same place as the display start, i.e. M_{HBSR} = M_{HDSR}.

This is a 10 bit register, with bit 14 the least significant.

5.9 Horizontal Display Start Register (HDSR) : Address 8CH

![Binary Representation]

This register defines the time, in units of 2 pixel periods, from the start of the HSYNC pulse to the start of the video display.

The value programmed here depends on the screen mode in use. If M pixels are required in this time, then:
- in 8 bits per pixel mode, value (M-5)/2 should be programmed into the HDSR. [M must be odd].
- in 4 bits per pixel mode, value (M-7)/2 should be programmed into the HDSR. [M must be odd].
- in 2 bits per pixel mode, value (M-11)/2 should be programmed into the HDSR. [M must be odd].
- in 1 bit per pixel mode, value (M-19)/2 should be programmed into the HDSR. [M must be odd].

This is a 10 bit register, with bit 14 the least significant.

5.10 Horizontal Display End Register (HDER) : Address 90H

![Binary Representation]

This register defines the time, in units of 2 pixel periods, from the start of the HSYNC pulse to the end of the video display. (i.e. the first pixel which is not display).

The value programmed here depends on the screen mode in use. If M pixels are required in this time, then:
- in 8 bits per pixel mode, value (M-5)/2 should be programmed into the HDSR. [M must be odd].
- in 4 bits per pixel mode, value (M-7)/2 should be programmed into the HDSR. [M must be odd].
- in 2 bits per pixel mode, value (M-11)/2 should be programmed into the HDSR. [M must be odd].
- in 1 bit per pixel mode, value (M-19)/2 should be programmed into the HDSR. [M must be odd].

This is a 10 bit register, with bit 14 the least significant.

5.11 Horizontal Border End Register (HBER) : Address 94H

![Binary Representation]

This register defines the time, in units of 2 pixel periods, from the start of the HSYNC pulse to the end of the border display. (i.e. the first pixel which is not border).

If M pixels are required in this time, then value (M-1)/2 should be programmed into the HBER. [M must be odd].

Again, if no border is required, this register must still be programmed such that M_{HBER} = M_{HDER}.

This is a 10 bit register, with bit 14 the least significant.
5.12 Horizontal Cursor Start Register (HCSR) : Address 98H

This register defines the time, in units of single pixel periods, from the start of the HSYNC pulse to the start of the cursor display.

If M pixels are required in this time, then value (M-6) should be programmed into the HCSR.

This is normally an 11 bit register, with bit 13 the least significant. Bits 11 and 12 must be zero except in the High Resolution mode. See section 6.6.

In this mode, where each 24MHz pixel is further divided into 4 pixels, the cursor sub-position can be defined by programming bits 11 & 12 of the HCSR, which will move the cursor position within the 24MHz pixel. Refer to section 6.6.

Note that only the cursor start position needs to be defined, as the cursor is automatically disabled after 32 pixels. If a cursor smaller than this is required, then the remaining bits in the cursor pattern should be programmed to logical colour 00 (transparent).

5.13 Horizontal Interlace Register (HIR) : Address 9CH

This register must be programmed if an interlaced sync. display is required. Otherwise it may be ignored.

If value L is written into the HCR, then value (L+1)/2 should be written into the HIR. [L must be odd].

This is a 10 bit register with bit 14 the least significant.

5.14 Vertical Cycle Register (VCR) : Address A0H

This register defines the period, in units of a raster, of the vertical scan, i.e. display time + flyback time.

If N rasters are required in a complete frame, then value (N-1) should be programmed into the VCR.

If an interlaced display is selected, (N-3)/2 must be programmed into the VCR. [N must be odd]. Here N is still the number of rasters in a complete frame, not a field.

This is a 10 bit register, with bit 14 the least significant.

5.15 Vertical Sync Width Register (VSWR) : Address A4H

This register defines the width, in units of a raster, of the VSYNC pulse.

If N rasters are required in the VSYNC pulse, then value (N-1) should be programmed into the VSWR.

The minimum value allowed for N is 1.

This is a 10 bit register, with bit 14 the least significant.

5.16 Vertical Border Start Register (VBSR) : Address A8H

This register defines the time, in units of a raster, from the start of the VSYNC pulse to the start of the border display.

If N rasters are required in this time, then value (N-1) should be programmed into the VBSR.

If no border is required, then this register must still be programmed, in this case to the same value as the VDSR.

This is a 10 bit register, with bit 14 the least significant.
5.17 Vertical Display Start Register (VDSR) : Address ACH

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 0 1 0 1 1 0 0
```
This register defines the time, in units of a raster, from the start of the VSYNC pulse to the start of the video display.
If N rasters are required in this time, then value (N-1) should be programmed into the VDSR.
This is a 10 bit register, with bit 14 the least significant.

5.18 Vertical Display End Register (VDER) : Address B0H

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 0 1 1 0 0 0 0
```
This register defines the time, in units of a raster, from the start of the VSYNC pulse to the end of the video display. (ie. the first raster on which the display is not present).
If N rasters are required in this time, then value (N-1) should be programmed into the VDER.
This is a 10 bit register, with bit 14 the least significant.

5.19 Vertical Border End Register (VBER) : Address B4H

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 0 1 1 0 1 0 0
```
This register defines the time, in units of a raster, from the start of the VSYNC pulse to the end of the border display. (ie. the first raster on which the border is not present).
If N rasters are required in this time, then value (N-1) should be programmed into the VBER.
If no border is required, then this register must be programmed to the same value as the VDER.
This is a 10 bit register, with bit 14 the least significant.

5.20 Vertical Cursor Start Register (VCSR) : Address B8H

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 0 1 1 0 0 0 0
```
This register defines the time, in units of a raster, from the start of the VSYNC pulse to the start of the cursor display.
If N rasters are required in this time, then value (N-1) should be programmed into the VCSR.
This is a 10 bit register, with bit 14 the least significant.

5.21 Vertical Cursor End Register (VCER) : Address BCH

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 0 1 1 1 0 0 0
```
This register defines the time, in units of a raster, from the start of the VSYNC pulse to the end of the cursor display. (ie. the first raster on which the cursor is not present).
If N rasters are required in this time, then value (N-1) should be programmed into the VCER.
This is a 10 bit register, with bit 14 the least significant.

5.22 Sound Frequency Register (SFR) : Address C0H

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 1 0 0 0 0 0 0 X X X X X X X X X X X X
```
This register defines the byte sample rate of the sound data. It is defined in units of 1μs.
If a sample period of Nμs is required, then (N-1) should be programmed into the SFR. N may take any value between 3 and 256.
This is a 9 bit register with bit 0 the least significant, Bit 8 in the SFR is used as a test bit, and should always be set to 1. When this bit is set LOW, all the internal timing signals are cleared.
6. Device Operation

6.1 The DMA Interface

The VIDC has 3 FIFOs into which DMA data is written. The Sound FIFO is four 32-bit words deep, and works independently from the other 2 FIFOs. The Video FIFO is eight 32-bit words deep, and the Cursor FIFO is again four 32-bit words deep.

6.1.1 Sound FIFO

Each word of data is strobed into the FIFO on the rising edge of SNDAK. Data is read out of the FIFO into a bytwide latch which then drives the DAC. When the last byte in the FIFO is read into the latch, the signal SNDREQ is driven LOW, requesting another 16 bytes of data. The signal SNDREQ is driven HIGH when the first SNDAK is received.

The time available to service this data request is dependent on the sound data rate. The minimum value allowed in the SFR is 2, which defines a byte-rate of 3us. Hence in this case the first word must be loaded into the FIFO less than 3us after the SNDREQ signal is generated.

6.1.2 Cursor FIFO

The Cursor FIFO contains 16 bytes of data, which is enough for 2 rasters of cursor display. When the VIDC is programmed to display a cursor, VIDREQ is driven LOW at the same time as HSYNC goes LOW on the first raster on which the cursor is to appear. Data is loaded into the FIFO on the rising edge of VIDAK. The FIFO must be filled completely (ie. 4 words) when the request is generated. The load cycle must be complete before the HSYNC pulse has ended.

VIDREQ is driven HIGH again when the first VIDAK is received. The cursor may be any number of rasters high, and the Cursor FIFO requests data during the HSYNC of every alternate raster on which it is displayed.

6.1.3 Video FIFO

The Video FIFO is eight 32-bit words deep, and it is arranged as a circular buffer. Data must always be loaded into it in blocks of 4 words, and this FIFO shares the same VIDREQ and VIDAK signals as the Cursor FIFO.

To accomodate the vastly different rates at which video data is required in the different modes, and to accomodate different DRAM speeds, the point at which more data is requested can be varied. This is controlled by bits 4 and 5 in the Control Register.

During the VSYNC pulse, the FIFO is cleared, and the signal VIDREQ is HIGH. After the HSYNC pulse of the first displayed raster, VIDREQ is driven LOW. Eight words must now be written into the FIFO by driving VIDAK LOW 8 times. This fills the FIFO. VIDREQ is set HIGH again when the fifth VIDAK is received.

Thereafter, the VIDREQ signal is set LOW whenever the FIFO empties to the point determined by bits 4 and 5 in the Control Register. The VIDREQ signal is normally set HIGH when the first VIDAK signal is received. However, if the data request is not serviced quickly, and the FIFO has emptied to the point where another 4 words have been read out when the first new data word arrives, then the VIDREQ signal will stay LOW, requesting another 4 words of data.
6.1.4 The Video DMA Interface

As noted above, the Cursor and Video FIFOs share the same DMA interface signals. Normally, a VIDRQ LOW during the HSYNC pulse is a request for Cursor data, and a VIDRQ LOW at any other time is a request for Video data. See Figure 1.

![Figure 1: Video & Cursor DMA](image)

However, often a video request happens just before the end of a raster display. (This is the data for the next raster.) The load cycle for this video request is allowed to overlap the HSYNC pulse, even if a cursor request happens during the HSYNC pulse. Note that in this case the VIDRQ signal may not be driven HIGH between these two cycles. The first cycle must be video data and the second cycle must be cursor data. The cursor load cycle must still be complete before the end of the HSYNC pulse. This is shown in Figure 2.

![Figure 2: Video DMA overlapping HSYNC](image)

6.2 Restrictions on Parameters

Certain restrictions must be applied to the screen parameters, most of which are system dependent. The following paragraphs assume the VIDC is being used in a system with the ARM and MEMC and 4/8MHz page mode DRAM. In this system DRAM cycles consist of an N-cycle (250ns) followed by up to 3 sequential S-cycles (125ns). Hence a VIDC FIFO 4-word load cycle consists of \( N + 3S \) which takes 625ns.

6.2.1 FIFO Request Pointer Values (Control Register D[4:5])

The Video FIFO is arranged as a circular buffer, though the core is asynchronous with a ripple-through time of 150ns from the top to the bottom. Data is loaded in blocks of 4 words, and is read out in bytes, starting with byte 0 of word 0. When the four bytes of word 0 are used, the pointer moves on to byte 0 of word 1 and so on. VIDRQ can be set LOW half way through reading the last byte of any of words 0-3 (and correspondingly 4-7) according to D[4:5] in the Control Register. Hence, in the high resolution video modes where the bytes are being consumed quickly, the request signal must be set at an earlier point than in the low resolution modes. The settings are defined in Table 4.

The request signal VIDRQ should be set LOW as soon as there will be enough room in the FIFO to accept the 4 words of data when they arrive. The minimum time between setting the request and receiving the last word of data is 187ns + 625ns = 812ns. [The 187ns figure is the minimum time in which MEMC can start a DMA cycle]. Now if the FIFO is full at the start, then it will have 4 words spare 150ns after the start of word 4. [150ns is the ripple time of a word through the FIFO]. Hence the request should be made at the first opportunity after (812ns - 150ns = 662ns) before the start of word 4. The request can be made halfway through the last byte of any of words 0 through 3 by programming the Control Register.
Table 4: FIFO Request Pointer settings.

```
Control Register  VIDREQ  Set at End of Words
0               0      0.4       
0               1      1.3       
1               0      2.6       
1               1      3.7       
```

Depending on the video mode in use, data can be read from the FIFO at 1.5, 2, 3, 4, 6, 8, 12, or 16MByte s⁻¹.

Figure 4 shows the case for the 16MByte s⁻¹ mode. The request must be set at the end of words 1 and 5.

```
0  1  2  3  4  5  6  7  0  1
```

*Figure 4: FIFO operating at 16MByte s⁻¹.*

Figure 5 shows the case for the 12MByte s⁻¹ mode. The request must be set at the end of words 2 and 6.

```
0  1  2  3  4  5  6  7  0
```

*Figure 5: FIFO operating at 12MByte s⁻¹.*

Figure 6 shows the case for the 8MByte s⁻¹ mode. Again the request must be set at the end of words 2 and 6.

In all the other modes, the request should be set at the end of words 3 and 7.

```
0  1  2  3  4  5  6
```

*Figure 6: FIFO operating at 8MByte s⁻¹.*

6.2.2 Horizontal Sync Pulse Width

The HSYNC pulse width must be long enough to allow a complete load of the cursor FIFO. This is made up as follows:

\[2 \times [N+3S] \text{ (current + cursor cycles)} + \text{syncmax} + 2 \times T_{prop},\]

ie. \(2 \times 625 + 312 + 100 = 1662\)ns.

\text{syncmax} is the maximum time MEMC can take to recognise the DMA request. \(T_{prop}\) is the time taken for the VIDREQ signal to reach MEMC, or the time taken for VIDAK to reach VIDC.

The pulse must also be long enough to allow the DMA Address Generator (DAG) in MEMC to reset the screen pointer. This may be as follows:

\[3 \times [N+3S] \text{ (current + cursor + sound cycles)} + \text{DAG react},\]

ie. \(3 \times 625 + 250 = 2125\)ns. This larger value must therefore be used.

6.2.3 Horizontal Front Porch Width

The front porch may be of zero length.

The total time from the end of display to the end of the HSYNC pulse must be more than 1912ns. As the HSYNC pulse width has to be at least 2125ns, this does not impose a restriction on the value of the front porch.

6.2.4 Horizontal Back Porch Width

The back porch must be long enough to allow the load of at least one word into the Video FIFO before the data is read out again. This is important at the start of the frame. Then the data is required in the bottom of the FIFO at least 4 pixel-times before the start of display, due to the pipelining in the VIDC. Hence the back porch must be greater than:

\[N+3S+N \text{ (current cycle + video N cycle)} + \text{syncmax} + 2 \times T_{prop} + \text{FIFO-ripple} + 4 \text{ pixels},\]

ie. \(250 + 375 + 250 + 312 + 100 + 150 + 4 \times 83 = 1770\)ns for 12MHz displays.

or \(250 + 375 + 250 + 312 + 100 + 150 + 4 \times 125 = 1937\)ns for 8MHz displays.

6.2.5 Vertical Sync, Pulse and Porch Width

There are no restrictions on the values of the vertical front porch, back porch or sync. width. The Vertical Sync. Width Register (VSWR) may be programmed to value 0 which gives a VSYNC width of one raster.
6.2.6 Horizontal Display Width
If vertical scrolling is required, then the number of bits in the pixels of each raster must be a multiple of 128. If vertical scrolling is not required, then the number of bits in the pixels of each raster must be a multiple of 32.

6.2.7 Border
The border cannot be disabled. If no border is required, then it should be programmed to start and finish in exactly the same place as the display (both vertically and horizontally).

6.2.8 Cursor Position
The cursor should not be programmed to be outside the display area vertically, but it may be programmed to start or end outside the display area horizontally. The cursor must not be programmed to "run off" the right hand side of the screen, though it may be programmed to start before the left hand side. If a cursor of, say only eight pixels wide is required, then the image should be programmed to be at the right hand end of the 32-pixel block, and the first 24 pixels should be programmed to be transparent. In this way, the displayed cursor may be positioned anywhere on the screen. Note that the cursor will not be displayed outside the border area either vertically or horizontally.

6.3 Display Formats

6.3.1 Screen Modes
14 of the possible 16 basic display modes are supported.

- 24MHz
  - 8 bits/pixel: Not Supported
  - 4 bits/pixel: 12MBytes s⁻¹
  - 2 bits/pixel: 6MBytes s⁻¹
  - 1 bit/pixel: 3MBytes s⁻¹
- 16MHz
  - 8 bits/pixel: 16MBytes s⁻¹
  - 4 bits/pixel: 8MBytes s⁻¹
  - 2 bits/pixel: 4MBytes s⁻¹
  - 1 bit/pixel: 2MBytes s⁻¹
- 12MHz
  - 8 bits/pixel: 12MBytes s⁻¹
  - 4 bits/pixel: 6MBytes s⁻¹
  - 2 bits/pixel: 3MBytes s⁻¹
  - 1 bit/pixel: 1.5MBytes s⁻¹
- 8MHz
  - 8 bits/pixel: 8MBytes s⁻¹
  - 4 bits/pixel: 4MBytes s⁻¹
  - 2 bits/pixel: 2MBytes s⁻¹
  - 1 bit/pixel: Not Supported

6.3.2 Data Display
Pixels are displayed starting at the top left hand corner of the screen, with the least significant bits of the first word in the FIFO.

In 8 bits/pixel mode, bits 0-7 of word 0 are the first displayed pixel.
In 4 bits/pixel mode, bits 0-3 of word 0 are the first displayed pixel.
In 2 bits/pixel mode, bits 0-1 of word 0 are the first displayed pixel.
In 1 bit/pixel mode, bit 0 of word 0 is the first displayed pixel.

6.3.3 Logical Data Fields
In 1 bit/pixel mode, the data field addresses the palette at location 0 or 1. The other 14 locations need not be programmed.
In 2 bits/pixel mode, the data field addresses the palette at locations 0 through 3. The other 12 locations need not be programmed.
In 4 bits/pixel mode, the data field addresses the palette at all 16 locations.
In 8 bits/pixel mode, the least significant 4 bits drive the palette as in 4 bits/pixel mode, and the most significant 4 bits drive the most significant bits of the RGB DACs directly.

6.3.4 Physical Data Fields
In 1,2,4 bits/pixel mode, the physical data field is:

<table>
<thead>
<tr>
<th>SUP.</th>
<th>BLUE</th>
<th>GREEN</th>
<th>RED</th>
</tr>
</thead>
<tbody>
<tr>
<td>D12</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
</tr>
<tr>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
</tr>
<tr>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

In 8 bits/pixel mode, the physical data field is:

<table>
<thead>
<tr>
<th>SUP.</th>
<th>BLUE</th>
<th>GREEN</th>
<th>RED</th>
</tr>
</thead>
<tbody>
<tr>
<td>D12</td>
<td>L7</td>
<td>D10</td>
<td>D9</td>
</tr>
<tr>
<td>L6</td>
<td>L5</td>
<td>D5</td>
<td>D4</td>
</tr>
<tr>
<td>L4</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>

- D<sub>10</sub>: These bits come from the palette field.
- L<sub>10</sub>: These bits come from the logical field.

6.3.5 Cursor Format
The cursor is the same format in all video modes, and is automatically defined to be 32 pixels wide, though it may be any number of rasters high. Any pixel may be defined as being transparent, enabling cursors of any shape to be constructed within the 32 pixel horizontal limit. The format is always 2 bits per pixel, with bits 0,1 in the first word in the Cursor FIFO representing the first pixel, etc. The logical cursor pixel bit-pairs are defined in Table 5.

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 5: Cursor logical colours

The cursor physical field is exactly as the video physical field in 1,2,4 bits/pixel modes.

<table>
<thead>
<tr>
<th>SUP.</th>
<th>BLUE</th>
<th>GREEN</th>
<th>RED</th>
</tr>
</thead>
<tbody>
<tr>
<td>D12</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
</tr>
<tr>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
</tr>
<tr>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>
6.3.6 Border Field
The border physical field is exactly as the video physical field in 1,2,4 bits/pixel modes.

<table>
<thead>
<tr>
<th>SUP</th>
<th>BLUE</th>
<th>GREEN</th>
<th>RED</th>
</tr>
</thead>
<tbody>
<tr>
<td>D12</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
</tr>
<tr>
<td>D8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
</tr>
<tr>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
</tr>
<tr>
<td>D0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6.4 Controlling the Screen

6.4.1 Screen On / Off
The simplest method of turning the screen off is to program the Vertical Display End Register (VDER) to be less than the VDSR. This will not generate any video requests, but will display the border colour over the whole screen. The border can be turned off either by programming it to physical colour black, or by programming the VARE to be greater than the VBER. Doing the latter will also disable the cursor, though cursor data requests will still be generated. Turning the screen back on should only be done during vertical flyback.

6.4.2 Cursor On / Off
The cursor should be turned off by setting the VCER to be less than the VCSR. [Value 0 is suggested]. This will also disable cursor data requests. Turning the cursor on, and moving it around should only be done during vertical flyback to prevent flash.

6.4.3 Writing to the Palettes & Other Registers
The palettes may be programmed reliably at any time, but are best programmed during vertical flyback. Changing the values of other registers should only be done during vertical flyback.

The signal FLYBK is set HIGH from the start of the first raster after the end of display (though it may still be border), until the start of the first raster which contains display data.

6.5 Video DAC Outputs

The Video DAC outputs are current sinks. Each DAC has a resolution of 4 bits, giving a linear transfer characteristic with 16 values. The magnitude of the output is a function of the video reference input current, with the maximum current sink being 15 times the reference input current.

In device VDC1, a digital input value of 4 zeros gives the maximum current sink, and a digital input value of 4 ones gives zero current sink.

In device VDC2, a digital input value of 4 zeros gives zero current sink, and a digital input value of 4 ones gives the maximum current sink.

The difference between the 2 devices results in a different output buffer circuit. A suitable circuit for VIDC1 is an emitter follower with appropriate level shifting. A suitable circuit for VIDC2 is shown in Figure 7. In this circuit, the diode, D1, should have similar characteristics to the base-emitter junction of TR1.

6.6 High Resolution Modes

The 4 bits of digital data which normally drive the red DAC are available to the user on pins VED(0-3). This pixel-rate bit-stream can be externally serialised to a single bit-stream of 4 times the VIDC pixel rate. With the VIDC operating at 24MHz, 4 bits/pixel mode, 96MHz bit-rates are generated giving very high resolution monochrome displays. Alternatively, with an external DAC, 48MHz grey-level displays are possible.

Referring to the Block Diagram, it will be noted that the data passes through the High Res. Shifter block before reaching the pins VED(0-3). This block is to enable the cursor to be positioned to any (96MHz) pixel. Note that this block also inverts the data from the red DAC.

When used in this mode, the VIDC must be programmed to a different set of values. But note that the "normal" analog modes of VIDC are still available simply by reprogramming; the addition of the shifter hardware will not affect the other modes, and the sound system is totally independent of this.

The following should be noted:

1. 4 bits per pixel should always be selected.

2. The programmed VIDC pixel rate is one quarter of the external pixel rate. The vertical timing parameters are unaffected by this as they are defined in units of a raster, but the horizontal timing parameters which are defined in units of 2 (34MHz) pixels can only be programmed in units of 8 (96MHz) pixels. There are now 4 times as many pixels on a line as are actually programmed. For example, if a display of 1024 * 1024 is required, the VIDC should be programmed to generate a display of 256 (horizontal) by 1024 (vertical).

3. All 16 locations of the video palette should be programmed to be a 1:1 logical to physical mapping. Only D[0:3] (red DAC values) need to be programmed, as D[4:11] are ignored. The supremacy bit (D[12]) may be used if required.

4. D[4,5] in the Border Colour Register must be set to zero. D[0:3] & D[12] may also be programmed if a border is required.
The cursor palette should be programmed to the following values:
- cursor colour 1: 10H
- cursor colour 2: 20H
- cursor colour 3: 50H
- Supremacy may also be used.

Then the 2 bits which define each cursor pixel are shown in Table 6.

<table>
<thead>
<tr>
<th>MSB</th>
<th>LSB</th>
<th>Colour</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>transparent</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>cursor black</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>do not use</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>cursor white</td>
</tr>
</tbody>
</table>

Table 6: Cursor logical colours, high res. mode

The VED should be arranged so that VED[0] is the first bit to be serialised.

6.7 External Synchronisation and Mixing

The VDIC has 2 signals associated with external synchronisation applications: SUP and SINK.

The signal SUP is an output which can be used to control an external multiplexer for mixing the VDIC output with that from an external source. All video and cursor logical colours from the palettes and the border colour can control SUP. When D[12] in any of the above registers is set and that colour is being displayed, SUP is driven LOW. The output is pipelined and is synchronous with the DAC outputs and the VED[0:3] signals.

The signal SINK is an input which when driven HIGH will reset the vertical counters to the first raster. If an interlaced sync. display is being generated, then SINK will reset the counters to the first raster of the odd field. The pulse applied to this pin must be shorter than a raster time. The horizontal counters are not affected by this signal. The horizontal synchronisation must be done by phase-locking (or in simple applications, by interrupting) the input clock CKIN. Remember that the sound system is also driven from a derivative of CKIN.

6.8 Composite Sync.

If D[7] in the Control Register is set HIGH, the VICSYNC pin will output a composite sync. pulse. This is synthesised from the exclusive-NOR of VSYNC and HSYNC.

6.9 Interlaced displays.

The VDIC can be programmed to generate an interlaced sync. display. Normally the video data in each field is the same. The VDIC Vertical Cycle Register is set to a value (N-3)/2, where N is the total number of rasters in a frame. There are N/2 rasters in the even and odd fields. On raster (N+1)/2, the VSYNC pulse is output and the cycle repeats, but this is now the odd field, so the VSYNC pulse is delayed by half a raster time as defined by the value in the HIR. On the first raster in the odd field after VSYNC, a dummy raster is inserted. This makes the odd field N/2 rasters long as well.
6.10 Sound System

The sound system consists of a four word FIFO and byte-wide latch which drive a 7-bit exponential DAC. The eighth bit steers the DAC output to one of 2 pairs of output pins, one pair designated "+" and the other pair designated "-". The sound signal is generated externally by integrating and then subtracting these two pairs of signals. This is shown in Figure 8 below. Here the integration is performed by the capacitor C.

![Diagram of sound system](image)

**Figure 8: Combination of signals to produce left channel output.**

Stereo image is synthesised by time-division multiplexing the output between the "left" and "right" pair of output signals. The first quarter of each sample is muted to allow for DAC settling and deglitching. The stereo image is specified for each channel by programming the corresponding Stereo Image Register.

The system can operate in 1, 2, 4 or 8 channel modes. In 8 channel mode, the channels are sampled sequentially, starting with the first byte of data, which is channel 0; the second byte of data is channel 1 and so on. The external integrating time constant must be long enough to integrate over a complete sample cycle. In 4 channel mode, the fifth byte to be sampled is again channel 0, so Stereo Image Register 5 must be programmed to the same value as Stereo Image Register 0, and so on. In 2 channel mode, Stereo image registers 0,2,4 and 6 correspond to channel 0 and Stereo Image Registers 1,3,5 and 7 correspond to channel 1. In single channel mode, all eight Stereo Image Registers need to be programmed to the same value.

The sample rate is selectable by the SFR in units of 1 μs, with a minimum value of 3 μs. In eight channel mode the bytes for each channel are sampled with one-eighth of the frequency of single channel mode for a given value in the SFR.

The DAC transfer characteristic consists of 8 linear segments (chords). Each chord consists of 16 steps, and the step size in one chord is twice the step size in the preceding chord. This gives an approximation to the "i255 law". Note that the order of the bits used to generate the sound values differs between VIDC1 and VIDC2. This is defined in the diagram below.

![Diagram of DAC transfer characteristic](image)

The outputs are current sinks. The magnitude of the output is a function of the sound reference input current. The reference current is equal to the step size in the highest chord, which is $8i$ in the figure above.
7. DC Parameters

7.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>supply voltage</td>
<td>-0.5</td>
<td></td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td>Vip</td>
<td>voltage on any pin</td>
<td>-0.5</td>
<td></td>
<td>+7</td>
<td>V</td>
</tr>
<tr>
<td>Ta</td>
<td>storage temperature</td>
<td>-40</td>
<td></td>
<td>+125</td>
<td>deg C</td>
</tr>
</tbody>
</table>

7.2 DC Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>supply voltage</td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>Vih</td>
<td>input logic “1”</td>
<td>2.4</td>
<td>Vdd</td>
<td>V</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Vil</td>
<td>input logic “0”</td>
<td>0</td>
<td>0.8</td>
<td>V</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>I_vout</td>
<td>output current</td>
<td>-2</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>video DACs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_sout</td>
<td>output current</td>
<td>-2</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>sound DAC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ta</td>
<td>ambient operating temperature</td>
<td>0</td>
<td>70</td>
<td>deg.C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
(1) Voltages measured with respect to VSS.
(2) IT - TTL compatible inputs.

KEY TO TABLES

Mes - Values measured in an ARM/MMEMC/VIDC/IOC system running at 8MHz
Nom - Nominal values
Lim - Values required to meet ARM/MMEMC/VIDC/IOC system specifications

7.3 DC Characteristics
measured at Vdd = +5.0V 25°C

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>Mes</th>
<th>Nom</th>
<th>Lim</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>supply current</td>
<td>17</td>
<td></td>
<td></td>
<td>mA</td>
<td>1</td>
</tr>
<tr>
<td>output short circuit current</td>
<td>25</td>
<td></td>
<td></td>
<td>mA</td>
<td>2</td>
</tr>
<tr>
<td>input / output latch current</td>
<td>200</td>
<td></td>
<td></td>
<td>mA</td>
<td>3</td>
</tr>
<tr>
<td>output Hi voltage wrt Vdd</td>
<td>-150</td>
<td></td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>output Lo voltage wrt Vss</td>
<td>150</td>
<td></td>
<td></td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>input Hi voltage threshold</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>input Lo voltage threshold</td>
<td>1.7</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>RVDDAC, RS DAC voltage wrt Vdd</td>
<td>1.3</td>
<td></td>
<td></td>
<td>V</td>
<td>4</td>
</tr>
<tr>
<td>voltage compliance, video DACs wrt Vdd at Iout = -2mA</td>
<td>1.8</td>
<td>1.7</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>current compliance, video DACs at Vdd = 0.7V</td>
<td>4.5</td>
<td>1</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>voltage compliance, sound DAC wrt Vdd at Iout = -2mA</td>
<td>1.5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>current compliance, sound DAC at Vdd = 0.7V</td>
<td>3</td>
<td>nA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>input capacitance</td>
<td>5.0</td>
<td>5.0</td>
<td>pF</td>
<td></td>
<td>5</td>
</tr>
</tbody>
</table>

NOTES:
(1) Measured at a pixel rate of 24MHz. This value does not include any current output by the video DACs.
(2) Not more than one output should be shorted to either rail at any time, and for no longer than 1 second.
(3) This value represents the current that input/output pins can tolerate before the chip latches up. As sustained latch-up is catastrophic, this value must never be approached.
(4) This assumes a 10K resistor to VDD.
(5) This value includes the capacitance of the chip carrier and socket.
8. AC Parameters

8.1 AC Operating Conditions

8.1.1 Input Clock

```
CHIN

--> t1 --<

<=-- t3 <=--
```

8.1.2 DMA Writes

```
D[0:31]

VIDAR, SNAK

<=-- t4 -->
<=-- t5
```

8.1.3 Register Writes

```
D[0:31]

VIDAR

<=-- t7 -->
<=-- t8 <=--
<=-- t9 -->
```

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>t1</td>
<td>CHIN High</td>
<td>20</td>
<td>20</td>
<td>&gt;6</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>t2</td>
<td>CHIN low</td>
<td>20</td>
<td>20</td>
<td>&gt;8</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>t3</td>
<td>CHIN frequency</td>
<td>24</td>
<td>24</td>
<td>Mhz</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>t4</td>
<td>DATA – STROBE setup VIDAR, SNAK</td>
<td>70</td>
<td>20</td>
<td>&gt;5</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>t5</td>
<td>DATA – STROBE hold VIDAR, SNAK</td>
<td>30</td>
<td>15</td>
<td>&gt;2</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>t6</td>
<td>STROBE pulse width VIDAR, SNAK</td>
<td>62</td>
<td>62</td>
<td>&gt;15</td>
<td>ns</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>t7</td>
<td>DATA – STROBE setup VIDAR</td>
<td>80</td>
<td>20</td>
<td>&gt;5</td>
<td>ns</td>
<td>1,2</td>
</tr>
<tr>
<td>t8</td>
<td>DATA – STROBE hold VIDAR</td>
<td>85</td>
<td>15</td>
<td>&gt;5</td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>t9</td>
<td>STROBE pulse width VIDAR</td>
<td>83</td>
<td>80</td>
<td>&gt;15</td>
<td>ns</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE:
1. The Limit values were measured for a sample VIDC. A factor of two should be allowed for process variations.
2. As the data also carries the address, the data must be set up before VIdW goes LOW.
8.2 AC Characteristics
measured at Vdd = +5.0V 25°C

8.2.1 Clock - Outputs

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Mea</th>
<th>Nom</th>
<th>Lim</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>t10</td>
<td>CKIN - SD[0:3]</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>t11</td>
<td>CKIN - VED[0:3], SUP</td>
<td>33</td>
<td>42</td>
<td></td>
<td>ns</td>
<td>1, 3</td>
</tr>
<tr>
<td>t12</td>
<td>CKIN - HS, V/CS, FLYBK</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
<td>3</td>
</tr>
<tr>
<td>t13</td>
<td>CKIN - HT</td>
<td>26</td>
<td></td>
<td></td>
<td>ns</td>
<td>3</td>
</tr>
<tr>
<td>t14</td>
<td>CKIN - ROUT, GOOT, ROUT</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
<td>1</td>
</tr>
<tr>
<td>t15</td>
<td>Analog rise / fall</td>
<td>7</td>
<td>10</td>
<td></td>
<td>ns</td>
<td>4</td>
</tr>
</tbody>
</table>

NOTES:
(1) For pixel rates of 12MHz and 24MHz, the outputs are referenced to the rising edge of CKIN. For pixel rates of 8MHz and 16MHz, the outputs are alternately referenced to either edge of CKIN.
(2) The SD[0:3] signals are output one pixel time before the corresponding VED[0:3] due to pipelining differences.
(3) All digital outputs measured into 40pF load.
(4) Assumes a 5pF external load.

8.2.2 NIBSEL - Output

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Mea</th>
<th>Nom</th>
<th>Lim</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>t16</td>
<td>NIBSEL - SD[0:3]</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
8.2.3 DMA Acknowledge - Request

D[0:31]

SNDAK, VIDAK

SNDRQ, VIDRQ

==>> i <= t17

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Mes</th>
<th>Nom</th>
<th>Lin</th>
<th>Units</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>t17</td>
<td>SNDRQ - SNDAK</td>
<td>25</td>
<td>40</td>
<td></td>
<td>na</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>VIDRQ - VIDAK</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
(1) VIDRQ or SNDRQ are cleared by the first VIDAK or SNDAK respectively, so long as no further request is pending.

9. Packaging

The device is packaged in a JEDEC B ceramic leadless chip carrier, or JEDEC C PLCC.

Suitable sockets are
(1) AMP 55159-1 for the ceramic device
(2) Burndy QILE58P-410T for the plastic device

These sockets both have a footprint as shown below.