The 16 Bit Memory Cell

Theory & Applications

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The 16 Bit Memory Cell: TMC 3162, TMC 3163 and TMC 3164, are monolithic devices utilizing HLTTL technology insuring capability with Transitron's broad capability in Transistor-Transistor Logic.

The Memory Cell is a bit oriented device, organized as 16 words one bit wide. The device is partitioned into four major functional areas: Data Bus, Storage, Sensing and Writing. The storage consists of 16 two transistor flip-flops (Figure 1) arranged in a 4 x 4 matrix, for address selection, which provides non-destructive readout bit storage and destructive read-in. Two sense amplifiers with open collector outputs (tied to Vcc through external resistors) are incorporated to provide double rail outputs and an ORing capability for expansion to a larger word capacity. Separate inverters provide individual control for writing zeros and ones into the storage flip-flops. By using common data buses between each side of the flip-flops, the sense amplifiers and the write inverters, fast reading and writing rates can be implemented into large memory systems.

The basic flip-flops used in the Memory Cell consists of a pair of triple emitter transistors connected in an inverting configuration (Figure 2), such that the collector of each transistor is cross-coupled to the base of the other. The collector resistor of the device in cut-off supplies base drive to the transistor in saturation. Corresponding pairs of emitters are bussed horizontally and vertically to form the X1 - X4, Y1 - Y4 coincident matrix.

The third emitter of each flip-flop joins a separate data bus for the "1" side and the "0" side, (Figure 2). The data bus for the "1" side of the flip-flop is common to the input of the sense amplifier S1 and the output of the write amplifier W1 and similarly the data bus for the "0" side of the flip-flop is common to the input of the sense amplifier S0 and the output of the write amplifier W0.

The third emitter therefore, of each flip-flop being individually connected to two data buses performs both the functions (under different write inverter input conditions) of sensing the state of a flip-flop and controlling its state. The common data bus therefore, performs the integral function of carrying information from the flip-flops to the sense amplifier in terms of their states and also carrying information to the flip-flops from the write inverter to control their states.

Since the state of a flip-flop is sensed at the emitter e3, common to the data bus (as opposed to the conventional method of sensing the collector voltage), the state of only one flip-flop may be determined during any interrogation of the device. The logic performed by the matrixing provides a convenient multiplexing of the sense amplifier input and the write amplifier output on a random access basis.

DATA BUS

An analysis of the Memory Cell depends largely on the voltage variations of the data buses. The device will therefore, be analysed from that point of view by considering:

(1) "Idle"-Mode - Voltage on all address select lines

V_{xy} \leq V_{xy} "S"

(2) "Half-Select" Mode - Voltage on a single address select line

V_{xy} \geq V_{xy} "S" all others at V_{xy} \leq V_{xy} "S"
(3) "Full-Select" Mode - Voltage on a pair of coincident address 
select lines $V_{xy} \geq V_{xy} \ "S"$ all others at 
$V_{xy} \leq V_{xy} \ "S"$.

Where $V_{xy} \ "S"$ = Threshold Voltage on X and Y Address Lines to prevent 
sensing.

$V_{xy} \ "S"$ = Threshold Voltage on X and Y Address Lines to insure sensing.

Since writing information into a cell location requires that the location 
is specified by a full selection, the write amplifier is essentially isolated 
from the rest of the device and does not require consideration until the 
"full-select" mode has been fully characterized. This assumption is verified 
in that which follows:

If the inputs to both write inverters is held at a potential $V_{W}$ of 0.9 
vols or lower, the input divide $D_6$ is forward biased and the base of transistor 
$T_6$ is clamped to the input voltage of 0.9 volts + the forward drop across $D_6$ 
which is sufficient to maintain $T_6$ in cut-off. Since $T_6$ cannot supply base 
drive to $T_8$, it is also in cut-off and it therefore draws no collector current 
except for a small leakage contribution and therefore is isolated from 
the data bus.

It can be seen in Figure 3 that the $V_{cc}$ supply resistor $R_5$ diode $D_2$ and the 
base-emitter junctions of $T_1$ and $T_2$ clamp the data bus to two $V_{be}$ drops above 
ground (approximately 1.5V) if no current is supplied from any flip-flop 
emitter tied to this bus and the write inverter is off. This condition (no 
current supplied from flip-flops) is sustained when there is no interrogation 
("idle" or "half-select" mode) of any flip-flops.

STORAGE

In a previous section it was noted that both data buses are clamped to 
approximately 1.5 volts if no bit location is addressed. Further examination, 
under identical conditions (Figure 4) reveals that the potential imposed on the 
base of the off transistor is equal to the voltage on the select line $V_{xy}$ plus 
the collector to emitter voltage of the saturated transistor $V_{CE(SAT)}$ or:

$$V_{B off} = V_{xy} + V_{CE(SAT)}$$

but

$$V_{B} = V_{xy}$$

$$V_{BE off} = V_{CE(sat)} \approx 0.3 \ \text{volts}$$

Since the voltage required to forward bias the base-emitter junction is 
approximately 0.7 volts this device is essentially in cut-off. Some small 
collector current in the form of leakage in the order of 10 microamps does flow 
but, it has no significant effect on the imposed voltage levels.

SELECTION CONSIDERATIONS

In order to properly apply this device, serious consideration must be 
given to the sinking requirements which determine the driver capability associ­
ated with the select lines. In calculating the sinking current, the idle mode 
may be used to determine the current contribution per emitter (Figure 5). Note 
that only the flip-flop transistors in saturation are shown since the transistors 
in cut-off contribute only leakage current.
During the "idle" mode the emitter e₃ (connected to the data bus) is back biased with the 1.5V developed by the sense amplifier clamp since all other emitters are held at $V_{xy"S"}$. This condition is analogous to a set of three common anode diodes connected to Vcc through a resistor (Figure 6). The remaining emitters (e₁ and e₂) those connected to the matrix, can be assumed to "current share" the total available current which contributes approximately equal currents to the X and Y select lines and therefore to the devices sinking these lines. If either the X or Y line (Figure 7) is raised to a voltage equal to threshold voltage to insure sensing ($V_{xy"S"}$) that emitter is back biased, and the current which formerly flowed in that line returns to ground through the address line which is maintained at $V_{xy"S"}$. This condition is referred to as a "half-select" mode and occurs to some cells during an operation in which a location is fully selected or only one select line is addressed. The cells that are "half-selected" are those common to the address lines which have been raised to $V_{xy"S"}$ (Figure 6). All the available current in the saturated transistor of the flip-flops, limited only by the collector resistors, $V_{BE\ ON}$ and $V_{CE\ (SAT)}$ flows to ground through the emitters, e₁ and e₂ if held at a voltage level $V_{xy"S"}$ by the devices sinking the select lines. Note: Increased interrogation speed may be implemented by overlapping X-Y selection.

Address Line Sinking Current Calculations

Idle Mode (Figure 5)

\[ V_x = V_y = V_e \]
\[ V_{C \ ON} = V_{B \ OFF} = V_e + V_{CE\ (SAT)} \]
\[ V_{B \ ON} = V_{BE\ ON} + V_e \]
\[ I = I_x = I_y = \frac{I_C + I_B}{2} \text{ assuming current shunting} \]

where $I$ = the current contribution per emitter

\[
I = \frac{V_{CC} - V_{C\ ON} + V_{CC} - V_{B\ ON}}{2R_C + 2R_C} - \frac{V_{C\ ON} - (V_e + V_{CE\ (SAT)}) + V_{CC} - (V_{BE\ (ON)} + V_e)}{2R_C + 2R_C} - \frac{2(V_{CC} - V_e) - (V_{CE\ (SAT)} + V_{BE\ (ON)})}{2R_C}
\]

\[ T = -55^\circ C \]
\[ I = \frac{2(5.5 - 0.25) - (0.2 + 0.075)}{2(3.37)} = 1.52 \text{ ma} \]

\[ T = +125^\circ C \]
\[ I = \frac{2(5.5 - 0.25) - (0.39 + 0.625)}{2(3.88)} = 1.21 \text{ ma} \]
Figure 5 indicates that the maximum current on any select line is \(4(I)\)
\[
I_{\text{sink (max)}} = 6.08 \, \text{mA}
\]
Half-Select and Full-Select (Figure 7 & 8)
These modes impose identical maximum sink requirements.
\[
I_{\text{sink (max)}} = 5(I) = 5(1.52) = 7.60 \, \text{mA}
\]

INPUT CHARACTERISTICS OF THE ADDRESS LINES

Referring to Figure 4, the Input Characteristics of the Select Lines, as
the input voltage on a pair of coincident address lines rises, between 0 volts
and point A, the input current decreases rapidly. This is due to the fact that
the current from half-selected bits is shared by selected inputs and grounded
inputs. At an input voltage between points A and B, the input current decreases
slightly; the emitters \(e_3\) still being back biased. Traversing the curve between
points B and C, the input current again decreases rapidly. This relatively
rapid decrease in input current is caused by the forward biasing of the emitter
\(e_3\) associated with the data bus. This switching of current to the data bus
occurs at a level of approximately \(1.5 + \Delta V\) volts, as the emitters \(e_1\) and \(e_2\)
become back biased and the emitter \(e_3\) becomes forward biased.

WRITE CYCLE

Writing information into a selected bit location is accomplished by first
selecting particular location by raising the voltage \(V_{xy}\) on a pair of coincident
lines to a voltage \(V_{xy "W"}\), keeping all other at \(V_{xy "W"}\).

Where \(V_{xy "W"}\) = Threshold voltage on X and Y Address Lines to insure writing.

Although this operation to this point is almost identical to interrogation
of a bit location, its purpose is to multiply the output of the write amplifiers
to the correct bit location. Since the selected inputs are at a potential to
insure writing, they can be assumed to be back biased and therefore disconnected
from the cell.

Let us assume for this discussion, that transistor \(Q_1\) is off and therefore,
\(Q_2\) is on. Then, the potential on the base of \(Q_1\) is approximately 1.8 volts and
the potential on its collector is 2.2 volts, remembering that the base and collector
of \(Q_1\) reside at the same potential as the collector and base of \(Q_2\) respectively,"through cross-coupling. If the voltage \(V_w\) on the input to the write
amplifier is raised to \(V_w "l"\), transistor \(T_R\) receives enough base drive to
saturate and pull its collector to a \(V_{CE}\) drop above ground. Since emitter \(e_3\)
of transistor \(Q_1\) is common to the collector of \(T_R\), the emitter - base junction
becomes forward biased pulling the collector of \(Q_1\) to a potential of \(V_{CE\, SAT}/Q1 + V_{CE\, SAT}/Q2\) above ground. The cross-coupled base of \(Q_2\) follows and the emitter-base
junction voltage drops to a \(V_{CE\, SAT}\) turning off \(Q_2\).

In the previous discussion writing was accomplished by selection of a pair
of coincident lines and then raising the write amplifier input. Although, this
implies that the selection lines must be raised before the write amplifier, this
is not the case. Both conditions may be initiated and terminated simultaneously,
(Figure 9).
Combined Fan-Out and Wire-OR Capabilities

The open collector outputs of the sense amplifiers when supplied with a proper load resistor ($R_L$), may be paralleled with other sense amplifier outputs or TTL gates to perform the wire-OR function; and, simultaneously will drive one to fifteen or thirty TTL loads. When no other open collector gates are paralleled, this gate may be used to drive fifteen or thirty TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and $I_{off}$ current (through paralleled outputs) will be available during a logical 1 level of the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of $R_L$ is determined by:

$$R_L = \frac{V_L}{IL}$$

Where: $V_L$ is voltage drop in volts, and $I_L$ is the current in amperes.

Logical 1 (off level) circuit calculations

The allowable voltage drop across the load resistor ($V_L$) is the difference between $V_{cc}$ applied and the $V_{out}$ (1) level required at the load:

$$V_L = V_{CC} - V_o \ "1" \ required$$

The total current through the load resistor ($I_L$) is the sum of the load currents ($I_{IN} \ "1"$) and off-level reverse currents $I_{oLK}$ through each of the wire-OR connected outputs:

$$I_L = M (I_{oLK}) + N (I_{IN} \ "1") \ to \ TTL \ loads$$

Therefore, calculations for the maximum value of $R_L$ would be:

$$R_L (max) = \frac{V_{CC} - V_o \ "1" \ required}{M (I_{oLK}) + N (I_{IN} \ "1")}$$

Where: $M =$ number of gates wire-OR connected, and $N =$ number of TTL loads.
Logical 0 (on level) Circuit Calculations

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-OR connected, the current through $R_L$ may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 20 mA, the maximum current which will ensure a logical 0 maximum of 0.45 volts.

Also, fan-out must be considered. Part of the 20 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through $R_L$.

Therefore, the equation used to determine the minimum value of $R_L$ would be:

$$R_L (\text{min}) = \frac{V_{CC} - V_\alpha \text{ "0" required}}{I_{\text{sink capability}} - I_{\text{sink from TTL Loads}}}$$
Calculation:

\[ RL_{(\text{min})} = \frac{V_{CC} - V_o \ "0" \ required}{I_{\text{sink}} \ capability \ -- \ I_{\text{sink}} \ from \ \text{TTL} \ \text{loads}} \]

\[ RL_{(\text{min})} = \frac{5 - 0.45}{20 \times 10^{-3} - 3.99 \times 10^{-3}} = \frac{4.55}{16 \times 10^{-3}} = 284 \ \Omega \]

**LOGICAL 0 CIRCUIT CONDITIONS**
Calculation:

\[
R_L (\text{max}) = \frac{V_{CC} - V_o \ "1" \text{ required}}{M (I_{OLK}) + N (I_{Load})}
\]

\[
R_L (\text{max}) = \frac{5 - 3.1}{1.0 \times 10^{-3} + .3 \times 10^{-3}} = \frac{1.9}{1.3 \times 10^{-3}} = 1460 \Omega
\]

Logical 1 Circuit Conditions
DEFINITIONS OF TERMS USED FOR SPECIFYING
MEMORY CELL OPERATION (0°C to 75°C)

Test $I_X$ "0"
Select current with X address line at logic "0":
measured value = 11 mA maximum. Select current can
be any value between zero milliamps and eleven milliamps.

Test $I_X$ "1"
Select current with X address line at logic "1":
measured value = 400 µA maximum. Select current can
be any value between zero microamps and four hundred
microamps.

Test $B_{V_X}$
Breakdown Voltage of X address line: measured value
= 5.5V minimum. X address line will not break down until
the voltage applied to the address line is increased to
a value equal to or greater than five point five volts.

Test $V_{xy}$ "W"
Threshold Voltage on X and Y address lines to insure writing:
measured value = 2.1V minimum. The Memory Cell is guaranteed
to write if the X and Y address lines are at a voltage equal
to or greater than two point one volts. (The Memory Cell
may still write if the voltage on the address lines is less
than two point one volts, but this is not guaranteed).

Test $V_{xy}$ "W"
Threshold Voltage on X and Y address lines to prevent writing:
measured value = 0.8V maximum. The Memory Cell is guaranteed
not to write if the X and Y address lines are at a voltage equal to or less than zero point eight volts.
(The Memory Cell may still not write if the voltage on the
address lines is greater than zero point eight volts, but
this is not guaranteed).

Test $V_{xy}$ "S"
Threshold Voltage on X and Y address lines to insure sensing:
measured value = 2.1V minimum. The Memory Cell is guaranteed
to sense the information stored in the matrix point under
observation if the X and Y address lines are at a voltage equal
to or greater than two point one volts. (The Memory Cell
may still sense information correctly when the address
lines are at a voltage less than two point one volts, but
this is not guaranteed).
Both write inverter inputs must be less than or equal to
$V_w$ "0" in order to obtain valid sense information.

Test $V_{xy}$ "S"
Threshold Voltage on X and Y address lines to prevent sensing:
measured value = 1.0V maximum. The Memory Cell is guaranteed
to not sense the information stored in the matrix point under
observation if the X and Y address lines are at a voltage equal to or less than one point zero volts. (The Memory Cell may still not sense when the address lines are at a voltage greater than one point zero volts, but this is not guaranteed). Both write inverter inputs must be less than or equal to $V_w$ "0" in order to obtain valid sense information.

Test $I_w$ "0"
Write line current with write line at logic "0": measured
value = 1.33 ma maximum. Write line current can be any value
between zero milliamps and one point three milliamps.
<table>
<thead>
<tr>
<th>Test</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Test $I_W$ &quot;1&quot;</td>
<td>Write line current with write line at logic &quot;1&quot;: measured value = 100 uA maximum. Write line current can be any value between zero microamps and one hundred microamps.</td>
</tr>
<tr>
<td>Test $B V_W$</td>
<td>Breakdown Voltage of write line: measured value = 5.5V minimum. Write line will not break down until the voltage applied to the write line is increased to a value equal to or greater than five point five volts.</td>
</tr>
<tr>
<td>Test $V_W$ &quot;1&quot;</td>
<td>Threshold Voltage of write line in logic &quot;1&quot; condition: measured value = 2.1V minimum. Writing voltage must be any value equal to or greater than two point one volts in order to guarantee writing into the selected cell.</td>
</tr>
<tr>
<td>Test $V_W$ &quot;0&quot;</td>
<td>Threshold Voltage of write line in logic &quot;0&quot; condition: measured value = 1.0V maximum. Writing voltage can be any value equal to or less than one point zero volts in order to guarantee not to write into the selected cell.</td>
</tr>
<tr>
<td>Test $V_{out}$ &quot;0&quot;</td>
<td>Voltage of sense output in logic &quot;0&quot; condition: measured value = 0.45V maximum. Sense output voltage must be any value equal to or less than zero point four five volts.</td>
</tr>
<tr>
<td>Test $V_{out}$ &quot;1&quot;</td>
<td>Voltage of sense output in logic &quot;1&quot; condition: measured value = 5.5V minimum. Sense output voltage can be equal to or greater than five point five volts in order to cause two hundred fifty microamps of current to flow into the sense output terminal.</td>
</tr>
<tr>
<td>Test $I_S$</td>
<td>Supply current: measured value = 60 mA maximum. Supply current can be any value between zero milliamps and sixty milliamps.</td>
</tr>
<tr>
<td>Test $B V_{ckt}$</td>
<td>Circuit breakdown voltage: measured value = 7.0V minimum. When eighty four milliamps is forced into the Vcc input (Pin 4) the voltage from Vcc to ground must be equal to or greater than seven point zero volts.</td>
</tr>
<tr>
<td>Test $twp$</td>
<td>Write pulse width: measured value = 25 nsec minimum. The write pulse must be high for at least twenty five nanoseconds during the time the X/Y bit selection lines are high in order to guarantee writing. One X-Y location high, all others low, &quot;1&quot; previously stored when testing $S_0$ and &quot;0&quot; previously stored when testing $S_1$.</td>
</tr>
<tr>
<td>Test $twr$</td>
<td>Write recovery time: measured value = 35 nanoseconds maximum. Write recovery time can be any value between zero and thirty five nanoseconds. One X-Y location high, all others low, &quot;1&quot; previously stored when testing $S_0$ and &quot;0&quot; previously stored when testing $S_1$.</td>
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**Test $T_d$ on**  
Output turn-on delay; measured value = 30 nsec maximum. Output turn-on delay can be any value between zero and thirty nanoseconds. One X-Y location switched, all others low, "1" previously stored when testing $S_1$, "0" previously stored when testing $S_0$.

**Test $T_d$ off**  
Turn-off delay: measured value = 30 nsec maximum. Output turn-off delay can be any value between zero and thirty nanoseconds. One X-Y location switched, all others low, "1" previously stored when testing $S_1$, "0" previously stored when testing $S_0$. 

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**Definitions of Terms Used for Specifying Memory Cell Operation (0°C to 75°C)**
DEFINITIONS OF TERMS USED FOR SPECIFYING MEMORY CELL OPERATION (-55°C to +125°C)

Test $I_x$ "O"  
Select current with X address line at logic "O": measured value = 11 ma maximum. Select current can be any value between zero milliamps and eleven milliamps.

Test $I_x$ "1"  
Select current with X address line at logic "1": measured value = 400 uA maximum. Select current can be any value between zero microamps and four hundred microamps.

Test $B_{Vx}$  
Breakdown Voltage of X address line: measured value = 5.5V minimum. X address line will not break down until the voltage applied to the address line is increased to a value equal to or greater than five point five volts.

Test $V_{xy}$ "W"  
Threshold Voltage on X and Y address lines to insure writing: measured value = 2.2V minimum. The Memory Cell is guaranteed to write if the X and Y address lines are at a voltage equal to or greater than two point two volts. (The Memory Cell may still write if the voltage on the address lines is less than two point one volts, but this is not guaranteed.)

Test $V_{xy}$ "W"  
Threshold Voltage on X and Y address lines to prevent writing: measured value = 0.75V maximum. The Memory Cell is guaranteed not to write if the X and Y address lines are at a voltage equal to or less than zero point eight volts. (The Memory Cell may still not write if the voltage on the address lines is greater than zero point seven five volts, but this is not guaranteed.)

Test $V_{xy}$ "S"  
Threshold Voltage on X and Y address lines to insure sensing: measured value = 2.2V minimum. The Memory Cell is guaranteed to sense the information stored in the matrix point under observation if the X and Y address lines are at a voltage equal to or greater than two point one volts. (The Memory Cell may still sense information correctly when the address lines are at a voltage less than two point two volts, but this is not guaranteed.) Both write inverter inputs must be less than or equal to $V_w$ "O" in order to obtain valid sense information.

Test $V_{xy}$ "S"  
Threshold Voltage on X and Y address lines to prevent sensing: measured value = 0.85V maximum. The Memory Cell is guaranteed to not sense the information stored in the matrix point under observation if the X and Y address lines are at a voltage equal to or less than zero point eight five volts. (The Memory Cell may still not sense when the address lines are at a voltage greater than one point zero volts, but this is not guaranteed.) Both write inverter inputs must be less than or equal to $V_w$ "O" in order to obtain valid sense information.
## Definitions of Terms Used for Specifying Memory Cell Operation (−55°C to +125°C)

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<td>Write line current with write line at logic &quot;O&quot;: measured value = 1.33 mA maximum. Write line current can be any value between zero milliamps and one point three milliamps.</td>
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<td><strong>Test $I_W$ &quot;1&quot;</strong></td>
<td>Write line current with write line at logic &quot;1&quot;: measured value = 100 μA maximum. Write line current can be any value between zero microamps and one hundred microamps.</td>
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<td><strong>Test $B V_w$</strong></td>
<td>Breakdown voltage of write line: measured value = 5.5V minimum. Write line will not break down until the voltage applied to the write line is increased to a value equal to or greater than five point five volts.</td>
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<td><strong>Test $V_w$ &quot;1&quot;</strong></td>
<td>Threshold voltage of write line in logic &quot;1&quot; condition: measured value = 2.2V minimum. Writing voltage must be any value equal to or greater than two point two volts in order to guarantee writing into the selected cell.</td>
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<td><strong>Test $V_w$ &quot;O&quot;</strong></td>
<td>Threshold voltage of write line in logic &quot;O&quot; condition: measured value = 0.9V maximum. Writing voltage can be any value equal to or less than zero point nine volts in order to guarantee not to write into the selected cell.</td>
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<td>Circuit breakdown voltage: measured value = 7.0V minimum. When eighty four milliamps is forced into the Vcc input (Pin 4) the voltage from Vcc to ground must be equal to or greater than seven point zero volts.</td>
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<td>Write pulse width: measured value = 25 nsec minimum. The write pulse must be high for at least twenty five nanoseconds during the time the X/Y bit selection lines are high in order to guarantee writing. One X-Y location high, all others low, &quot;1&quot; previously stored when testing $S_0$ and &quot;O&quot; previously stored when testing $S_1$.</td>
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DEFINITIONS OF TERMS USED FOR SPECIFYING MEMORY CELL OPERATION (-55°C to +125°C)

Test twr

Write recovery time: measured value = 40 nanoseconds maximum. Write recovery time can be any value between zero and forty nanoseconds. One X-Y location high, all others low, "1" previously stored when testing S₀, and "O" previously stored when testing S₁.

Test Tᵈ on

Output turn-on delay; measured value = 35 nsec maximum. Output turn-on delay can be any value between zero and thirty-five nanoseconds. One X-Y location switched, all others low, "1" previously stored when testing S₁, "O" previously stored when testing S₀.

Test Tᵈ off

Turn-off delay: measured value = 35 nsec maximum. Output turn-off delay can be any value between zero and thirty-five nanoseconds. One X-Y location switched, all others low, "1" previously stored when testing S₁, "O" previously stored when testing S₀.
Fig. 1

Note: Pull-up resistors at the output of sense amplifiers are external.
Fig. 2  HLSTL 16-bit Memory Element

Circuit diagram
Figure 3  Developing Clamp on Data Buss
Input Characteristics of X-Y Select Lines at 25°C
Address Select Line Current Distribution
Idle Mode

NOTE: ONLY SATURATED TRANSISTORS ARE SHOWN.

Figure 5
Figure 6  Diode Analogy for Multiple Emitter Transistor
Address Select Line Current Distribution
"Half Select" Mode

NOTE: ONLY SATURATED TRANSISTORS ARE SHOWN.

Figure 7
Address Select Line Current Distribution
"Full-Select Mode"

NOTE: ONLY SATURATED TRANSISTORS ARE SHOWN.

Figure 8
SWITCHING TEST CIRCUIT AND WAVEFORMS

**Figure 9**

**LOW CURRENT TURN-ON DELAY**

vs. TEMPERATURE

![Graph](image)

**HIGH CURRENT TURN-ON DELAY**

vs. TEMPERATURE

![Graph](image)

**LOW CURRENT TURN-OFF DELAY**

vs. TEMPERATURE

![Graph](image)

**HIGH CURRENT TURN-OFF DELAY**

vs. TEMPERATURE

![Graph](image)
Applications

Figure 20 64-bit Serial Memory

Figure 21 64-bit Serial Memory with Single Rail Input and NRZ Output

Figure 22 64 word n-bit Memory
Write enable

X Address Lines

0 1 2 3 4 5 6 7

Y Address Lines

0 1 2 3 4 5 6 7

Fig. 20

64-bit Memory Element using
4 16-bit KLTTL Memory Elements
Figure 21 64 Bit Serial Memory with Single Rail Input and NRZ Output
Logic Diagram of a 64 word Memory with n bits

Remarks: Quad 2-input Line Driver TNG 5511 can be used for Driver Network and HILTTL Non Inverting Gate TNG 6252 for Decode Network