Sylvania universal high level logic integrated circuits
In the time that Sylvania's two lines of integrated circuits have been available, both SUHL* I and SUHL II have proven to be the highest quality saturated transistor-transistor logic available in the industry.

By early 1965, Sylvania had developed several series of circuits using the unusually efficient basic SUHL I circuit. The computer industry found that it was a low-cost, extremely reliable line that reduced cycle counts without compromising even the severest systems requirements. Today, SUHL I circuits are providing designers with the largest selection of compatible digital functions designed especially for tomorrow's computer systems.

Then in August, 1965, Sylvania announced SUHL II, the first integrated circuit line that satisfies extreme high-speed requirements while allowing all other vital characteristics to maintain their full levels of efficiency. Previously, several other manufacturers had reached comparable speeds, but only at the cost of tradeoffs in noise immunity, logic levels, power drain, temperature stability, fan-out vs. fan-in, or capacitance drive.

Both SUHL lines are characterized by high noise margin, fast speed, high logic swing, high fan-out, low power and capacitance drive capability. And both SUHL lines are interchangeable, pin-for-pin. SUHL is the fastest saturated logic family available today for applications down to 5 nanoseconds.

The diagrams and other information on the following pages provide important facts on all Sylvania SUHL circuits.

*Sylvania Universal High Level Logic

**> Automated 14-point probe test.
The SUHL TTL integrated circuit line is designed to serve all logic requirements of typical computer systems. All SUHL circuits are characterized into two temperature ranges: −55°C to +125°C for military applications and 0°C to +75°C for industrial and commercial use. Further, the designer has a choice of standard or prime fanout capability within each temperature range. All other electrical parameters and all pin connections are compatible, thereby allowing a single logic-system design to be applicable to either military or industrial markets. And, all SUHL I circuits are designed for applications up to and including 20 megacycles, with gate propagation delays in the range of 10 nanoseconds.

**High Noise Immunity**
Every circuit in the line contains an additional level-shifting transistor to permit positive or negative noise immunity of over 1 volt at 25°C and 500 mv at 125°C. Operating on a single power supply of +5.0 volts, the circuits provide a logic swing of greater than 3 volts.

**High Fan-Out**
As a direct result of Sylvania's buried-layer diffusion process, all SUHL integrated circuits have output transistors with very low Vce(SAT). This provides fan-out capability as high as 20, with various types ranging from 6 minimum to 16 minimum. The unique design of the line driver provides fanouts as high as 40 without sacrifice of speed or noise immunity. An active transistor pull-up network in the output of each circuit allows rapid charging of capacitance loads. The output is at very low impedance in either the ON or OFF state, which greatly minimizes the pick up of noise. Also, absolute short-circuit protection is built into every circuit as a result of a series resistor in the pull-up network.

**Low Power Dissipation**
All SUHL circuits are designed with an extremely low speed-power product. With 20 megacycle switching speeds, the power dissipation per gate is only 15 milliwatts—a direct benet of Sylvania’s ultra-fine masking technology. In addition, all circuits have transistor-transistor logic inputs which provide the logic capabilities and features of conventional diode-transistor logic, but offer considerably higher speed than DTL inputs.

**High Fan-In**
By utilizing low cost expanders, SUHL integrated circuits are able to provide fan-in capabilities as high as 18. Use of optimized TTL input geometries and special processes keep input leakage currents very low. These currents have a minimal effect on the logic “1” level of the driving gate due to the self compensating effect of the active pull-up network. Further, the level-shifting amplifier circuit between the input and output of the gate provides complete independence of fan-in from fan-out, eliminating the need for interaction rules.

Sylvania’s optimum utilization of the combination of buried-layer diffusion and epitaxy results in very low Vce (SAT), low capacitance, high voltage breakdowns and very high frequency performance. Extremely small geometries and dimensional tolerances on the order of one-half micron (.00002”), make the parasitic capacitances so small they are less than equal to the stray capacitances of equivalent discrete component circuits.

**SUHL I Basic Circuit**

![SUHL I Basic Circuit](image)
## Typical Characteristics (+25°C, ±5 volts)

### SUHL I Typical Characteristics (+25°C, ±5.0 volts)

<table>
<thead>
<tr>
<th>Function</th>
<th>Type Nos.</th>
<th>Ipd (nsec)</th>
<th>Avg. Power (mw)</th>
<th>Noise Immunity (+/−(volts))</th>
<th>Military Prime FO</th>
<th>Military Std. FO</th>
<th>Industrial Prime FO</th>
<th>Industrial Std. FO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual 4-Input NAND/NOR Gate</td>
<td>SG-40, SG-41, SG-42, SG-43</td>
<td>10</td>
<td>15</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Expandable Quad 2-Input OR Gate</td>
<td>SG-50, SG-51, SG-52, SG-153</td>
<td>12</td>
<td>30</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Single 8-Input NAND/NOR Gate</td>
<td>SG-60, SG-61, SG-62, SG-63</td>
<td>12</td>
<td>15</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Exclusive-OR with Complement</td>
<td>SG-90, SG-91, SG-92, SG-93</td>
<td>11</td>
<td>35</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Expandable Triple 3-Input OR Gate</td>
<td>SG-100, SG-101, SG-102, SG-103</td>
<td>12</td>
<td>25</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Expandable Dual 4-Input OR Gate</td>
<td>SG-110, SG-111, SG-112, SG-113</td>
<td>12</td>
<td>20</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Expandable Single 8-Input NAND/NOR Gate</td>
<td>SG-120, SG-121, SG-122, SG-123</td>
<td>18</td>
<td>15</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Dual 4-Input Line Driver/ Lamp Driver</td>
<td>SG-130, SG-131, SG-132, SG-133</td>
<td>25</td>
<td>30</td>
<td>1.1</td>
<td>1.5</td>
<td>30</td>
<td>15</td>
<td>24</td>
</tr>
<tr>
<td>Quad 2-Input NAND/NOR Gate</td>
<td>SG-140, SG-141, SG-142, SG-143</td>
<td>10</td>
<td>15</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Quad 2-Input OR Expander</td>
<td>SG-150, SG-151, SG-152, SG-153</td>
<td>4</td>
<td>20</td>
<td>1.1</td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Triple 2-Input Bus Driver</td>
<td>SG-160, SG-161, SG-162, SG-163</td>
<td>15</td>
<td>15</td>
<td>1.1</td>
<td>1.5</td>
<td>15</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td>Dual 4-Input OR Expander</td>
<td>SG-170, SG-171, SG-172, SG-173</td>
<td>3</td>
<td>5</td>
<td>1.1</td>
<td>1.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dual 4-Input AND Expander</td>
<td>SG-180, SG-181, SG-182, SG-183</td>
<td>1.1</td>
<td>1.5</td>
<td>22</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Typical Curves

- **Average Propagation Delay Time vs. Capacitance Loading**
  - At +5V, 25°C
  - SUHL I

- **Output Voltage vs. Input Voltage**
  - VCC = +5.0 V
  - IOUT = +20 mA
  - IOUT = −1.5 mA
  - TA = +25°C

![Typical Curves](image-url)
General Characteristics for all SUHL I Elements

<table>
<thead>
<tr>
<th>Absolute Maximum Ratings</th>
<th>Military</th>
<th>Industrial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>8</td>
<td>7</td>
<td>Vdc</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-55° to +125°</td>
<td>0° to +75°</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65° to +200°</td>
<td>-65° to +200°</td>
<td>°C</td>
</tr>
</tbody>
</table>

Electrical Characteristics at 25° C, Vcc = 5V

<table>
<thead>
<tr>
<th>Input Characteristics</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic 1 Voltage</td>
<td>1.7</td>
<td>5.5</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Logic 1 Current</td>
<td>100</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Logic 0 Voltage</td>
<td>1.2</td>
<td></td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Logic 0 Current</td>
<td>1.0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Capacitance</td>
<td>2.0</td>
<td></td>
<td></td>
<td>pf</td>
</tr>
<tr>
<td>Positive Noise Immunity*</td>
<td>1.0</td>
<td></td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Negative Noise Immunity</td>
<td>1.0</td>
<td></td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Frequency</td>
<td>20</td>
<td></td>
<td></td>
<td>mcs</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Output Characteristics</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic 1 Voltage²</td>
<td>3.0</td>
<td>3.5</td>
<td>3.8</td>
<td>Volts</td>
</tr>
<tr>
<td>Logic 0 Voltage</td>
<td>0.26</td>
<td>0.45</td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>10</td>
<td></td>
<td>45.0</td>
<td>mA</td>
</tr>
<tr>
<td>Propagation Delay Time/Gate</td>
<td>10</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

Fan-Out

1. Noise immunity is that voltage superimposed on the input which will not propagate beyond the following stage. *2. With max Logic 0 on input.
Set-Reset Flip-Flop

Two-Phase SR Clocked Flip-Flop

Single-Phase SRT Flip-Flop

J-K Flip-Flop (AND Inputs)

J-K Flip-Flop (OR Inputs)
Sylvania’s new line of high speed saturated digital logic circuits—SUHL-II—solves high speed system requirements without compromising system performance characteristics. Consisting of totally compatible 6 nanosecond gates and 30 megacycle J-K flip-flops, the new line is designed to operate from a single 5-volt power supply. All SUHL-II circuits have high noise immunity, fan-out, and capacitance drive capability. And, extra packages are not required to restore logic levels or noise margin at the system level.

Stable logic swings have been maintained through use of saturated logic. This results in stable propagation times over broad operating temperature excursions without recourse to additional bias supplies, complex loading rules, and external clamping and shielding. Also, low power OR expansion is accomplished without degradation of fan-out and without capacitively loading the gate output.

All SUHL-II circuits are totally compatible with and may be used in conjunction with all standard SUHL circuits.

The SUHL-II line is available in two package configurations: The Sylvania-designed 14-lead flat pack, and Sylvania’s new hermetically sealed 14-lead plug-in package.

**Features:**

- High speed saturated logic:
  - 6 Nsec gates, 30Mc J-K flip-flops
  - High noise immunity: $+1.0$ Volts @ 25°C
  - High logic swing: Logic "0"=0.25V
  - Logic "1"=3.5V
- No logic level restorations necessary
- Single 5V power supply
- Two operating temperature ranges:
  - Military $-55^\circ$C to $125^\circ$C
  - Industrial $0^\circ$C to $+75^\circ$C
- Low power drain independent of fan-in or fan-out; typically 22MW/gate function

- Capacitance drive capability designed into all circuits
- No complex loading rules, inputs and outputs isolated
- Low output impedance, saturated logic; not subject to oscillations
- Low power wired-OR expansions without fan-out degradation
- Completely compatible with and can be intermixed with all standard SUHL circuits

**SUHL-II Basic Circuit**

---

**SUHL-II speed**

Vertical-1V/cm  
Horizontal-20nsec/cm  
A-output from SUHL II gate  
B-output from SUHL II J-K flip flop  
C-output from last gate
**SUHL II TYPICAL CHARACTERISTICS (+25°C, ±5.0 volts)**

<table>
<thead>
<tr>
<th>Function</th>
<th>Type Nos.</th>
<th>tpd (nsec)</th>
<th>Avg. Power (mw)</th>
<th>Noise Immunity ±(volts)</th>
<th>Military Prime FO Std. FO</th>
<th>Industrial Prime FO Std. FO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Expandable Dual 4-Input OR Gate</td>
<td>SG-210, SG-211, SG-212, SG-213</td>
<td>7</td>
<td>30</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>Quad 2-Input NAND/NOR Gate</td>
<td>SG-220, SG-221, SG-222, SG-223</td>
<td>6</td>
<td>22</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>Quad 2-Input OR Expander</td>
<td>SG-230, SG-231, SG-232, SG-233</td>
<td>2</td>
<td>28</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>Dual 4-Input NAND/NOR Gate</td>
<td>S-240, SG-241, SG-242, SG-243</td>
<td>6</td>
<td>22</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>Expandable Quad 2-Input OR Gate</td>
<td>SG-250, SG-251, SG-252, SG-253</td>
<td>7.5</td>
<td>43</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>Single 8-Input NAND/NOR Gate</td>
<td>SG-260, SG-261, SG-262, SG-263</td>
<td>6</td>
<td>22</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>Dual 4-Input OR Expander</td>
<td>SG-270, SG-271, SG-272, SG-273</td>
<td>2</td>
<td>6.7</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>J-K Flip-Flop (AND Inputs)</td>
<td>SF-250, SF-251, SF-252, SF-253</td>
<td>30mc</td>
<td>55</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
<tr>
<td>J-K Flip-Flop (OR Inputs)</td>
<td>SF-260, SF-261, SF-262, SF-263</td>
<td>30mc</td>
<td>55</td>
<td>1.0</td>
<td>1.5</td>
<td>11</td>
</tr>
</tbody>
</table>

**Typical Curves**

**AVERAGE PROPAGATION DELAY TIME VS CAPACITANCE LOADING**

**AT +5V, 25°C**

SUHL II
Packaging

All Sylvania Integrated Circuits are available in two package configurations: the Sylvania-designed 14-lead flat pack and Sylvania's new Plug-in Package. Both alumina filled glass packages use high temperature glass seals. In addition, the package coefficient of expansion precisely matches that of the Kovar leads. All SUHL-I and SUHL-II integrated circuits are manufactured under super-clean and controlled ambient conditions to insure highest reliability. Assembly is accomplished with an all aluminum wire-bonding system that completely eliminates unpredictable "opens" caused by the formation of an inter-metallic compound, popularly referred to as "Purple Plague," which occurs when gold is bonded to aluminum in the presence of silicon.

Every sealed circuit is sequentially processed through +300°C temperature aging, -55°C to +125°C temperature-cycling, 20,000 g centrifuge and leak testing to assure the user of the highest degree of product integrity.

14 Lead Flat Pack

Sylvania's new 14-lead flat pack is manufactured using high temperature, hard glass seals. The monolithic chips are brazed directly to a Kovar base plate providing a thermal resistance of 0.1°C/mw from junction to case. Pin connections are designed for optimum systems simplification with regard to inputs, outputs and cross-overs. Further, the same pin numbers are used for B+ and ground on every circuit, and these power-supply and ground pins are offset to avoid burn-out if the package is inadvertently mounted upside down.

Sylvania Plug-in Package

Sylvania's new Plug-in Package is specifically designed for low cost assembly in two-sided printed circuit boards. The alumina filled glass package provides extremely low thermal resistance and features a Kovar base plate with up-from-the-chip bonding and gold plated Kovar leads formed into a 0.020" diameter for both strength and reliable solderability. The 100 mil pin centers permit both broad drill tolerances and wide printed circuit lines while the leads provide a 0.035" standoff for venting. The SUHL plug-in package leads form two seven pin rows, 300 mils apart along the sides of the package. Consequently, an installed package is readily accessible for in-place checkout.
Every sealed SUHL Circuit is 100% sequentially processed through the following Quality Control Tests:

- **Stabilization Bake** . . . . for 60 hours at 300°C to stabilize surfaces and to stress the package

- **Thermal Cycling** . . . . 5 cycles consisting of plunging the package into −55° and +125° air ambient. This test stresses the assembly on a cyclic basis.

- **Centrifuge** . . . . 20,000 g’s in Y1 plane to stress leads and seal

- **Oil Bubble Leak Test** . . . . at 150°C to test hermeticity

- **DC Testing** . . . . to check all DC parameters at rated temperatures

- **AC Testing** . . . . to check switching parameters
SYLVANIA
ELECTRONIC COMPONENTS
GROUP
SALES OFFICES

ATLANTA
2115 Sylvan Road, S.W.
Atlanta, Georgia 30310
404-766-3633

BALTIMORE
31 Allegheny Avenue
Towson 4, Maryland 21204
301-623-2550

CHICAGO
2110 North Cornell Avenue
Melrose Park, Illinois 60160
312-345-0100

CLEVELAND
4848 West 130th Street
Cleveland, Ohio 44135
216-252-0500

DALLAS
100 Fordyce Street
Dallas, Texas 75207
214-741-4836

DAYTON
333 West First Street
Dayton, Ohio 45402
513-223-6227

DETROIT
10800 Ford Road
Dearborn, Michigan 48126
313-582-8754

FLORIDA
1520 Edgewater Drive
Orlando, Florida 32804
305-241-9681

FORT WAYNE
4740 Coldwater Road
Fort Wayne, Indiana 46805
219-483-1145

LOS ANGELES
6505 East Gayhart Street
Los Angeles, California 90054
213-723-5371

MASSACHUSETTS
Lakeside Office Park, North Avenue
Wakefield, Mass. 01880
617-245-6840

MINNEAPOLIS
2211 E. Hennepin Street
Minneapolis, Minnesota 55413
612-331-9363

NEW ORLEANS
5510 Jefferson Highway
New Orleans, Louisiana 70123
504-339-6970

NEW YORK
1000 Huyler Street
Teterboro, New Jersey 07602
201-298-9484

NEW YORK—UPSTATE
Johnson Street
Seneca Falls, New York 13138
315-568-5881

PHILADELPHIA
4700 Parkside Avenue
Philadelphia, Pennsylvania 19131
215-477-5000

PITTSBURGH
300 Mount Lebanon Boulevard
Pittsburgh, Pennsylvania 15234
412-531-4974

ST. LOUIS
5010 Kemper Avenue
St. Louis, Missouri 63139
314-664-8974

SAN FRANCISCO
1811 Adrian Road
Burilingame, California 94010
415-697-3500

SYRACUSE
5700 West Genesee Street
Camillus, New York 13031
315-672-3111

WASHINGTON, D.C.
1120 Connecticut Avenue, N.W.
Washington, D.C. 20036
202-337-6600

INTERNATIONAL
730 Third Avenue
New York, N. Y. 10017
212-551-1000

CANADA
6233 Cote de Liesse Road
Monreal 9, Quebec, Canada
514-631-4201

EUROPE, AFRICA, NEAR EAST
21—Rue du Rhone
Geneva, Switzerland

MANUFACTURING
SEMICONDUCTOR DIVISION
Woburn, Mass. 01801
617-933-3500

SYLVANIA
SUBSIDIARY OF
GENERAL TELEPHONE & ELECTRONICS GTE