Asynchronous Communication Interface Adapter (ACIA)

The R6551 Asynchronous Communication Interface Adapter (ACIA) provides a program-controlled interface between 8-bit microprocessor-based systems and serial communication data sets and modems.

With its on-chip baud rate generator, the R6551 is capable of transmitting 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16 times an external clock rate. The R6551 has programmable word lengths of 5, 6, 7, or 8 bits; even, odd or no parity; 1, 1/2, or 2 stop bits.

With the R6551, a crystal is the only required external support component — eliminating the multiple-component support that is typically needed.

In addition, the R6551 is designed for maximum programmed control from the CPU, to simplify hardware implementation. A control register and a separate command register permit the CPU to easily select the R6551’s operating modes and check data, parameters and status.

**Ordering Information**

<table>
<thead>
<tr>
<th>Order Number</th>
<th>Package Type</th>
<th>Frequency</th>
<th>Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>R6551P</td>
<td>Plastic</td>
<td>1 MHz</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>R6551AP</td>
<td>Plastic</td>
<td>2 MHz</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>R6551C</td>
<td>Ceramic</td>
<td>1 MHz</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>R6551AC</td>
<td>Ceramic</td>
<td>2 MHz</td>
<td>0°C to +70°C</td>
</tr>
</tbody>
</table>

**Features**

- Compatible with 8-bit microprocessors
- Full duplex or half duplex operation with buffered receiver and transmitter
- 15 programmable Baud Rates (50 to 19,200)
- Receiver data rate may be identical to baud rate or may be 16 times the external clock input
- Data set/modem control functions
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Software reset
- Program-selectable serial echo mode
- Two chip selects
- 2 MHz or 1 MHz clock rate
- Single +5V ±5% power supply
- 28-pin plastic or ceramic DIP
- Full TTL compatibility

**R6551 Pin Configuration**

- **VSS**
  - 1
  - 28: R/W
  - 29: D2
  - 30: TRG
- **CS0**
  - 2
  - 27: I/R
- **CS1**
  - 3
  - 26: D7
- **RES**
  - 4
  - 25: D6
- **RXD**
  - 5
  - 24: D5
- **TXD**
  - 6
  - 23: D4
- **RS0**
  - 7
  - 22: D3
- **CTS**
  - 8
  - 21: D2
- **DSR**
  - 9
  - 20: D1
- **DTR**
  - 10
  - 19: DO
- **RTS**
  - 11
  - 18: D0
- **DSR**
  - 12
  - 17: D9
- **DTR**
  - 13
  - 16: D8
- **RXD**
  - 14
  - 15: VCC

**R6551 Interface Diagram**
INTERNAL ORGANIZATION

R6551 Block Diagram

Transmitter/Receiver

Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then RxC becomes an output pin and can be used to slave other circuits to the R6551.

Transmitter/Receiver Clock Circuits

Transmit and Receive Data Registers

These registers are used as temporary data storage for the 6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

- Bit 0 is the leading bit to be transmitted.
- Unused data bits are the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

- Bit 0 is the leading bit received.
- Unused data bits are the high-order bits and are "0" for the receiver.
- Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Control Register

The Control Register selects the desired baud rate, frequency source, word length, and the number of stop bits.

Command Register

The Command Register controls specific modes and functions.
**Status Register**

The Status Register reports the status of various R6551 functions.

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parity Error*</td>
<td>0 = No Parity Error</td>
<td>1 = Parity Error Detected</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Framing Error*</td>
<td>0 = No Framing Error</td>
<td>1 = Framing Error Detected</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overrun*</td>
<td>0 = No Overrun</td>
<td>1 = Overrun Has Occurred</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receiver Data Register Full</td>
<td>0 = Not Full</td>
<td>1 = Full</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transmitter Data Register Empty</td>
<td>0 = Not Empty</td>
<td>1 = Empty</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Carrier Detect (DCD)</td>
<td>0 = DCD low (Detect)</td>
<td>1 = DCD high (Not Detect)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data Set Ready (DSR)</td>
<td>0 = DSR low (Ready)</td>
<td>1 = DSR high (Not Ready)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interrupt (IRQ)</td>
<td>0 = No Interrupt</td>
<td>1 = Interrupt Has Occurred</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R6551 Status Register

**INTERFACE SIGNAL DESCRIPTION**

**RES (Reset)**

During system initialization a low on the RES input will cause internal registers to be cleared.

**Q2 (Input Clock)**

The input clock is the system Q2 clock and is used to synchronize all data transfers between the system microprocessor and the R6551.

**R/W (Read/Write)**

The R/W is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/W pin allows the processor to read the data supplied by the R6551. A low on the R/W pin allows a write to the R6551.

**IRQ (Interrupt Request)**

The IRQ pin is an interrupt output from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common IRQ microprocessor input. Normally a high level, IRQ goes low when an interrupt occurs.

**D0-D7 (Data Bus)**

The D0-D7 pins are the eight data lines used to transfer data between the processor and the R6551. These lines are bi-directional and are normally high-impedance, except during Read cycles when the R6551 is selected.

**CS0, CS1 (Chip Selects)**

The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The R6551 is selected when CS0 is high and CS1 is low.

**RS0, RS1 (Register Selects)**

The two register select lines are normally connected to the processor address lines to allow the processor to select the various R6551 internal registers. The following table indicates the internal register select coding:

<table>
<thead>
<tr>
<th>RS1</th>
<th>RS0</th>
<th>Write</th>
<th>Read</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Transmit Data Register</td>
<td>Receiver Data Register</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Programmed Reset (Data is &quot;Don't Care&quot;)</td>
<td>Status Register</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Command Register</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Control Register</td>
<td></td>
</tr>
</tbody>
</table>

Note that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear Bits 0 through 4 in the Command Register and Bit 2 in the Status Register. The Programmed Reset is slightly different from the Hardware Reset (RES); these differences are described in the individual register definitions.

**ACIA/Modem Interface Signal Description**

**XTLI, XTLQ (Crystal Pins)**

These pins are normally directly connected to the external crystal (1.8432 MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTLQ pin, in which case the XTLQ pin must float. XTLI is the input pin for the transmit clock.

**TxD (Transmit Data)**

The TxD output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected, or under control of an external clock (as selected by the Control Register).

**RxD (Receive Data)**

The RxD input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock (as selected by the Control Register).

**RxC (Receive Clock)**

The RxC is a bi-directional pin which serves as either the receiver 16x clock input or the receiver 16x clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.
**RTS (Request to Send)**

The RTS output pin is used to control the modem from the processor. The state of the RTS pin is determined by the contents of the Command Register.

**CTS (Clear to Send)**

The CTS input pin is used to control the transmitter operation. The enable state is with CTS low. The transmitter is automatically disabled if CTS is high.

**DTR (Data Terminal Ready)**

This output pin is used to indicate the status of the R6551 to the modem. A low on DTR indicates the R6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

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**DSR (Data Set Ready)**

The DSR input pin is used to indicate to the R6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready". DSR is a high-impedance input and must be connected. If unused, it should be driven high or low, but not switched.

**DCD (Data Carrier Detect)**

The DCD input pin is used to indicate to the R6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. Like DSR, DCD is a high-impedance input, and must be connected.

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**READ/WRITE CYCLE CHARACTERISTICS**

\(^{(V_{CC} = 5.0 \pm 5\%, T_A = 0 \text{ to } 70^\circ C, \text{ unless otherwise noted)}}\)

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>1 MHz</th>
<th>2 MHz</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td><strong>Min</strong></td>
<td><strong>Max</strong></td>
<td><strong>Min</strong></td>
</tr>
<tr>
<td>Cycle Time</td>
<td>t\text{CYC}</td>
<td>1.0</td>
<td>40</td>
<td>0.5</td>
</tr>
<tr>
<td>\O Pulse Width</td>
<td>t\text{C}</td>
<td>400</td>
<td>–</td>
<td>200</td>
</tr>
<tr>
<td>Address Set-Up Time</td>
<td>t\text{AC}</td>
<td>120</td>
<td>–</td>
<td>70</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>t\text{CAH}</td>
<td>0</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>R/W Set-Up Time</td>
<td>t\text{WC}</td>
<td>120</td>
<td>–</td>
<td>70</td>
</tr>
<tr>
<td>R/W Hold Time</td>
<td>t\text{CWH}</td>
<td>0</td>
<td>–</td>
<td>0</td>
</tr>
<tr>
<td>Data Bus Set-Up Time</td>
<td>t\text{DCW}</td>
<td>150</td>
<td>–</td>
<td>60</td>
</tr>
<tr>
<td>Data Bus Hold Time</td>
<td>t\text{HW}</td>
<td>20</td>
<td>–</td>
<td>20</td>
</tr>
<tr>
<td>Read Access Time (Valid Data)</td>
<td>t\text{CDR}</td>
<td>–</td>
<td>200</td>
<td>–</td>
</tr>
<tr>
<td>Read Hold Time</td>
<td>t\text{HR}</td>
<td>20</td>
<td>–</td>
<td>20</td>
</tr>
<tr>
<td>Bus Active Time (Invalid Data)</td>
<td>t\text{CDA}</td>
<td>40</td>
<td>–</td>
<td>40</td>
</tr>
</tbody>
</table>

\((t_f\text{ and } t_f = 10 \text{ to } 30 \text{ ns})\)

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![Timing Diagram](image)

Write Timing Characteristics

Read Timing Characteristics
TRANSMIT/RECEIVE CHARACTERISTICS

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>1 MHz</th>
<th>2 MHz</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit/Receive Clock Rate</td>
<td>t_{CCY}</td>
<td>400*</td>
<td>400*</td>
<td>ns</td>
</tr>
<tr>
<td>Transmit/Receive Clock High Time</td>
<td>t_{CH}</td>
<td>175</td>
<td>175</td>
<td>ns</td>
</tr>
<tr>
<td>Transmit/Receive Clock Low Time</td>
<td>t_{CL}</td>
<td>175</td>
<td>175</td>
<td>ns</td>
</tr>
<tr>
<td>XTLI to TxD Propagation Delay</td>
<td>t_{DD}</td>
<td>-</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>RTS Propagation Delay</td>
<td>t_{DLY}</td>
<td>-</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>IRQ Propagation Delay (Clear)</td>
<td>t_{IRQ}</td>
<td>-</td>
<td>500</td>
<td>500</td>
</tr>
</tbody>
</table>

\[ t_r, t_f = 10 \text{ to } 30 \text{ ns} \]

The baud rate with external clocking is:

\[
\text{Baud Rate} = \frac{1}{16 \times T_{CCY}}
\]

NOTE: TxD rate is 1/16 TxC rate

Transmit Timing with External Clock

\[ \phi_2 \]

Interrupt and Output Timing

Receive External Clock Timing

PACKAGE OUTLINES

28 LEAD CERAMIC

28 LEAD PLASTIC