NCL2020 - FLOPPY DISK CONTROLLER

GENERAL DESCRIPTION

The NCL2020 is a single chip, floppy disk controller for the PC/AT compatible systems. It combines the industry standard FDC, analog data separator, write precompensation, clock generation, data rate selection and all Host/Drive interface drivers/receivers. The NCL2020 provides all control and communications between the host and floppy drive(s).

FEATURES

- IBM PC/AT compatible format and bus interface
- IBM PC/AT compatible commands and register
- DMA/PIO data transfer
- Embedded address decoder for chip and register select
- No adjustment, no external components analog VCO
- Programable data transfer rates (250,300,500Kb)
- Embedded drivers/receivers for both host and drive
- Recalibrate up to 77 tracks
- Data scan function
- Supports overlap seek
- Supports up to 2 drives
- Full CMOS LSI
- Single +5 volt supply
- Single 24Mhz crystal input
- Available in 100 pin flat pack
- Controls 5.25" and 3.5" drives

100 pin flat pack
FUNCTIONAL DESCRIPTION

**FDC** - Industry standard floppy disk controller. Recalibrate up to 77 cylinders.

**Data Separator** - Generates the window for data separation from raw read data (MFM). Includes phase comparator to generate VCO control signal.

**VCO** - Voltage controlled oscillator. Center frequency is 4Mhz with 1.25mhz/v sensitivity.

**OSC/Divider** - Generates all clocks for each function block from external 24Mhz crystal. Divider is programmable for the different data rates.

**Address Decoder** - Address decode for chip select and task register select. Decodes both primary and secondary addresses.

**Host Interface Driver/Receiver** - Bi-directional Bus driver/receiver. Bus drive capability is 12mA TTL.

**Drive Interface Driver/Receiver** - FDD drive interface drivers/receivers. Drive capability is 38mA. Schmitt Trigger line receivers.

**Register** - Consists of diskette control register and digital input/output register

**Drive Interface Control** - Logic to control floppy disk(s) and generate proper write pre-compensation.
NCL2020 - FLOPPY DISK CONTROLLER

TYPICAL APPLICATION
(PC/AT)
## PIN ASSIGNMENTS

<table>
<thead>
<tr>
<th>PIN#</th>
<th>NAME</th>
<th>PIN#</th>
<th>NAME</th>
<th>PIN#</th>
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<th>NAME</th>
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<td>TVF8</td>
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<td>INDEX</td>
<td>51</td>
<td>DRL</td>
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<td>A6</td>
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<td>TVF5</td>
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<td>VSS3K</td>
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<td>VSS3F</td>
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<td>WPRT</td>
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<td>STPL</td>
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<td>A4</td>
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<td>VDD5C</td>
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<td></td>
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<td>25</td>
<td>REDT</td>
<td>50</td>
<td>VSS3J</td>
<td>75</td>
<td>A5</td>
<td>100</td>
<td>VSS5C</td>
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</table>

## I/O PIN DESCRIPTION

### Host interface

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0 to A9</td>
<td>PC/AT buss address lines (input)</td>
</tr>
<tr>
<td>DB0 to DB7</td>
<td>Bi-directional, Tri-stated data buss (input/output)</td>
</tr>
<tr>
<td>RD/</td>
<td>Low true, signal to read data or status of LSI (input)</td>
</tr>
<tr>
<td>WR/</td>
<td>Low true, signal to write data or command to LSI (input)</td>
</tr>
<tr>
<td>AEN</td>
<td>Address enable from host. Held true during DMA transfer (input)</td>
</tr>
<tr>
<td>DRQ</td>
<td>Data request for DMA mode (output)</td>
</tr>
<tr>
<td>INT</td>
<td>Set true when the command execution is completed (output)</td>
</tr>
</tbody>
</table>

### DACK/

Low true, acknowledged data request, DRQ (output)

### TC

Request for data transfer termination (output)

### SRES

System reset (input)

### RESET

Internal reset signal, used for power on reset (input)

### DECE

Set true, enables internal address decoder (input)

### CS/

Low true, chip select. Signal valid only when DECE set low (input)

### PA2D

Selects primary or secondary address for internal address decoder (input)

- Low = 3FXh
- High = 37Xh
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Drive Interface

DIRL
Sets direction of head movement (output)
  Low = toward spindle/ID
  High = away from spindle/OD

STPL
Low active, pulse for track to track actuator movement (output)

HSSL
Head select (output)
  Low = head 1
  High = head 0

MOT1
Motor on for drive 0 (output)

MOT2
Motor on for drive 1 (output)

DSL1
Low active, selects drive 0 (output)

DSL2
Low active, selects drive 1 (output)

REWL/DENS
Density select (output)
  High = high density
  Low = standard density

POLT
Tied high, inverts REWL/DENS signal

WRDT
Write data, serial clock and data bits to selected drive (output)

WRGT
Low active, enables write operation to selected drive (output)

TRK0
Low active, drive at track 0 (input)

READY
Low active, drive is ready for seek, read or write (input)

INDEX
Low active, drive heads are at beginning of track (input)

REDT
Read data, raw data from selected drive (input)

WRPT
Low active, drive media is write protected (input)

NOTE:

TVFS/TVF6
Manufacturing test pins, must be connected together for normal operation

Power Pins

VDD5A, VDD5B, VDD5C, VDD6
Digital, +5 volt supply

VSS5A, VSS5B, VSS5C, VSS6
Digital, GND

VDD4A, VDD4B, VDD4C
Tri-state, +5 volt supply

VSS4A, VSS4B, VSS4C
Tri-state, GND

VDD1
VFO/analog, +5 volt supply

VSS1
VFO/analog, GND

VDD2, VDD2A
Oscillator, +5 volt supply

VSS2
Oscillator, GND

VDD3
38mA drive, +5 volt supply

VSS3A to VSS3K
38mA drive, GND

NCL2020 Write Precomp Values

125ns @ 500KB
208ns @ 300KB
250ns @ 250KB
INTERNAL REGISTERS

NCL2020 controller, PC/AT compatible register addresses.

Register Address

<table>
<thead>
<tr>
<th>PRI</th>
<th>SEC</th>
<th>READ</th>
<th>WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>3F2</td>
<td>372</td>
<td>------</td>
<td>digital output</td>
</tr>
<tr>
<td>3F4</td>
<td>374</td>
<td>main status</td>
<td>main status</td>
</tr>
<tr>
<td>3F5</td>
<td>375</td>
<td>diskette data</td>
<td>diskette data</td>
</tr>
<tr>
<td>3F6</td>
<td>376</td>
<td>------</td>
<td>fixed disk</td>
</tr>
<tr>
<td>3F7</td>
<td>377</td>
<td>digital input</td>
<td>diskette control</td>
</tr>
</tbody>
</table>

Digital Output Register

The digital output register is an output only register used to control drive motor(s), drive selection and feature enable.

Bit 7 reserved
Bit 6 reserved
Bit 5 motor enable, drive 1
Bit 4 motor enable, drive 0
Bit 3 enable interrupts and DMA
Bit 2 reset
Bit 1 reserved
Bit 0 drive select (0=0)

Digital Input Register

The digital input register is a read only register. Only bit 7 is utilized in the floppy control.

Bit 7 diskette change
Bit 6 fixed disk
Bit 5
Bit 4
Bit 3
Bit 2
Bit 1
Bit 0 fixed disk

Diskette Control Register

The diskette control register is used to select the desired data rates which controls the internal clock generation. Only bits 1 and 0 are used.

<table>
<thead>
<tr>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>= 500Kbit</td>
</tr>
<tr>
<td>0 1</td>
<td>= 300Kbit</td>
</tr>
<tr>
<td>1 0</td>
<td>= 250Kbit</td>
</tr>
</tbody>
</table>

Main Status Register

The main status register contains the status information of the selected floppy drive and may be accessed at any time.

Bit 7 request for master
Bit 6 data input/output (0=data from host)
Bit 5 non DMA mode
Bit 4 FDC busy
Bit 3 reserved
Bit 2 reserved
Bit 1 drive 1 busy
Bit 0 drive 0 busy

Status Register 0

Bit 7,6 interrupt code
00 = normal termination
01 = abrupt termination
10 = invalid command
11 = abnormal termination

Bit 5 seek end (1=seek complete)
Bit 4 equipment check (1=fault/no trk 0)
Bit 3 not ready
Bit 2 head address
Bit 1 unit select 1
Bit 0 unit select 0

Status Register 1

Bit 7 end of cylinder
Bit 6 not used
Bit 5 data error (CRC)
Bit 4 overrun
Bit 3 not used
Bit 2 no data/sector
Bit 1 not writeable
Bit 0 missing address mark

Status Register 2

Bit 7 not used
Bit 6 control mark
Bit 5 data error (data field)
Bit 4 wrong cylinder
Bit 3 scan equal hit
Bit 2 scan not satisfied
Bit 1 bad cylinder
Bit 0 missing address mark (data field)
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Status Register 3

- Bit 7: fault
- Bit 6: write protected
- Bit 5: ready
- Bit 4: track 0
- Bit 3: two sided
- Bit 2: head address
- Bit 1: unit select 0
- Bit 0: unit select 1

NCL2020 COMMAND SET

Compatible to industry standard 765 FDC, the NCL2020 is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the host and the result of the command may also be a multibyte transfer back to the host. With multibyte transfers, each command has three phases; command, execution and result phase.

Command Phase - FDC receives all information required to perform a particular operation.
Execution Phase - FDC performs the operation it was told to do.
Result Phase - After the operation is complete, status and other information are made available to the host.

COMMANDS

- Read Data
- Read Deleted Data
- Write Data
- Write Deleted Data
- Read ID
- Format A Track
- Read A Track
- Scan Equal
- Scan Low or Equal
- Scan High or Equal
- Seek
- Recalibrate
- Sense Interrupt Status
- Sense Device Status
- Specify

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings
- Power supply VDD: -0.5 to 7.0 volts
- Input voltage VI: -0.5 to VDD +/-0.5volts
- Output voltage VO: -0.5 to VDD +/-0.5volts
- Operating current: 70 mA
- Operating temperature: 0 C to 65 C
- Storage temperature: -65 C to 150 C
- Lead temperature: 260 C for max. of 10 sec.

DC Characteristics
- VDD = 5v +/-5%, 0 to 65 C
- VDC supply VDD: 4.75 to 5.25 vdc
- High level input voltage VIH: 2.0 to VDD +/-0.3v
- Low level input voltage VIL: -0.3 to 0.8v
- High level output voltage VOH: 2.4 to VDDv
- Low level output voltage VOL: 0.0 to 0.4v
- Low level output current VOLD: 38mA @ 0.4v
- Supply current ICC: TBA
- Tristate
  - High level output voltage VOHT: -3mA @ 4.0v
  - Low level output voltage VOLT: 12mA @ 0.4v
- Schmitt Trigger
  - Input voltage
    - VT+ = 1.6 to 2.0v
    - VT- = 0.9 to 1.3v
NCL2020 TIMING DIAGRAMS

RESET, SRES TIMING

**NOTE:**
Requires a minimum of 2 ms wait before a read/write to internal registers

COMMAND SET/DATA SET TIMING

- **A0 to A9**
- **DB0 to DB7**
- **WR**
- **RD**
- **AEN**

0 ns minimum

200 ns minimum
STATUS READ/DATA READ TIMING

A0 to A9

DB0 to DB7

WR
RD

AEN

low

80 ns min
0 ns min
200 ns min
0 ns minimum

0 ns min

DMA, WRITE TIMING

DB0 to DB7

DRQ
DACK

WR
RD

AEN
TC

140 ns max
high

0 ns minimum
0 ns min
50 ns min
0 ns min
0 ns min
DMA READ TIMING

DB0 to DB7

80 ns minimum

DRQ
DACK

140 ns max

WR
RD

200 ns min

AEN
TC

0 ns min

50 ns min

50 ns min

SEEK OPERATION TIMING

DSL1,2

2 us min

42 us min

48us min

DIRL

12 us min

66 us min

STPL

10us min

INDEX TIMING

500ns min (500Kbps)
1 us min (250Kbps)

166.7ms +/- 3%
WRITE OPERATION TIMING

<table>
<thead>
<tr>
<th>DENSITY</th>
<th>T1</th>
<th>T2</th>
<th>T3</th>
<th>T4</th>
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<tbody>
<tr>
<td>High Density</td>
<td>150 -</td>
<td>2us</td>
<td>4us</td>
<td>3us</td>
</tr>
<tr>
<td>(500Kbits)</td>
<td>1100ns</td>
<td>+/-10ns</td>
<td>+/-20ns</td>
<td>+/-15ns</td>
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<tr>
<td>Normal Density</td>
<td>150 -</td>
<td>4us</td>
<td>8us</td>
<td>6us</td>
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<tr>
<td>(250Kbits)</td>
<td>2100ns</td>
<td>+/-20ns</td>
<td>+/-40ns</td>
<td>+/-30ns</td>
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<tr>
<td>Normal Density</td>
<td>150 -</td>
<td>3.33us</td>
<td>6.67us</td>
<td>5us</td>
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<tr>
<td>(300Kbits)</td>
<td>1800ns</td>
<td>+/-17ns</td>
<td>+/-33ns</td>
<td>+/-25ns</td>
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<tr>
<td>Format</td>
<td>FM</td>
<td>FM</td>
<td>FM</td>
<td>MFM</td>
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READ OPERATION TIMING

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<tbody>
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<td>High Density</td>
<td>200ns</td>
<td>2us</td>
<td>4us</td>
<td>3us</td>
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<tr>
<td>(500Kbits)</td>
<td>+/-50ns</td>
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<td>+/-800ns</td>
<td>+/-600ns</td>
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<tr>
<td>Normal Density</td>
<td>200ns</td>
<td>4us</td>
<td>8us</td>
<td>6us</td>
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<tr>
<td>(250Kbits)</td>
<td>+/-50ns</td>
<td>+/-800ns</td>
<td>+/-1600ns</td>
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<tr>
<td>Normal Density</td>
<td>200ns</td>
<td>3.33us</td>
<td>6.67us</td>
<td>5us</td>
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<tr>
<td>(300Kbits)</td>
<td>+/-50ns</td>
<td>+/-667ns</td>
<td>+/-1333ns</td>
<td>+/-1000ns</td>
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<tr>
<td>Format</td>
<td>FM</td>
<td>FM</td>
<td>FM</td>
<td>MFM</td>
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</tbody>
</table>
AC CHARACTERISTICS

Power Supply Ripple
VFO supply, 50 mV maximum
Other, 100 mV maximum

Data Separator
Analog "one shot" pulse
-5 to 5% @ VDD = 5v +/-5%
0 to 70 C
VCO center frequency
-10 to 10% @ VDD = 5v +/-5%
0 to 70 C
control voltage = 2v

VCO control voltage variation
1.0 min, 1.25 typ, 1.5Mhz/V max
@ VDD = 5v, 25 C
control voltage = 2 to 3v

Read data detection frequency (00H)
500Kbit/s = 1.42 min, 2.00 typ, 2.58us max
300Kbit/s = 2.35 min, 3.33 typ, 4.30us max
250Kbit/s = 2.68 min, 4.00 typ, 5.16us max

Maximum OSC Frequency
24Mhz @ VDD = 5v +/-5%
0 to 70 C
NCL2020 - FLOPPY DISK CONTROLLER

DATA WINDOW TIMING

READ DATA

ONE SHOT OUTPUT

Phase Comparison

Phase Difference

WIND WINDOW

DATA

PHYSICAL DIMENSIONS (mm/tol. +/- 0.1)

80

51

81

50

100

31

1

30

0.65

0.30

20.0

25.6 +/- 0.4

14.0

19.6

+/- 0.4

0.15 +/- 0.05

1.5 +/- 0.3

2.8

2.7
JUMPER DESCRIPTION (NCL5034 eval. board)

JP1 - Jumpered, selects PS/2 mode (inverts REWL/DENS signal for 1.44 MB floppy)

JP2 - Jumpered, selects 3FX secondary address, open selects 37X primary address
NCL2020 EVALUATION

Samples of the NCL2020 floppy disk controller are available in both chip and board forms.

The NCL5034 board is PC/AT compatible and allows easy evaluation of the NCL2020. No other equipment is required.

Contact NCLA for further information.

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