Multi-Drop Channel-Link Operation

CHANNEL-LINK OPERATION

The Channel-Link chipset is configured to provide high speed data transmission over a reduced size interconnect. With the 7 to 1 mux/demux architecture cable and connector reductions of up to 80% are possible. LVDS also provides a low noise system due to the use of current mode LVDS line drivers, a small signal swing of ~300 mV typical, and differential signaling. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range. LVDS is also very noise tolerant, as the receivers support a tight 100 mV threshold and a wide ±1V common mode operating range.
LVDS PCB TECHNIQUES:
LVDS features fast edge rates, therefore the interconnect between transmitters and receivers will act as a transmission line. The PCB traces that form this interconnect must be designed with care. The following general guidelines should be adhered to:

- Hand route or review very closely auto-routed traces.
- Locate the Transmitters and Receivers close to the connectors to minimize PCB trace length for off PCB applications.
- Traces should be laid out for differential impedance control (space between traces needs to be controlled). See Figure 4 and AN-905 for equations.
- Minimize the distance between traces of a pair to maximize common mode rejection.
- Place adjacent LVDS trace pairs at least twice as far away (as the distance between the conductors of the pair) (see Figure 4).
- Place TTL/CMOS (large dV signals) far away from LVDS, at least three times (>3S) away or on a different signal layer. (See Figure 4.)
- Match electrical length of all LVDS lines.
- Keep stubs as short as possible.
- Avoid crossing slots in the ground plane.
- Avoid 90° bends (use two 45s).
- Minimize the number of via on LVDS traces.
- Maintain equal loading on both traces of the pair to preserve balance.
- Match impedance of PCB trace to connector to media (cable) to termination to minimize reflections (emissions) for cabled applications (typically 100Ω differential mode impedance).
- Select a termination resistor to match the differential mode characteristic impedance of the interconnect, 2% tolerance is recommended.
- Locate the termination within 1/2 (<1) inch of the receiver inputs if not using a fly-by termination method.
- Use surface mount components to minimize parasitic L & C for bypass caps and termination resistors.
- Use a 4 layer PCB (minimum).
- Bypass each LVDS package at the device pin (Bulk bypass nearby also) with parallel capacitors (0.1 µF/0.01 µF/0.001 µF) on each of the supply pins (VCC, LVDSVCC, and PLLVCC).

SUMMARY
Channel-Link provides a versatile high speed data transmission system. It allows for many possibilities of configurations and deployments solving unique problems to special application needs. This application note focused on a distribution application where a Channel-Link Transmitter is connected to several Receivers. Bus configuration along with PCB recommendations were presented. Following these recommendations and guidelines will help ensure that the signal fidelity on the interconnect is maintained and supports error-free transmission.

REFERENCE
For additional information on Channel-Link applications and operation, please see the following application notes located on the National website at:
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