Interfacing the DP8420A/21A/22A to the 29000 Utilizing the Burst Access Mode

INTRODUCTION

This application note describes how to interface the 29000 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). The DP8422A supports the 29000 in the burst access mode. It is assumed that the reader is already familiar with 29000 access cycles and the DP8422A modes of operation.

IA. Description of Designs #1 and #2, the 29000 in burst access mode on the instruction bus, allowing operation up to 25 MHz with four wait states in normal accesses and one or two wait states in burst accesses

The two designs of this application note consist of the DP8422A DRAM controller, a single PAL (PAL16L8D), several flip-flops, and several logic gates. These parts interface to the 29000 as shown in the block diagrams. This design accommodates two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 32 Mbytes (using 4M-bit X 1 DRAMs).

This memory design supports burst accesses by the 29000 to the instruction bus but could also support burst accessing to the data bus given a few minor changes. Design #1 inserts 4 wait states in normal accesses and 2 wait states in burst accesses. Design #2 inserts 4 wait states in normal accesses and 1 wait state in burst accesses. When idle states occur during a burst access the next occurring access will only have one wait state.

This application allows page mode DRAMs to be used by holding RAS low after an access is completed (IRDY low) until either a refresh request or a new access request (IREQ) is generated. If IREQ (Instruction Burst Request) has transitioned low the next sequential word is accessed from the DRAM via a page mode access. This access involves incrementing the column address (DP8422A COLINC input high) and toggling the CAS outputs via the PAL ECAS output. The instruction burst acknowledge (IBACK) input is driven low except in the case of a refresh request (RFREQ) or new access (IREQ) being requested.

If the user wants to do dual accessing with the DP8422A DRAM controller, address buffers (74AS244s) must be added to the address, ECAS0–3, LOCK, and REN inputs. Note that the DP8422A DRAM controller could be used to allow instruction memory accessing thru Port A. The instruction memory could be loaded thru a data memory interface to Port B.

The logic shown in these applications form a complete 29000 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A. arbitration between Port A, and refreshing the DRAM;
B. the insertion of wait states to the processor (Port A) when needed;
C. remaining in burst access mode unless a refresh request (RFREQ) or new instruction request is generated;
D. incrementing the column address during burst mode accesses; and
E. guaranteeing the RAS and CAS low and precharge times.

The timing calculations for this design are included in this application note.

When using the DP8420A/21A/22A at or above 20 MHz the user should program three clock periods of precharge. This is because two clock periods of precharge at 20 MHz will only guarantee 77 ns of RAS precharge (2 clocks at 20 MHz) to AREQ high (14 ns). If the RAS precharge is 77 ns then the time between AREQ transitions should be at least 96 ns.

IB. High Performance NO WAIT State 29000 System

A higher performance 29000 system (similar to the ones discussed in this application note) could be designed using the DP8422A by accessing four RAS banks at once, this could allow zero wait state burst accesses. An example of this method using 2 DRAM banks is shown at the end of this application note. If 2 DRAM controllers were used (4 BANKs) burst accesses could execute in zero wait states. The COLINC inputs to the two DRAM controllers would be staggered in time as well as the four ECAS outputs (B0ECAS–B3ECAS) from the 29000 control logic block.

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II. 29000 Programming mode bits

<table>
<thead>
<tr>
<th>Programming Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0 = 1</td>
<td>RAS low four clocks, RAS precharge of three clocks</td>
</tr>
<tr>
<td>R1 = 1</td>
<td>DTACK will be asserted on the positive edge of CLK following the access RAS</td>
</tr>
<tr>
<td>R2 = 1</td>
<td>No WAIT states during burst accesses</td>
</tr>
<tr>
<td>R3 = 0</td>
<td>DTACK output</td>
</tr>
<tr>
<td>R4 = 0</td>
<td>Non-address pipelining to support burst accessing</td>
</tr>
<tr>
<td>R5 = 0</td>
<td>RAS and CAS groups selected by “B1”. This mode allows two RAS and four CAS outputs to go low during an access.</td>
</tr>
<tr>
<td>R6 = X</td>
<td>Select based upon the input clock frequency. Example: if the DELCLK frequency is 20 MHz then choose C0,1,2 = 0,0,0 (divide by ten, this will give a frequency of 2 MHz).</td>
</tr>
<tr>
<td>R7 = 1</td>
<td>Column address setup time of 0 ns.</td>
</tr>
<tr>
<td>R8 = 1</td>
<td>Row address hold time of 15 ns</td>
</tr>
<tr>
<td>R9 = X</td>
<td>Delay CAS during write accesses to one clock after RAS transitions low.</td>
</tr>
<tr>
<td>C0 = X</td>
<td>Latching of the address inputs, needed for the burst accessing capability of the 29000 (COLINC input in particular).</td>
</tr>
<tr>
<td>C1 = X</td>
<td>Access mode 1</td>
</tr>
<tr>
<td>C2 = X</td>
<td>Program with low voltage level</td>
</tr>
<tr>
<td>C3 = X</td>
<td>Program with high voltage level</td>
</tr>
<tr>
<td>C4 = 0</td>
<td>Program with either low voltage level (don’t care condition)</td>
</tr>
<tr>
<td>C5 = 0</td>
<td>Design 1 and Design 2, with four wait states per normal access and one or two wait states per burst access</td>
</tr>
<tr>
<td>C6 = 1</td>
<td>Maximum time to address valid (with respect to 25 MHz clock): 14 ns (29000 data sheet #6)</td>
</tr>
<tr>
<td></td>
<td>Maximum time to ADS low (with respect to 25 MHz clock): 9 ns (74AS374 clock to Q, tPHL)</td>
</tr>
<tr>
<td></td>
<td>Minimum ADS low setup time to CLK high (DP8422-25 needs 25 ns, #400b): 40 ns (one clock period, 25 MHz) - 9 ns (#2) - 31 ns</td>
</tr>
<tr>
<td></td>
<td>Minimum address setup time to ADS low (DP8422-25 needs 14 ns, #404): 40 ns (One clock period, 25 MHz) + 2 ns (minimum 74AS374 clock to Q) - 14 ns (#1) - 28 ns</td>
</tr>
<tr>
<td></td>
<td>Minimum CS setup time to CLKA high (DP8422-25 needs 5 ns, #401): 24 ns (#4) - 9 ns (74AS138 decoder) - 15 ns</td>
</tr>
<tr>
<td></td>
<td>Determining tRAC (RAS access time needed by the DRAM): 200 ns (five clock periods at 25 MHz) - 40 ns (one clock period, T1) - 9 ns (#2) - 6 ns (29000 data setup time, #9a) - 7 ns (74F245S) - 29 ns (CLK to RAS low) - 109 ns</td>
</tr>
</tbody>
</table>

0 = Program with low voltage level
1 = Program with high voltage level
X = Program with either low voltage level (don’t care condition)

III. 29000 25 MHz timing calculations for Design #1 and Design #2, with four wait states per normal access and one or two wait states per burst access

1. Maximum time to address valid (with respect to 25 MHz clock): 14 ns (29000 data sheet #6)
2. Maximum time to ADS low (with respect to 25 MHz clock): 9 ns (74AS374 clock to Q, tPHL)
3. Minimum ADS low setup time to CLK high (DP8422-25 needs 25 ns, #400b): 40 ns (one clock period, 25 MHz) - 9 ns (#2) - 31 ns
4. Minimum address setup time to ADS low (DP8422-25 needs 14 ns, #404): 40 ns (One clock period, 25 MHz) + 2 ns (minimum 74AS374 clock to Q) - 14 ns (#1) - 28 ns
5. Minimum CS setup time to CLKA high (DP8422-25 needs 5 ns, #401): 24 ns (#4) - 9 ns (74AS138 decoder) - 15 ns
6. Determining tRAC (RAS access time needed by the DRAM): 200 ns (five clock periods at 25 MHz) - 40 ns (one clock period, T1) - 9 ns (#2) - 6 ns (29000 data setup time, #9a) - 7 ns (74F245S) - 29 ns (CLK to RAS low) - 109 ns

Therefore the tRAC of the DRAM must be 109 ns or less.
7. Determining tCAC (CAS access time needed by the DRAM) and tAA (column address access time): 200 ns - 40 ns - 9 ns - 6 ns - 7 ns - 82 ns (CLK to CAS low) = 56 ns
Therefore the tCAC and tAA (access time from the column address) of the DRAM must be 56 ns or less. COMMON 100 ns DRAMS WILL MEET THIS tRAC, tAA, AND tCAC PARAMETER.
8. Minimum setup of DTACK1 to the 74AS374 ONLY, (need 2 ns): 40 ns (one clock period) - 28 ns (DP8422A-25 DTACK1 delay, #18) - 12 ns
9. Minimum IRDY setup time to IRDY being sampled (12 ns is needed by the 29000, #9): 40 ns (one clock period) - 9 ns (maximum 74AS374 clock to Q output delay) - 31 ns
10a. Determining $t_{CAC}$ during a burst access for Design #1:
120 ns (3 clock periods) — 20 ns (one half clock period during which $CAS$ is high) — 10 ns (PAL16L8 maximum propagation delay) — 12 ns (74AS52 propagation delay driving $= 125$ pF with damping resistor and other associated delays) — 6 ns (data setup time) — 7 ns (74F245) — 65 ns
Therefore the $t_{CAC}$ of the DRAM must be $\leq 65$ ns

10b. Determining $t_{CAC}$ during a burst access for Design #2:
80 ns (2 clock periods) — 20 ns (one half clock period during which $CAS$ is high) — 10 ns (PAL16L8 maximum propagation delay) — 12 ns (74AS52 propagation delay driving $= 125$ pF with damping resistor and other associated delays) — 6 ns (data setup time) — 7 ns (74F245) — 25 ns
Therefore the $t_{CAC}$ of the DRAM must be $\leq 25$ ns

11a. Determining IAA during a burst access for Design #1:
160 ns (4 clock periods, because $IRDY$ inverts is COLINC) — 39 ns (DP8422A COLINC to Q’s valid, #27) — 121 ns $\geq$ IAA.

11b. Determining IAA during a burst access for Design #2:
120 ns (3 clock periods, because $IRDY$ inverted is COLINC) — 39 ns (DP8422A COLINC to Q’s valid, #27) — 81 ns $\geq$ IAA.

IV. 29000 PAL equations, Design #1, 2 wait states during burst accesses. Written in National Semiconductor PLAN™ format

PAL16L8D

CLK CS IREQ IBREQ DTACK2 AREQ IRDY IRDY3 RREQD GND RESET IBACK ECAS ECAS1 DOACC ENDAC1 IREQ ENDACC IREQH VCC

If (VCC) IBACK = AREQ*RREQD*IREQ+DTACK2 +AREQ*RREQD+IREQ
+IBACK*RREQ+RREQD

If (VCC) ECAS = AREQ+ECAS1*DOACC+RESET +AREQ*DOACC+IRDY+CLR+RESET +AREQ*DOACC+IRDY+1+RESET +ECAS*ECAS1*CLK+RESET +ECAS*CLK+RESET

If (VCC) ECAS1 = IRDY+CLK +ECAS1+CLK

If (VCC) DOACC = AREQ*RREQD*RREQD+RESET +CS+IREQ+IREQ+AREQ+RESET +DOACC+IRDY+RESET

If (VCC) ENDAC1 = IREQ+IREQ +RREQD+IRDY +RREQD+AREQ+IREQ +ENDACC+AREQ +RESET

If (VCC) IREQ = AREQ+IREQ +IREQ+AREQ+RESET

If (VCC) IREQH = DTACK2*AREQ+IRDY+IRDY3+IREQH +AREQ+IRDY+IRDY3+IREQ+CLK*DOACC +IRDY+1+IRDY+AREQ

If (VCC) AREQ = CS+IREQ+IRDY+ENDAC+RESET +AREQ+ENDACC+RESET +AREQ+DOACC+RESET

29000 PAL equations, Design #2, 1 wait state during burst accesses. Written in National Semiconductor PLAN format

PAL16L8D

CLK CS IREQ IBREQ DTACK2 AREQ IRDY IRDY3 RREQD GND RESET IBACK ECAS ECAS1 DOACC ENDAC1 IREQ ENDACC IREQH VCC

If (VCC) IBACK = AREQ*RREQD*IREQ+DTACK2 +AREQ*RREQD+IREQ
+IBACK*RREQ+RREQD

If (VCC) ECAS = AREQ+ECAS1*DOACC+RESET +AREQ*DOACC+IRDY+CLR+RESET +AREQ*DOACC+IRDY+1+RESET +ECAS*ECAS1*CLK+RESET +ECAS*CLK+RESET

If (VCC) ECAS1 = IRDY+CLK +ECAS1+CLK

If (VCC) DOACC = AREQ*RREQD*RREQD+RESET +CS+IREQ+IREQ+AREQ+RESET +DOACC+IRDY+RESET

If (VCC) ENDAC1 = IREQ+IREQ +RREQD+IRDY +RREQD+AREQ+IREQ +ENDACC+AREQ +RESET

If (VCC) IREQ = AREQ+IREQ +IREQ+AREQ+RESET

If (VCC) IREQH = DTACK2*AREQ+IRDY+IRDY3+IREQH +AREQ+IRDY+IRDY3+IREQ+CLK*DOACC +IRDY+1+IRDY+AREQ

If (VCC) AREQ = CS+IREQ+IRDY+ENDACC+RESET +AREQ+ENDACC+RESET +AREQ+DOACC+RESET

Key: Reading PAL equations written in PLAN

EXAMPLE EQUATIONS: READ = CS+EP+ADS1D+CLKA +READ+ADS1D +READ+CLKA

This example reads: the output “READ” will transition low on the next rising “CLK” clock edge (given that one of the following conditions are valid a setup time before “CLK” transitions high):
1. the input “CS+RD” is high AND the input “ADS1D” is high AND the input “CLKA” is low, OR
2. the output “READ” is low AND the input “ADS1D” is low, OR
3. the output “READ” is low AND the input “CLKA” is high
V. 29000 application note PAL and 74AS374 outputs

What follows is a brief explanation of the PAL and 74AS374 outputs:

**AREQ1** This combinational output of the PAL is sampled at the next rising clock edge (74AS374) to provide the ADS and AREQ outputs that drive the DP8422A DRAM accesses. This output is held low to allow burst accessing until either a new access is requested by the 29000 (IREQ) or a refresh is requested (RFRQ).

**IRDY** This combinational output of the PAL is sampled at the next rising clock edge (74AS374) to provide the IRDY output that terminates each 29000 access.

**IREQ** This combinational output of the PAL is used internal to the PAL as an indication of IREQ having transitioned high. It is useful in determining when the 29000 is terminating a burst access to request an access to another page (IREQH is IREQ low).

**ENDACC** This combinational output of the PAL is used internal to the PAL as an indication of when to terminate a burst, or single, access. It indicates a new page access (IREQ), a refresh request (RFRQ), or a hardware reset (RESET) operation. Accesses are only terminated after IRDY is issued or during idle states when no accesses are pending.

**AREQ** See AREQ1 explanation.

**IRDY** See IRDY1 explanation.

**IRDY3** This output (74AS374) is used as a state input to the PAL. This term is IRDY delayed by one clock period.

**RFRQD** This clocked output is used to synchronize the DP8422A RFRQ output.

**DTACK2** This clocked output is generated from the DP8422A DTACK1 output and is synchronized to the next rising clock edge.

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**Block Diagram of 29000/DP8422A Design at 25 MHz (Instruction memory interface to Port A, Port B could be used as a data memory interface to load the instructions into the DRAM)**

TL/F/10394–1
High Performance 2900 System Block Diagram Using 2 DRAM Banks, This System Could Be of Still Higher Performance by Extending It to 4 DRAM Banks
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