82C5059 SINGLE CHIP PC-AT DISK CONTROLLER

Memory Controller Features
- Two Independent DMA Channels
- 13 Megabyte Device Bandwidth at 40MHz Clock
- 20-bit Address and 16-Bit Transfer Count Registers For Each Channel
- Holding Registers for Addresses Counts for Non-Contiguous Memory Transfers
- Bus Access Resolved on Channel Priority Basis
- Programmable:
  - Interrupt Polarity
  - Auto-Count Re-Initialization
  - Memory Access Cycle Timing (2 To 5 Clock Cycles)
- Buffer Memory Address for 64K SRAM (2 Memory Chip Enables for 32K x 8 SRAM)
- DRAM Support For Up To 1 Megabyte

Programmable Data Sequencer Features
- High Level Instruction Set
- Supports up to 20MHz Serial Bit Rate (NRZ)
- Programmable Disk Format
- NRZ Serial Disk Interface
- Direct Interface to ESDI Type Drives

- Multi-Sector Transfer Capability with Automatic Sector Increment
- Programmable Automatic ID Retries
- ESDI ID Sync Timeout Programmable
- ESDI Write Gate to AM ENABLE Programmable
- Format Track With Data From Buffer
- Programmable Write Gate Disable for Embedded Servo
- 32, 48, 56 Bit ECC Polynomial

AT Interface Features
- Direct Interface to AT-Compatible Systems, Including 40-Pin Bus Interface
- High Current Drivers for Host Interface
- Schmidt Trigger Inputs Form Host Interface
- Configurable Primary or Secondary Address
- 2 Word FIFO
- Automatic BUSY, INTRQ and ECC Mode
- Flexible Interrupt Capability
- Advanced 1.5 µ CMOS, Low Power Technology
- 100-Pin Quad Flat Pack Packaging
82C5059 SINGLE-CHIP PC-AT CONTROLLER

PC-AT DATA

MEMORY INTERFACE

HOST PC-AT INTERFACE FIFO AND CONTROL CIRCUITS

PC-AT DATA

PC-AT CONTROL

MICROPROCESSOR INTERFACE

MEMORY ADDRESS AND CONTROL 16/ 9/

TWO-CHANNEL DMA CONTROLLER

HOST AND PC-AT CONTROL BUS

CONTROL

MICROPROCESSOR ADDRESS, DATA, CONTROL, AND STATUS INTERFACE

MICROPROCESSOR ADDRESS BUS

ADDRESS AND DATA BUS

SCSI INTERRUPT

SEQUENCE INTERRUPT

DMA INTERRUPT

CONTROL

WINCHESTER AND FLOPPY-DISK INTERFACE

READ REFERENCE CLOCK

READ CLOCK

WRITE DATA (NRZ) TO DISK

WRITE DATA (NRZ) FROM DISK

INDEX

SECTOR/ADDRESS-MARK FOUND

ADDRESS MARK ENABLE

INTERNAL CONTROL AND STATUS BUS

64 x 8 RAM SEQUENCER AND STATE CONTROL

CONTROL

CONTROL

CONTROL

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Introduction

The 82C5059 Single Chip PC-AT Controller is a CMOS LSI Applications Specific Integrated Circuit (ASIC) designed to be the primary component in a high-performance intelligent PC-AT Winchester disk controller system. The 82C5059 single chip controller provides three essential functions in a disk controller system: it manages the flow of data for a serial peripheral, it controls access to the external RAM buffer memory that is required for such transfers and it directly interfaces to a PC-AT type system bus. The 82C5059 is designed to be used with a microprocessor having either a Z8- or 8051-type bus structure.

The 82C5059 consists of three functional sections:

1. A DMA controller
2. A data sequencer
3. A PC-AT interface controller

The 82C5059 incorporates a dual-bus architecture, providing separate ports for microprocessor and memory buffer operations. With the goal of achieving the highest possible performance, this dual-bus structure is used so that disk data transfers can occur simultaneously with microprocessor operations.

In the DMA controller, Channel 0 is used for moving blocks of data between the data sequencer and the external buffer, while Channel 1 is used for moving blocks of data between the PC-AT host interface and the buffer. When the data sequencer is not using Channel 0, this channel can also be used to allow the microprocessor to access the RAM buffer. DMA controller operation is programmed by writing the DMA controller registers, while operation may be monitored by reading the DMA controller registers.

The programmable data sequencer provides format control, error detection, and serial/parallel (SERDES) conversion functions normally associated with disk controllers. It is designed to be used with NRZ (Non-Return to Zero) interfaces such as those used in the ESDI (Enhanced Small Device Interface) or any of the CHIPS family of encode/decode VCO devices. Flexible operation of the sequencer is made possible by write registers that program its operation, while read registers allow the firmware to monitor operation. In addition, complete flexibility in disk formatting is permitted by a 64-byte on-device format RAM, which is accessed through three of the data sequencer write registers (WR25, WR30 & WR31).

In addition to an external RAM buffer, a byte-oriented microprocessor such as the Z8 or 8051, with its associated memory, the 82C5059 may be connected with the CHIPS 10C5070 Encode/Decode.PLL for MFM encoding/decoding up to 5 Mbits/second, or the 10C5027 Encode/Decode.PLL for RLL 2,7 encoding/decoding up to 10 Mbits/second thus providing a complete controller solution for an embedded PC-AT interfacing disk drive.

Ordering Information

The 82C5059 can be ordered using the following part number:

F82C5059 (100-Pin QFP)

Evaluation samples are available now. Production orders accepted with standard leadtimes.
F82C5059 Typical System Configuration